Data Sheet

B50610

10/100/1000BASE-T Gigabit Ethernet Transceiver

GENERAL DESCRIPTION

The Broadcom® B50610 is a triple-speed 1000BASE-T/100BASE-TX/10BASE-T Gigabit Ethernet (GbE) transceiver integrated into a single monolithic CMOS chip. The device performs all physical-layer functions for 1000BASE-T, 100BASE-TX, and 10BASE-T Ethernet on standard category 5 UTP cable. 10BASE-T can also run on standard category 3, 4, and 5 UTP. The B50610 is a highly integrated solution combining digital adaptive equalizers, ADCs, phase-locked loops, line drivers, encoders, decoders, echo cancellers, crosstalk cancellers, and all required support circuitry. Based on Broadcom's proven Digital Signal Processor technology, the B50610 is designed to be fully compliant with RGMII, allowing compatibility with industry-standard Ethernet MACs and switch controllers.

Designed for reliable operation over worst-case category 5 cable, the B50610 automatically negotiates with its link partner to determine the highest possible operating speed. The device detects and corrects most common wiring problems. The B50610 features CableChecker™ diagnostics, which detects common cable problems including shorts, opens, and cable length.

APPLICATIONS

- GbE switches and uplinks

FEATURES

- Single-chip integrated triple-speed Ethernet transceiver
- 1000BASE-T IEEE 802.3ab
- 100BASE-TX IEEE 802.3u
- 10BASE-T IEEE 802.3™
- Supports only RGMII MAC interface
- Supports SOFT-RESET
- Ethernet@Wirespeed™
- Integrated voltage regulator
- Trace matched output impedance
- Lineside loopback
- Low EMI emissions
- Cable plant diagnostics
- Robust CESD tolerance
- Support for jumbo packets up to 10 KB
- Detection and correction of pair swaps (MDI crossover), pair skew, and pair polarity
- Advanced power management
- IEEE 1149.1 (JTAG) boundary scan
- Super isolate mode
- 100-pin FBGA and 48-pin MLP packages

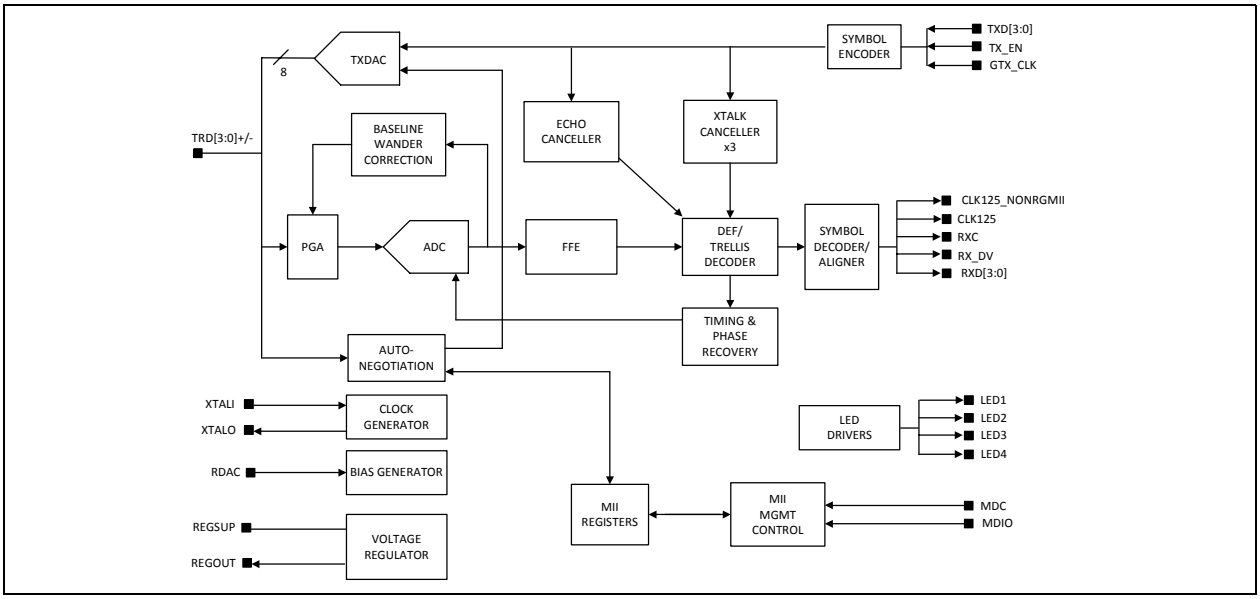

Figure 1: Functional Block Diagram

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REVISION HISTORY

Revision	Date	Change Description
B50610-DS07-R	09/18/09	**Updated:** • Table 1, "Hardware Mode Selection," on page 1 • G10, D2/H5 in Table 2, "Hardware Signal Descriptions," on page 11 • "Standby Power-Down Mode" on page 21 • Note in "CLK125 and CLK125_NONRGMII Clock Output" on page 22 • "Ultra-Low Power-Down Mode" on page 22 • Table 14, "48-Pin MLP Active Pin Test Function in JTAG Mode," on page 32 • Table 16, "48-Pin MLP RGMII Mode," on page 33 • Table 20, "48-Pin MLP Package RGMII Mode Selection," on page 34 • "LED Modes" on page 35 • Bits 15:6 in Table 47, "1000BASE-T/100BASE-TX/10BASE-T Power/MII Control Register (Address 18h, Shadow Value 010)," on page 72 • Bits 14:12 in Table 48, "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register (Address 18h, Shadow Value 100)," on page 73 • "CLK125 Output" on page 89 • "CLK125_NONRGMII Disable" on page 95 • "Digital Pin Operating @ 3.3V or 2.5V OVDD" in Table 84, "DC Characteristics," on page 119
B50610-DS06-R	06/15/09	**Updated:** • "Ethernet@Wirespeed™ Mode" on page 41 • "Expansion Register 08H: 10BT Controls" on page 128
B50610-DS05-R	04/29/09	**Updated:** • Figure 1, "Functional Block Diagram," on page i • Regulator graphic in Table 3, "Hardware Signal Descriptions," on page 20 • "CLK125 and CLK125_NONRGMII Clock Output" on page 37 • Table 4, "1000BASE-T External Loopback With External Loopback Plug," on page 40 • Table 5, "1000BASE-T External Loopback Without External Loopback Plug," on page 40 • Table 7, "100BASE-TX External Loopback Without External Loopback Plug," on page 40 • Table 9, "10BASE-T External Loopback Without External Loopback Plug," on page 40 • Table 13, "Programmable LEDs," on page 45 • "48-Pin MLP Package Hardware Configuration" on page 46 • Table 85, "Main Differences Between Standard and RoHS-Compliant Packages," on page 136 • Table 88, "Ordering Information," on page 140 **Added:** • "JTAG Mode" on page 46 • Table 15, "48-Pin MLP Active Pin Test Function in JTAG Mode," on page 47 • "Normal Operation Mode and PHYA Mode" on page 47 • "PHY Address" on page 47 • Table 16, "48-Pin MLP PHY Address Based on PHYA[0] and TEST[3:2] Settings," on page 47 • Table 17, "48-Pin MLP RGMII Mode," on page 47 • "RGMII LED Mode" on page 47 • "LOM LED Mode" on page 48 • Table 18, "48-Pin MLP LOM LED Link Signal Rate Reporting," on page 48 • Table 19, "48-Pin MLP RGMII Modes for LOM LED Operation," on page 48

Revision	*Date*	*Change Description*
B50610-DS04-R	12/09/08	**Updated:** • Cover page • Figure 1, ”Functional Block Diagram,” on page i • Table 1, ”Hardware Mode Selection,” on page 1 through Table 3, ”Hardware Signal Descriptions,” on page 19 • Figure 4, ”Typical RGMII-to-10/100/100BASE-T Application,” on page 2 • Figure 7, ”100-Pin FBGA Pinout Diagram, Top View,” on page 29 • ”Reset” on page 34 • ”Standby Power-Down Mode” on page 35 through ”Ultra-Low Power-Down Mode” on page 36 • Table 15, ”Using TEST[3:2] Pins to Set JTAG, Normal Operation, and PHYA Modes,” on page 45 • Table 19, ”Register Map,” on page 52 • Table 22, ”1000BASE-T/100BASE-TX/10BASE-T PHY Identifier Register (Addresses 02h and 03h),” on page 59 • Table 49, ”1000BASE-T/100BASE-TX/10BASE-T Register 1Ch Shadow Values,” on page 97 and Table 50, ”1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 Register (Address 1Ch, Shadow Value 00010),” on page 98 • ”TXC/RXC Disable During Auto Power-Down Mode” on page 102 • ”External Control 1 Register” on page 108 • Table 80, ”Main Differences Between Standard and RoHS-Compliant Packages,” on page 133 • Table 83, ”Ordering Information,” on page 137 **Added:** • Figure 12, ”Internal Loopback Mode,” on page 37 through Figure 14, ”External Loopback Mode,” on page 38
B50610-DS03-R	07/15/08	**Updated:** • ”Internal Voltage Regulator” on page 8. • Table 2, ”Hardware Signal Descriptions,” on page 11. • Table 13, ”Programmable LEDs,” on page 43. • ”1000BASE-T/100BASE-TX/10BASE-T PHY Identifier” on page 58. • ”Thermal Information” on page 136.
B50610-DS02-R	06/12/08	**Updated:** • RGMII HSTL voltage function in Table 1, ”Hardware Mode Selection,” on page 1 • Table 2, ”Hardware Signal Descriptions,” on page 11 • Table 2, ”Hardware Signal Descriptions,” on page 11Table 16, ”48-Pin MLP Package RGMII Mode Selection,” on page 45 • Table 74, ”RGMII Input Timing (Normal Mode): GTXCLK and TXD[3:0],” on page 127 • Table 75, ”RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0],” on page 128 • Figure 16, ”RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0],” on page 128 • Table 76, ”RGMII Output Timing (Normal Mode): RXC and RXD[3:0],” on page 129

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B50610-DS02-R (cont,)	06/12/08	• Table 77, ”RGMII Output Timing (Delayed Mode): RXC and RXD[3:0],” on page 130 • Table 78, ”Absolute Maximum Ratings,” on page 131 • Table 79, ”DC Characteristics,” on page 131 • Table 80, ”Main Differences Between Standard and RoHS-Compliant Packages,” on page 133 **Added:** • Figure 7, ”BCM50610 48-Pin MLP Pinout Diagram, Top View,” on page 32 ”REFCLK Input Timing” on page 125
B50610-DS01-R	04/18/08	**Updated:** • Bit 15:5 in Table 24, ”1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Expansion Register (Address 06h),” on page 51 • Bit 8:7 in Table 41, ”10BASE-T Register (Address 18h, Shadow Value 001),” on page 70 • Bit 15:6 in Table 42, ”1000BASE-T/100BASE-TX/10BASE-T Power/MII Control Register (Address 18h, Shadow Value 010),” on page 72 • Bit 7:3 in Table 44, ”1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control Register (Address 18h, Shadow Value 111),” on page 75 • Bit 1 in Table 49, ”1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 Register (Address 1Ch, Shadow Value 00010),” on page 85 • Default values in Table 55, ”1000BASE-T/100BASE-TX/10BASE-T LED Status Register (Address 1Ch, Shadow Value 01000),” on page 90 • Bit 2 in Table 56, ”1000BASE-T/100BASE-TX/10BASE-T LED Control Register (Address 1Ch, Shadow Value 01001),” on page 92
B50610-DS00-R	02/28/08	Initial release.

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OVERVIEW

The Broadcom® B50610 is a single-chip Gigabit Ethernet (GbE) transceiver that performs all of the physical layer (PHY) interface functions for 1000BASE-T, 100BASE-TX, and 10BASE-T Ethernet on Category 5 unshielded twisted-pair (UTP) cabling. The 10BASE-T operation is supported on Category 3, 4, and 5 UTP cabling. The B50610 connects to a Media Access Controller (MAC) or switch controller through an RGMII interface.

The device connects directly to the twisted-pair wiring of the network (through isolation transformers) on the other side. The B50610 is designed to be fully compliant with the IEEE 802.3 standard. It can be programmed to auto-negotiate its operating speed and duplex mode based on the capabilities of the link partner and the quality of the cabling plant.

The B50610 device adheres to Broadcom's quality procedures and meets or exceeds the performance and functionality tested as part of our comprehensive product characterization, qualification, and functional verification process.

MODES OF OPERATION

The B50610 operates in RGMII-copper (10/100/1000BASE-T) mode.

In the 100-pin FBGA package, the B50610 can be configured for various modes of RGMII operation by using mode select pins. Table 1 lists the available modes that can be selected.

In the 48-pin MLP package, when TEST[3:2] = 00 or 11, LED[3] is sampled as MODE_SEL[1]. If TEST[3:2] = 00 or 11, and LED[4] is 0, LED[2] is sampled during reset as MODE_SEL[0].

See “48-Pin MLP Package Hardware Configuration” on page 32 for details.

For the 48-pin MLP package, MODE_SEL[1:0] can also be configured via registers 1Ch Shadow Value “01011” bits[4:3] after reset.

Table 1: Hardware Mode Selection

MODE_SEL[1]	*MODE_SEL[0]*	*Function*
0	0	RGMII 3.3V
0	1	RGMII 2.5V
1	0	RGMII HSTL (1.8V)
1	1	RGMII 3.3V (see note)

Note:

- In the 100-pin BGA package, set MODE_SEL[1:0] to 11 to select RGMII 3.3V mode.
- In the 48-pin MLP package, MODE_SEL[1:0] set to 11 is Reserved.

The block diagram of typical application is shown in Figure 2 on page 2.

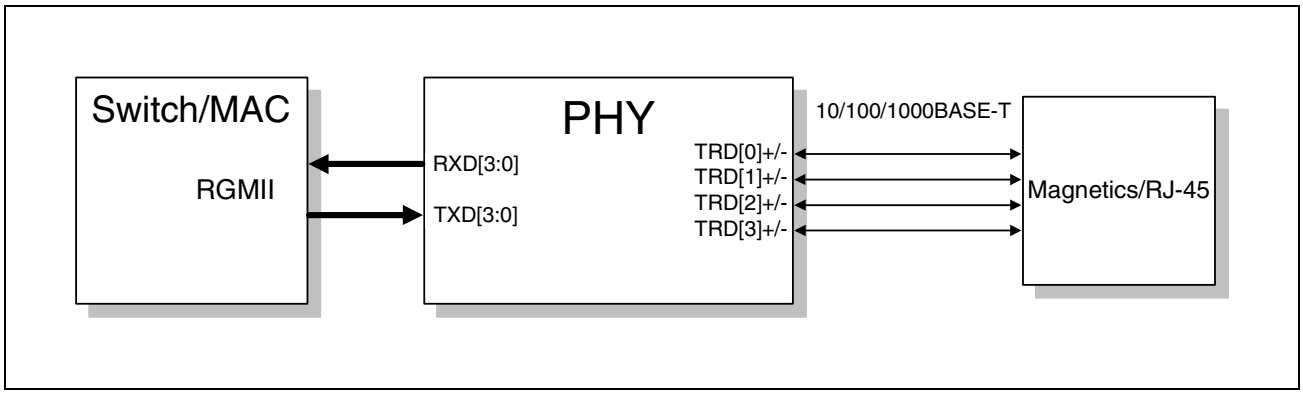


Figure 2: Typical RGMII-to-10/100/100BASE-T Application

Reduced Gigabit Media Independent Interface

The Reduced Gigabit Media Independent Interface (RGMII) is a subset of the Gigabit Media Independent Interface (GMII), which allows the MAC with a reduced pin count to connect to the PHY. Compared to GMII, the number of data signal pins required to and from the MAC is reduced to half by clocking data on both the rising and falling edge of the transmit clock. This makes the RGMII digital data bit transmission rate effectively twice that of the GMII, while the clock speed remains the same. The RGMII and GMII interfaces use the same hardware and internal circuitry, though only TXD[3:0] and RXD[3:0] signals are used in RGMII mode. For information about this mode, see "RGMII Interface" on page 28.

Media Independent Interface

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer when the device is functioning in 10BASE-T and 100BASE-TX modes. The transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL.

Management Interface

The B50610 contains a large set of management registers. The Status and Control registers of the B50610 are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz. The management interface supports the defined Status and Control registers of IEEE 802.3, Clauses 22, 28, 37, and 40. In addition, the B50610 contains multipurpose registers for extended software control.

Encoder

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs pre-equalization for 100m of Category 3 cabling. In

100BASE-TX mode, the B50610 transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start-of-stream delimiter (/J/K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in "Stream Cipher" on page 6. The scrambled data is then encoded into MLT3 signal levels.

In 1000BASE-T mode, the B50610 simultaneously transmits and receives a continuous data stream on all 4 pairs of the Category 5 cable. Byte-wide data from the transmit data pins is scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the 4 twisted pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first 2 bytes of the preamble with a start-of-stream delimiter and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the MAC to separate packets within a multiple-packet burst and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data pins while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE standard 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHY.

DECODER

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn to zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the B50610 asserts the MII receive error (RX_ER) signal. RX_ER is also asserted when the link fails or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder.
- Descrambled.
- Translated back into byte-wide data.

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 00h. Carrier extend codes are replaced with 0Fh or 1Fh. The decoded data is driven onto the RGMII receive data pins. Decoding complies with IEEE standard 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHY.

CARRIER SENSE

In 1000BASE-T RGMII mode, the carrier sense information is encoded into the control signals. For details, see "Operational Description" on page 20. When Carrier Sense is asserted, the RGMII pin RX_CTL will be asserted [0,1] and RXD[7:0] pin are FF. For details, please refer to the Reduced Gigabit Media Independent Interface (RGMII) specification.

LINK MONITOR

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the TRD± pins for the presence of valid link pulses.

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the link fail state and the transmission and reception of data packets are disabled. When a valid signal is detected on the receive pair for a minimum of 1 μs, the link monitor enters link-pass state and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 microsecond, the link monitor enters the link-pass state and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 μs, the link monitor enters the link-fail state and the transmission and reception of data packets are then disabled.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The B50610 achieves optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions up to 100m on Category 5 twisted-pair cabling (100m on Category 3 UTP cable for 10BASE-T mode). The all-digital nature of the design makes the performance very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

ECHO CANCELER

Because of the bidirectional nature of the channel in 1000BASE-T mode, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

CROSSTALK CANCELER

The B50610 transmits and receives a continuous data stream on four channels. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

ANALOG-TO-DIGITAL CONVERTER

Each receive channel has its own 125 MHz Analog-to-Digital Converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High-power supply noise rejection
- Fast settling time
- Low bit error rate

CLOCK RECOVERY/GENERATOR

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25 MHz crystal input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other end is configured as the slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

BASELINE WANDER CORRECTION

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The B50610 automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides perfect DC balance.

MULTIMODE TX DIGITAL-TO-ANALOG CONVERTER

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high-frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation and thus reducing system complexity for routing and bill of materials.

STREAM CIPHER

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bitwide linear feedback shift register (LFSR), producing a 2047-bit nonrepeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bitwide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remappings of the 33-bitwide LFSR output. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bitwide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The B50610 enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals. When the B50610 detects loss of synchronization, it notifies the remote PHY of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the B50610 is forced into the link-fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

WIRE MAP AND PAIR SKEW CORRECTION

During 1000BASE-T operation, the B50610 has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the B50610) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable
- Polarity errors caused by the swapping of wires within a pair

The B50610 also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The B50610 can tolerate delay skews of up to 64 ns. Auto-negotiation must be enabled to take advantage of the wire map correction.

During 10/100 Mbps operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

AUTOMATIC MDI CROSSOVER

Note: This function only operates when the copper auto-negotiation is enabled.

During copper auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The B50610 can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the B50610 normally transmits on the TRD[0]± pin and receives on the TRD[1]± pin.

When connecting to another device that does not perform MDI crossover, the B50610 automatically switches its TRD± pin pairs, when necessary, to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

During 1000BASE-T operation, the B50610 swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. During 100BASE-TX and 1000BASE-T operation, pair swaps automatically occur within the device and do not require user intervention.

10/100BASE-T Forced Mode Auto-MDIX

Note: This function only operates when the copper auto-negotiation is disabled.

This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-T and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for a least 4 seconds, then auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100Tx idles are detected. Once detected, the PHY returns to forced mode operation.

The user should set the same speed in register 0 and the auto-negotiation advertisement register 4.

Example: To force 100Tx full-duplex, write register 0 with 2100h and register 4 with 0181h. The feature is enabled by writing register 18h, shadow 7, bit 9 = 1. Copper link can be determined by reading register 19h, bit 2.

Auto-Negotiation

The B50610 negotiates its mode of operation over the copper media using the auto-negotiation mechanism, defined in the IEEE 802.3u and IEEE 802.3ab specifications. When the auto-negotiation function is enabled, the B50610 automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The B50610 can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex
- 100BASE-TX full-duplex and/or half-duplex
- 10BASE-T full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be enabled or disabled by hardware and software control, but is always required for 1000BASE-T operation. For details on auto-negotiation using Next Page Exchange, see “Next Page Exchange” on page 28.

Energy Detect

The energy-detect feature provides an output signal (EnergyDetect) indicating the presence or absence of energy being received on the copper analog input pins of the chip. Additionally, the copper energy-detection status can be monitored from register 1Ch, shadow 11111, bit 5. See “Operational Description” on page 20 for details.

Internal Voltage Regulator

Control circuitry for voltage regulator has been provided for designs where 1.2V supply is not available. The circuits allow sources at from 2.5V to 3.3V to be reduced to 1.2V. This regulator utilize internal dropping elements and do not require external components. See “Internal Voltage Regulator” on page 29 for details.

POWER-DOWN MODES

Three low-power modes are supported in the B50610:

- Ultra-low power-down mode (IDDQ)
- Standby power-down mode
- Auto power-down mode

For details, see "Auto Power-Down Mode" on page 21.

Additional power savings can be made by:

- Using 2.5V instead of 3.3V for OVDD
- Using external 1.2V supply rather than the internal regulator

JUMBO PACKETS

In copper mode, packets up to 10 KB in length can be supported with the following register writes:

- Register 18h, shadow 000, bit 14 = 1 (default = 0)
- Register 10h, bit 0 = 1 (default = 0)

Section 2: Hardware Signal Descriptions

The following conventions are used in Table 2 on page 11:

- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open drain output
- OT= Tristateable signal
- B = Bias
- PU = Internal pull-up
- PD = Internal pull-down
- SOR= Sample on reset
- CS= Continuously sampled
- ST = Schmitt trigger

The following conventions are used to express the I/O types in Table 2 on page 11. The I/O pin type is useful in referencing the DC pin characteristics contained in "Electrical Characteristics" on page 119:

- XT = Crystal inputs/outputs pin type
- D = Digital pin type
- G = RGMII pin type
- A = Analog pin type
- PECL = Positive Emitter Coupled Logic

Note: Pin groups that are not found on a certain package are represented by an en dash (–).

Note: Refer to the *B50610 Design Guide Application Note* for additional information regarding the configurations and bypassing of the power supply pins.

Table 2: Hardware Signal Descriptions

100-Pin FBGA	*48-Pin MLP*	*Label*	*I/O Type*	*Description*
Media Connections				
K1/K2 K4/K3 K5/K6 K8/K7	14/15 18/17 20/21 24/23	TRD[0]± TRD[1]± TRD[2]± TRD[3]±	A	**Transmit/Receive Pairs.** In 1000BASE-T mode, differential data from copper media is transmitted and received on all four TRD± signal pairs. In auto-negotiation, 10BASE-T, and 100BASE-TX modes, the B50610 normally transmits on TRD[0]± and receives on TRD[1]±. Auto-MDIX operation can reverse the pairs. There is 50Ω internal termination on each pin, so no external termination is required. Since this device incorporates voltage driven DAC, it does not require magnetics center-tap supply. Instead, connect the magnetics center-tap to AC ground through individual 0.1 µF cap.
Clock				
E9		CLK125	O,G	**MAC Reference Clock.** Continuous 125 MHz output generated off the PLL (phase locked to the XTALI input). This clock output remains active and stable during both hardware and software reset. This clock is powered by OVDD_RGMII power.
B1		CLK125_NONRGMII	O	**125 MHz Clock Output.** Continuous 125 MHz output and generated off the PLL (phase lock to the XTAL input). This clock output remains active and stable during both hardware and software reset. This clock is powered by OVDD power.
F1 F2	8 7	XTALI XTALO	I/XT O/XT	**25 MHz Crystal Oscillator Input/Output.** A continuous 25 MHz reference clock must be supplied to the B50610 by connecting a 25 MHz crystal between these two pins or by driving XTALI with an external 25 MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTALO unconnected.
RGMII				
A7	40	GTXCLK	I_{PD} G	**RGMII Transmit Clock.** 2.5/25/125 MHz input. This clock is continuously driven from the MAC. It is used to synchronize the transmit data in 1000BASE-T (RGMII) mode.
C7 C8 B6 B7	39 38 37 36	TXD[0] TXD[1] TXD[2] TXD[3]	I_{PD} G	**Transmit Data Input.** Byte-wide transmit data is input synchronously to the RGMII Transmit Clock.
A8	35	TX_EN	I_{PD} G	**Transmit Enable.** Active-high. When TX_EN is asserted, the data on the TXD pins is encoded and transmitted.
A2	33	RXC	OT G	**Receive Clock.** 2.5/25/125 MHz output. This clock is recovered from the incoming analog waveforms and is used to synchronize the receive data outputs: 1000BASE-TX mode; the clock is 125 MHz, byte-aligned on RXD[3:0]. 100BASE-TX mode; the clock is 25 MHz, nibble-aligned on RXD[3:0]. 10BASE-T mode; the clock is 2.5 MHz, nibble-aligned on RXD[3:0].
D4 D3 C3 C4	32 31 28 27	RXD[0] RXD[1] RXD[2] RXD[3]	OT G	**Receive Data Outputs.** Byte-wide receive data output synchronous with the receive clock.

Table 2: Hardware Signal Descriptions (Cont.)

100-Pin FBGA	48-Pin MLP	Label	I/O Type	Description
B2	26	RX_DV	OT, G	**Receive Data Valid For Port1**. Active-high. RX_DV indicates that a receive frame is in progress and that the data present on the RXD output pins is valid.
D2 H5		MODE_SEL[1] MODE_SEL[0]	I_{PU}	**MODE_SEL[1]/MODE_SEL[0] Function** 0 1 RGMII (2.5V) 1 0 RGMII HSTL 1.8V 1 1 RGMII (3.3V) 0 0 RGMII (3.3V) In the 100-pin FBGA package, use the MODE_SEL[1] and MODE_SEL[0] pins to select RGMII mode. In the 48-pin package, see "48-Pin MLP Package Hardware Configuration" on page 32 for details.
E3	48	MDC	I_{PD}, ST	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions.
F4	47	MDIO	I/O_{PU}, D,ST	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
Mode				
H10	41	PHYA[0]	I_{PD}, SOR	**PHY Address Selects.** Active-high. Sampled on reset. The PHY address selects the MII management PHY address. In the 100-pin FBGA package, the device goes into isolate mode when the PHY address is strapped to 00000. To get out of isolate mode, write to register 00h, bit 10 = 0. **Test Clock.** In the 48-pin MLP package, if TEST[3:2] = 01, PHYA[0] is used for the JTAG function. PHYA[0]=TCK. JTAG serial clock. **PHYA Mode.** In the 48-pin MLP package, if TEST[3:2] = 11, the PHY address is 0x18+PHYA[0]. This allows the chip to have PHY address of 0, 1, 24, and 25. See "48-Pin MLP Package Hardware Configuration" on page 32 for details.
E4	46	RESET	I_{PU}, CS, ST	**Reset.** Active-low, Schmitt Trigger Input. The B50610 requires a hardware RESET prior to normal operation. Configuration settings obtained via Hardware Strap Option pins are latched on the rising edge of RESET. During RESET, if PHYAD[4:0] = 00000, then all RGMII signals are tristated.
G7	45	LED[1]	I_{PU}, O	**LED[1].** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 30 for details. This pin can be Programmed to alternate modes. See "General-Purpose LED Programmability" on page 31 for details. LED[1] is a dual function pin. In the 100-pin FBGA package, LED[1] is sampled during reset as ANEN (copper auto-negotiation select). Active-high. Sampled on reset. When this pin is high, copper auto-negotiation is enabled. When low, copper auto-negotiation is disabled. After reset, auto-negotiation configuration is under software control. **Test Mode Select.** In the 48-pin MLP package, if TEST[3:2] = 01, LED[1] is used for JTAG function and LED[1] = TMS. JTAG mode select input.

Table 2: Hardware Signal Descriptions (Cont.)

100-Pin FBGA	*48-Pin MLP*	*Label*	*I/O Type*	*Description*
G6	44	LED[2]	I_{PU}, O	**LED[2].** LED2 pin/Full–Duplex. This is a dual function pin. Polarity is determined at reset. See "Dual Input Configuration/LED Output Function" on page 30 for details. For programming to alternate modes, see "General-Purpose LED Programmability" on page 31 for details. In the 100-pin FBGA package, this pin is sampled during power on reset. If low, it sets the chip to Half-Duplex mode during normal operation. If high, it sets the chip to Full-Duplex mode during normal operation. These modes can also be changed by software. In the 48-pin MLP package, if TEST[3:2] = 00 or 11, LED[2] is sampled during reset as MODE_SEL[0] if the device is not configured in LOM LED mode. **Test Data Input.** In the 48-pin MLP package, if TEST[3:2] = 01, LED[2] is used for the JTAG function and LED[2] = TDI. JTAG serial data input.

Table 2: Hardware Signal Descriptions (Cont.)

100-Pin FBGA	48-Pin MLP	Label	I/O Type	Description
H6	43	LED[3]	I_{PU}, O	**LED[3]/LED[4].** LED[3] and LED[4] are dual function pins. In the 100-pin FBGA package, LED3 and LED4 are sampled during reset as SPD0 and F1000. Polarity is determined at reset. See "Dual Input Configuration/LED Output Function" on page 30 for details. For programming to alternate modes, see "General-Purpose LED Programmability" on page 31 for more details. **100-pin FBGA Hardware Configuration.** Speed Select. Active-high. These pins set the default copper advertisement of the B50610 according to the following: LED1 LED4 LED3 Description 0 0 0 Force 10BASE-T 0 0 1 Force 100BASE-T 0 1 X Force 1000BASE-T 1 0 0 Auto-negotiate 10BASE-T 1 0 1 Auto-Negotiate 10/100BASE-T 1 1 0 Auto-Negotiate 10/100/1000BASE-T 1 1 1 Auto-Negotiate1000BASE-T (default value) FORCE 1000BASE-T mode is for test purposes only, and disabling auto-negotiation can lead to link configuration mismatches and no-link situations.The Annex 28D.5 extensions required for the Clause 40 (1000BASE-T) IEEE 802.3 specification require auto-negotiation during 1000BASE-T operation. There are no standards that govern a protocol for 1000BASE-T operation without auto-negotiation. Broadcom recommends enabling and using auto-negotiation. For systems that only need 1000BASE-T functionality, Broadcom recommends that auto-negotiation be enabled with only 1000BASE-T advertised and that the advertising bits for all other modes be disabled. If this pin is programmed to output interrupts, it becomes an open drain output. **48-pin MLP Hardware Configuration.** In the 48-pin MLP package, set the copper advertisement to Auto-Negotiate 10/100/1000BASE-T by default. If TEST[3:2] = 00 or 11, LED[3] is sampled as MODEL_SEL[1] and LED[4] is sampled as LOM LED mode. **Test Data Output.** If TEST[3:2] = 01, LED[3] is used for JTAG function and LED[3]=TDO. JTAG serial data output. See "48-Pin MLP Package Hardware Configuration" on page 32 for details.
G10	42	LED[4]	I_{PU}, O, Od	
F5		LOWPWR	I_{PD} CS	**Low Power**. Active-high. If this pin is high, the device enters ultra-low power-down mode (IDDQ). This mode can also be entered through software by writing to register 1C, shadow value 01100, bit 0 =1. To exit, force IDDQ mode, set LOWPWR = 0 and issue a $\overline{\text{RESET}}$. See "Ultra-Low Power-Down Mode" on page 22.
Test				
D7		TCK	I_{PU}	**Test Clock.** JTAG serial clock.
D6		TDI	I_{PU}	**Test Data Input.** JTAG serial data input.
F10		TDO	O, D	**Test Data Output.** JTAG serial data output.
D8		TMS	I_{PU}	**Test Mode Select.** JTAG mode select input.

Table 2: Hardware Signal Descriptions (Cont.)

100-Pin FBGA	*48-Pin MLP*	*Label*	*I/O Type*	*Description*
E10		TRST	I_{PU} CS	**JTAG Reset.** Active-low. Resets the JTAG controller. This signal must be pulled low during normal operation.
H8 H9 G8 G9	 6 5	TEST0 TEST1 TEST2 TEST3	I_{PD} CS	**Test Mode Enables.** Active-high. These pins must always be pulled low during normal operation. These pins are used by Broadcom for test purposes only. In the 48-pin MLP package, when TEST[3:2] = 01, enable JTAG mode; LED[1], LED[2], LED[3], and PHYA[0] are used for TMS,TDI,TDO, and TCK. If TEST[3:2] = 11, the PHY address is 0x18+PHYA[0]. This allows the chip to have PHY address of 0, 1, 24, and 25. See "48-Pin MLP Package Hardware Configuration" on page 32 for details.
RDAC Bias				
H1	10	RDAC	B	**DAC Bias Resistor.** Adjusts the reference current of the transmitter digital-to-analog converter. A 1.24 kΩ +/-1% resistor is connected between the RDAC pin and GND
Regulator				
G3	4	REGIN	PWR	**Regulator supply input.** 2.5V to 3.3V input.
F3	3	REGOUT	PWR	**Regulator output.** 1.2V.

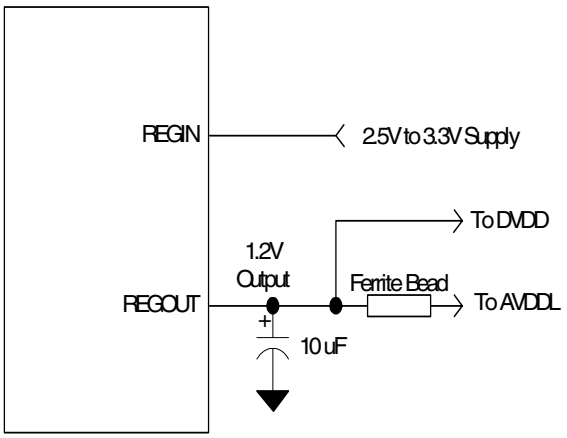


Table 2: Hardware Signal Descriptions (Cont.)

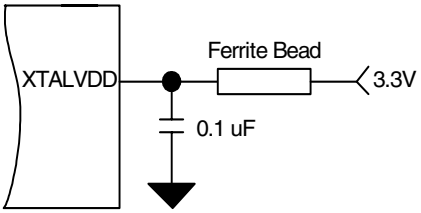
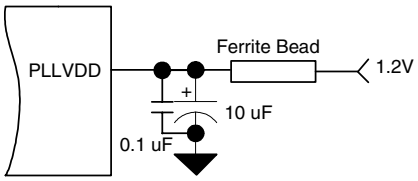
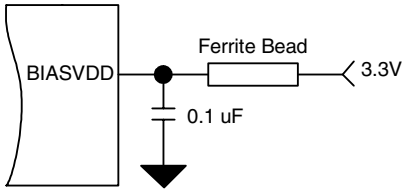
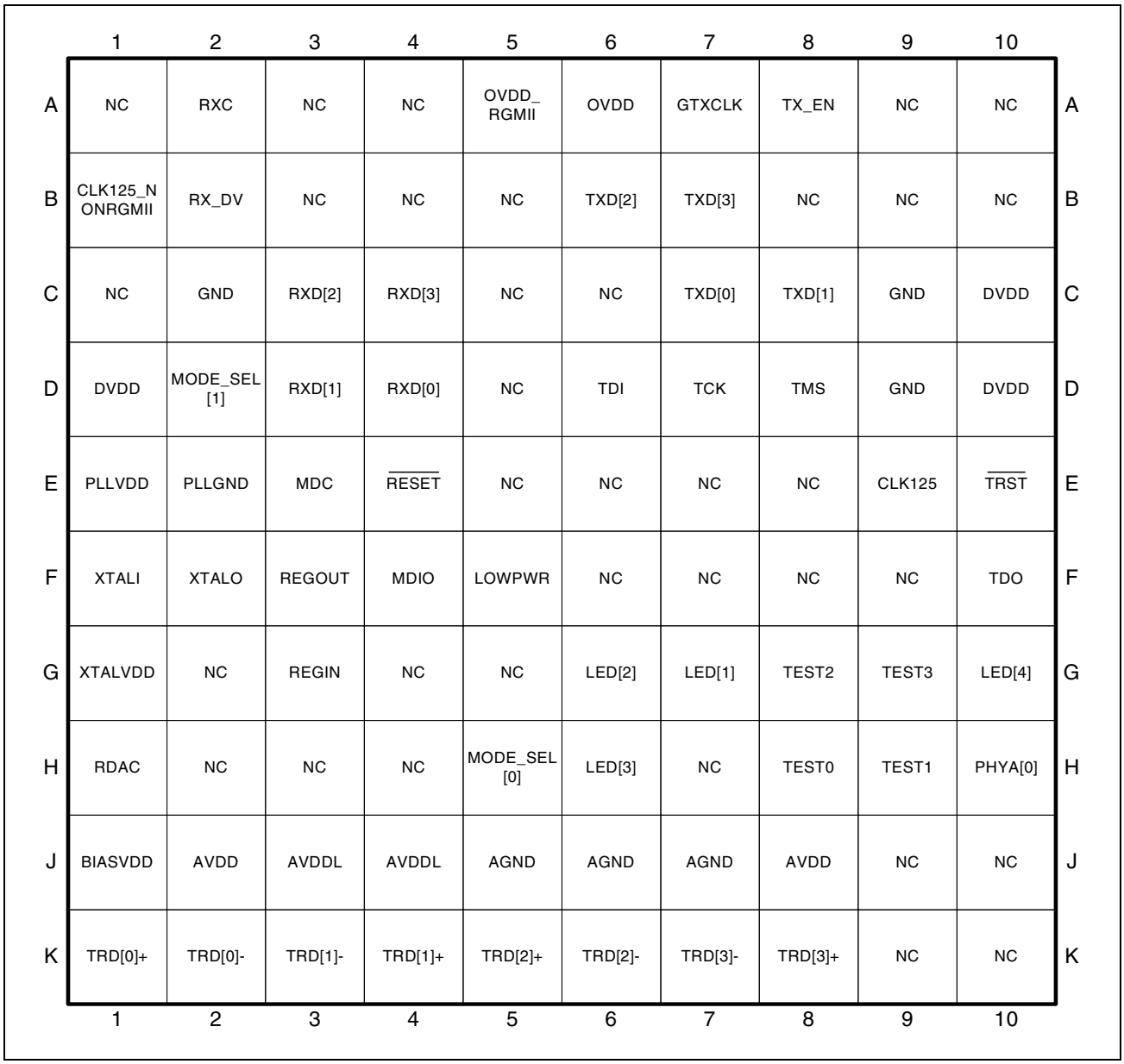
100-Pin FBGA	*48-Pin MLP*	*Label*	*I/O Type*	*Description*
A5	29, 34	OVDD_RGMII	PWR	1.8V for HSTL mode; 2.5V or 3.3V for RGMII pads.
A6	1	OVDD	PWR	2.5V or 3.3V for non-RGMII pads.
C10, D1, D10	2, 30	DVDD	PWR	1.2V power for digital core.
J3, J4	13, 19, 25	AVDDL	PWR	1.2V power for analog core.
J2, J8	16, 22	AVDD	PWR	3.3V power for analog core.
G1	9	XTALVDD	PWR	3.3V Crystal supply**.**
				
E1	11	PLLVDD	PWR	1.2V PLL supply
				
J1	12	BIASVDD	PWR	**Bias VDD.** +3.3V. Normally filtered with a low resistance ferrite bead such as a Murata BLM11A601S or equivalent, as well as a 0.1 µF capacitor.
				
E2		PLLGND	GND	**PLL ground**
J5, J6, J7		AGND	GND	**Analog ground**
C2, C9, D9		GND	GND	**Digital ground**
—	Paddle Ground	GND	GND	**Paddle ground**

Table 2: Hardware Signal Descriptions (Cont.)

100-Pin FBGA	*48-Pin MLP*	*Label*	*I/O Type*	*Description*
No Connect				
A1, A3, A4, A9, A10, B3, B4, B5, B8, B9, B10, C1, C5, C6, D5, E5, E6, E7, E8, F6, F7, F8, F9, G2, G4, G5, H2, H3, H4, H7, J9, J10, K9, K10		NC	NC	**No connect pins.** Do not connect these pins to any other pin, and do not connect them together.



	1	2	3	4	5	6	7	8	9	10	
A	NC	RXC	NC	NC	OVDD_ RGMII	OVDD	GTXCLK	TX_EN	NC	NC	A
B	CLK125_N ONRGMII	RX_DV	NC	NC	NC	TXD[2]	TXD[3]	NC	NC	NC	B
C	NC	GND	RXD[2]	RXD[3]	NC	NC	TXD[0]	TXD[1]	GND	DVDD	C
D	DVDD	MODE_SEL [1]	RXD[1]	RXD[0]	NC	TDI	TCK	TMS	GND	DVDD	D
E	PLLVDD	PLLGND	MDC	$\overline{\text{RESET}}$	NC	NC	NC	NC	CLK125	$\overline{\text{TRST}}$	E
F	XTALI	XTALO	REGOUT	MDIO	LOWPWR	NC	NC	NC	NC	TDO	F
G	XTALVDD	NC	REGIN	NC	NC	LED[2]	LED[1]	TEST2	TEST3	LED[4]	G
H	RDAC	NC	NC	NC	MODE_SEL [0]	LED[3]	NC	TEST0	TEST1	PHYA[0]	H
J	BIASVDD	AVDD	AVDDL	AVDDL	AGND	AGND	AGND	AVDD	NC	NC	J
K	TRD[0]+	TRD[0]-	TRD[1]-	TRD[1]+	TRD[2]+	TRD[2]-	TRD[3]-	TRD[3]+	NC	NC	K
	1	2	3	4	5	6	7	8	9	10	

Figure 3: 100-Pin FBGA Pinout Diagram, Top View

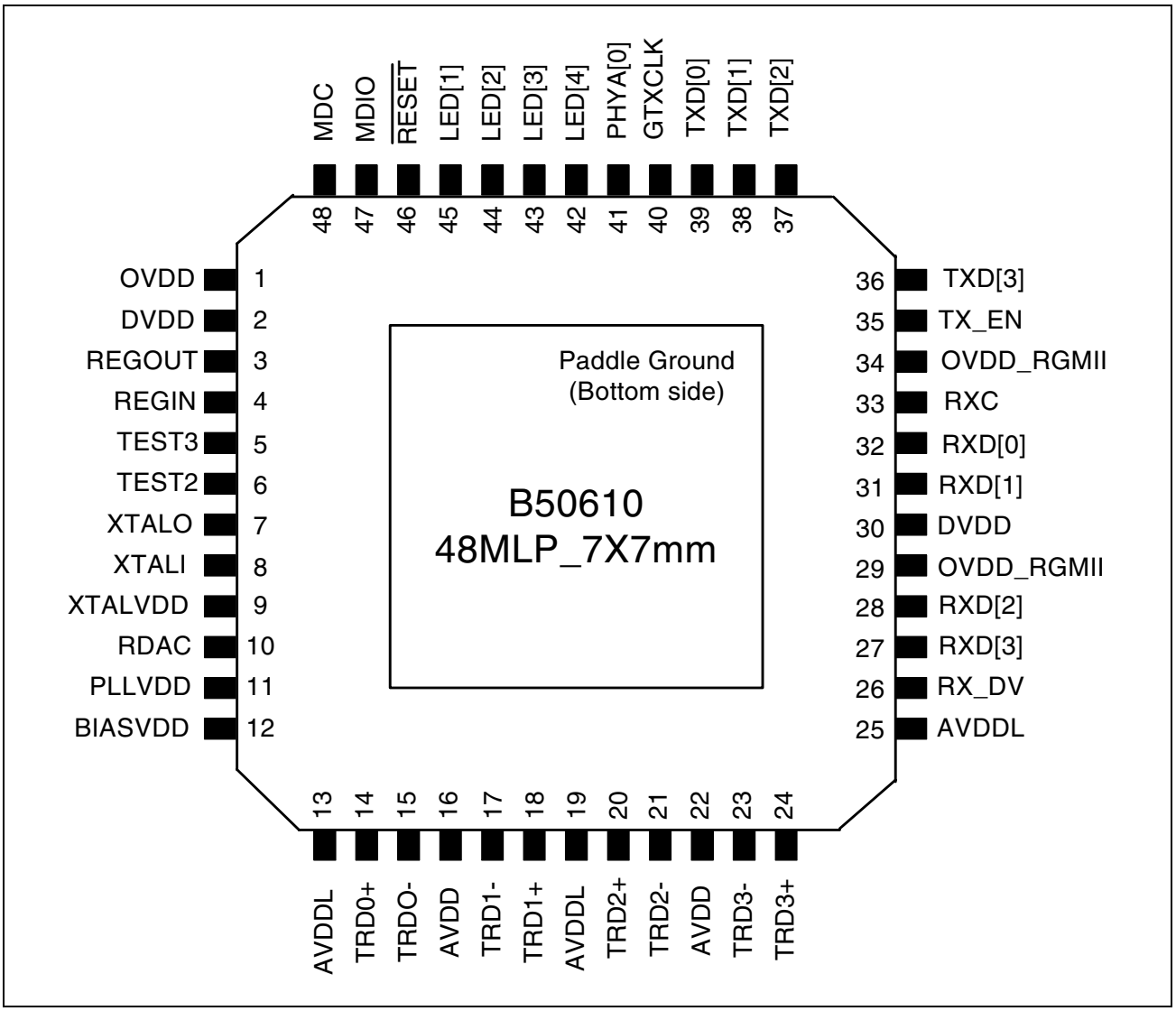


Figure 4: B50610 48-Pin MLP Pinout Diagram, Top View

Section 3: Operational Description

RESET

The B50610 provides a hardware reset pin, RESET, which resets all internal nodes to a known state. The reset pin must be asserted for at least 2.0 µs. Hardware reset should always be applied to the B50610 after power-up.

The B50610 also has a software reset capability. To enable the software reset, a 1 must be written to bit 15 of the MII Control register (address 00h). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if 0 is written to this bit.

The B50610 supports a SOFT-RESET feature. If enable this function, set PHY register 0x00h bit 15 value of “1” will be a soft reset. This soft reset will reset everything expect for the MDIO registers. The feature is OFF by default and must be enabled by setting register 1Ch, shadow value 01011, bit 6 = 1. After enabling the SOFT-RESET function, the PHY register 00h bit15 will not be able to self clear. Write a 0 to bit 15 of the MII Control register (address 00h) to clear it after software reset.

Mode pins that are labelled sample on reset (SOR) are latched during hardware reset. Similarly, software resets also latch new values for some SOR mode pins, except for those pins that contain LED functions. SOR mode pins that contain LED functions during normal operation retain the values latched during the previous hardware reset.

During reset, the PHY output pins connected to MAC are driven low. However, if the PHY address is set to 00h, the device is placed into isolate mode, and the PHY output pins are tristated during and after reset.

PHY ADDRESS

The B50610 allows a unique PHY address for MII management. The address is set through the logic value of the PHYA[0] pin latched during reset. The PHY checks each MII management read or write command on its MDIO pin and performs the operation only if the address in the command matches the latched PHY address stored in the device.

Setting the PHY address to 00h puts the device into isolate mode during and after reset. To return to normal operation, write a 0 to bit 10 of the MII Control register (address 00h).

ISOLATE MODE

The B50610 can be isolated from the RGMII MAC interface by writing a 1 to bit 10 of the Table 24 on page 42. When the transceiver is put into isolate mode, all RGMII MAC inputs are ignored, and all RGMII MAC outputs are tristated. While in isolate mode, the PHY still sends out link pulses or FLPs, depending on whether the PHY was configured for forced or auto-negotiation mode. A link is established if the link partner is forced or is advertising the same technologies. The MII management pins (MDC and MDIO), along with the MII registers, operate normally. In 100-pin BGA package, when the PHY address is set to 0 and the device is reset (hardware or software), the device will be put into isolate mode. Alternatively, setting bit 10 of the Table 24 on page 42 puts the transceiver in isolate mode. In either case, clearing the same bit removes the device from Isolate mode.

The B50610 can also be put into super isolate mode by writing to register 18h, shadow value 010, bit 5 = 1. Super Isolate mode tristates the RGMII outputs, ignores the RGMII input signals, and disables the transmission of copper link pulses. This mode is useful when the B50610 needs to coexist with another PHY on the same adapter card, where only one PHY is active. Unlike the Isolate mode, the super isolate mode is available only when the B50610 device is in the copper mode.

STANDBY POWER-DOWN MODE

The B50610 can be placed into standby power-down mode using software commands. In this mode, all PHY functions, except the serial management interface and CLK125 output, are disabled. To enter standby power-down mode, set "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)" on page 42, bit 11 = 1. There are three ways to exit this mode:

- Clear MII Control register (address 00h), bit 11 = 0.
- Set the software RESET bit 15, MII Control register (address 00h).
- Assert the hardware $\overline{\text{RESET}}$ pin.

Reads or writes to any MII register other than MII Control register (address 00h) while the device is in the standby power-down mode may cause unpredictable results. Upon exiting standby power-down mode, the B50610 remains in an internal reset state for 40 µs, and then resumes normal operation. When clearing the "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)" on page 42 bit 11 = 0, the internal reset state does not reset the writable MII management registers.

In the 100-pin BGA package, to save additional power, CLK125 output can be disabled by setting register 1Ch, shadow value 00101, bit 0 = 0. CLK125_NONRGMII output can be disabled by setting register 1Ch, shadow value 01011, bit 7 = 1. Also, the DLL can be powered down by setting register 1Ch, shadow value 00101, bit 1 = 0. These writes should be performed before enabling the standby power-down mode.

AUTO POWER-DOWN MODE

The B50610 can be placed into auto power-down mode to reduce chip power when the signal from the copper link partner is not present. Auto power-down mode works whether the device has copper auto-negotiation enabled or disabled. This mode is enabled by setting "Auto Power-Down Register (Address 1Ch, Shadow Value 01010)" on page 93, bit 5 = 1. However, when the B50610 is in forced 10 or 100 mode, the "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control Register (Address 18h, Shadow Value 111)" on page 75, bit 9 should be set to 1. When auto power-down mode is enabled, the B50610 automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. When the B50610 is in Auto Power-down mode, it wakes up after 2.7s or 5.4s (determined by bit 4 of "Auto Power-Down Register (Address 1Ch, Shadow Value 01010)" on page 93) and sends link pulses while monitoring for energy from the link partner. The B50610 enters normal operation and establishes a link if energy is detected, otherwise, wake-up mode continues for a duration of 84 to 1260 ms. This is determined by the timer bits [3:0] of "Auto Power-Down Register (Address 1Ch, Shadow Value 01010)" on page 93 before going back to low-power mode.

Additional power savings can be realized by disabling the DLL by writing to "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)" on page 89, bit 1 = 0. This automatically disables the DLL when energy is lost. The DLL is automatically enabled during wake-up or when energy is detected. Do not enable this mode if the CLK125 or CLK125_NONRGMII signals are used by a MAC that needs a continuously running clock source.

TXC and RXC outputs can be disabled during auto power-down by setting the "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)" on page 89, bit 8 =1.

CLK125 AND CLK125_NONRGMII CLOCK OUTPUT

In the 100-pin FBGA package, two 125 MHz output clocks are generated by the B50610 device from a 5× PLL, using the 25 MHz clock at XTALI as a reference. One is CLK125, and another one is CLK125_NONRGMII. CLK125 is powered by OVDD_RGMII, and CLK125_NONRGMII is powered by OVDD. Two 125 MHz clocks should be used only when in RGMII mode to drive ASIC and MAC clock inputs. Two clock outputs remain active during and after hardware or software reset. Two clock outputs remain active when the power-down bit (bit 11) in "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)" on page 42 is set. There are two register bits to individually disable and enable clock output. Both CLK125 and CLK125_NONRGMII are enabled by default.

There are two ways to disable the CLK125 output:

- Powering down the DLL as described in "Auto Power-Down Mode" on page 21
- In 100-pin BGA, by setting "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)" on page 89 bit 0 = 0
- In 48-pin MLP, by setting "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)" on page 89 bit 0 = 1

There are two ways to disable the CLK125_NONRGMII output:

- Powering down the DLL as described in "Auto Power-Down Mode" on page 21
- Setting "External Control 1 Register (Address 1Ch, Shadow Value 01011)" on page 95 bit 7 = 1

Note: Two CLK125 and CLK125_NONRGMII pads are disabled in the normal 48-pin MLP package. For 48-pin MLP packages, Reg 1Ch, shadow value 00101, bit 0 = 1 means disable. For 100-pin BGA package, Reg 1Ch, shadow value 00101, bit 0 = 1 means enable.

ULTRA-LOW POWER-DOWN MODE

The B50610 can be placed into the ultra-low power-down mode (IDDQ), consuming the lowest power possible while voltage is being supplied to the device. This mode is especially useful for saving battery life in laptop designs when the user does not require a network connection. In the 100-pin FBGA, the B50610 has a dedicated LOWPWR pin that is continuously sampled, allowing this feature to be easily entered or exited.

Use the following methods to enter and exit the ultra-low power-down mode:

- To enter ultra-low power-down mode (hardware method), force the LOWPWR pin high (see the following note for details on reset requirements prior to entering ultra-low power-down mode).
- To enter ultra-low power-down mode (software method), write to register 1Ch, shadow value 01100, bit 0 = 1.
- To exit ultra-low power-down mode (100-pin FBGA), set the LOWPWR pin low by doing one of the following:
  - Issue a software reset by writing to "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)" on page 42 bit 15 = 1
  - Issue a hardware reset by forcing the RESET pin low. See Table 76 on page 112 for reset timing information
- To exit ultra-low power-down mode (48-pin MLP), issue a hardware reset by forcing the /RESET pin low. See Table 76

on page 112 for reset timing information.

Note: If B50610 enters ultra-low power-down mode by writing register 1Ch, shadow value 01100, bit 0 =1, the only way to exit ultra-low power-down mode is by issuing a hardware reset.

RESET REQUIREMENTS

For normal operation (non-IDDQ mode), the LOWPWR pin must be kept low during and after either software or hardware reset. At least one hardware reset is required before entering IDDQ mode to ensure that the B50610 is properly configured before going into IDDQ mode. The LOWPWR pin must never be pulled high during hardware reset. Doing so may result in unpredictable behavior.

Note: The B50610 remains in ultra-low power-down mode until a logical low is detected on the LOWPWR pin. After exiting IDDQ mode, normal operation can be resumed following either a hardware or software reset of the chip. The software reset can be used only if a hardware reset has been done at least once since power was applied to the B50610.

INTERNAL LOOPBACK MODE

All packets sent through the RGMII TXD pins are looped back internally to the RGMII RXD pins. The transmitter outputs TRD± are set to high impedance, and incoming packets on the cable are ignored. Loopback mode can be entered by writing a 1 to bit 14 of the MII Control register (Address 00h). To resume normal operation, bit 14 of the MII Control register must be 0.

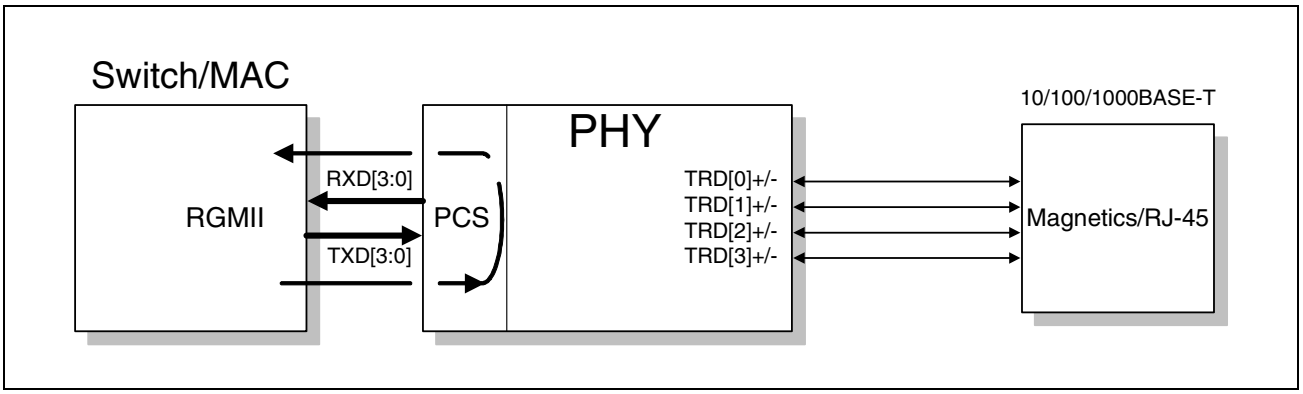


Figure 5: Internal Loopback Mode

LINESIDE (REMOTE) LOOPBACK MODE

Lineside loopback mode allows the testing of the copper MDI interface from the link partner. This mode is enabled by setting bit 15 of the "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register (Address 18h, Shadow Value 100)" on page 73.The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. The PCS receive data appears on the MAC interface. The MAC interface can be tristated by setting bit 11 of the "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register (Address 18h, Shadow Value 100)" on page 73.

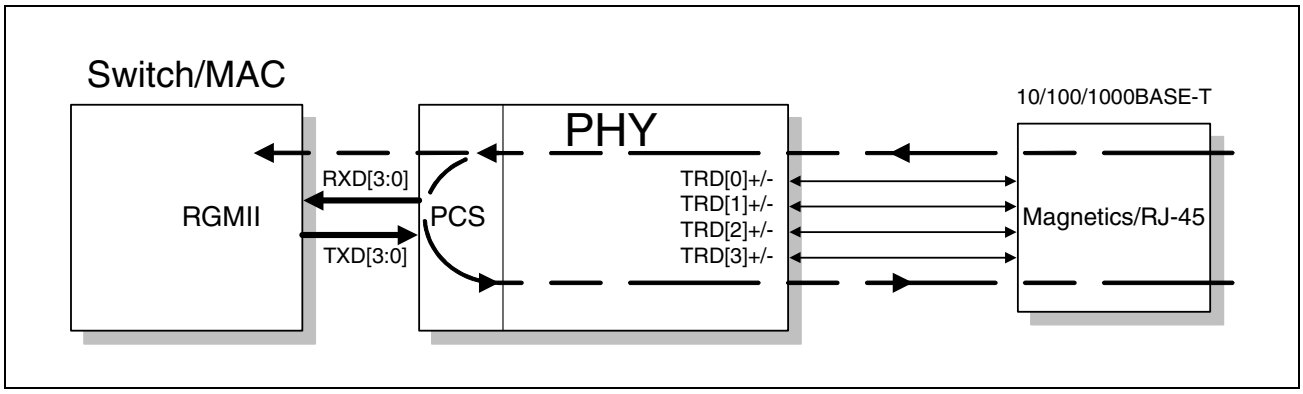


Figure 6: Lineside (Remote) Loopback Mode

EXTERNAL LOOPBACK MODE

The External Loopback mode allows in-circuit testing of the B50610 as well as the transmit path through the magnetics and the RJ-45 connector. External Loopback can be performed with or without a jumper block. External loopback using a jumper block tests the path through the magnetics and RJ45 connector. External loopback without the jumper block, only tests the B50610's transmit and receive circuitry. In 1000BASE-T, 100BASE-TX, and 10BASE-T modes, a jumper block must be inserted into the RJ-45 connector to support external loopback. The jumper block should have the following RJ-45 pins connected together:

1----------3
2----------6
4----------7
5----------8

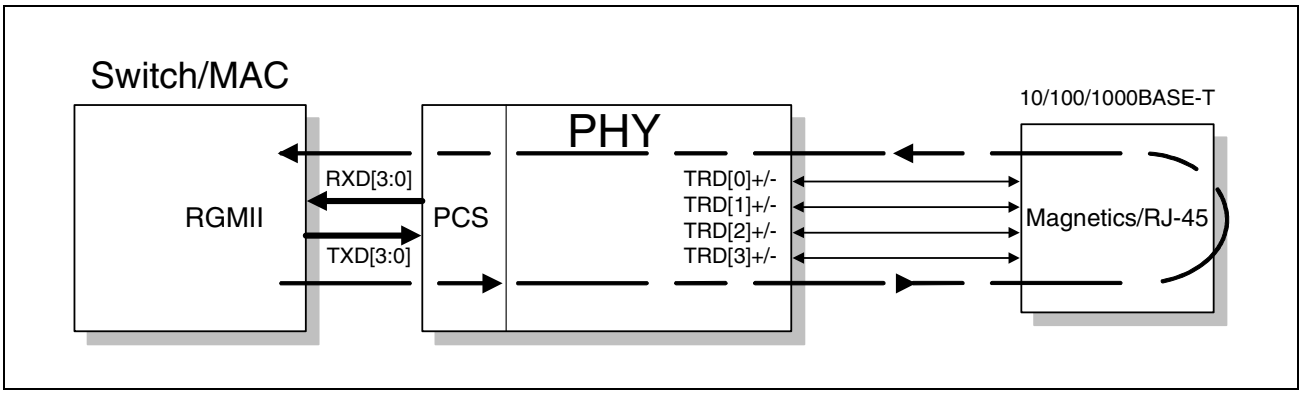


Figure 7: External Loopback Mode

The following tables describe how the external loopback is enabled for 1000BASE-T, 100BASE-TX, and 10BASE-T modes with and without a jumper block.

Table 3: 1000BASE-T External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 1800h to register 09h	Enable 1000BASE-T Master mode
Write 0140h to register 00h	Enable Force 1000BASE-T
Write 8400h to register 18h	Enable External Loopback mode with external loopback plug

Table 4: 1000BASE-T External Loopback Without External Loopback Plug

Register Writes	*Comments*
Write 1800h to register 09h	Enable 1000BASE-T Master mode
Write 0140h to register 00h	Enable Force 1000BASE-T
Write 0014h to register 18h	Enable External Loopback mode without external loopback plug
Write 8400h to register 18h	Enable External Loopback mode

Table 5: 100BASE-TX External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 2100h to register 00h	Enable Force 100BASE-TX Full-Duplex mode
Write 8400h to register 18h	Enable External Loopback mode with external loopback plug

Table 6: 100BASE-TX External Loopback Without External Loopback Plug

Register Writes	*Comment*
Write 2100h to register 00h	Enable force 100BASE-TX full-duplex mode
Write 0014h to register 18h	Enable external loopback mode without external loopback plug
Write 8400h to register 18h	Enable external loopback mode

Table 7: 10BASE-TX External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 0100h to register 00h	Enable force 10BASE-T full-duplex mode
Write 8400h to register 18h	Enable external loopback mode with external loopback plug

Table 8: 10BASE-T External Loopback Without External Loopback Plug

Register Writes	*Comments*
Write 0100h to register 00h	Enable force 10BASE-T full-duplex mode
Write 0014h to register 18h	Enable external loopback mode without external loopback plug
Write 8400h to register 18h	Enable external loopback mode

Note: To exit the external loopback mode, Broadcom recommends a software or hardware reset.

FULL-DUPLEX OPERATION

The B50610 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable.

When auto-negotiation is disabled, full-duplex operation can be enabled by setting bit 8 of the "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)" on page 42. The default value is controlled by the FDX pin at reset.

When auto-negotiation is enabled, the full-duplex capability is advertised for:

- 10BASE-T when bit 6 in the "1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement Register (Address 04h)" on page 48 is set.
- 100BASE-TX when bit 8 in the "1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement Register (Address 04h)" on page 48 is set.
- 1000BASE-T when bit 9 in the "1000BASE-T Control Register (Address 09h)" on page 55 is set.

In the 100-pin FBGA package, the default value of all three advertisement bits is controlled by the $\overline{\text{LED1/ANEN}}$, FDX, F1000, and SPD0 pins, but the bits can be overwritten at any time after reset.

ETHERNET@WIRESPEED™ MODE

As equipment is upgraded from Fast Ethernet to Gigabit, some cable plants that operate perfectly at 10/100 Mbps speeds can lock up using standard IEEE-compliant Gigabit PHYs. Broadcom PHYs provide Ethernet@Wirespeed functionality to prevent lockup. This function is fully compatible with IEEE standards and needs only to be implemented on one end of a link. When enabled, a link continues to be established even if pair 3 or 4 is broken, missing, or shorted.

Ethernet@Wirespeed must be enabled in software by setting register 0x18, shadow 111, bit 4 = 1. Wirespeed downgrades are set in register 0x1C, shadow 4h, bits 4:2 as follows:

000 = downgrade after 2 failed link attempts.

001 = downgrade after 3 failed link attempts.

010 = downgrade after 4 failed link attempts.

011 = downgrade after 5 failed link attempts. (Default Value)

.....

111 = downgrade after 9 failed link attempts.

MASTER/SLAVE CONFIGURATION

In 1000BASE-T mode, the B50610 and its link partner perform loop timing. One end of the link must be configured as the timing master and the other end as the slave, as defined by IEEE 802.3ab. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port as the slave. However, if both partners are configured with identical repeater/DTE settings, each will generate an 11-bit random seed. The partner with the higher seed is configured as the master. If the local PHY and the link partner happen to generate the same random seed, auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave) or the random seeds match seven consecutive times, the B50610 sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register, and auto-negotiation is restarted.

NEXT PAGE EXCHANGE

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the B50610 and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the B50610 is configured to advertise 1000BASE-T capability.

The B50610 also supports software controlled Next Page exchanges. When bit 15 of Table 27 on page 48 is written to a 1, all Next Page transactions are controlled through the MII management interface. This includes the three 1000BASE-T Next Pages, which are always sent first. The B50610 automatically generates the appropriate message code field for the 1000BASE-T pages. When the B50610 is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the B50610 is not configured to advertise 1000BASE-T capability and bit 15 of the "1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement Register (Address 04h)" on page 48 is 0, the B50610 does not advertise Next Page ability.

RGMII INTERFACE

The B50610 can communicate with Ethernet MACs through a reduced-pin-count Gigabit MII known as RGMII. This interface reduces the number of MAC signal pins by half with respect to GMII. Transmit and receive data are transferred on both edges of the GTXCLK and RXC clocks, respectively. The GTXCLK and RXC clock rates are:

- 125 MHz for 1000 Mbps data
- 25 MHz for 100 Mbps data
- 2.5 MHz for 10 Mbps data

Data is sent with the least significant nibble first. In the 100-pin FBGA package, the RGMII mode can be enabled by hardware. See Table 1: "Hardware Mode Selection," on page 1 for an explanation of hardware-enabled settings. In the 48-pin MLP package, the RGMII mode can be enabled by hardware or software. See "External Control 1 Register" on page 95 for an explanation of hardware-enabled settings.

To enable by software, write register 1Ch, shadow 01011, bits [4:3]. See "External Control 1 Register" on page 95.

While in copper mode, the RGMII receive timing can be adjusted, if needed, by software control. The RXD-to-RXC skew time can be delayed by approximately 1.9 ns by setting bit 8 of register 18h, shadow value 111.

The RGMII transmit timing can be adjusted, if needed, by software or hardware control. The TXD to GTXCLK delay time can be increased by approximately 1.9 ns by setting bit 9 of register 1Ch, shadow value 00011. Using these timing adjustments, the board designer can eliminate the need for board delay traces required by the RGMII specification.

Table 9: RGMII Transmit Data

RGMII Signal	*Signal Latched at GTXCLK Rising Edge*	*Signal Latched at GTXCLK Falling Edge*
TX_EN	TX_EN	TX_EN (XOR) TX_ER
TXD[3]	TXD[3]	TXD[7]
TXD[2]	TXD[2]	TXD[6]
TXD[1]	TXD[1]	TXD[5]

Table 9: RGMII Transmit Data

RGMII Signal	*Signal Latched at GTXCLK Rising Edge*	*Signal Latched at GTXCLK Falling Edge*
TXD[0]	TXD[0]	TXD[4]

Table 10: RGMII Receive Data

RGMII Signal	*Signal Latched at RXC Rising Edge*	*Signal Latched at RXC Falling Edge*
RX_DV	RX_DV	RX_DV (XOR) RX_ER
RXD[3]	RXD[3]	RXD[7]
RXD[2]	RXD[2]	RXD[6]
RXD[1]	RXD[1]	RXD[5]
RXD[0]	RXD[0]	RXD[4]

INTERNAL VOLTAGE REGULATOR

One voltage regulator is provided to ease power supply requirements for designs which may otherwise lack a 1.2V power supply. The regulator is internal and does not rely on external components.

The regulator output pin REGOUT automatically outputs 1.2V when REGIN is supplied with 2.5V to 3.3V.

When connected as described, the output pin REGOUT is brought out to allow filtering and power distribution.

Note: The regulator can supply a maximum of 200 mA.

DUAL INPUT CONFIGURATION/LED OUTPUT FUNCTION

All four LEDs pins have secondary functions. These pins serve as an input pin during the power-on/reset sequence. The logic level of the pin is sampled at reset and configures the secondary function. After the reset process is completed, the pin acts as an output LED during normal operation. The polarity of the output LED is determined based on the latched input value at reset. For example, if the value at the pin is high during reset, the LED output during normal operation is active-low. The user must first decide, based on the individual application, the values of the input configuration pin shown in Table 11 to provide the correct device configuration. The LED circuit must then be configured to accommodate either an active-low or active-high LED output (see Figure 8).

Table 11: Dual Input Configuration/LED Outputs

LED Output (Normal Operation)	*Input Configuration Pin (Latched During Reset)*
LED1	ANEN (100-pin FBGA Package)

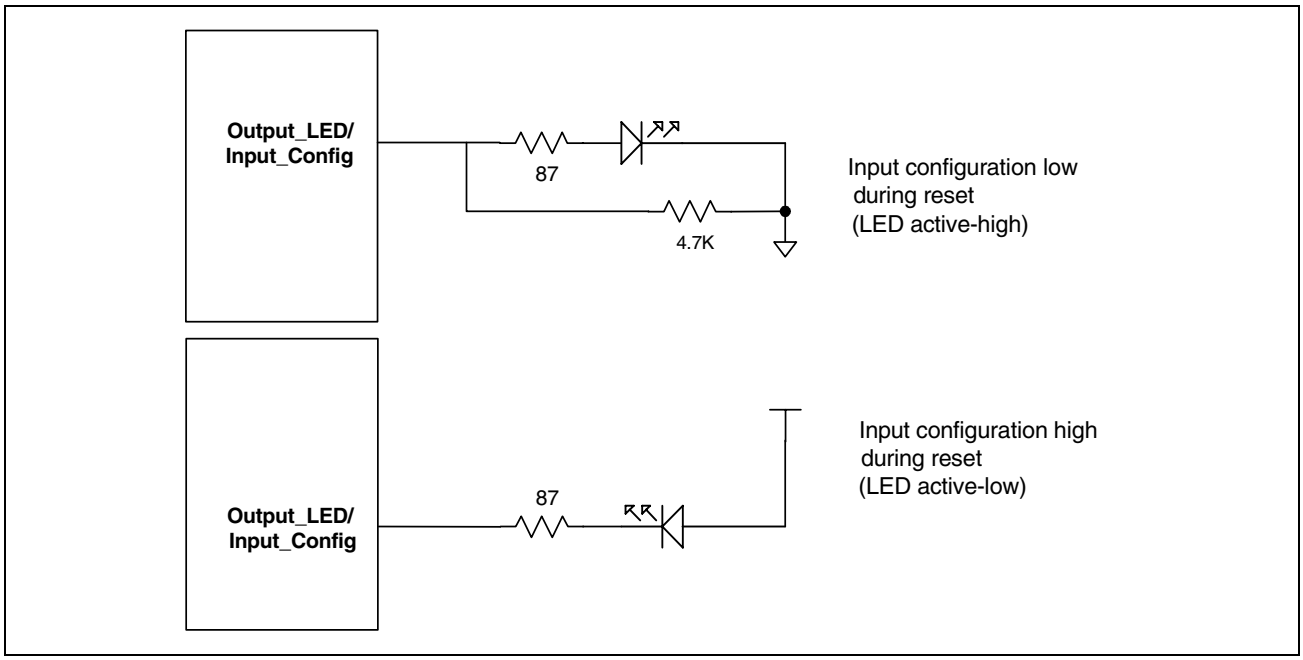


Figure 8: LED Circuit for Dual Input Configuration/LED Output Pins

GENERAL-PURPOSE LED PROGRAMMABILITY

The B50610 has four LED pins that can be programmed to one of many useful LED functions. Four 4-bit control register words are provided to allow the user to select the LED function for each of the pins. These control words are located in register 1Ch, shadow value 01101 and shadow value 01110. Table 12 details each of the four programmable LEDs, their corresponding register bits, and default settings.

Table 12: Programmable LEDs

100-Pin FBGA	*48-Pin MLP*	*Pin Name*	*Register Bits*	*Default Value*	*Default Function*
G7	45	LED1	Register 1C, Shadow Value 01101, Bits[3:0]	0000	LINKSPD[1]
G6	44	LED2		0001	LINKSPD[2]
H6	43	LED3	Register 1C, Shadow Value 01110, Bits[3:0]	0011	ACTIVITY
G10	42	LED4	Register 1C, Shadow Value 01110, Bits[7:4]	0110	INTR

Each of the output functions exists as an internal device signal that is multiplexed to a given general-purpose LED pin when the corresponding register bits are written with the appropriate register value. Figure 9 is a graphical representation of the multiplexer functionality of the programmable LED and uses LED1 as an example.

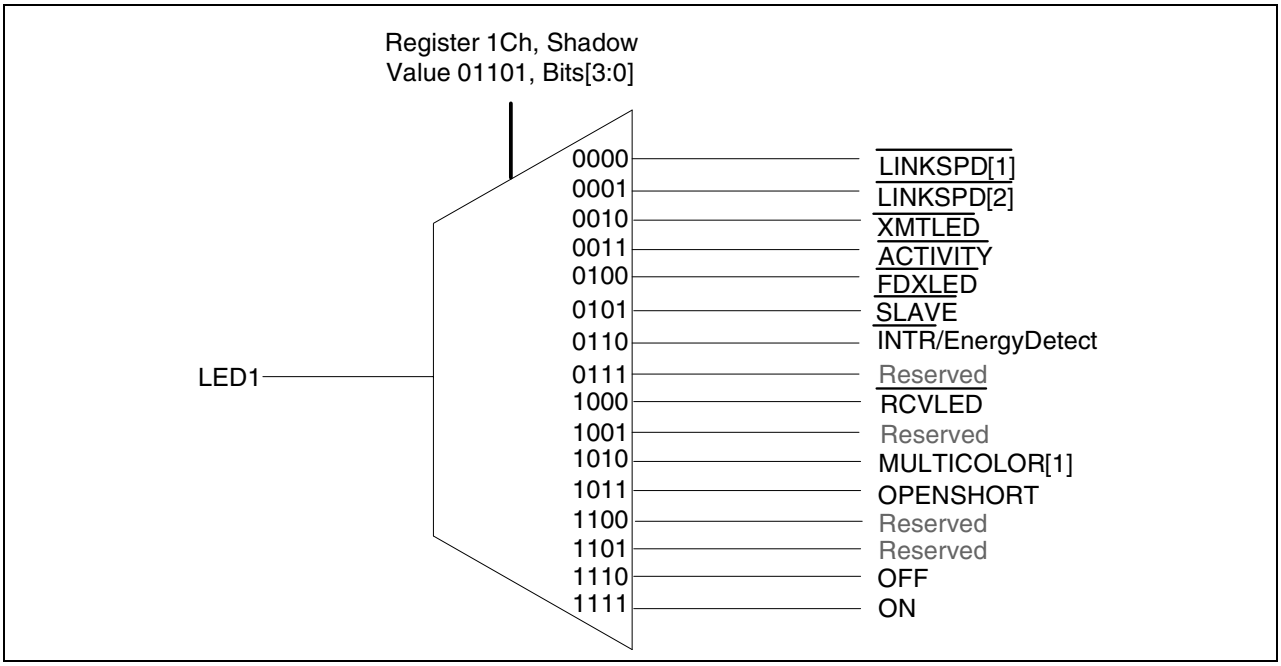


Figure 9: Programmable LED Multiplexer

When LEDs are programmed to $\overline{\text{LINKSPD[1]}}$ and $\overline{\text{LINKSPD[2]}}$ function, it indicates the link and speed status of the copper interface as shown in Table 13 on page 32.

Table 13: LINKSPD[2:1] LED Function

LINKSPD[2]	*$\overline{\text{LINKSPD[1]}}$*	*Link/Speed*
0	0	Linked @ 1000BASE-T
0	1	Linked @ 100BASE-TX
1	0	Linked @ 10BASE-T
1	1	No link

48-PIN MLP PACKAGE HARDWARE CONFIGURATION

Test pins TEST[3:2] can be used to set the B50610 to enter three different modes: JTAG mode (test mode), normal operation mode, and PHYA mode.

JTAG MODE

When TEST[3:2] = 01, the device enters in a test mode where JTAG operations can be executed. In this mode, the following pins change their regular functions for the JTAG signal functions.

Table 14: 48-Pin MLP Active Pin Test Function in JTAG Mode

Pin Names	*Active Function*
LED[3]	TDO
LED[2]	TDI
LED[1]	TMS
PHYA[0]	TCK

NORMAL OPERATION MODE AND PHYA MODE

When TEST[3:2] = 00 or 11, the device will operate normally. In these two modes, the user must decide the configuration (operation mode) of B50610. There are three sets of parameters that must be provisioned for the device: PHY address, RGMII mode, and LOM LED mode.

PHY Address

The physical address of the B50610 is determined by the voltage levels in PHYA[0] and TEST[3:2] pins. Table 15 shows the four possible PHY addresses for the B50610.

Table 15: 48-Pin MLP PHY Address Based on PHYA[0] and TEST[3:2] Settings

		TEST[3:2]	
PHYA[0]	–	00	11
	0	0x0	0x18
	1	0x1	0x19

RGMII LED Mode

RGMII modes can be selected by setting LED[3:2] during power on reset. Table 16 shows the various MAC interface (RGMII) modes available in the device.

Note: LED[4] = 0.

Table 16: 48-Pin MLP RGMII Mode

LED[3:2]	*MAC RGMII Mode*
0 0	RGMII 3.3V
0 1	RGMII 2.5V
1 0	RGMII HSTL 1.8V
1 1	Reserved

LOM LED Mode

LOM LED mode is a simplified LED reporting mode that uses LED[2:1] to show the operating link signal rate. Table 17 shows the definition of LED link signal rate reporting. The LOM LED can be enabled by pull-high LED[4] during power on reset.

Table 17: 48-Pin MLP LOM LED Link Signal Rate Reporting

LED[2:1]	*MAC RGMII Mode*
0 0	–
1 0	1G Link
0 1	100M Link
1 1	Others

This mode has two RGMII modes (voltage-level communicating with MAC) shown in Table 18.

Table 18: 48-Pin MLP RGMII Modes for LOM LED Operation

LED[3]	*MAC RGMII Mode*
0	RGMII 3.3V
1	RGMII HSTL 1.8V

TEST AND LED CONFIGURATION MATRIX

Table 19 and Table 20 show the 48-pin MLP package TEST[3:2] and LED[4:1] hardware configuration matrix.

Table 19: Using TEST[3:2] Pins to Set JTAG, Normal Operation, and PHYA Modes

TEST[3:2]	*JTAG Mode 01*	*Normal Operation 00*		*PHYA Mode 11*	
LED[4][a]	–	1a	0	1a	0
LED[3]	TDO	MODE_SEL[1]	MODE_SEL[1]	MODE_SEL[1]	MODE_SEL[1]
LED[2]	TDI	–	MODE_SEL[0]	–	MODE_SEL[0]
LED[1]	TMS	–	–	–	–
PHYA[0]	TCK	PHYA[0]	PHYA[0]	0x18+PHYA[0]	0x18+PHYA[0]

a. LED[4] is sampled during reset as LOM LED mode, active-high. When LED[4] is set to non-LOM LED mode, LED[2] will be MODE_SEL[0] function, active-high.

Table 20: 48-Pin MLP Package RGMII Mode Selection

RGMII Mode	*MODE_SEL[1,0]*	*Pin Configuration*			
RGMII 3.3V	00	TEST[3:2]=00 or 11	LED[3]=0	LED[2]=0	LED[4]=0
RGMII 2.5V	01	TEST[3:2]=00 or 11	LED[3]=0	LED[2]=1	LED[4]=0
RGMII HSTL 1.8V	10	TEST[3:2]=00 or 11	LED[3]=1	LED[2]=0	LED[4]=0
Reserved	11	TEST[3:2]=00 or 11	LED[3]=1	LED[2]=1	LED[4]=0
RGMII 3.3V	00	TEST[3:2]=00 or 11	LED[3]=0	LED[2]=X[a]	LED[4]=1
RGMII HSTL 1.8V	10	TEST[3:2]=00 or 11	LED[3]=1	LED[2]=X[a]	LED[4]=1

a. X = Don’t care

For the 48-pin MLP package, LOM LED mode and MODE_SEL[1:0] can also be configured via registers 1Ch Shadow Value “01011” bits[4:2] after reset.

INTERRUPT FUNCTION

The B50610 can be programmed to provide an interrupt output based on changes in the PHY status. Each individual interrupt condition is represented by a read-only bit in the "1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah)" on page 80. Interrupts can be individually masked by setting or clearing bits in the interrupt mask register, in "1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh)" on page 83. When an unmasked interrupt condition occurs, programmed LED pins to $\overline{\text{INTR}}$ function are driven low until the interrupt is cleared. Most interrupts are cleared automatically by reading the Interrupt Status register.

The interrupt function can be globally disabled by setting the interrupt disable bit, register 10h, bit 12. The $\overline{\text{INTR}}$/EnergyDetect pin can be changed to indicate an energy-detect function by setting register 1Ch, shadow value 00100, bit 1= 1.

LED MODES

Many additional LED functions and modes are supported by the B50610. Table 21 on page 36 describes many of these modes in detail.

The LEDs can be forced on by setting bit 4 of register 10h. This forces all LEDs on continuously. Similarly, the LEDs can be forced off continuously by setting bit 3 of register 10h. This overrides all other LED modes except the force LEDs ON mode. Any LED output pin programmed to be in the INTR mode is open-drain, to allow multiple devices to be connected in a wire-OR fashion. For all other LED modes, LED output pins are continuously driven.

Table 21 on page 36 describes the different modes in which each individual pin can be programmed. For each pin, the modes are listed in order of priority. For example, when the receive LED is programmed to one of the link-utilization modes, the register bit enabling activity/link LED mode is not relevant. The last mode listed for each pin is the default mode.

MULTICOLOR LED

The $\overline{\text{MULTICOLOR}}$ mode uses two programmable LED output pins to control one single LED unit that is capable of producing three different colors: green, amber, red. The multicolor LED mode is enabled by writing value B4AAh to "1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101)" on page 97. After this register write, the multicolor LED signals appear on LED1 and LED2. Alternatively, the multicolor LED can be output on LED3 and LED4 by writing B8AAh to "1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 Register (Address 1Ch, Shadow Value 01110)" on page 99. The subfunction and other parameters can be selected by setting control bits in Table 72 on page 107, "Expansion Register 05h: Multicolor LED Flash Rate Controls" on page 109, and "Expansion Register 06h: Multicolor LED Programmable Blink Controls" on page 110.

OPEN/SHORT LED

The OPENSHORT LED is a function of the cable diagnostic mode. The OPENSHORT LED can be programmed to appear on any of the programmable LEDs by writing to the appropriate LED Selector register.

> ***Example:*** Write value B40Bh to "1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101)" on page 97.

This LED turns on after the cable diagnostic function is completed and when an open or short is found on any of the four cable pairs attached to the PHY.

ENERGY LINK LED

When one of the programmable LED outputs is programmed in the ENERGYLNK mode, the LED uses blinking and solid on appearances to indicate energy detection and valid links. The ENERGYLNK LED is off when there is no link or energy detected. The LED blinks as soon as energy is detected on the wire. When the link is established, the LED remains continuously on for the duration. Shortly after a loss of energy is detected, the ENERGYLNK LED begins to blink and remains in this state for the length of the Disconnect Timer value, defined in Register 1Ch, Shadow value 10000, bits 3:0. After the timer expires, the LED is turned off.

ADDITIONAL LED MODES

Some of the LEDs can also be programmed to additional modes. The different modes that each LED output can assume are described in Table 21 on page 36. Because the modes are listed in the order of priority for each pin, the register bit enabling activity/link LED mode is not relevant when the receive LED is programmed to one of the link utilization modes. The last mode listed for each pin is the default mode. The table is valid for devices configured to RGMII Copper mode only.

Table 21: LED Modes

LEDs	*Description*
All LEDs (except for INTR and OPENSHORT modes)	Force LEDs: • On (register 10h, bit 4 = 1): LED is on solid. • Off (register 10h, bit 3 = 1): LED is off solid.
All LEDs	• General purpose I/O input mode • General purpose I/O output mode (default) Register address 1Ch, shadow value 01111, bits 3:0 = 0000. Each port can be individually programmed to input or output mode.

Table 21: LED Modes (Cont.)

LEDs	*Description*
$\overline{\text{ACTIVITY}}$ LED	Link utilization: This mode provides the estimated activity in terms of blink rate. The blink rate of the LED increases as the activity duty cycle increases by 10% increments. For duty cycles of 0.001%–10%, the LED blinks at 3 Hz; for duty cycles of 10%–20%, the LED blinks at 6 Hz; and for duty cycles of 90%–96%, the LED blinks at 30 Hz. Though the frequency of the LED blink increases, the duty cycle of the LED stays at about 50%. This LED mode is enabled to include all activity, transmit activity only, or receive activity only. • Transmit (register 1Ch, shadow value 01001, bits[1:0] = 01) • Receive (register 1Ch, shadow value 01001, bits[1:0] = 10) • Activity (register 1Ch, shadow value 01001, bits[1:0] = 11) Activity/link LED (register 1Ch, shadow value 01001, bits 4 = 1; register 10h, bit 5 = 0): LED is off when there is no link. The LED is on when there is a link. The LED blinks when the link is up and there is either transmit or receive activity. The LED blinks with a 167 ms cycle and a 50% duty cycle. Receive (register 1Ch, shadow value 01001, bit 3 = 0): This mode expresses receive activity in either of the two modes described below: • Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if activity occurs. Activity (default): This mode expresses both transmit and receive activity in either of the two modes described below. • Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if activity occurs.
$\overline{\text{XMTLED}}$ LED	• Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for entire cycle if TX activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if TX activity occurs.
$\overline{\text{RCVLED}}$ LED	• Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if TX activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if TX activity occurs.
$\overline{\text{INTR}}$ LED/SD Input (Open Drain)	• Force interrupt (register 10h, bit 11 = 1): LED is forced continuously on. • Disable interrupt (register 10h, bit 12 = 1): LED is forced continuously off. • Normal interrupt (default): LED is forced continuously on until interrupt is cleared.
LOM LED Mode	In the 48-pin MLP package, if TEST[3:2] pins are 00 or 11, LED[4] can be used to set the B50610 to enter LOM LED mode. Active-high.

Status	*LED[2]*	*LED[1]*
1000BASE-T	1	0
100BASE-T	0	1
10BASE-T	1	1
No link	1	1

Section 4: Register Summary

MII Management Interface Register Programming

The B50610 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MII management interface registers are written and read serially, using the MDIO and MDC pins. A clock of up to 12.5 MHz must drive the MDC pin of the B50610. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

Preamble (PRE)

To signal the beginning of an MII instruction after reset, at least 32 consecutive 1 bits must be written to the MDIO pin of the B50610. A preamble of thirty-two 1 bits is required only for the first read or write following reset. If bit 6 of MII register 01h is cleared, a preamble is always required. A preamble of fewer than thirty-two 1 bits causes the remainder of the instruction to be ignored.

Start of Frame (ST)

A 01 pattern indicates that the start of the instruction follows.

Operation Code (OP)

A read instruction is indicated by 10, while a write instruction is indicated by 01.

PHY Address (PHYAD)

A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.

Register Address (REGAD)

A 5-bit register address follows, with the MSB transmitted first. The addresses for the registers used by the B50610 are shown in Table 23 on page 40.

Turnaround (TA)

The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is performed, 10 must be sent to the B50610 chip during these 2 bit times. When a read operation is performed, the MDIO pin of the MAC must be put in a high-impedance state during these bit times. The B50610 transceiver drives the MDIO pin to 0 during the second bit time.

DATA

The last 16 bits of the instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first. During a read operation, the data bits are driven by the B50610 with the MSB transmitted first.

The complete management frame format is summarized in Table 22.

When writing to the MDIO pin, the bit value must be stable for 10 ns before the rising edge of the MDC and must be held valid for 10 ns after the rising edge of the MDC. When reading from the MDIO pin, the data bit is valid at the rising edge of the MDC until the next falling edge of the MDC.

Example: To put a PHY with address 00001 into loopback mode, issue the following write MII instruction:

1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000

To determine if a PHY is in the link-pass state, issue the following read MII instruction:

1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ

The B50610 drives the MDIO line during the last 17 bit times. If the link status is good, the third bit from the end (bit 2) is 1.

Table 22: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*Data*	*Direction*
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Driven to B50610 Driven by B50610
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Driven to B50610

REGISTER MAP

The following table contains the set of registers for the B50610 transceiver.

Table 23: Register Map

Address	*Register Table*
1000BASE-T/100BASE-TX/10BASE-T Registers	
00h	"1000BASE-T/100BASE-TX/10BASE-T MII Control" on page 42
01h	"1000BASE-T/100BASE-TX/10BASE-T MII Status" on page 44
02h–03h	"1000BASE-T/100BASE-TX/10BASE-T PHY Identifier" on page 47
04h	"1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement" on page 48
05h	"1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Link Partner Ability" on page 50
06h	"1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Expansion" on page 52
07h	"1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit" on page 53
08h	"1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page" on page 54
09h	"1000BASE-T Control" on page 55
0Ah	"1000BASE-T Status" on page 56
0Ch–0Eh	Reserved (do not read from or write to a reserved register)
0Fh	"1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status" on page 58
10h	"1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control" on page 59
11h	"1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status" on page 62
12h	"1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter" on page 65
13h	"1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter" on page 65
14h	"1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter" on page 65
15h–16h	Reserved. (Do not read from or write to a reserved register except for accessing the Expansion registers through register 15h.)
17h	"1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access" on page 66
18h	• "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 67 • "10BASE-T" on page 70 • "1000BASE-T/100BASE-TX/10BASE-T Power/MII Control" on page 72 • "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register" on page 73 • "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control" on page 75
19h	"1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary" on page 77
1Ah	"1000BASE-T/100BASE-TX/10BASE-T Interrupt Status" on page 80
1Bh	"1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask" on page 83

Table 23: Register Map (Cont.)

Address	*Register Table*
1Ch	• "1000BASE-T/100BASE-TX/10BASE-T Spare Control 1" on page 85 • "1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control" on page 87 • "1000BASE-T/100BASE-TX/10BASE-T Spare Control 2" on page 88 • "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3" on page 89 • "1000BASE-T/100BASE-TX/10BASE-T LED Status" on page 90 • "1000BASE-T/100BASE-TX/10BASE-T LED Control" on page 92 • "1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down" on page 93 • "External Control 1 Register" on page 95 • "1000BASE-T/100BASE-TX/10BASE-T LED Selector 1" on page 97 • "1000BASE-T/100BASE-TX/10BASE-T LED Selector 2" on page 99 • "1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status" on page 100
1Dh	• "1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed" on page 101 • "1000BASE-T/100BASE-TX/10BASE-T HCD Status" on page 102
1Eh	"1000BASE-T/100BASE-TX/10BASE-T Test Register 1" on page 105
1Fh	Reserved. (Do not read from or write to a reserved register.)
Registers (Enabled by Register 1Ch, Shadow Value 11111, Bit 0 = 1)	
07h–0Eh	Reserved. (Do not read from or write to reserved register.)
Expansion Registers: Read/Write Through Register 15h (Accessed by Writing to Register 17h, Bits [11:0] = 1111 + Expansion Register Number)	
00h	"Expansion Register 00h: Receive/Transmit Packet Counter" on page 106
04h	"Expansion Register 04h: Multicolor LED Selector" on page 107
05h	"Expansion Register 05h: Multicolor LED Flash Rate Controls" on page 109
06h	"Expansion Register 06h: Multicolor LED Programmable Blink Controls" on page 110

REGISTER NOTATIONS

In the register description tables, the following notation in the R/W column is used to describe the ability to read or write:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Self-clearing
- CR = Clear on reset

Reserved bits must be written as the default value and ignored when read.

1000BASE-T/100BASE-TX/10BASE-T REGISTERS DESCRIPTIONS

1000BASE-T/100BASE-TX/10BASE-T MII CONTROL

Table 24: 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)

Bit	Name	R/W	Description	Default
15	Reset	R/W SC	1 = PHY reset 0 = Normal operation	0
14	Internal Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Speed Selection (LSB)	R/W	Bits [6,13]: 1 1 = Reserved 1 0 = 1000 Mbps 0 1 = 100 Mbps 0 0 = 10 Mbps	SPD0 pin and F1000 pin
12	Auto-negotiation Enable	R/W	1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	ANEN
11	Power Down	R/W	1 = Power down 0 = Normal operation	0
10	Isolate	R/W	1 = Electrically isolate PHY from RGMII 0 = Normal operation	0
9	Restart Auto-negotiation	R/W SC	1 = Restarting auto-negotiation 0 = Auto-negotiation restart complete	0
8	Duplex Mode	R/W	1 = Full-duplex 0 = Half-duplex	FDX pin
7	Collision Test Enable	R/W	1 = Enable the collision test mode 0 = Disable the collision test mode	0
6	Speed Selection (MSB)	R/W	Work in conjunction with bit 13	F1000 pin
5:0	Reserved	R/W	Write as 00h, ignore on read	00h

Reset

To reset the B50610 by software control, a 1 must be written to bit 15 of the MII Control register. This bit clears itself after the reset process is complete and does not need to be cleared using a second MII write. Writes to other MII Control register bits have no effect until the reset process is completed, which requires approximately 2.0 µs. Writing a 0 to this bit has no effect. A 1 is returned when this bit is read during the reset process; otherwise, it returns a 0.

Internal Loopback

The B50610 can be placed into internal loopback mode by setting bit 14 of the MII Control register. Loopback mode can be cleared by writing a 0 to bit 14 of the MII Control register or by resetting the chip. A 1 is returned when this bit is read and the chip is in loopback mode; otherwise, it returns a 0.

Speed Selection (LSB)

When auto-negotiation is disabled, bits 6 and 13 of the MII Control register can be used to manually select the speed of operation. When bit 6 is set and bit 13 is cleared, 1000BASE-T operation is selected. When bit 6 is cleared and bit 13 is set, 100BASE-TX operation is selected. When both bits are cleared, 10BASE-T operation is selected. Setting both bits is not permitted. When read, these bits return the last value written. The default values of these bits are determined by the state of the SPD0 and F1000 pins at reset.

Auto-Negotiation Enable

When bit 12 of the MII Control register is set, the B50610 mode of operation is controlled by auto-negotiation. When this bit is cleared, the B50610 mode of operation is determined by the Manual Speed, Duplex mode, and Master/Slave Configuration bits. A 1 is returned when this bit is read with auto-negotiation enabled; otherwise, it returns a 0. The default value of this bit is determined by the state of the ANEN pin at reset.

Power-Down

When bit 11 of the MII Control register is set, the B50610 is placed into low-power standby mode.

Isolate

The B50610 can be isolated from the RGMII bus by setting bit 10 of the MII Control register. All RGMII outputs are tristated, and all RGMII inputs are ignored. Because the management interface is still active, isolate mode can be cleared by writing a 0 to bit 10 of the MII Control register or by resetting the chip. A 1 is returned when this bit is read and the chip is in isolate mode; otherwise, it returns a 0. The default of this bit is a 0.

Restart Auto-Negotiation

Setting bit 9 of the MII Control register forces the auto-negotiation process to be restarted, regardless of the current state of the auto-negotiation state machine. When auto-negotiation is enabled, setting this bit restarts the auto-negotiation process. Clearing this bit has no effect. This bit is self-clearing. After the auto-negotiation process has restarted, it returns a value of 0.

Duplex Mode

When auto-negotiation is disabled, duplex mode can be controlled by writing to bit 8 of the MII Control register. Setting this bit forces the B50610 into full-duplex operation, and clearing this bit forces the B50610 into half-duplex operation. When this bit is read, it returns the last value written. The default value of this bit is determined by the FDX pin at reset.

Speed Selection (MSB)

When auto-negotiation is disabled, bits 6 and 13 of the MII Control register can be used to manually select the speed of operation. When bit 6 is set and bit 13 is cleared, 1000BASE-T operation is selected. When bit 6 is cleared and bit 13 is set, 100BASE-TX operation is selected. When both bits are cleared, 10BASE-T operation is selected. Setting both bits is not permitted. When read, these bits return the last value written. The default values of these bits are determined by the state of the SPD0 and F1000 pins at reset.

Collision Test

The B50610 can be placed into Collision Test mode by setting to bit 7 of the MII Control register. In this mode, the COL pin is asserted whenever the TX_EN pin is driven high. The Collision Test mode can be cleared by writing a 0 to bit 7 of the MII Control register or by resetting the chip. A 1 is returned when this bit is read and the chip is in Collision Test mode; otherwise, it returns a 0.

1000BASE-T/100BASE-TX/10BASE-T MII STATUS

Table 25: 1000BASE-T/100BASE-TX/10BASE-T MII Status Register (Address 01h)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capable	RO L	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
14	100BASE-X Full-duplex Capable	RO H	1 = 100BASE-X full-duplex capable 0 = Not 100BASE-X full-duplex capable	1
13	100BASE-X Half-duplex Capable	RO H	1 = 100BASE-X half-duplex capable 0 = Not 100BASE-X half-duplex capable	1
12	10BASE-T Full-duplex Capable	RO H	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1
11	10BASE-T Half-duplex Capable	RO H	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1
10	100BASE-T2 Full-duplex Capable	RO L	1 = 100BASE-T2 full-duplex capable 0 = Not 100BASE-T2 full-duplex capable	0
9	100BASE-T2 Half-duplex Capable	RO L	1 = 100BASE-T2 half-duplex capable 0 = Not 100BASE-T2 half-duplex capable	0
8	Extended Status	RO H	1 = Extended status information in reg 0Fh 0 = No extended status information in reg 0Fh	1
7	Reserved	RO	Ignore on read	0
6	Management Frames Preamble Suppression	RO H	1 = Preamble can be suppressed 0 = Preamble always required	1
5	Auto-negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation in progress	0
4	Remote Fault	RO LH	1 = Remote fault detected 0 = No remote fault detected	0
3	Auto-negotiation Ability	RO H	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link-Pass state) 0 = Link is down (link fail state)	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO H	1 = Extended register capabilities 0 = No extended register capabilities	1

100BASE-T4 Capable

The B50610 is not capable of 100BASE-T4 operation and returns a 0 when bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-X Full-Duplex Capable

The B50610 is capable of 100BASE-TX full-duplex operation and returns a 1 when bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-X Half-Duplex Capable

The B50610 is capable of 100BASE-X half-duplex operation and returns a 1 when bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

10BASE-T Full-Duplex Capable

The B50610 is capable of 10BASE-T full-duplex operation and returns a 1 when bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

10BASE-T Half-Duplex Capable

The B50610 is capable of 10BASE-T half-duplex operation and returns a 1 when bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-T2 Full-Duplex Capable

The B50610 is not capable of 100BASE-T2 full-duplex operation and returns a 0 when bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-T2 Half-Duplex Capable

The B50610 is not capable of 100BASE-T2 half-duplex operation and returns a 0 when bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Extended Status

The B50610 contains IEEE Extended Status register at address 0Fh and returns a 1 when bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Management Frames Preamble Suppression

The B50610 accepts MII management frames whether or not they are preceded by the preamble pattern, and returns a 1 when bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Note: Preamble is still required on the first read or write**.**

Auto-Negotiation Complete

The B50610 returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when auto-negotiation is complete and the contents of registers 4, 5, and 6 are valid. This bit returns a 0 while auto-negotiation is in progress.

Remote Fault

The B50610 returns a 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when its link partner has signaled a remote fault condition. When a remote fault occurs, the bit is set and remains so until the remote fault condition has been cleared and the register is read.

Auto-Negotiation Ability

Even if the auto-negotiation function has been disabled, the B50610 is capable of performing IEEE auto-negotiation and returns a 1 when bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Link Status

The B50610 returns a 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when the link monitor is in the link-pass state (indicating that a valid link has been established); otherwise, it returns a 0. When a link failure occurs, the Link Status bit is latched at 0 and remains so until the bit is read and the B50610 is in the link-pass state.

Jabber Detect

Jabber detection is performed within the PHY and the result is latched into this bit. When a jabber condition has been detected, the B50610 returns a 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register. The bit is cleared by reading.

Extended Capability

The B50610 supports Extended Capability registers and returns a 1 when bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

1000BASE-T/100BASE-TX/10BASE-T PHY IDENTIFIER

Table 26: 1000BASE-T/100BASE-TX/10BASE-T PHY Identifier Register (Addresses 02h and 03h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:0	Address 02: ID MSBs	RO	16 MSBs of PHY Identifier	0x0143 (hex)
15:0	Address 03: ID LSBs	RO	16 LSBs of PHY Identifier	0xBD63 (hex)

The IEEE has issued an Organizationally Unique Identifier (OUI) to Broadcom Corporation. This 24-bit number allows devices made by Broadcom to be distinguished from all other manufacturers. The OUI combined with model numbers and revision numbers assigned by Broadcom precisely identifies a device manufactured by Broadcom.

The [15:0] bits of MII register 02h (PHYID HIGH) contain OUI bits [3:18]. The [15:0] bits of MII register 03h (PHYID LOW) contain the most significant OUI bits [19:24], 6 Manufacturer's Model Number bits, and 4 Revision Number bits. The two least significant OUI binary bits are not used.

Broadcom Corporation's OUI is 00-0A-F7, expressed as a hexadecimal value. The binary OUI is 0000-0000-0101-0000-1110-1111. The model number for the B50610 is 16h (010110 binary). Revision numbers start with 0h and are incremented by 1 for each chip modification.

- PHYID HIGH[15:0] = OUI[3:18]
- PHYID LOW[15:0] = OUI[19:24] + Model[5:0] + Revision [3:0]

Table 26 shows the result of concatenating these values to form the PHY identifiers for the B50610.

1000BASE-T/100BASE-TX/10BASE-T AUTO-NEGOTIATION ADVERTISEMENT

Table 27: 1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement Register (Address 04h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Next page ability supported 0 = Next page ability not supported	0
14	Reserved	R/W	Write as 0, ignore on read	0
13	Remote Fault	R/W	1 = Advertise remote fault detected 0 = Advertise no remote fault detected	0
12	Reserved Technology	R/W	Write as 0, ignore on read	0
11	Asymmetric Pause	R/W	1 = Advertise asymmetric pause 0 = Advertise no asymmetric pause	0
10	Pause Capable	R/W	1 = Capable of full-duplex pause operation 0 = Not capable of pause operation	0
9	100BASE-T4 Capable	R/W	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
8*	100BASE-TX Full-duplex Capable	R/W	1 = 100BASE-TX full-duplex capable 0 = Not 100BASE-TX full-duplex capable	Changed by hardware pin settings
7*	100BASE-TX Half-duplex Capable	R/W	1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	Changed by hardware pin settings
6*	10BASE-T Full-duplex Capable	R/W	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	Changed by hardware pin settings
5*	10BASE-T Half-duplex Capable	R/W	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	Changed by hardware pin settings
4:0	Selector Field	R/W	00001 indicates IEEE 802.3 CSMA/CD	00001

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Bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register must be set when the management software wants to control Next Page exchange. When this bit is cleared, Next Page exchange is controlled automatically by the B50610. When this bit is cleared and the B50610 is not advertising 1000BASE-T capability, no Next Page exchange occurs.

Remote Fault

Setting bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register sends a remote fault indication to the link partner during auto-negotiation. Writing a 0 to this bit clears the Remote Fault transmission bit. This bit returns a 1 when advertising remote fault; otherwise, it returns a 0.

Reserved Technology

Bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is reserved for future versions of the auto-negotiation standard and must always be written as 0.

Asymmetric Pause

When bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50610 advertises that asymmetric pause is preferred. When the bit is cleared, the B50610 advertises that asymmetric pause is not

needed. This bit returns a 1 when advertising asymmetric pause; otherwise, it returns a 0. When advertising asymmetric pause, bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register indicates the preferred direction of the pause operation. Setting bit 10 indicates that the pause frames flow toward the B50610. Clearing bit 10 indicates that pause frames flow toward the link partner.

Pause Capable

When bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50610 advertises full-duplex pause capability. When the bit is cleared, the B50610 advertises no pause capability. This bit returns a 1, when advertising pause capability; otherwise, it returns a 0.

100BASE-T4 Capable

The B50610 does not support 100BASE-T4 capability. Do not write a 1 to bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register.

100BASE-TX Full-Duplex Capable

When bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50610 advertises 100BASE-TX full-duplex capability. When the bit is cleared, the B50610 advertises no 100BASE-TX full-duplex capability. This bit returns a 1 when advertising 100BASE-TX full-duplex capability; otherwise, it returns a 0. This bit updates during reset based on configuring the hardware pins in the following way:
FDX AND (F1000 OR SPD0) AND NOT (F1000 AND SPD0).

100BASE-TX Half-Duplex Capable

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50610 advertises 100BASE-TX half-duplex capability. When the bit is cleared, the B50610 advertises no 100BASE-TX half-duplex capability. This bit returns a 1 when advertising 100BASE-TX half-duplex capability; otherwise, it returns a 0. This bit updates during reset based on configuring the hardware pins in the following way:
NOT FDX AND (F1000 OR SPD0) AND NOT (F1000 AND SPD0).

10BASE-T Full-Duplex Capable

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50610 advertises 10BASE-T full-duplex capability. When the bit is cleared, the B50610 advertises no 10BASE-T full-duplex capability. This bit returns a 1 when advertising 10BASE-T full-duplex capability; otherwise, it returns a 0. This bit updates during reset based on configuring the hardware pins in the following way:
FDX AND NOT (F1000 AND SPD0).

10BASE-T Half-Duplex Capable

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50610 advertises 10BASE-T half-duplex capability. When the bit is cleared, the B50610 advertises no 10BASE-T half-duplex capability. This bit returns a 1 when advertising 10BASE-T half-duplex capability; otherwise, it returns a 0. This bit updates during reset based on configuring the hardware pins in the following way:
NOT FDX AND NOT (F1000 AND SPD0).

Selector Field

Bits [4:0] of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register indicate the protocol type. Value 00001 indicates that the B50610 belongs to the 802.3 class of PHY transceivers.

1000BASE-T/100BASE-TX/10BASE-T AUTO-NEGOTIATION LINK PARTNER ABILITY

Table 28: 1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Link Partner Ability Register (Address 05h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Link partner has Next Page ability 0 = Link partner does not have Next Page ability	0
14	Acknowledge	RO	1 = Link partner has received link code word 0 = Link partner has not received link code word	0
13	Remote Fault	RO	1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault	0
12	Reserved Technology	RO	Write as 0, ignore on read	0
11	Asymmetric Pause	RO	1 = Link partner wants asymmetric pause 0 = Link partner does not want asymmetric pause	0
10	Pause Capable	RO	1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation	0
9	100BASE-T4 Capable	RO	1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable	0
8	100BASE-TX Full-duplex Capable	RO	1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable	0
7	100BASE-TX Half-duplex Capable	RO	1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner not 100BASE-TX half-duplex capable	0
6	10BASE-T Full-duplex Capable	RO	1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable	0
5	10BASE-T Half-duplex Capable	RO	1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable	0
4:0	Protocol Selector Field	RO	Link partner protocol selector field	00000

Note: As indicated by bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T MII status register, the values contained in the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation link partner ability register are only guaranteed to be valid after auto-negotiation has successfully completed.

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The B50610 returns a 1 in bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner wants to transmit Next Page information.

Acknowledge

The B50610 returns a 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has acknowledged reception of the link code word; otherwise, it returns a 0.

Remote Fault

The B50610 returns a 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised detection of a remote fault; otherwise, it returns a 0.

Reserved Technology

Bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register is reserved for future versions of the auto-negotiation standard and must be ignored when read.

Asymmetric Pause

The B50610 returns a 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised asymmetric pause; otherwise, it returns a 0.

Pause Capable

The B50610 returns a 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised Pause Capability; otherwise, it returns a 0.

100BASE-T4 Capable

The B50610 returns a 1 in bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-T4 capability; otherwise, it returns a 0.

100BASE-TX Full-Duplex Capable

The B50610 returns a 1 in bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-TX full-duplex capability; otherwise, it returns a 0.

100BASE-TX Half-Duplex Capable

The B50610 returns a 1 in bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-TX half-duplex capability; otherwise, it returns a 0.

10BASE-T Full-Duplex Capable

The B50610 returns a 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 10BASE-T full-duplex capability; otherwise, it returns a 0.

10BASE-T Half-Duplex Capable

The B50610 returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 10BASE-T half-duplex capability; otherwise, it returns a 0.

Protocol Selector Field

Bits [4:0] of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register return the value of the link partner's advertised Protocol Selector field.

1000BASE-T/100BASE-TX/10BASE-T AUTO-NEGOTIATION EXPANSION

Table 29: 1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Expansion Register (Address 06h)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Write as 000h. Ignore on read	003h
4	Parallel Detection Fault	RO LH	1 = Parallel link fault detected 0 = Parallel link fault not detected	0
3	Link Partner Next Page Ability	RO	1 = Link partner has Next Page capability 0 = Link partner does not have Next Page capability	0
2	Next Page Capable	RO LH	1 = B50610 is Next Page capable 0 = B50610 is not Next Page capable	1
1	Page Received	RO LH	1 = New page has been received from link partner 0 = New page has not been received	0
0	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation	0

Parallel Detection Fault

When a parallel detection fault has occurred in the auto-negotiation state machine, bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register returns a 1. When a parallel detection fault occurs, this bit is latched at 1 and remains so until the register is read. If a parallel detection fault has not occurred since the last time it was read, this bit returns a 0.

Link Partner Next Page Ability

The B50610 returns a 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register when the link partner needs to transmit Next Page information; otherwise, it returns a 0. This bit is a copy of bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register.

Next Page Capable

When bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register is read, the B50610 supports Next Page capability and returns a 1.

Page Received

The B50610 returns a 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns a 0.

Link Partner Auto-Negotiation Ability

When the link partner shows auto-negotiation capability, the B50610 returns a 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register. Before any auto-negotiation information is exchanged or if the link partner does not comply with IEEE auto-negotiation, the bit returns a 0.

1000BASE-T/100BASE-TX/10BASE-T NEXT PAGE TRANSMIT

Table 30: 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit Register (Address 07h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Additional next pages follow 0 = Sending last Next Page	0
14	Reserved	RO	Write as 0, ignore on read	0
13	Message Page	R/W	1 = Formatted page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Complies with message 0 = Cannot comply with message	0
11	Toggle	RO	Toggles between exchanges of different next pages	0
10:0	Message/Unformatted Code Field	R/W	Next page message code or unformatted data	001h

Next Page

Bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit register must be set to indicate that more Next Pages are to be sent. This bit must be cleared to indicate that this is the last Next Page to be transmitted. When this bit is read, it returns the last value written.

Message Page

Bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit register must be set to indicate that a formatted message page is being sent. This bit must be cleared to indicate that an unformatted page is being sent. When this bit is read, it returns the last value written.

Acknowledge2

When this bit is set, the B50610 indicates that it can comply with the Next Page request. When this bit is cleared, the B50610 indicates that it cannot comply with the Next Page request. When this bit is read, it returns the last value written.

Toggle

This bit toggles between different Next Page exchanges to ensure a functional synchronization to the link partner.

Message/Unformatted Code Field

These 11 bits make up the message code defined by IEEE 802.3, Clause 28, Annex C, when sending formatted pages. When sending unformatted Next Pages, these 11 bits contain an arbitrary data value.

1000BASE-T/100BASE-TX/10BASE-T LINK PARTNER RECEIVED NEXT PAGE

Table 31: 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page Register (Address 08h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional next pages follow 0 = Sending last Next Page	0
14	Acknowledge	RO	1 = Acknowledge 0 = No acknowledge	0
13	Message Page	RO	1 = Formatted page 0 = Unformatted page	0
12	Acknowledge2	RO	1 = Complies with message 0 = Cannot comply with message	0
11	Toggle	RO	Toggles between exchanges of different next pages	0
10:0	Message Code field	RO	Next Page message code or unformatted data	000h

Next Page

When the link partner has indicated that more Next Pages are to be sent, bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns a 1. This bit returns a 0 when the link partner indicates that this is the last Next Page to be transmitted.

Acknowledge

Bit 14 returns a 1 to indicate that the link partner has received and acknowledged a Next Page. The bit returns a 0 until the link partner has acknowledged the page.

Message Page

Bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns a 1 to indicate that the link partner has sent a formatted message page. This bit returns a 0 when the link partner has sent an unformatted page.

Acknowledge2

When the link partner has indicated that it can comply with the Next Page request, bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns a 1. When the link partner has indicated that it cannot comply with the Next Page request, this bit returns a 0.

Toggle

To ensure a functional synchronization to the B50610 transceiver, the link partner toggles this bit between different Next Page exchanges.

Message Code Field

These 11 bits make up the message code defined by IEEE 802.3, Clause 28, Annex C, when the link partner has sent a formatted page. When the link partner has sent unformatted next pages, these 11 bits contain an arbitrary data value.

1000BASE-T CONTROL

Table 32: 1000BASE-T Control Register (Address 09h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:13	Test Mode	R/W	1 X X = Test mode 4—Transmitter distortion test 0 1 1 = Test mode 3—Slave transmit jitter test 0 1 0 = Test mode 2—Master transmit jitter test 0 0 1 = Test mode 1—Transmit waveform test 0 0 0 = Normal operation	000
12	Master/Slave Configuration Enable	R/W	1 = Enable master/slave manual configuration value 0 = Automatic master/slave configuration	0
11	Master/Slave Configuration Value	R/W	1 = Configure PHY as master 0 = Configure PHY as slave	0
10	Repeater/DTE	R/W	1 = Repeater/switch device port 0 = DTE device	0
9	Advertise 1000BASE-T Full-duplex Capability	R/W	1 = Advertise 1000BASE-T full-duplex capability 0 = Advertise no 1000BASE-T full-duplex capability	FDX AND F1000
8	Advertise 1000BASE-T Half-duplex Capability	R/W	1 = Advertise 1000BASE-T half-duplex capability 0 = Advertise no 1000BASE-T half-duplex capability	F1000
7:0	Reserved	RO	Write as 0, ignore on read	00h

Test Mode

The B50610 can be placed in one-of-four transmit test modes by writing bits [15:13] of the 1000BASE-T Control register. The transmit test modes are defined in IEEE 802.3ab. When read, these bits return the last value written.

Master/Slave Configuration Enable

When bit 12 of the 1000BASE-T Control register is set, the B50610 master/slave mode is configured using the manual master/slave configuration value. When the bit is cleared, master/slave mode is configured using the automatic resolution function. This bit returns a 1 when manual master/slave configuration is enabled; otherwise, it returns a 0.

Master/Slave Configuration Value

When bit 12 of the 1000BASE-T Control register is set, bit 11 of the 1000BASE-T Control register determines the B50610 master/slave mode of operation. When bit 11 is set, the B50610 is configured as the master. When bit 11 is cleared, the B50610 is configured as the slave. When read, this bit returns the last value written.

Repeater/DTE

When bit 10 of the 1000BASE-T Control register is set, the B50610 advertises that it is a repeater or switch device port. When the bit is cleared, the B50610 advertises that it is a data terminal equipment (DTE) port. The advertised value is used in the automatic master/slave configuration resolution. The link partner, which advertises repeater mode is configured to master if the opposing link partner advertises DTE; otherwise, this bit has no effect. This bit returns a 1 when advertising repeater/switch mode; otherwise, it returns a 0.

Advertise 1000BASE-T Full-Duplex Capability

When bit 9 of the 1000BASE-T Control register is set, the B50610 advertises 1000BASE-T full-duplex capability. When the bit is cleared, the B50610 advertises no 1000BASE-T full-duplex capability. This bit returns a 1 when advertising 1000BASE-T full-duplex capability; otherwise, it returns a 0. *The default value of this bit is determined by the state of the FDX pin at reset.*

Advertise 1000BASE-T Half-Duplex Capability

When bit 8 of the 1000BASE-T Control register is set, the B50610 advertises 1000BASE-T half-duplex capability. When the bit is cleared, the B50610 advertises no 1000BASE-T half-duplex capability. This bit returns a 1 when advertising 1000BASE-T half-duplex capability; otherwise, it returns a 0.

1000BASE-T STATUS

Table 33: 1000BASE-T Status Register (Address 0Ah)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Master/Slave Configuration Fault	RO LH	1 = Master/slave configuration fault detected 0 = No master/slave configuration fault detected	0
14	Master/Slave Configuration Resolution	RO	1 = Local transmitter is master 0 = Local transmitter is slave	0
13	Local Receiver Status	RO	1 = Local receiver OK 0 = Local receiver not OK	0
12	Remote Receiver Status	RO	1 = Remote receiver OK 0 = Remote receiver not OK	0
11	Link Partner 1000BASE-T Full-duplex Capability	RO	1 = Link partner is 1000BASE-T full-duplex capable 0 = Link partner not 1000BASE-T full-duplex capable	0
10	Link Partner 1000BASE-T Half-duplex Capability	RO	1 = Link partner is 1000BASE-T half-duplex capable 0 = Link partner not 1000BASE-T half-duplex capable	0
9:8	Reserved	RO	Write as 00, ignore on read	00
7:0	Idle Error Count	RO CR	Number of idle errors since last read	00h

Note: As indicated by bit 5 of the MII Status register, the values contained in bits 14, 11, and 10 of the 1000BASE-T Status register are guaranteed to be valid only after auto-negotiation has successfully completed.

Master/Slave Configuration Fault

When a master/slave configuration fault has occurred during auto-negotiation, the B50610 returns a 1 in bit 15 of the 1000BASE-T Status register. When a configuration fault occurs, the bit is latched at 1 and remains so until either the register is read, auto-negotiation is restarted by writing bit 9 in the MII Control register, or auto-negotiation completes successfully with no master/slave configuration fault.

Master/Slave Configuration Resolution

When the B50610 transceiver has been configured as the master, it returns a 1 in bit 14 of the 1000BASE-T Status register. When the B50610 transceiver has been configured as the slave, it returns a 0.

Local Receiver Status

The B50610 transceiver returns a 1 in bit 13 of the 1000BASE-T Status register when the local receiver status is OK; otherwise, it returns a 0.

Remote Receiver Status

The B50610 returns a 1 in bit 12 of the 1000BASE-T Status register when the remote receiver status is OK; otherwise, it returns a 0.

1000BASE-T Full-Duplex Capability

The B50610 returns a 1 in bit 11 of the 1000BASE-T Status register when the link partner has advertised 1000BASE-T full-duplex capability; otherwise, it returns a 0.

1000BASE-T Half-Duplex Capability

The B50610 returns a 1 in bit 10 of the 1000BASE-T Status register when the link partner has advertised 1000BASE-T half-duplex capability; otherwise, it returns a 0.

Idle Error Count

The B50610 counts the number of idle errors received while the local receiver status is OK. Bits 7 through 0 of the 1000BASE-T Status register return the number of idle errors counted since the last register read. The counter freezes at the maximum value (FFh) to prevent overflow.

1000BASE-T/100BASE-TX/10BASE-T IEEE EXTENDED STATUS

Table 34: 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status Register (Address 0Fh)

Bit	Name	R/W	Description	Default
15	1000BASE-X Full-duplex Capable	RO L	1 = 1000BASE-X full-duplex capable 0 = Not 1000BASE-X full-duplex capable	0
14	1000BASE-X Half-duplex Capable	RO L	1 = 1000BASE-X half-duplex capable 0 = Not 1000BASE-X half-duplex capable	0
13	1000BASE-T Full-duplex Capable	RO H	1 = 1000BASE-T full-duplex capable 0 = Not 1000BASE-T full-duplex capable	1
12	1000BASE-T Half-duplex Capable	RO H	1 = 1000BASE-T half-duplex capable 0 = Not 1000BASE-T half-duplex capable	1
11:0	Reserved	RO	Write as 000h, ignore on read	000h

1000BASE-X Full-Duplex Capable

The B50610 is not capable of 1000BASE-X full-duplex operation and returns a 0 when bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-X Half-Duplex Capable

The B50610 is not capable of 1000BASE-X half-duplex operation and returns a 0 when bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T Full-Duplex Capable

The B50610 is capable of 1000BASE-T full-duplex operation and returns a 1 when bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T Half-Duplex Capable

The B50610 is capable of 1000BASE-T half-duplex operation and returns a 1 when bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T/100BASE-TX/10BASE-T PHY EXTENDED CONTROL

Table 35: 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control Register (Address 10h)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as zero	0
14	Disable Automatic MDI Crossover	R/W	1 = Automatic MDI crossover disabled 0 = Automatic MDI crossover enabled	0
13	Transmit Disable	R/W	1 = Transmitter outputs disabled 0 = Normal operation	0
12	Interrupt Disable	R/W	1 = Interrupt status output disabled 0 = Interrupt status output enabled	0
11	Force Interrupt	R/W	1 = Force interrupt status to active 0 = Normal operation	0
10	Bypass 4B/5B Encoder/Decoder (100BASE-T)	R/W	1 = Transmit and receive 5B codes over MII pins 0 = Normal MII	0
9	Bypass Scrambler/Descrambler (100BASE-T)	R/W	1 = Scrambler and descrambler disabled 0 = Scrambler and descrambler enabled	0
8	Bypass MLT3 Encoder/Decoder (100BASE-T)	R/W	1 = Bypass NRZI/MLT3 encoder and decoder 0 = Normal operation	0
7	Bypass Receive Symbol Alignment (100BASE-T)	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Reset Scrambler (100BASE-T)	R/W SC	1 = Reset scrambler to initial state 0 = Normal scrambler operation	0
5	Enable LED Traffic mode	R/W	1 = LED Traffic mode enabled 0 = LED Traffic mode disabled	0
4	Force LEDs On	R/W	1 = Force all LEDs into on state 0 = Normal LED operation	0
3	Force LEDs Off	R/W	1 = Force all LEDs into off state 0 = Normal LED operation	0
2:1	Reserved	R/W	Write as 00, ignore on read	00
0	1000BASE-T PCS transmit FIFO Elasticity (copper mode)	R/W‘	1 = High latency 0 = Low latency	0

MAC/PHY Interface Mode

Bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register selects the Interface mode between the MAC and the PHY. This bit must be set to 0 for normal operation.

Disable Automatic MDI Crossover

The automatic MDI crossover function can be disabled by setting bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. When the bit is cleared, the B50610 performs the automatic MDI crossover function (see "Automatic MDI Crossover" on page 7 for details).

Transmit Disable

The transmitter can be disabled by setting bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The transmitter outputs (TRD[3:0]±) are forced into a high-impedance state.

Interrupt Disable

When this bit is set, the interrupt pin is forced to its inactive state except when the Force Interrupt bit is set.

Force Interrupt

When this bit is set, the INTR pin is forced to its active state.

Bypass 4B/5B Encoder/Decoder (100BASE-T)

The 100BASE-TX4B/5B encoder/decoder can be bypassed by setting bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The transmitter sends 5B codes from the TX_ER and TXD[3:0] pins directly to the scrambler. TX_EN is ignored and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places descrambled and aligned 5B codes onto the RX_ER and RXD[3:0] pins. CRS is still asserted when a valid frame is received.

Bypass Scrambler/Descrambler (100BASE-T)

The 100BASE-TX stream cipher function can be disabled by setting bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The stream cipher function can be re-enabled by writing a 0 to this bit.

Bypass MLT3 Encoder/Decoder (100BASE-T)

The 100BASE-TX MLT3 encoder and decoder can be bypassed by setting bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. NRZ data is transmitted and received on the cable. The MLT3 encoder can be re-enabled by clearing this bit.

Bypass Receive Symbol Alignment (100BASE-T)

100BASE-TX receive symbol alignment can be bypassed by setting bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. When used in conjunction with the bypass 4B/5B encoder/decoder bit, unaligned 5B codes are placed directly on the RX_ER and RXD[3:0] pins.

Reset Scrambler (100BASE-T)

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the B50610 resets the scrambler to an all 1 state. This bit is self-clearing and always returns 0 when read.

Enable LED Traffic Mode

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the B50610 enables the LED traffic mode for $\overline{\text{ACTIVITYLED}}$ and $\overline{\text{XMITLED}}$. When the bit is cleared, the B50610 disables the LED traffic mode.

Force LEDs On

When bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the B50610 forces all LEDs into the on state. When the bit is cleared, the B50610 resets all LEDs to normal operation.

Force LEDs Off

When bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the B50610 forces all LEDs into the off state. When the bit is cleared, the B50610 resets all LEDs to normal operation.

1000BASE-T PCS Transmit FIFO Elasticity (Copper Mode)

When bit 0 of the PHY Extended Control register is set, the B50610 sets the FIFO elasticity to high latency. In this mode, the B50610 can transmit packets up to 9 kilobytes in length. When this bit is cleared, the FIFO elasticity is set to low latency. In this mode, the B50610 can transmit packets up to 4.5 kilobytes in length. Setting this bit to 1 adds 16 ns to the 1000BASE-T transmit latency.

1000BASE-T/100BASE-TX/10BASE-T PHY EXTENDED STATUS

Table 36: 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status Register (Address 11h)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Base Page Selector Field Mismatch	RO LH	1 = Link Partner Base Page Selector field mismatched Advertised Selector field since last read 0 = No mismatch detected since last read	0
14	Reserved	RO	Write as 0, ignore on read.	0
13	MDI Crossover State	RO	1 = Crossover MDI mode 0 = Normal MDI mode	0
12	Interrupt Status	RO	1 = Unmasked interrupt currently active 0 = Interrupt cleared	0
11	Remote Receiver Status	RO LL	1 = Remote receiver OK 0 = Remote receiver not OK since last read	0
10	Local Receiver Status	RO LL	1 = Local receiver OK 0 = Local receiver not OK since last read	0
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Link Status	RO	1 = Link pass 0 = Link fail	0
7	CRC Error Detected	RO LL	1 = CRC error detected 0 = No CRC error since last read	0
6	Carrier Extension Error Detected	RO LH	1 = Carrier extension error detected since last read 0 = No carrier extension error since last read	0
5	Bad SSD Detected (False Carrier)	RO LH	1 = Bad SSD error detected since last read 0 = No bad SSD error since last read	0
4	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read 0 = No bad ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Auto-Negotiation Base Page Selector Field Mismatch

When this bit is set, the auto-negotiation base page selector does not match the Advertised Selector field since the previous read. When this bit reads back a 0, there is no mismatched Page Selector field and Advertised Selector field.

MDI Crossover State

When the B50610 is automatically switching the transmit and receive pairs to communicate with a remote device, the B50610 returns a 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. This bit returns a 0 when the B50610 is in normal MDI mode.

Interrupt Status

The B50610 returns a 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when any unmasked interrupt is currently active; otherwise, it returns a 0.

Remote Receiver Status

When the remote receiver status is OK, the B50610 returns a 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. When the B50610 detects that the remote receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

Local Receiver Status

When the local receiver status is OK, the B50610 returns a 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. When the B50610 detects that the local receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

Locked

The B50610 returns a 1 in bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when the descrambler is locked to the incoming data stream; otherwise, it returns a 0.

Link Status

The B50610 returns a 1 in bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when the device has established a link; otherwise, it returns a 0.

CRC Error Detected

The B50610 returns a 1 in bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a CRC error has been detected since the last time this register was read; otherwise, it returns a 0.

Carrier Extension Error Detected

The B50610 returns a 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a carrier extension error has been detected since the last time this register was read; otherwise, it returns a 0.

Bad SSD Detected (False Carrier)

The B50610 returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a bad start-of-stream error has been detected since the last time this register was read; otherwise, it returns a 0.

Bad ESD Detected (Premature End)

The B50610 returns a 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a bad end-of-stream error has been detected since the last time this register was read; otherwise, it returns a 0.

Receive Error Detected

The B50610 returns a 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a packet was received with an invalid code since the last time this register was read; otherwise, it returns a 0.

Transmit Error Detected

The B50610 returns a 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a packet was received with a transmit error code since the last time this register was read; otherwise, it returns a 0.

Lock Error Detected

The B50610 returns a 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if the descrambler has lost lock since the last time this register was read; otherwise, it returns a 0.

MLT3 Code Error Detected

The B50610 returns a 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if an MLT3 coding error has been detected in the receive data stream since the last time this register was read; otherwise, it returns a 0.

1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter

Table 37: 1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter Register (Address 12h)

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter	R/W CR	Number of non-collision packets with receive errors since last read	0000h

Receive Error Counter

This counter increments each time the B50610 receives a noncollision packet containing at least 1 receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears when read.

1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter

Table 38: 1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter Register (Address 13h)

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	Write as 00h, ignore on read	00h
7:0	False Carrier Sense Counter	R/W CR	Number of false carrier sense events since last read	00h

False Carrier Sense Counter

The False Carrier Sense Counter increments each time the B50610 detects a false carrier sense on the receive input. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter

Table 39: 1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter Register (Address 14h)

Bit	Name	R/W	Description	Default
15:8	Local Receiver NOT_OK Counter	R/W CR	Number of times local receiver was NOT_OK since last read	00h
7:0	Remote Receiver NOT_OK Counter	R/W CR	Number of times B50610 detected that the remote receiver was NOT_OK since last read	00h

Local Receiver NOT_OK Counter

This counter increments each time the local receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Remote Receiver NOT_OK Counter

This counter increments each time the remote receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

1000BASE-T/100BASE-TX/10BASE-T EXPANSION REGISTER ACCESS

Table 40: 1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as 0h, ignore on read	0h
11:8	Expansion Register Select	R/W	1111 = Expansion register selected 0000 = Expansion register not selected All Others= Reserved (Do not use)	0h
7:0	Expansion Register Accessed	R/W	Sets the Expansion register number accessed when read/write to register 15h.	00h

Expansion Register Select

Setting bits [11:8] to 1111 enable the reading from and writing to the Expansion registers through register 15h. These bits should be cleared after the Expansion registers are accessed or when the Expansion registers are not being accessed. See "Expansion Registers" on page 106 for details.

Expansion Register Accessed

Bits [7:0] of the Expansion Register Access register set the Expansion register number accessed. The Expansion register is read/write through register 15h when bits [11:8] of this register are set to 1111. The available expansion registers are listed in the following table.

Table 41: Expansion Register Select Values

Expansion Register	Register Name
00h	"Expansion Register 00h: Receive/Transmit Packet Counter" on page 106
04h	"Expansion Register 04h: Multicolor LED Selector" on page 107
05h	"Expansion Register 05h: Multicolor LED Flash Rate Controls" on page 109
06h	"Expansion Register 06h: Multicolor LED Programmable Blink Controls" on page 110

1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register

The following table lists the available 18h registers.

Table 42: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Values Access

Shadow Value	*Register Name*
000	"1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 67
001	"10BASE-T" on page 70
010	"1000BASE-T/100BASE-TX/10BASE-T Power/MII Control" on page 72
100	"1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register" on page 73
111	"1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control" on page 75

The following table shows the read from register 18h, shadow value zzz.

Table 43: Reading Register 18h

Register Reads/Writes	*Description*
Write register 18h, bits [2:0] = 111	This selects the Miscellaneous Control register, shadow value 111. All reads must be done through the Miscellaneous Control register.
Bit [15] = 0	This allows only bits [14:12] and [2:1] to be written.
Bits [14:12] = zzz	This selects shadow value register zzz to be read.
Bits [11: 3] = <don't care>	When bit [15] = 0, these bits are ignored.
Bits [2:0] = 111	This sets the Shadow Register Select to 111 (Miscellaneous Control register).
Read register 18h	Data read back is the value from shadow register zzz.

Table 44 shows the write to register 18h, shadow value yyy.

Table 44: Writing Register 18h

Register Writes	*Description*
Set Bits [15:3] = Preferred write values	Bits [15:3] contain the preferred bits to be written to.
Set Bits [2:0] = yyy	This enables shadow value register yyy to be written. For shadow value 111, bit 15 must also be written.

Table 45: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000)

Bit	Name	R/W	Description	Default
15	External Loopback	R/W	1 = External Loopback enabled 0 = Normal operation	0
14	Extended Packet Length	R/W	1 = Allow reception of extended length packets 0 = Allow normal length Ethernet packets only	0
13:12	Edge Rate Control (1000BASE-T)	R/W	00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns	00
11	Reserved	R/W	Write as 0, ignore on read	0
10	Transmit Mode	R/W	1 = Normal operation 0 = Test mode	1
9:8	Reserved	R/W	Write as 0, ignore on read	0
7	Disable Partial Response Filter	R/W	1 = Transmitter partial response filter disabled 0 = Transmitter partial response filter enabled	0
6	Reserved	R/W	Write as 0, ignore on read	0
5:4	Edge Rate Control (100BASE-TX)	R/W	00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns	00
3	Reserved	R/W	Write as 0, ignore on read	0
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	000

External Loopback

When bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, external loopback operation is enabled. When the bit is cleared, normal operation resumes.

Extended Packet Length

When bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, the B50610 receives packets up to 18 KB in length. When the bit is cleared, the B50610 only receives packets up to 4.5 KB in length.

Edge Rate Control (1000BASE-T)

Bits 13 and 12 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 control the edge rate of the 1000BASE-T transmit DAC output waveform.

Transmit Mode

Bit 10 of the Auxiliary Control register shadow value 000 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register must be set for normal PHY operation.

Disable Partial Response Filter

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, the transmitter partial response filter is disabled. When the bit is cleared, the transmitter partial response filter is enabled.

Edge Rate Control (100BASE-TX)

Bits 5 and 4 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 control the edge rate of the 100BASE-TX transmit DAC output waveform.

Shadow Register Select

The Auxiliary Control register provides access to eight registers using a shadow technique. The lower 3 bits written define which set of 13 upper bits is used in accordance with “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000)” on page 68, defined under bits [2:0]. See the note in “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register” on page 67 describing reading from and writing to register 18h.

The register set previously shown is for normal operation, obtained when the lower 3 bits are 000.

10BASE-T

Table 46: 10BASE-T Register (Address 18h, Shadow Value 001)

Bit	Name	R/W	Description	Default
15	Manchester Code Error	RO LH	1 = Manchester code error (10BASE-T) 0 = No Manchester code error	0
14	EOF Error	RO LH	1 = EOF error detected (10BASE-T) 0 = No EOF error detected	0
13	Polarity Error	RO	1 = Channel polarity inverted 0 = Channel polarity correct	0
12	Block RX_DV Extension (IPG)	R/W	1 = Block RX_DV for 4 additional RXC cycles for IPG 0 = Normal operation	0
11	10BASE-T TXC Invert Mode	R/W	1 = Invert TXC output 0 = Normal operation	0
10	Reserved	RO	Write as 0, ignore on read	0
9	Jabber Disable	R/W	1 = Jabber function disabled 0 = Jabber function enabled	0
8:7	Reserved	RO	Write as 0, ignore on read	10
6	10BASE-T Echo Mode	R/W	1 = Echo transmit data to receive data 0 = Normal operation	0
5	SQE Enable Mode	R/W	1 = Enable SQE 0 = Disable SQE	0
4	10BASE-T No Dribble	R/W	1 = Correct 10BASE-T dribble nibble 0 = Normal operation	0
3	Reserved	RO	Write as 0, ignore on read	0
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	001

Manchester Code Error

When a Manchester code violation is received, bit 15 of the 10BASE-T register returns a 1. This bit is valid only during 10BASE-T operation.

EOF Error

When the end-of-frame (EOF) sequence was improperly received (or not received at all), bit 14 of the 10BASE-T register returns a 1. This bit is valid only during 10BASE-T operation.

Polarity Error

When an analog input polarity error has been detected and corrected, bit 13 of the 10BASE-T register returns a 1. This bit is valid only during 10BASE-T operation.

Block RX_DV Extension (IPG)

When bit 12 of the 10BASE-T register is set, blocking of the RX_DV signal is extended for an additional 4 RXC cycles to extend the IPG.

10BASE-T TXC Invert Mode

When bit 11 of the 10BASE-T register is set, the polarity of the 10BASE-T transmit clock is inverted. Clearing this bit restores normal transmit clock polarity. This bit is valid only during 10BASE-T operation.

Jabber Disable

Setting bit 9 of the 10BASE-T register allows the user to disable the jabber detect function defined in the IEEE standard. When a transmission request has exceeded a maximum time limit, this function shuts off the transmitter. Clearing this bit or resetting the chip restores normal operation. Reading this bit returns the value of jabber detect disable. This bit is valid only during 10BASE-T operation.

1000BASE-T Signal Detect Threshold

Setting bit 8 of the 10BASE-T register enables the low 1000BASE-T signal detect threshold. The bit is cleared when in the Normal or Default mode.

10BASE-T Signal Detect Threshold

Setting bit 7 of the 10BASE-T register enables the low 10BASE-T signal detect threshold. The bit is cleared when in the Normal or Default mode.

10BASE-T Echo Mode

When bit 6 of the 10BASE-T register is enabled during 10BASE-T half-duplex transmit operation, the transmitted data is replicated on the receive data pins and the TXEN signal echoes on the RX_DV pin. The TXEN signal also echoes on the CRS pin, and CRS deassertion directly follows the TXEN deassertion.

SQE Enable Mode

Setting bit 5 of the 10BASE-T register enables SQE mode. Clearing disables it. This bit is valid only during 10BASE-T operation.

10BASE-T No Dribble

When bit 4 of the 10BASE-T register is set, the PHY rounds down to the nearest nibble when dribble bits are present on the 10BASE-T input stream.

Shadow Register Select

The 10BASE-T register provides access to 8 registers using shadow technique. The lower 3 bits written define which set of 13 upper bits are used in accordance with Table 46 on page 70, defined under bits [2:0]. See the note on “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register” on page 67 describing reading from and writing to register 18h. The register set previously shown is for 10BASE-T operation, obtained when the lower 3 bits are 001.

1000BASE-T/100BASE-TX/10BASE-T POWER/MII CONTROL

Table 47: 1000BASE-T/100BASE-TX/10BASE-T Power/MII Control Register (Address 18h, Shadow Value 010)

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Write as 013h, ignore on read.	013h
5	Super Isolate	R/W	1 = Isolate mode with no link pulses transmitted 0 = Normal operation	0
4:3	Reserved	R/W	Write as 00, ignore on read	00
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	010

Super Isolate

Setting bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Power/MII Control register places the B50610 into the Super Isolate mode. Similar to the Isolate mode, all RGMII inputs are ignored and all RGMII outputs are tristated. All link pulses are suppressed.

Shadow Register Select

The 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register provides access to 8 registers using a shadow technique. The lower 3 bits written define which set of 13 upper bit is used in accordance with the table defined under bits [2:0] above. See the note in "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 67 describing reading from and writing to register 18h.

The register set previously shown is for power/MII control, obtained when the lower 3 bits are 010.

1000BASE-T/100BASE-TX/10BASE-T MISCELLANEOUS TEST REGISTER

Table 48: 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register (Address 18h, Shadow Value 100)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Lineside [Remote] Loopback Enable	R/W	1 = Enable lineside [remote] loopback from MDI (cable end) receive packet, through PCS and back to MDI transmit packet. 0 = Disable loopback	0
14:12	Reserved	R/W	Write as 100, ignore on read	100
11	Lineside [Remote] Loopback Tri-state	R/W	1 = Tristate the receive MII pins (CRS, RXDV, RXD, and so forth) when lineside [remote] loopback is enabled 0 = Lineside [remote] loopback packets appear on MII	0
10:5	Reserved	R/W	Write as 00h, ignore on read	00h
4	Swap RX MDIX	RO	1 = RX and TX operate on same pair 0 = Normal operation	0
3	10BASE-T Half-Out	R/W	1 = Transmit 10BASE-T at half amplitude 0 = Normal operation	0
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	100

Lineside [Remote] Loopback Enable

Setting bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test register enables lineside (remote) loopback of the copper receive packet back out through the MDI transmit path.

Lineside [Remote] Loopback Tristate

Setting this bit tri-states the receive MII pins when the device is in Lineside (remote) Loopback mode.

Swap RX MDIX

When bit 4 of the Miscellaneous Test register is set to a 1, the transmitter and receiver operate on the same twisted pair. This function is for use in a test mode where the transmitter output is detected by the receiver attached to the same pair.

10BASE-T Half-Out

When operating in 10BASE-T mode, setting bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test register to 1 reduces the output of the transmitter to half of its normal amplitude. Clearing this bit restores full amplitude operation. This function is used in a test mode where an unterminated output generates a signal with twice the amplitude of a terminated output.

Shadow Register Select

The Miscellaneous Test register provides access to 8 registers using a shadow technique. The lower 3 bits written define which set of 13 upper bits is used in accordance with Table 48 under bits [2:0]. See the note on “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register” on page 67 describing reading from and writing to register 18h.

The register set previously shown is for miscellaneous testing, obtained when the lower 3 bits are 100.

1000BASE-T/100BASE-TX/10BASE-T MISCELLANEOUS CONTROL

Table 49: 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control Register (Address 18h, Shadow Value 111)

Bit	Name	R/W	Description	Default
15	Write Enable (Bits 11:3)	R/W SC	1 = Write bits [14:0] 0 = Only write bits [14:12] and [2:0]	0
14:12	Shadow Register Read Selector	R/W	000 = Normal operation 001 = 10BASE-T register 010 = Power Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register These bits are written when bit 15 is not set. This sets the shadow value for address 18h register read.	000
11	Packet Counter Mode	R/W	1 = Receive packet Counter 0 = Transmit Packet Counter	0
10	Reserved	R/W	Write as 0, ignore on read	0
9	Force Auto-MDIX Mode	R/W	1 = Auto-MDIX is enabled when auto-negotiation is disabled 0 = Auto-MDIX is disabled when auto-negotiation is disabled	0
8	RGMII RXD to RXC Skew	R/W	1 = Enable 0 = Disable	1
7:3	Reserved	R/W	Write as 0, ignore on read.	11100
2:0	Shadow Register Select	R/W	000 = Auxiliary register 001 = 10BASE-T register 010 = Power Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	111

Write Enable (Bits 11:3)

If bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register is set when writing to this register, then bits [11:3] of this register can be modified. Bits [2:0] and [14:12] can always be written regardless of the state of bit 15.

When this bit is set, bits [11:3] are written. When this bit is cleared, only bits [14:12] and [2:0] are written.

Shadow Register Read Selector

Bits [14:12] of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register are written, regardless of the value of bit 15. These bits determine the shadow value for an MII register 18h read operation. See the note in "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 67 describing reading from and writing to register 18h.

Packet Counter Mode

Bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register sets the Packet Counter mode in Expansion register 00h. The counter counts the receive packet when this bit is set; otherwise, it counts the transmit packet.

Force Auto-MDIX Mode

Bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register enable the Auto-MDIX mode while auto-negotiation is disabled. The default is to disable the auto-MDIX function when auto-negotiation is disabled.

RXD–to–RXC

Skew time can be increased by approximately 1.9 ns for 1000BASE–T mode, 4 ns for 100BASE–T mode, and 50 ns for 10BASE–T mode by setting Register 18h, SV 111, bit 8 = 1. Enabling this timing adjustment eliminates the need for board trace delays, as required by the RGMII specification.

Shadow Register Select

Using a shadow technique, the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register provides access to 8 registers. The lower 3 bits written define which set of 13 upper bits are used in accordance with Table 49, defined under bits 2:0.

See the note on "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 67 describing reading from and writing to register 18h. The register set previously shown is for miscellaneous control obtained when the lower 3 bits are 111.

1000BASE-T/100BASE-TX/10BASE-T AUXILIARY STATUS SUMMARY

Table 50: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary Register (Address 19h)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation in progress	0
14	Auto-negotiation Complete Acknowledge	RO LH	1 = Entered auto-negotiation link good check state 0 = State not entered since last read	0
13	Auto-negotiation Acknowledge Detect	RO LH	1 = Entered auto-negotiation acknowledge detect state 0 = State not entered since last read	0
12	Auto-negotiation Ability Detect	RO LH	1 = Entered auto-negotiation ability detect state 0 = State not entered since last read	0
11	Auto-negotiation Next Page Wait	RO LH	1 = Entered auto-negotiation Next Page wait state 0 = State not entered since last read	0
10:8	Auto-negotiation HCD (Current Operating Speed and Duplex Mode)	RO	111 = 1000BASE-T full-duplex[a] 110 = 1000BASE-T half-duplex[a] 101 = 100BASE-TX full-duplex[a] 100 = 100BASE-T4 011 = 100BASE-TX half-duplex[a] 010 = 10BASE-T full-duplex[a] 001 = 10BASE-T half-duplex[a] 000 = No highest common denominator or auto-negotiation not complete	000
7	Parallel Detection Fault	RO LH	1 = Parallel link fault detected 0 = Parallel link fault not detected	0
6	Remote Fault	RO	1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault	0
5	Auto-negotiation Page Received	RO LH	1 = New page has been received from link partner 0 = New page has not been received	0
4	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability 0 = Link partner does not perform auto-negotiation	0
3	Link Partner Next Page Ability	RO	1 = Link partner has Next Page capability 0 = Link partner does not have Next Page capability	0
2	Link Status	RO	1 = Link is up (link-pass state) 0 = Link is down (link fail state)	0
1	Pause Resolution—Receive Direction	RO	1 = Enable pause receive 0 = Disable pause receive	0
0	Pause Resolution—Transmit Direction	RO	1 = Enable pause transmit 0 = Disable pause transmit	0

a. Indicates the negotiated HCD when auto-negotiation enable = 1, or indicates the manually selected speed and Duplex mode when auto-negotiation enable = 0.

Auto-Negotiation Complete

When auto-negotiation is complete, the B50610 returns a 1 in bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register. This bit returns a 0 while auto-negotiation is in progress.

Auto-Negotiation Complete Acknowledge

The B50610 returns a 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the link good check state since the last time this register was read; otherwise, it returns a 0.

Auto-Negotiation Acknowledge Detect

The B50610 returns a 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the acknowledge detect state since the last time this register was read; otherwise, it returns a 0.

Auto-Negotiation Ability Detect

The B50610 returns a 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the ability detect state since the last time this register was read; otherwise, it returns a 0.

Auto-Negotiation Next Page Wait

The B50610 returns a 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the Next Page wait state since the last time this register was read; otherwise, it returns a 0.

Auto-Negotiation HCD (Current Operating Speed and Duplex Mode)

Bits 10:8 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register report the mode of operation negotiated between the B50610 and its link partner. As reported by bit 15 of the Auxiliary Status Summary register, the bits return **000** until auto-negotiation has completed. When the auto-negotiation function has been disabled, bits [10:8] report the manually selected mode of operation.

Parallel Detection Fault

When a parallel detection fault has occurred in the auto-negotiation state machine, bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register returns a 1. When a parallel detection fault occurs, this bit is latched to a 1 and remains so until the next register read. This bit returns a 0 when a parallel detection fault has not occurred since the last time it was read.

Remote Fault

The B50610 returns a 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner has detected a remote fault; otherwise, it returns a 0.

Auto-Negotiation Page Received

The B50610 returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns a 0.

Link Partner Auto-Negotiation Ability

The B50610 returns a 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged or if the link partner does not comply with IEEE auto-negotiation, the bit returns a 0.

Link Partner Next Page Ability

The B50610 returns a 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner needs to transmit Next Page information; otherwise, it returns a 0.

Link Status

The B50610 returns a 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link status is good; otherwise, it returns a 0.

Pause Resolution—Receive Direction and Transmit Direction

When auto-negotiation has completed, the B50610 returns the result of the pause resolution function for full-duplex flow control on bits [1:0] of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register. When bit 1 returns a 1, the link partner can send pause frames toward the local device. When bit 0 returns a 1, pause frames can be transmitted by the local device to the link partner. These bits are only guaranteed to be valid when bit 15 of the Auxiliary Status Summary register is 1.

1000BASE-T/100BASE-TX/10BASE-T INTERRUPT STATUS

Table 51: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah)

Bit	Name	R/W	Description	Default
15	Energy Detect Change	RO LH	1 = Filtered energy detect change since last read (enabled by register 1Ch, shadow 00101, bit 5 = 1) 0 = Interrupt cleared	0
14	Illegal Pair Swap	RO LH	1 = Illegal pair swap detected 0 = Interrupt cleared	0
13	MDIX Status Change	RO LH	1 = MDIX status changed since last read 0 = Interrupt cleared	0
12	Exceeded High Counter Threshold	RO	1 = Value in one or more counters is above 32K 0 = All counters below 32K	0
11	Exceeded Low Counter Threshold	RO	1 = Value in one or more counters is above 128K 0 = All counters below 128K	0
10	Auto-negotiation Page Received	RO LH	1 = Page received since last read 0 = Interrupt cleared	0
9	No HCD Link	RO LH	1 = Negotiated HCD, did not establish link 0 = Interrupt cleared	0
8	No HCD	RO LH	1 = Auto-negotiation returned HCD = none 0 = Interrupt cleared	0
7	Negotiated Unsupported HCD	RO LH	1 = Auto-negotiation HCD not supported by B50610 0 = Interrupt cleared	0
6	Scrambler Synchronization Error	RO LH	1 = Scrambler synchronization error occurred since last read 0 = Interrupt cleared	0
5	Remote Receiver Status Change	RO LH	1 = Remote receiver status changed since last read 0 = Interrupt cleared	0
4	Local Receiver Status Change	RO LH	1 = Local receiver status changed since last read 0 = Interrupt cleared	0
3	Duplex Mode Change	RO LH	1 = Duplex mode changed since last read 0 = Interrupt cleared	0
2	Link Speed Change	RO LH	1 = Link speed changed since last read 0 = Interrupt cleared	0
1	Link Status Change	RO LH	1 = Link status changed since last read 0 = Interrupt cleared	0
0	CRC Error	RO LH	1 = CRC error occurred since last read 0 = Interrupt cleared	0

The INTR output is asserted when any bit in 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register is set and the corresponding bit in the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask register is cleared.

Energy Detect Change

This bit indicates the copper ED changed since the last read.

Illegal Pair Swap

The B50610 returns a 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when an uncorrectable pair swap error on the twisted-pair cable has been detected since the last time this register was read; otherwise, it returns a 0.

MDIX Status Change

The B50610 returns a 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a link pulse or 100BASE-TX carrier was detected on a different pair than previously detected since the last time this register was read; otherwise, it returns a 0.

Exceeded High Counter Threshold

The B50610 returns a 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when one or more of the counters in registers 12–14h is above 32 000; otherwise, it returns a 0.

Exceeded Low Counter Threshold

The B50610 returns a 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when one or more of the counters in registers 12–14h is above 128 000; otherwise, it returns a 0.

Auto-Negotiation Page Received

The B50610 returns a 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns a 0.

No HCD Link

When the negotiated HCD is not able to establish a link, bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns a 1 by the B50610. The bit is cleared when the register is read.

No HCD

When auto-negotiation returns no HCD, bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns a 1 by the B50610. The bit is cleared when the register is read.

Negotiated Unsupported HCD

When the auto-negotiation HCD is not supported by the B50610, bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns a 1. The B50610 does not support 100BASE-T4. The bit is cleared when the register is read.

Scrambler Synchronization Error

The B50610 returns a 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a scrambler synchronization error has been detected since the last time this register was read; otherwise, it returns a 0.

Remote Receiver Status Change

The B50610 returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the remote receiver status has changed since the last time this register was read; otherwise, it returns a 0.

Local Receiver Status Change

The B50610 returns a 1 in bit 4 of the Interrupt Status register when the local receiver status has changed since the last time this register was read; otherwise, it returns a 0.

Duplex Mode Change

The B50610 returns a 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the Duplex mode has changed since the last time this register was read; otherwise, it returns a 0.

Link Speed Change

The B50610 returns a 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the link speed has changed since the last time this register was read; otherwise, it returns a 0.

Link Status Change

The B50610 returns a 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the link status has changed since the last time this register was read; otherwise, it returns a 0.

CRC Error

The B50610 returns a 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a receive CRC error has been detected since the last time this register was read; otherwise, it returns a 0.

1000BASE-T/100BASE-TX/10BASE-T INTERRUPT MASK

Table 52: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh)

Bit	Name	R/W	Description	Default
15	Energy Detect Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
14	Illegal Pair Swap	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
13	MDIX Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
12	Exceeded High Counter Threshold	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
11	Exceeded Low Counter Threshold	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
10	Auto-negotiation Page Received	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
9	HCD No Link	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
8	No HCD	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
7	Negotiated Unsupported HCD	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
6	Scrambler Synchronization Error	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
5	Remote receiver status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
4	Local receiver status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
3	Duplex mode Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
2	Link Speed Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
1	Link Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
0	CRC Error	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1

Interrupt Mask Vector

When bit *n* of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask register is written to 1, the interrupt corresponding to the same bit in the Interrupt Status register is masked. The status bits still operate normally when the interrupt is masked, but do not generate an interrupt output. When the bit is written to 0, the interrupt is unmasked.

1000BASE-T/100BASE-TX/10BASE-T Register 1Ch Access

Reading and writing to the 1000BASE-T/100BASE-TX/10BASE-T register 1Ch is through register 1Ch bits 15:10. Bits 14:10 set the shadow value of register 1Ch, and bit 15 enables the writing of the bits 9:0. Setting bit 15 allows writing to bits [9:0] of register 1Ch. To read register 1C shadow zzzzz, set writes to register 1Ch with bit 15 = 0 and bits 14:10 to zzzzz first. The subsequent register read from register 1Ch contains the shadow zzzzz register value. All of the register 1Ch shadow values are listed in the following table.

Table 53: 1000BASE-T/100BASE-TX/10BASE-T Register 1Ch Shadow Values

Shadow Value	*Register Name*
00010	“1000BASE-T/100BASE-TX/10BASE-T Spare Control 1” on page 85
00011	“1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control” on page 87
00100	“1000BASE-T/100BASE-TX/10BASE-T Spare Control 2” on page 88
00101	“1000BASE-T/100BASE-TX/10BASE-T Spare Control 3” on page 89
01000	“1000BASE-T/100BASE-TX/10BASE-T LED Status” on page 90
01001	“1000BASE-T/100BASE-TX/10BASE-T LED Control” on page 92
01010	“1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down” on page 93
01011	“External Control 1 Register” on page 95
01101	“1000BASE-T/100BASE-TX/10BASE-T LED Selector 1” on page 97
01110	“1000BASE-T/100BASE-TX/10BASE-T LED Selector 2” on page 99
01111	“1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status” on page 100

1000BASE-T/100BASE-TX/10BASE-T SPARE CONTROL 1

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 register 1Ch with the shadow value in bits [14:10] = 00010.

Table 54: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 Register (Address 1Ch, Shadow Value 00010)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00010 = Spare Control 1 register	00010
9:4	Reserved	R/W	Write as 00h, ignore when read.	00h
3	Reserved	R/W	Write as 00h, ignore when read.	00h
2	Linkspeed	R/W	0 = Normal 1 = Dual Link speed indication	0
1	Reserved	R/W	Write as 00h, ignore when read.	1
0	Link LED Mode	R/W	1 = Enable link LED mode $\overline{\text{LINKSPD}}$[2:1] = speed 00: 1000BASE-T link 01: 100BASE-TX link 10: 10BASE-T link or no link $\overline{\text{SLAVE}}$ = Active low 10/100/1000BASE-T link 0 = Normal link LED mode	0

Write Enable

During a write to this register, setting Spare Control 1 register bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 00010 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 register address 1Ch.

Linkspeed

When Linkspeed bit is 0 (default), LINKSPD[2] and LINKSPD[1] provide link status as shown in Table 55.

Table 55: Default LED1 and LED2 Status

Status	*LINKSPD[2]*	*LINKSPD[1]*
1000BASE-T link	0	0
100BASE-T link	0	1
10BASE-T link	1	0
No link	1	1

Note: Using this mode, it is possible to connect LED1 and LED2 pins directly to a back-to-back connected, integrated LED block that can indicate a 1000BASE-T link or a 100BASE-T gigabit link only.

When Linkspeed bit is 1, LINKSPD[2] and LINKSPD[1] provide link status as shown in Table 56.

Table 56: Linkspeed LED1 and LED2 Status

Status	*LINKSPD[2]*	*LINKSPD[1]*
1000BASE-T link	1	0
100BASE-T link	0	1
10BASE-T link	1	1
No link	1	1

Link LED Mode

Bit 0 of 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 register 1Ch with shadow value 00010 selects the link LED mode. When this bit is set, it enables the link LED mode. The $\overline{\text{LINKSPD2}}$/$\overline{\text{LINKSPD1}}$ are Link/Speed LED and $\overline{\text{SLAVE}}$ LED is $\overline{\text{LINK}}$ LED to indicate a link for 10BASE-T, 100BASE-TX, or 1000BASE-T. When this bit is cleared, the $\overline{\text{LINKSPD2}}$, $\overline{\text{LINKSPD1}}$, and $\overline{\text{SLAVE}}$ are in normal mode.

1000BASE-T/100BASE-TX/10BASE-T CLOCK ALIGNMENT CONTROL

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control register 1Ch with shadow value in bits [14:10] = 00011.

Table 57: 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control Register (Address 1Ch, Shadow Value 00011)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00011 = Clock Alignment Control register	00011
9	GTXCLK Clock Delay Enable	R/W	1 = Enable GTXCLK delay 0 = Normal mode (bypass GTXCLK delay)	1
8:0	Reserved	R/W	Write as 000h, ignore when read.	000h

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment register bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 00011 to enable read/write to the Clock Alignment Control register address 1Ch.

GTXCLK Clock Delay Enable

Setting bit 9 of 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control register 1Ch with shadow value 00011 enables the GTXCLK internal delay. When this bit is cleared, the GTXCLK delay is bypassed.

1000BASE-T/100BASE-TX/10BASE-T SPARE CONTROL 2

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 00100.

Table 58: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 Register (Address 1Ch, Shadow Value 00100)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00100 = Spare Control 2 register	00100
9:5	Reserved	R/W	Write as 00h, ignore when read.	00h
4:2	Reserved	R/W	Write as 011, ignore on read.	011
1	Energy Detect on INTR Pin	R/W	1 = Routes Energy Detect to interrupt signal. Use LED selectors (register 1Ch shadow 01101 and 01110) and program to INTR mode. 0 = INTR pin is Interrupt function.	0
0	Reserved	R/W	Write as 0, ignore when read.	0

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] must be set to 00100 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 register.

Energy Detect on INTR Pin

Bit 1 enables the signal detect or energy detect input on the INTR pin. Set the LED selector register to enable INTR LED mode (1Ch shadow 01101 or 01110 set bit [7:4]/[3:0] to 0110 depending on the LED).

1000BASE-T/100BASE-TX/10BASE-T SPARE CONTROL 3

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 00101.

Table 59: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00101 = Spare Control 3 register	00101
9	Reserved	R/W	Write as 0, ignore when read.	0
8	TXC/RXC Disable During Auto Power-Down	R/W	1 = Disable TXC/RXC during auto power-down when there is not energy on the cable.	0
7:2	Reserved	R/W	Write as 07h, ignore when read.	07
1	CLK125 Auto Power-Down	R/W	1 = Auto power down of CLK125 is disabled. 0 = Auto power down of CLK125 is enabled.	1
0	CLK125 Output	R/W	1 = Enable CLK125 output 0 = Disable CLK125 output	1

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow register values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 00101 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 register.

TXC/RXC Disable During Auto Power-Down Mode

TBD

CLK125 Auto Power-Down

Clearing this bit enables the auto power-down mode of the CLK125 output. This feature enables additional power savings. This feature should only be used during auto power-down mode.

CLK125 Output

For the 100-pin BGA package, setting this bit enables the CLK125 output; clearing this bit disables the CLK125 output.

For the 48-pin MLP packages, setting this bit disable the CLK125 output; clearing this bit enable the CLK125 output.

1000BASE-T/100BASE-TX/10BASE-T LED STATUS

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 01000.

Table 60: 1000BASE-T/100BASE-TX/10BASE-T LED Status Register (Address 1Ch, Shadow Value 01000)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01000 = LED Status register	01000
9	Reserved	R/O	Write as 0, ignore when read.	0
8	$\overline{\text{Slave}}$ Indicator	RO	1 = Master mode 0 = Slave mode	0
7	$\overline{\text{FDX}}$ Indicator	RO	1 = Half-duplex mode 0 = Full-duplex mode	0
6	$\overline{\text{INTR}}$ Indicator	RO	1 = No active Interrupt 0 = Interrupt activated	1
5	Reserved	RO	Write as 0, ignore when read.	0
4:3	$\overline{\text{LINKSPD}}$ Indicator	RO	11 = No link 10 = 10BASE-T LINK 01 = 100BASE-TX LINK 00 = 1000BASE-T LINK	11
2	$\overline{\text{Transmit}}$ Indicator	RO	1 = No transmit activity 0 = Transmit activity	1
1	$\overline{\text{Receive}}$ Indicator	RO	1 = Not receive activity 0 = Receive activity	1
0	Reserved	RO	Write as 0, ignore when read.	1

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01000 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Status register.

$\overline{\text{Slave}}$ Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 8 returns a 0, the device is in the slave mode. When this bit returns a 1, the device is not in the slave mode.

$\overline{\text{FDX}}$ Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 7 returns a 0, the device is in the full-duplex mode. When this bit returns a 1, the device is not in the full-duplex mode.

$\overline{\text{INTR}}$ Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 6 returns a 0, the device is in the interrupted mode. When this bit returns a 1, the device is not in the interrupted mode.

$\overline{\text{LINKSPD}}$ Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bits 4:3 return a 00, the device is in the 1000BASE-TX Link mode. When these bits return a 01, the device is in the 100BASE-TX link mode. When these bits return a 10, the device is in the 10BASE-T link mode. When these bits return an 11, the device is not linked.

$\overline{\text{Transmit}}$ Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 2 returns a 0, the device is in transmit mode. When this bit returns a 1, the device is not in transmit mode.

$\overline{\text{Receive}}$ Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 1 returns a 0, the device is in receive mode. When this bit returns a 1, the device is not in receive mode.

1000BASE-T/100BASE-TX/10BASE-T LED CONTROL

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 01001.

Table 61: 1000BASE-T/100BASE-TX/10BASE-T LED Control Register (Address 1Ch, Shadow Value 01001)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01001 = LED Control register	01001
9:6	Reserved	R/W	Write as 00000, ignore when read.	00000
5	Reserved	R/W	Write as 0, ignore when read.	0
4	Activity/Link LED Enable	R/W	1 = Drive activity/link data on $\overline{\text{ACTIVITY}}$ LED 0 = Drive activity data on $\overline{\text{ACTIVITY}}$ LED	0
3	$\overline{\text{ACTIVITY}}$ LED Enable	R/W	1 = Drive activity data on $\overline{\text{ACTIVITY}}$ LED 0 = Drive receive data on $\overline{\text{ACTIVITY}}$ LED	1
2	Remote Fault LED Enable	R/W	Indicate remote fault 1 = Indicate remote fault 0 = Normal operation	0
1:0	Link Utilization LED Selector	R/W	00 = Normal activity (fixed blink rate) 01 = Transmit activity with variable blink rate 10 = Receive activity with variable blink rate 11 = Transmit/receive activity with variable blink rate ***Note:*** This mode has higher priority than the activity LED Enable mode in bit 3.	00

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01001 to enable read/write to the register address 1Ch.

Activity/Link LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 4 drives activity/link data on $\overline{\text{ACTIVITY}}$ LED.

$\overline{\text{ACTIVITY}}$ LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 3 drives activity data on $\overline{\text{ACTIVITY}}$ LED. Otherwise, it drives receive data on $\overline{\text{ACTIVITY}}$ LED.

Remote Fault LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 2 drives remote fault LED.

Link Utilization LED Selector

These bits apply to the LED programmed to the ACTIVITY mode only. In the activity LED mode, the LED expresses an estimated activity in terms of blink rate. The blink rate of the LED increases as the activity duty cycle increases by increments of 10%. For duty cycles of 0.001% to10%, the LED blinks at 3 Hz; for duty cycles of 10% to 20%, the LED blinks at 6 Hz; and for duty cycles of 90% to 96%, the LED blinks at 30 Hz. Even though the frequency of the LED blink increases, the duty cycle of the LED stays at about 50%. The ACTIVITY LED can be programmed to display the following:

- 00 = Normal activity (fixed blink rate)
- 01 = Transmit activity with variable blink rate
- 10 = Receive activity with variable blink rate
- 11 = Transmit/receive activity with variable blink rate

1000BASE-T/100BASE-TX/10BASE-T AUTO POWER-DOWN

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register 1Ch with shadow value in bits [14:10] = 01010.

Table 62: Auto Power-Down Register (Address 1Ch, Shadow Value 01010)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01010 = Auto Power-Down register	01010
9:6	Reserved	R/W	Write as 0h, ignore when read.	0h
5	Auto Power-Down Mode	R/W	1 = Auto power-down mode enabled 0 = Auto power-down mode disabled	0
4	Sleep Timer Select	R/W	1 = Sleep timer is 5.4s. 0 = Sleep timer is 2.7s.	0
3:0	Wake-up Timer Select	R/W	Counter for wake-up timer in units of 84 ms. 0001 = 84 ms 0010 = 168 ms ... 1111 = 1.26s	0001

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 01010 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register address 1Ch.

Auto Power-Down Mode

Setting this bit enables the auto power-down mode.

Sleep Timer Select

Setting this bit changes the wake-up time leaving auto power-down mode.

Wake-up Timer Select

The port continues wake-up mode for a time based on the count stored in this register. The minimum value is 84 ms and the maximum value is 1.26s. This only applies when the part is in auto power-down mode.

EXTERNAL CONTROL 1 REGISTER

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 01011.

Table 63: External Control 1 Register (Address 1Ch, Shadow Value 01011)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0], 0 = Read bits [9:0].	0
14:10	Shadow Register Selector	R/W	01011 = External Control 1 register	01011
9:8	Reserved	R/W	Write as 0h, ignore when read.	0h
7	CLK125_NONRGMII Disable	R/W	1 = CLK125_NONRGMII clock output disable 0 = CLK125_NONRGMII clock output enable	0
6	SOFT-RESET Enable	R/W	1 = SOFT-RESET function enable 0 = SOFT-RESET function disable	0
5	Reserved	R/W	Write as 0h, ignore when read.	0h
4	MODE_SEL[1]	R/W	MODE_SEL[1], in 48-pin MLP package only.	LED[3] pin
3	MODE_SEL[0]	R/W	MODE_SEL[0], in 48-pin MLP package only.	LED[2] pin
2	LOM LED Mode	R/W	1 = LOM LED mode enabled, in 48-pin MLP package only. 0 = LOM LED mode disabled, in 48-pin MLP package only.	LED[4] pin
1: 0	Reserved	R/W	Write as 0h, ignore when read.	0h

Write Enable

During a write to this register, setting External Control 1 register bit 15 to a 1 allows writing to bits[9:0] of this register. To read the values of bits[9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits[14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits[9:0].

Shadow Register Selector

Register bits[14:10] must be set to 01011 to enable read/write to the External Control 1 register address 1Ch.

CLK125_NONRGMII Disable

Register bit 7 disables CLK125_NONRGMII clock output. To save additional power, CLK125_NONRGMII output can be disabled by setting this bit to 1. In the 48-pin MLP package, bit 7 is set to 1 for disabling CLK125_NONRGMII by the default value.

SOFT-RESET Enable

Register bit 6 enables SOFT-REST feature. After enable this function, set PHY register 0x00h bit 15 value of “1” will be a soft reset. This soft reset will reset everything expect for the MDIO registers.

After enabling the SOFT-RESET function, the PHY register 0x00h bit 15 will not be able to self clear. Write a “0” to bit 15 of the MII Control register (address 00h) to clear it after software reset.

MODE_SEL[1:0]

Setting these bits selects the different RGMII MODE.

Note: Bit 3 MODE_SEL[0] default value is LED[2] strap if LOM LED Mode = 0. The default value is 0 if LOM LED Mode = 1. If LOM LED Mode = 1, LED[2] strap is ignored.

LOM LED Mode

Setting this bit enables LOM LED MODE.

Note: This register bit 4:2 are only applicable when the device is in the 48-pin MLP package.

External Control 2 Register

The following is enabled by External Control 2 Register register 1Ch with shadow value in bits [14:10] = 01100.

Table 64: External Control 2 Register (Address 1Ch, Shadow Value 01100)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01100 = External Control 2 register	01100
9:1	Reserved	R/W	Write as 00, ignore when read.	00
0	Enable IDDQ	R/W	For the 100-pin FBGA package, IDDQ mode can be activated by setting this register bit, test0=0, test1 = 0, and reset_n = 1. For the 48-pin MLP package, IDDQ mode can be activated by setting this register bit, (test3, test2) = 00 or 11, and reset_n = 1	0

Write Enable

During a write to this register, setting External Control 2 register bit 15 to a 1 allows writing to bits [7:0] of this register. For reading the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01100 to enable read/write to the External Control 2 register address 1Ch.

Enable IDDQ

The B50610 can be placed into the ultra–low power–down mode (IDDQ), consuming the lowest power possible while voltage is being supplied to the device. This mode is especially useful for saving battery life in laptop designs when the user does not require a network connection. In the 100-pin FBGA package, the B50610 has a dedicated LOWPWR pin that is continuously sampled, allowing this feature to be easily entered or exited. See “Ultra-Low Power-Down Mode” on page 22 for more details.

1000BASE-T/100BASE-TX/10BASE-T LED SELECTOR 1

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value in bits [14:10] = 01101.

Table 65: 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01101 = LED Selector 1 register	01101
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED2 Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{LED2/FDX}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{REMOTE FAULT}}$ 1000: $\overline{\text{RCVLED}}$ 1001: Reserved 1010: $\overline{\text{MULTICOLOR[2]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: Reserved 1101: Reserved 1110: Off (high) 1111: On (low)	0001
3:0	LED1 Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{LED2/FDX}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{REMOTEFAULT}}$ 1000: $\overline{\text{RCVLED}}$ 1001: Reserved 1010: $\overline{\text{MULTICOLOR[1]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: Reserved 1101: Reserved 1110: Off (high) 1111: On (low)	0000

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Selector register 1 bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01101 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Selector register 1 address 1Ch.

LED2 ($\overline{\text{LINKSPD[2]}}$) Selector

Bits [7:4] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value 01101 select the LED2 mode.

LED1 ($\overline{\text{LINKSPD[1]}}$) Selector

Bits [3:0] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value 01101 select the LED1 mode.

1000BASE-T/100BASE-TX/10BASE-T LED SELECTOR 2

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value in bits [14:10] = 01110.

Table 66: 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 Register (Address 1Ch, Shadow Value 01110)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01110 = LED Selector 2 register	01110
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED4 Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{LED2/FDX}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{REMOTEFAULT}}$ 1000: $\overline{\text{RCVLED}}$ 1001: Reserved 1010: $\overline{\text{MULTICOLOR[2]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: Reserved 1101: Reserved 1110: Off (high) 1111: On (low)	0110
3:0	LED3 Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{LED2/FDX}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{REMOTEFAULT}}$ 1000: $\overline{\text{RCVLED}}$ 1001: Reserved 1010: $\overline{\text{MULTICOLOR[1]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: Reserved 1101: Reserved 1110: Off (high) 1111: On (low)	0011

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01110 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register address 1Ch.

LED4 ($\overline{\text{INTR}}$) Selector

Bits [7:4] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value 01110 select the LED2 mode.

LED3 ($\overline{\text{ACTIVITYLED}}$) Selector

Bits [3:0] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value 01110 select the LED1 mode.

1000BASE-T/100BASE-TX/10BASE-T LED GPIO CONTROL/STATUS

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register 1Ch with shadow value in bits [14:10] = 01111.

Table 67: 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status Register (Address 1Ch, Shadow Value 01111)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01111 = LED GPIO Control/Status register	01111
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED I/O Status	RO	Bit 7: LED4 pin status Bit 6: LED3 pin status Bit 5: LED2 pin status Bit 4: LED1 pin status 1 = LED pin is an input. 0 = LED pin is an output.	0h
3:0	Programmable LED I/O Control	R/W	Bit 3: LED4 pin control Bit 2: LED3 pin control Bit 1: LED2 pin control Bit 0: LED1 pin control 1 = Disable LED output 0 = Enable LED output	0h

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bits [14:10] must be set to 01111 to enable read/write to the register address 1Ch.

LED I/O Status

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bits [7:4] read back the status of the LED pin.

Programmable LED I/O Control

Setting 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bits [3:0] sets the LED pin to disable LED output. Clearing LED GPIO Control/Status register bits [3:0] sets the LED pin to enable LED output.

1000BASE-T/100BASE-TX/10BASE-T MASTER/SLAVE SEED

Table 68: 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed Register (Address 1Dh) Bit 15=0

Bit	*Name*	*R/W*	*Description*	*Default*
15	Enable Shadow Register	R/W	1 = Select shadow register 0 = Normal operation Writes to the selected register are done on a single cycle.	0
14	Master/Slave Seed Match	RO LH	1 = Seeds match. 0 = Seeds do not match.	0
13	Link Partner Repeater/DTE Bit	RO	1 = Link partner is a repeater/switch device port. 0 = Link partner is a DTE device port.	0
12	Link Partner Manual Master/Slave Configuration Value	RO	1 = Link partner is configured as master. 0 = Link partner is configured as slave.	0
11	Link Partner Manual Master/Slave Configuration Enable	RO	1 = Link partner manual master/slave configuration enabled 0 = Link partner manual master/slave configuration disabled	0
10:0	Local Master/Slave Seed Value	R/W	Returns the automatically generated M/S random seed.	000h

Enable Shadow Register

When bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register is cleared, the Master/Slave Seed register is selected. If bit 15 is set, the shadow HCD Status register is selected for read/write.

Master/Slave Seed Match

Bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns a 1 when the master/slave seed matches; otherwise, it returns a 0.

Link Partner Repeater/DTE Bit

When this read-only bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns a 1, it indicates that the link partner is configured as a repeater or a switch. If this bit returns a 0, it indicates that the link partner is configured as a DTE port.

Link Partner Manual Master/Slave Configuration Value

When this read-only bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns a 1, it indicates that the link partner is configured as a master. If this bit returns a 0, it indicates that the link partner is configured as a slave.

Link Partner Manual Master/Slave Configuration Enable

When this read-only bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns a 1, it indicates that the link partner manual master/slave configuration is enabled. If this bit returns a 0, the link partner manual master/slave configuration is disabled.

Local Master/Slave Seed Value

Bits [10:0] of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register return the automatically generated local master/slave seed value.

1000BASE-T/100BASE-TX/10BASE-T HCD STATUS

Table 69: 1000BASE-T/100BASE-TX/10BASE-T HCD Status Register (Address 1Dh) Bit 15=1

Bit	*Name*	*R/W*	*Description*	*Default*
15	Enable Shadow Register	R/W	1 = Select Shadow register 0 = Normal operation	0
14	Reserved	RO	Write as 0, ignore on read	0
13	Reserved	RO	Write as 0, ignore on read	0
12	Reserved	RO LH	Write as 0, ignore on read	0
11	HCD 1000BASE-T FDX	RO LH	1 = Gigabit full-duplex occurred since last read 0 = HCD cleared	0
10	HCD 1000BASE-T	RO LH	1 = Gigabit half-duplex occurred since last read 0 = HCD cleared	0
9	HCD 100BASE-TXFDX	RO LH	1 = 100BASE-TX full-duplex occurred since last read 0 = HCD cleared	0
8	HCD 100BASE-T	RO LH	1 = 100BASE-TX half-duplex occurred since last read 0 = HCD cleared	0
7	HCD 10BASE-T FDX	RO LH	1 = 10BASE-T full-duplex occurred since last read 0 = HCD Cleared	0
6	HCD 10BASE-T	RO LH	1 = 10BASE-T half-duplex occurred since last read 0 = HCD cleared	0
5	HCD 1000BASE-T FDX (Link Never Came Up)	RO LH	1 = Gigabit full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0

Table 69: 1000BASE-T/100BASE-TX/10BASE-T HCD Status Register (Address 1Dh) Bit 15=1 (Cont.)

Bit	Name	R/W	Description	Default
4	HCD 1000BASE-T (Link Never Came Up)	RO LH	1 = Gigabit half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
3	HCD 100BASE-TX FDX (Link Never Came Up)	RO LH	1 = 100BASE-TX full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
2	HCD 100BASE-T (Link Never Came Up)	RO LH	1 = 100BASE-TX half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
1	HCD 10BASE-T FDX (Link Never Came Up)	RO LH	1 = 10BASE-T full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
0	HCD 10BASE-T (Link Never Came Up)	RO LH	1 = 10BASE-T half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0

Note: Bits 12:0 are cleared when auto-negotiation is disabled via MII register 0 bit 12 or restarted via MII register 0 bit 9**.**

Enable Shadow Register

When bit 15 of 1000BASE-T/100BASE-TX/10BASE-T HCD Status register is cleared, the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register is selected. If bit 15 is set, the shadow HCD Status register (auto-negotiation highest common denominator resolution) is selected for read/write. This bit must set to be able to read/write to the HCD Status register.

HCD 1000BASE-T FDX

When bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a Gigabit full-duplex HCD has occurred since the last read.

HCD 1000BASE-T

When bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a Gigabit half-duplex HCD has occurred since the last read.

HCD 100BASE-TX FDX

When bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 100BASE-TX full-duplex HCD has occurred since the last read.

HCD 100BASE-T

When bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 100BASE-TX half-duplex HCD has occurred since the last read.

HCD 10BASE-T FDX

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 10BASE-T full-duplex HCD has occurred since the last read.

HCD 10BASE-T

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 10BASE-T half-duplex HCD has occurred since the last read.

HCD 1000BASE-T FDX (Link Never Came Up)

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a Gigabit full-duplex HCD has occurred, but the link has not been established since the last read.

HCD 1000BASE-T (Link Never Came Up)

When bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a Gigabit half-duplex HCD has occurred, but the link has not been established since the last read.

HCD 100BASE-TX FDX (Link Never Came Up)

When bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 100BASE-TX full-duplex HCD has occurred, but the link has not been established since the last read.

HCD 100BASE-TX (Link Never Came Up)

When bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 100BASE-TX half-duplex HCD has occurred, but the link has not been established since the last read.

HCD 10BASE-T FDX (Link Never Came Up)

When bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 10BASE-T full-duplex HCD has occurred, but the link has not been established since the last read.

HCD 10BASE-T FDX (Link Never Came Up)

When bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 10BASE-T half-duplex HCD has occurred, but the link has not been established since the last read.

1000BASE-T/100BASE-TX/10BASE-T TEST REGISTER 1

Table 70: 1000BASE-T/100BASE-TX/10BASE-T Test Register 1 (Address 1Eh)

Bit	Name	R/W	Description	Default
15	CRC Error Counter Selector	R/W	1 = Receiver NOT_OK Counters (register 14h) becomes 16-bit CRC error counter (CRC errors are counted only after this bit is set). 0 = Normal operation	0
14:13	Reserved	R/W	Write as 00h, ignore when read.	00h
12	Force Link 10/100/ 1000BASE-T	R/W	1 = Force Link State machine into a link pass state. 0 = Normal operation	0
11:8	Reserved	R/W	Write as 00h, ignore when read.	00h
7	Manual Swap MDI State	R/W	1 = Manually swap MDI state 0 = Normal operation	0
6:0	Reserved	R/W	Write as 00h, ignore when read.	00h

CRC Error Counter Selector

Setting this bit enables the "1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter Register (Address 14h)" on page 65 to start counting CRC errors and store the counts in register 14h.

Force Link

Setting bit 12 = 1 forces the Link State Machine into the link pass state.

Manual Swap MDI State

Setting bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Test register 1 manually swaps the MDI transmit and receive pairs during forced 100BASE-TX and 10BASE-T operation. When this bit is set, the B50610 transceiver transmits on pairs TRD± {1} and receives on TRD[0]± when operating in 100BASE-TX and 10BASE-T modes. If this bit is cleared, the B50610 transmits on pairs TRD[0]± and receives on TRD[1]± when operating in 100BASE-TX and 10BASE-T modes. This bit is ignored when the auto-negotiation is enabled.

EXPANSION REGISTERS

EXPANSION REGISTER 00H: RECEIVE/TRANSMIT PACKET COUNTER

Expansion register 00h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 66 bits 11:0 = F00h, and read/write access is through register 15h.

Table 71: Expansion Register 00h: Receive/Transmit Packet Counter

Bit	Name	R/W	Description	Default
15:0	Packet Counter	R/W CR	Returns the transmitted and received packet count.	0000h

Packet Counter

The mode of this counter is set by bit 11 of "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control Register (Address 18h, Shadow Value 111)" on page 75. Either receive or transmit packets are counted. This counter is cleared on read and freezes at FFFFh.

EXPANSION REGISTER 04H: MULTICOLOR LED SELECTOR

Expansion register 04h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 66 bits 11:0 = F04h, and read/write access is through register 15h.

Table 72: Expansion Register 04h: Multicolor LED Selector

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as 00h, ignore on read.	00h
9	Flash Now	R/W SC	1 = Initiate a multicolor LED flash. This works only when the multicolor selector is set to 0111.	0
8	In Phase	R/W	1 = $\overline{\text{MULTICOLOR[1]}}$ and $\overline{\text{MULTICOLOR[2]}}$ are in phase. 0 = $\overline{\text{MULTICOLOR[1]}}$ and $\overline{\text{MULTICOLOR[2]}}$ are in opposite phase. ***Note:*** This is only valid when Multicolor LED Selector bits are set to 0000, 0010, 0011, 0110, 0111, 1000, 1001, 1010.	0
7:4	$\overline{\text{MULTICOLOR[2]}}$ LED Selector	R/W	Selects the Multicolor mode for $\overline{\text{MULTICOLOR[2]}}$ LED 0000: Encoded link/activity LED 0001: Encoded speed LED 0010: Activity flash LED 0011: Full-duplex LED 0100: Forced off 0101: Forced on 0110: Alternating LED (toggling between two of the states at 50% duty cycle with a 320 ms period) 0111: Flashing LED (toggling between 2 of the states with an 80 ms period) 1000: Link LED 1001: Activity LED 1010: Programmable blink LED	0h
3:0	$\overline{\text{MULTICOLOR[1]}}$ LED Selector	R/W	Selects the Multicolor mode for $\overline{\text{MULTICOLOR[1]}}$ LED 0000: Encoded link/activity LED 0001: Encoded speed LED 0010: Activity flash LED 0011: Full-duplex LED 0100: Forced off 0101: Forced on 0110: Alternating LED (toggling between 2 of the states at 50% duty cycle with a 320 ms period) 0111: Flashing LED (toggling between 2 of the states with an 80 ms period) 1000: Link LED 1001: Activity LED 1010: Programmable blink LED	0h

Flash Now

Asserting this bit causes a single flash to occur on either $\overline{\text{MULTICOLOR[2:1]}}$ LED, as long as its multicolor selector is set to 0111.

In Phase

When both LEDs are selected to the same mode, the $\overline{\text{MULTICOLOR[2:1]}}$ output pins toggle at the same time. This bit determines whether the pins are identical to each other or are inverses of each other. When the two LED pins are attached to a special multicolored LED, the resulting LED colors alternate either between off/amber (in phase) or red/green (out of phase).

$\overline{\text{MULTICOLOR[2]}}$ LED Selector

The bits [7:4] select the multicolor LED mode for $\overline{\text{MULTICOLOR[2]}}$. The user must determine what functions should appear on the two LED pins.

Example: For a different color toggling operation than the operation previously mentioned (such as red/amber), the user can put one of the selectors to the preferred toggle mode and other selector to a forced one.

$\overline{\text{MULTICOLOR[1]}}$ LED Selector

Bits [3:0] select the multicolor LED mode for $\overline{\text{MULTICOLOR[1]}}$.

EXPANSION REGISTER 05H: MULTICOLOR LED FLASH RATE CONTROLS

Expansion register 05h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 66 bits 11:0 = F05h, and read/write access is through register 15h.

Table 73: Expansion Register 05h: Multicolor LED Flash Rate Controls

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as 0h, ignore on read.	0h
11:6	Alternating Rate	R/W	Determines the width and gap for multicolor LED selector 0110 (alternating LED mode). 00h = 21 ms width, 21 ms gap 01h = 42 ms width, 42 ms gap 02h = 63 ms width, 63 ms gap ... 07h = 168 ms width, 168 ms gap ... 3Fh = 1.344s	07h
5:0	Flash Rate	R/W	Determines the width and minimum gap of every flash pulse for multicolor LED selector 0000 (encoded link/Activity mode), 0010 (Activity Flash mode) and 0111 (Flashing LED mode). 00h = 21 ms width, 21 ms gap 01h = 42 ms width, 42 ms gap 02h = 63 ms width, 63 ms gap ... 3Fh = 1.344s	01h

Alternating Rate

Setting Bits [11:6] changes the width and gap of the alternating LED modes. These bits are only valid when the $\overline{\text{MULTICOLOR}}$[1] LED Selector and/or the $\overline{\text{MULTICOLOR}}$[2] LED Selector bits = 0110. The duty cycle of the LEDs is exactly 50%.

Flash Rate

Setting Bits [5:0] determines the width and minimum gap of the flashing pulse. These bits are only valid when the $\overline{\text{MULTICOLOR}}$[1] LED Selector and/or the $\overline{\text{MULTICOLOR}}$[2] LED Selector bits = 0000, 0010, or 0111. The duty cycle of the flash rate is not exactly 50%.

EXPANSION REGISTER 06H: MULTICOLOR LED PROGRAMMABLE BLINK CONTROLS

Expansion register 06h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 66 bits 11:0 = F06h, and read/write access is through register 15h.

Table 74: Expansion Register 06h: Multicolor LED Programmable Blink Controls

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Write as 000h, ignore on read.	000h
5	Blink Update Now	R/W	1 = Change to the new blink rate now. 0 = Wait 1s before changing the blink rate. Controls when a change in the blink rate is actually displayed on the Programmable Blink LED.	0
4:0	Blink Rate	R/W	Programs the number of blinks per second of the Programmable Blink LED 00000 = No blink 00001 = 1 blink per second 00010 = 2 blinks per second 00011 = 3 blinks per second ... 11111 = 31 blinks per second	00000

Blink Update Now

Setting bit 5 updates the blink rate immediately. Clearing this bit causes the blink rate to be updated after the 1s interval timer expires. This bit is only valid when the $\overline{\text{MULTICOLOR[1]}}$ LED Selector and/or the $\overline{\text{MULTICOLOR[2]}}$ LED Selector bits = 0000, 0010, or 0111.

Blink Rate

Setting bits [4:0] determines the blink rate of the Programmable Blink LED. These bits are only valid when the $\overline{\text{MULTICOLOR[1]}}$ LED Selector and/or the $\overline{\text{MULTICOLOR[2]}}$ LED Selector bits = 0000, 0010, or 0111.

EXPANSION REGISTER 08H: 10BT CONTROLS

Expansion register 08h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 66 bits 11:0 = F08h, and read/write access is through register 15h.

Table 75: Expansion Register 08H: 10BT Controls

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as 000h, ignore on read.	000h
9	Auto Early DAC Wake	R/W	1 = Turn on automatic early DAC wake power savings mode. 0 = Turn off automatic early DAC wake power savings mode.	1
8:0	Reserved	R/W	Write as 001h, ignore on read.	001h

Auto Early DAC Wake

Setting bit 9 = 1 turns on automatic early DAC wake power savings mode. Setting bit 9 = 0 turns off automatic early DAC wake power savings mode

Note: Auto Early DAC Wake should be set to 0 as default.

Section 5: Timing and AC Characteristics

Table 76: Reset Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
Power up to $\overline{\text{RESET}}$ deassertion	RESET_PU	10	–	–	ms
$\overline{\text{RESET}}$ deassertion to normal PHY operation	RESET_WAIT	20	–	–	µs
$\overline{\text{RESET}}$ pulse length	RESET_LEN	2	–	–	µs
RESET rise/fall time	–	–	–	25	ns

Note:

- When $\overline{\text{RESET}}$ is low the following also needs to be true:
  - Valid clock signal at the XTALI input.
- All external power supplies need to be stable.
- Internal regulator output REGOUT need approximately 1 ms to stabilize after the voltage to the regulator input pin REGIN is stable.
- MII register read/write access and normal PHY operation can start at the end of the RESET_WAIT time.
- RESET_PU must be performed when the device is first powered up. Software reset or RESET_LEN do not need to be performed after RESET_PU.
- Software reset or RESET_LEN should not be performed until after RESET_PU and RESET_WAIT have been completed. After issuing a software reset or a RESET_LEN, normal PHY operation can begin after waiting RESET_WAIT time of 20 µs.
- CLK125 output remains active and stable during hardware and software reset.

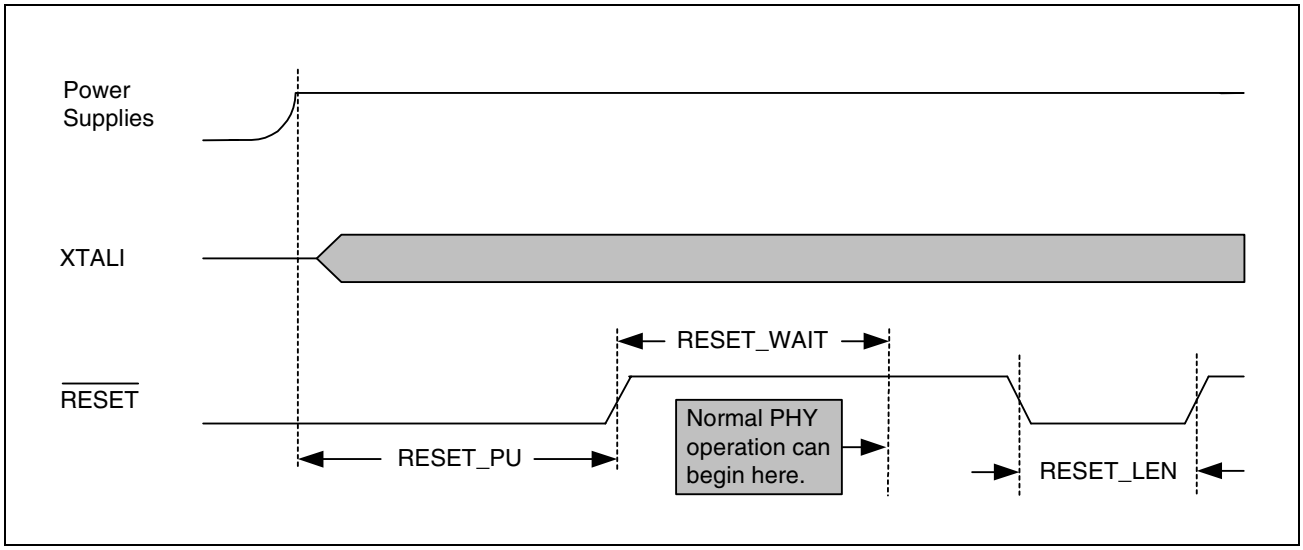


Figure 10: Reset Timing

REFCLK INPUT TIMING

Table 77: REFCLK Input Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
Frequency	C_{freq}	–	25	–	MHz
Accuracy	–	-50	–	+50	ppm
Duty Cycle Distortion[a]	–	40	–	60	%
Rise/Fall time[b]	T_r/T_f	–	–	4	ns
RMS Phase Jitter[c]	–	–	–	1.5	ps-rms

Note: Do not use PLL-based oscillators or zero-delay buffers as a source for REFCLK because this introduces excessive jitter that may result in unacceptable bit error rate performance.

a. Measured at 50% point.
b. Measured at the 20% to 80% points.
c. Fj = 12 kHz to 20-MHz offset frequency.

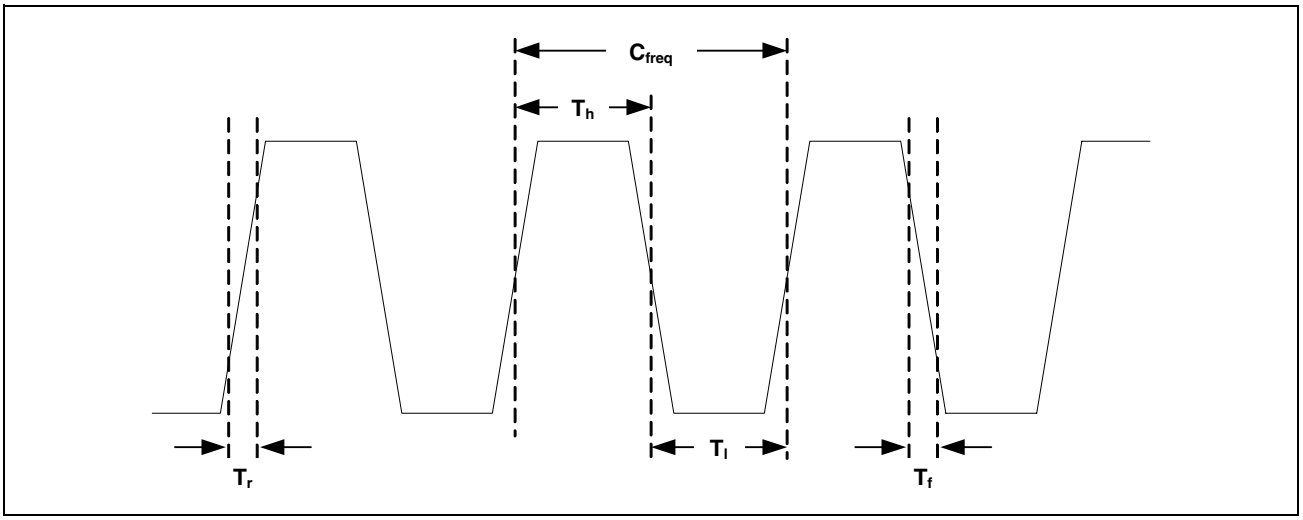


Figure 11: REFCLK Input Timing

Table 78: Management Interface Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
MDC cycle time	MDC_CYCLE	80	–	–	ns
MDC high/low		30	–	–	ns
MDIO input setup time to MDC rising	MDIO_SETUP	10	–	–	ns
MDIO input hold time from MDC rising	MDIO_HOLD	10	–	–	ns
MDIO output delay from MDC rising	MDIO_DELAY	0	–	50	ns

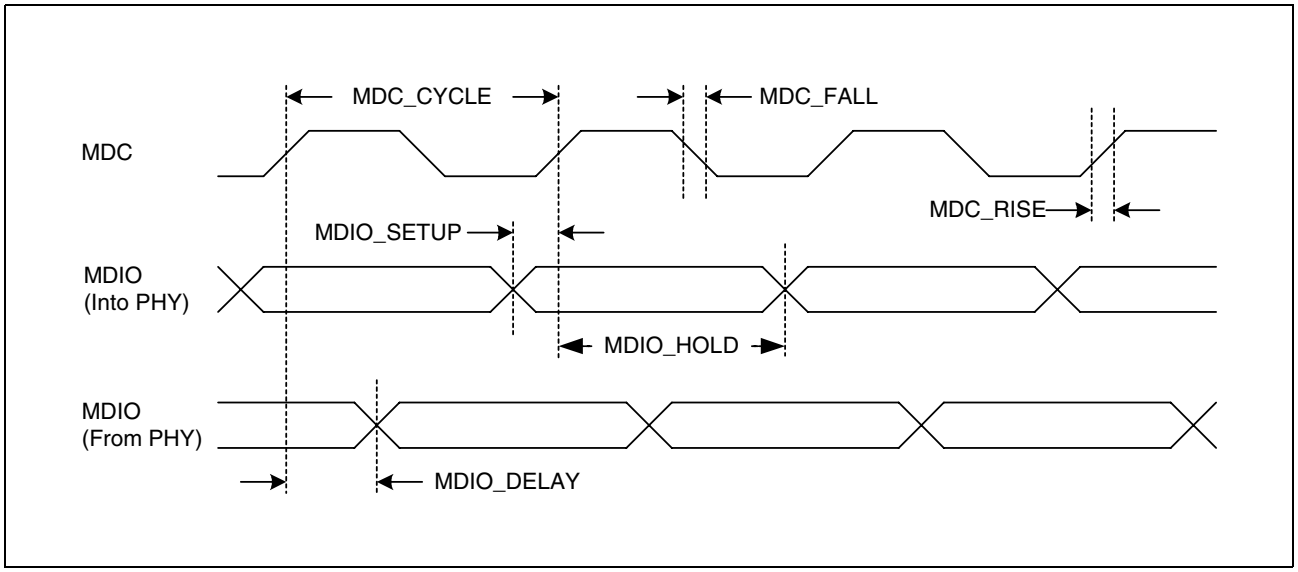


Figure 12: Management Interface Timing

Table 79: RGMII Input Timing (Normal Mode): GTXCLK and TXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
GTXCLK clock period	–	–	8	–	ns
GTXCLK pulse width	–	3600	–	–	ps
Input setup time	T_setup	1000	–	–	ps
Input hold time	T_hold	1000	–	–	ps

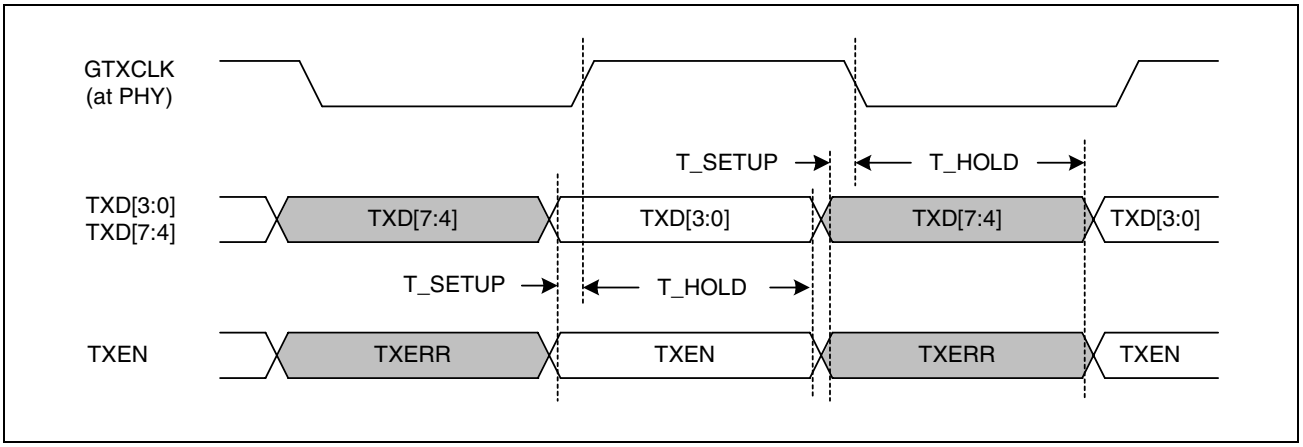


Figure 13: RGMII Input Timing (Normal Mode): GTXCLK and TXD[3:0]

Table 80: RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
GTXCLK clock period	–	–	8	–	ns
GTXCLK pulse width	–	3600	–	–	ps
Input setup time	T_setup_{DLY}	-900	–	–	ps
Input hold time	T_hold_{DLY}	2900	–	–	ps

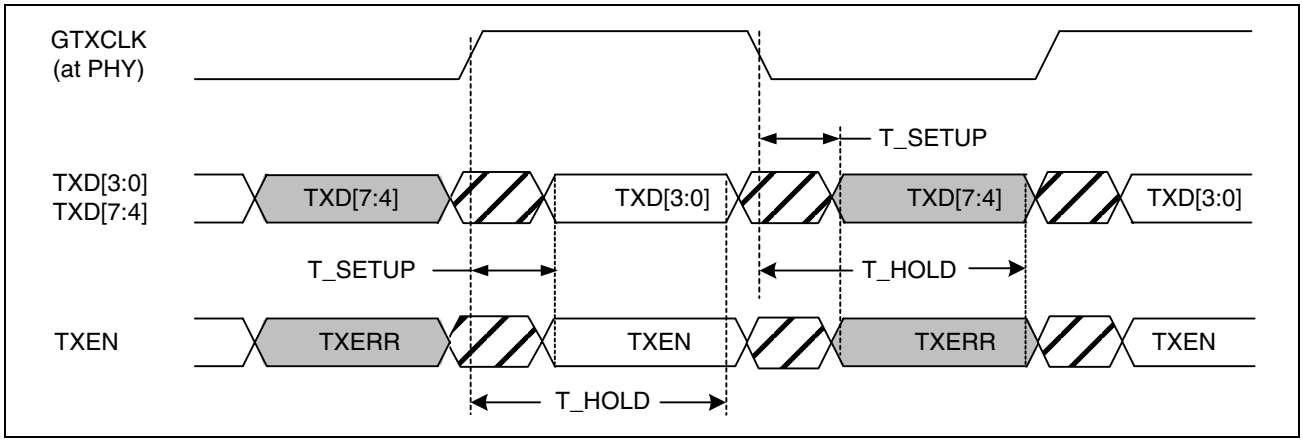


Figure 14: RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0]

Table 81: RGMII Output Timing (Normal Mode): RXC and RXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
RXC clock period	T_clk	–	8.0	–	ns
RXC clock pulse width	T_cw	3.6	–	–	ns
Data valid to clock transition: Available setup time at the output source	T_suav	-500	–	+500	ps
Clock transition to data valid: Available hold time at the output source	T_hav	3.1	–	–	ns

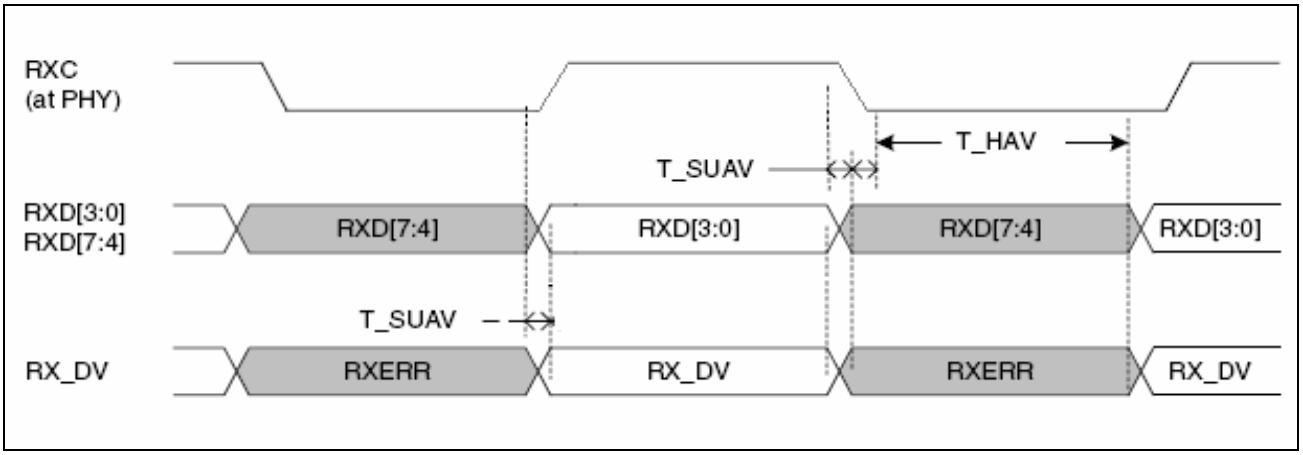


Figure 15: RGMII Output Timing (Normal Mode): RXC and RXD[3:0]

Table 82: RGMII Output Timing (Delayed Mode): RXC and RXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
RXC clock period	T_clk	–	8.0	–	ns
RXC clock pulse width	T_cw	3.6	–	–	ns
Data valid to clock transition: Available setup time at the output source	T_suav_{DLY}	1.2	2.0	–	ns
Clock transition to data valid: Available hold time at the output source	T_hav	1.2	–	–	ns

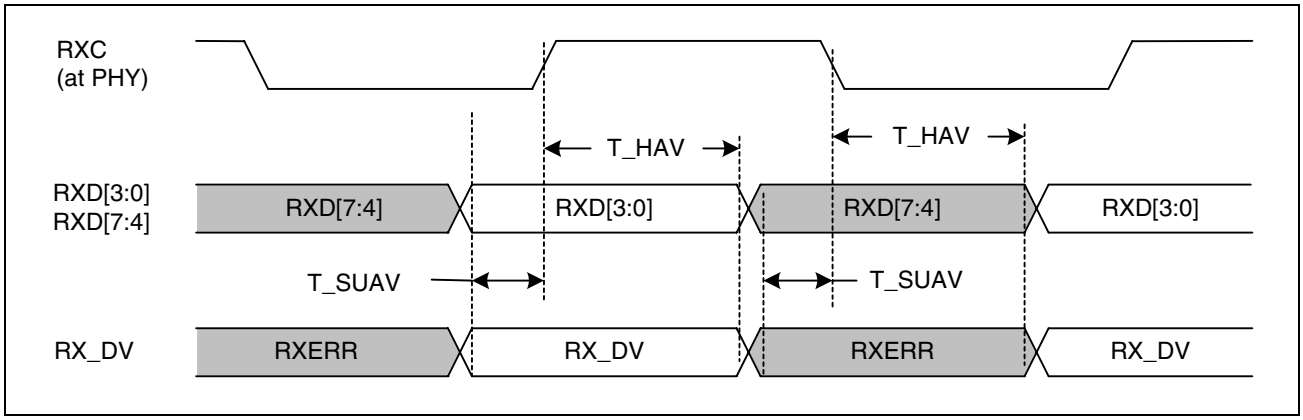


Figure 16: RGMII Output Timing (Delayed Mode): RXC and RXD[3:0]

Section 6: Electrical Characteristics

Table 83: Absolute Maximum Ratings

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*
Supply voltage (OVDD, OVDD_RGMII)	–	GND – 0.3	3.8	V
Supply voltage (AVDD, PVDD, BIASVDD, XTALVDD)	–	GND – 0.3	3.8	V
Supply voltage (AVDDL, DVDD, PLLVDD)	–	GND – 0.3	1.4	V
Storage temperature	T_{STG}	–40	125	°C
ESD protection	V_{ESD}	–1000	1000	V

Note: These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 84: DC Characteristics

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Condition*
Power Supply					
Supply current 3.3V	I_{OVDD}	–	–	mA	–
Supply voltage 3.3V	V_{OVDD}	2.38	3.46	V	–
Supply voltage 3.3V	V_{OVDD_RGMII}	3.14	3.46	V	–
Supply voltage 2.5V	V_{OVDD_RGMII}	2.38	2.62	V	–
Supply voltage 1.8V	V_{OVDD_RGMII}	1.71	1.89	V	–
Supply current 3.3V	$I_{AVDD, BIASVDD, XTALVDD}$	–	–	mA	–
Supply voltage 3.3V	$V_{AVDD, BIASVDD, XTALVDD}$	3.14	3.46	V	–
Supply current 1.2V	$I_{AVDDL, DVDD, PLLVDD}$	–	–	mA	–
Supply voltage 1.2V	$V_{AVDDL, DVDD, PLLVDD}$	1.14	1.26	V	–
XTALI Pin					
Input low voltage (XTALI)	V_{IL}	–0.30	0.80	V	XTALI Pin
Input high voltage (XTALI)	V_{IH}	1.70	XTALVDD	V	XTALI Pin
Digital Pin Operating @ 3.3V or 2.5V OVDD					
Input high voltage, digital (D) pin	V_{IH}	2.0	OVDD	V	–
Input low voltage, digital (D) pin	V_{IL}	–0.30	0.80	V	–
Output high voltage, digital (D) pin	V_{OH}	OVDD-0.40	–	V	I_{OH} = –8 mA
Output low voltage, digital (D) pin	V_{OL}	–	0.40	V	I_{OL} = 8 mA

Table 84: DC Characteristics (Cont.)

Parameter	Symbol	Minimum	Maximum	Unit	Condition
RGMII Pin Operating @ 3.3V OVDD_RGMII					
Input high voltage, RGMII (G) pin	V_{IH}	1.70	OVDD	V	–
Input low voltage, RGMII (G) pin	V_{IL}	–0.30	0.90	V	–
Output high voltage, RGMII (G) pin	V_{OH}	2.1		V	I_{OH} = –1 mA
Output low voltage, RGMII (G) pin	V_{OL}	0	0.50	V	I_{OL} = 1 mA
RGMII Pin Operating @ 2.5V OVDD_RGMII					
Input high voltage, RGMII (G) pin	V_{IH}	1.70	–	V	–
Input low voltage, RGMII (G) pin	V_{IL}	–	0.70	V	–
Output high voltage, RGMII (G) pin	V_{OH}	2.0	OVDD	V	I_{OH} = –1 mA
Output low voltage, RGMII (G) pin	V_{OL}	0	0.4	V	I_{OL} = 1 mA
RESET, MDIO, MDC Pins					
Positive edge threshold	VT+	2.0	OVDD	V	$\overline{\text{RESET}}$, MDIO, MDC pins
Negative edge threshold	VT–	-0.3	0.8	V	$\overline{\text{RESET}}$, MDIO, MDC pins
Hysteresis	V_{HYST}	250	400	mV	$\overline{\text{RESET}}$, MDIO, MDC pins

Section 7: Mechanical and Thermal

RoHS-Compliant Packaging

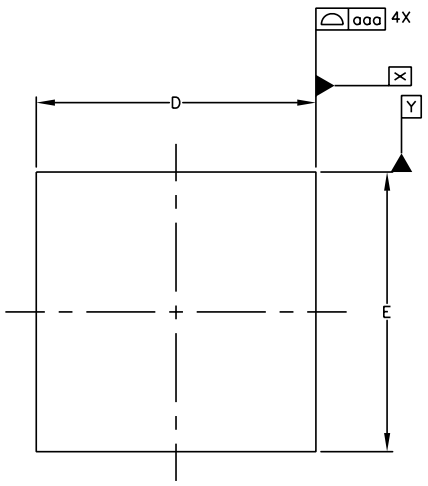
Broadcom offers both a standard package and an RoHS package that is compliant with RoHS and WEEE directives. Standard parts are also compliant with these directives, except for Pb (>1000 ppm). Table 85 on page 121 shows the main differences between standard and RoHS-compliant parts.

RoHS-compliant parts have the letter G added to the top line of the part marking. Standard parts (non Pb-free parts) are NOT compatible with the Pb-free surface-mount process. Refer to the PACKAGING-AN10*X*-R application note for more details.

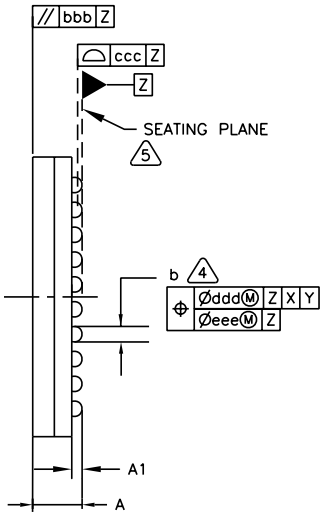
Table 85: Main Differences Between Standard and RoHS-Compliant Packages

Part Number	*Package*	*Solder Composition/Lead Plating Composition*	*Maximum Reflow Temperature*
B50610C1KFB	100-pin FBGA (Standard package)	63%Sn, 37%Pb	225°C
B50610C1KFBG	100-pin FBGA (RoHS compliant package)	95.5%Sn, 3%Ag, 0.5%Cu	255°C
B50610C1KML	48-pin MLP (Standard package)	85%Sn/15%Pb	225°C
B50610C1KMLG	48-pin MLP (RoHS compliant package)	100%Sn (Matte)	260°C

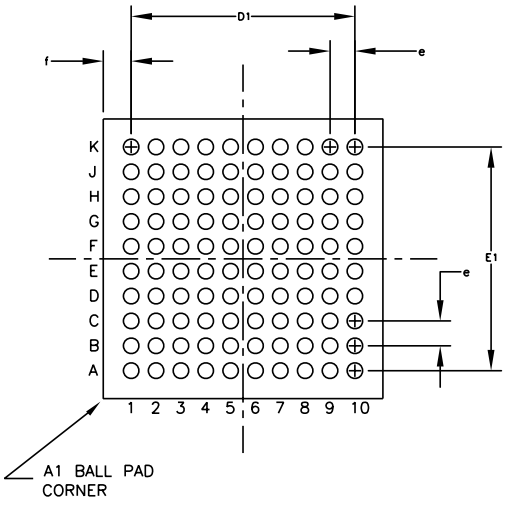
MECHANICAL INFORMATION



TOP VIEW



SIDE VIEW



BOTTOM VIEW
(100 SOLDER BALLS)

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.73
A1	0.28	0.33	0.40
D	8.80	9.00	9.20
D1		7.20 BSC	
E	8.80	9.00	9.20
E1		7.20 BSC	
b	0.45	0.50	0.55
e		0.80 BSC	
f	0.65	0.90	1.00
aaa	–	–	0.10
bbb	–	–	0.20
ccc	–	–	0.12
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD-008-1074-001

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

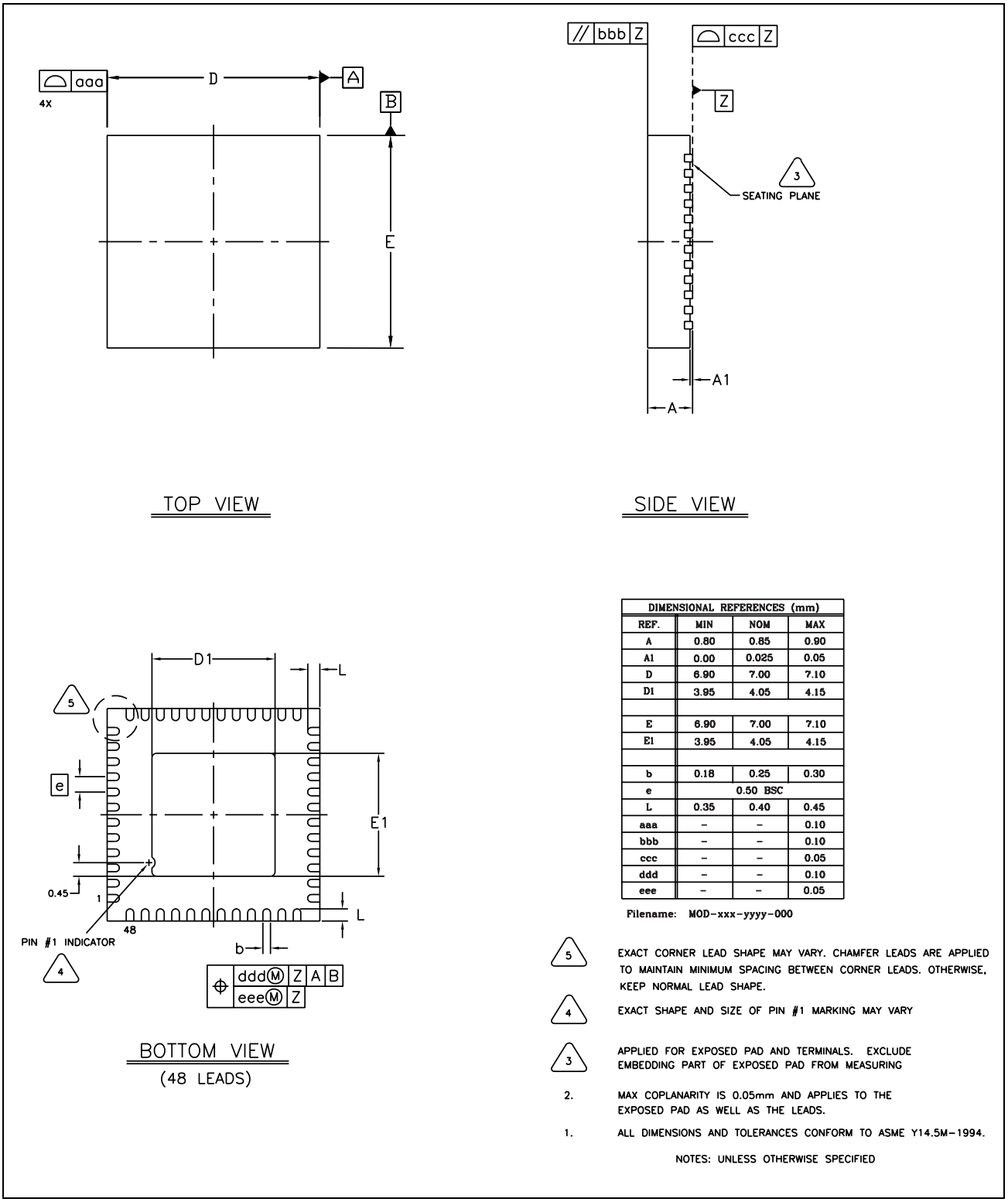
3. THE BASIC SOLDER BALL GRID PITCH IS 0.80mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-205F, VARIATION AB.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 17: 100-Pin FBGA Package



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.025	0.05
D	6.90	7.00	7.10
D1	3.95	4.05	4.15
E	6.90	7.00	7.10
E1	3.95	4.05	4.15
b	0.18	0.25	0.30
e		0.50 BSC	
L	0.35	0.40	0.45
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD-xxx-yyyy-000

5 EXACT CORNER LEAD SHAPE MAY VARY. CHAMFER LEADS ARE APPLIED TO MAINTAIN MINIMUM SPACING BETWEEN CORNER LEADS. OTHERWISE, KEEP NORMAL LEAD SHAPE.

4 EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY

3 APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING

2. MAX COPLANARITY IS 0.05mm AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 18: 48-Pin MLP Package

THERMAL INFORMATION

This section includes basic thermal information pertaining to the B50610 in the 100-pin FBGA and 48-pin MLP packages.

- Table 86 provides a comparison of Theta-J_A versus airflow for the 100-pin FBGA package.

Theta-J_C for this package is 30.29°C/W. Theta-J_B for this package is 39.31°C/W. The B50610 100-pin FBGA is designed and rated for a maximum junction temperature of 125°C.

Table 86: Theta-J_A vs. Airflow for the 100-pin FBGA Package

100-pin FBGA Package	*Air Flow (feet per minute)*				
	0	*100*	*200*	*400*	*600*
Theta-J_A (C/W)	62.88	59.79	58.67	57.29	56.35
PSI-JT	2.31	2.56	2.76	3.07	3.31

- Table 87 provides a comparison of Theta-J_A versus airflow for the 48-pin MLP package.

Theta-J_C for this package is 28.22°C/W. Theta-J_B for this package is 6.58°C/W. The B50610 48-pin MLP is designed and rated for a maximum junction temperature of 125°C.

Table 87: Theta-J_A vs. Airflow for the 48-pin MLP Package

48-pin MLP Package	*Air Flow (feet per minute)*				
	0	*100*	*200*	*400*	*600*
Theta-J_A (C/W)	34.33	30.49	29.34	28.19	27.48
PSI-JT	3.85	3.96	4.02	4.07	4.15

Section 8: Ordering Information

Table 88: Ordering Information

Part Number	*Package*	*Ambient Temperature*
B50610C1KFB	100-pin FBGA (Standard package)	0°C to +70°C
B50610C1KFBG	100-pin FBGA (RoHS compliant package)	0°C to +70°C
B50610C1KML	48-pin MLP (Standard package)	0°C to +70°C
B50610C1KMLG	48-pin MLP (RoHS compliant package)	0°C to +70°C

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