Highly Integrated Wireless Transmitter

Descriptions

CPS8100 is a highly efficient, Qi-compliant, magnetic inductive wireless power transmitter IC with wide input voltage range of 3.9V to 26V. It supports secure bi-directional communication with wireless power receiver (ASK/FSK), flexible communication interface ports, as well as reliable over-voltage/current/ temperature protection schemes.

It includes buck converter, low dropout linear regulator, DC-DC controller, full bridge drivers, communication modulator/de-modulator, foreign object detection (FOD), a multi-channel 12-bit ADC, and ARM processor core and on-chip MTP for maximize software flexibility while consuming extremely low standby power.

The CPS8100 is available in a Pb-free, small QFN 6mmx6mm, 48 pin package. This product is rated over an operating temperature range of -40 to 105°C.

Features

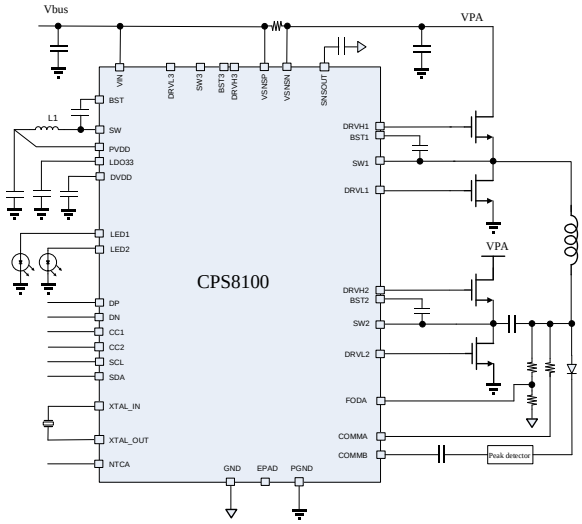
- WPC 1.2.4 compliant wireless power transmitter
- Integrated ARM core, 34KB MTP, 32KB ROM, 6KB SRAM
- Read-Protected/Write-Protected for MTP
- Support update MTP through CC or DP/DN line
- Support I2C interface
- Integrated 2x UART interface
- Flexible adaptor support: QC2.0/QC3.0/PD3.0/SCP/AFC
- Flexible output power with external MOSFET
- Integrated 3 pairs half bridge driver
- Integrated Buck or Boost controller
- Support double Rx charging application
- Integrated external crystal driver
- Low Power Mode
- Over voltage/current/ temperature protection
- RoHS, Halogen-Free and Lead-Free Compliant

Applications

Wireless Fast Charge Transmitter for:

- Charging Pad
- Smart Phone
- MP3 Player
- Blue Tooth
- Tablets
- Accessories

Typical Application



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1. Descriptions

1.1. Block Diagram

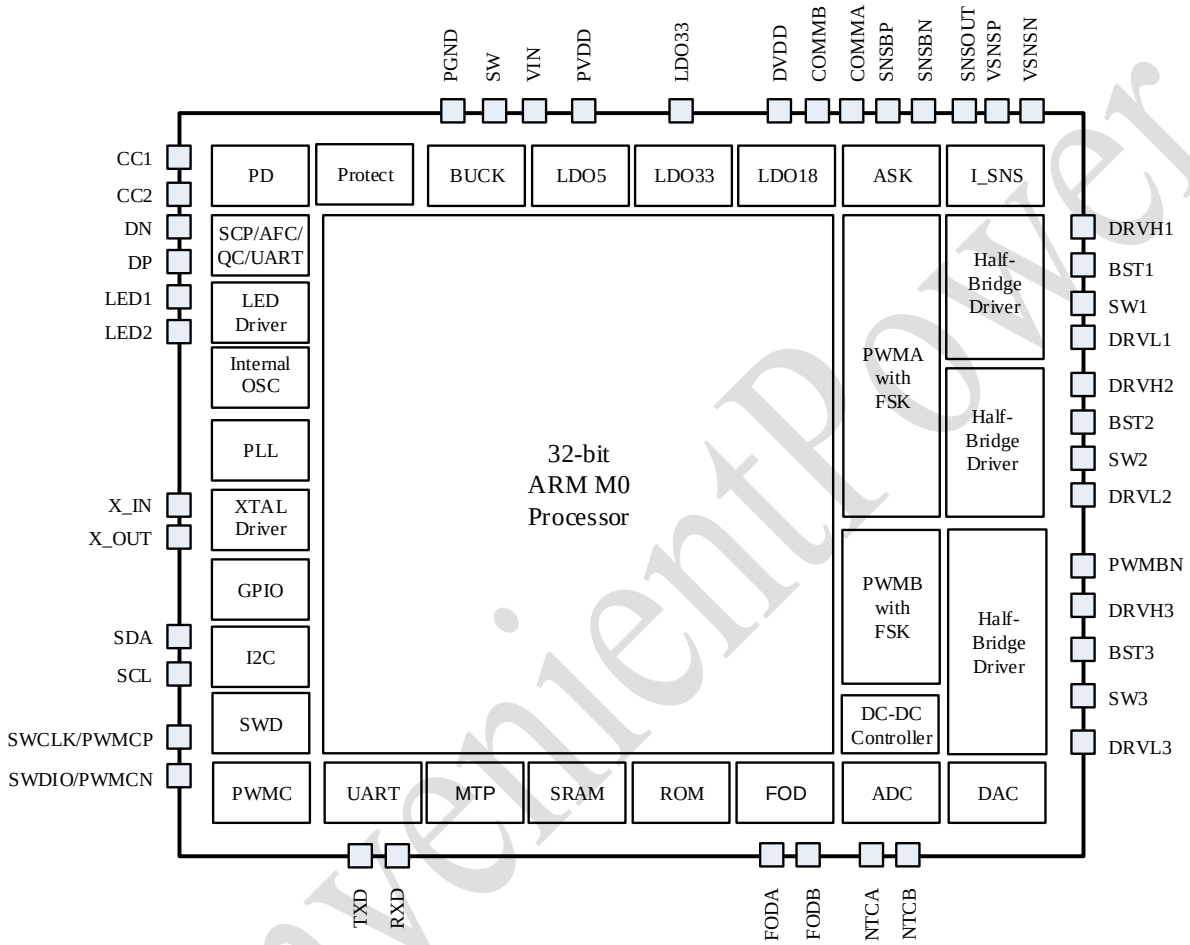
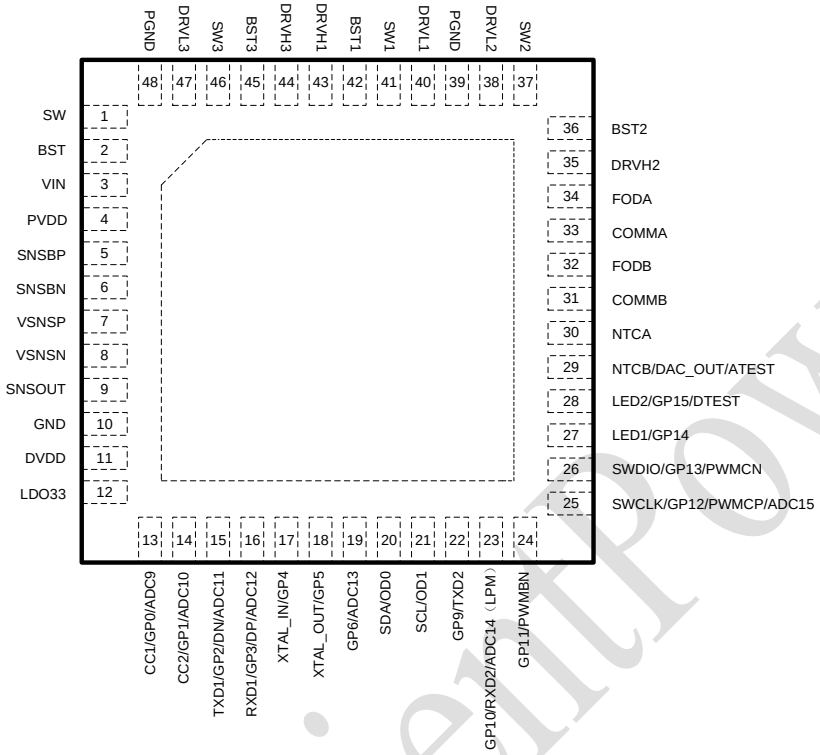


Figure 1.1 Block Diagram

1.2. Pin Information

Pin configuration (Top view)



1.3. Pin Descriptions

Table 1.3 Pin Descriptions

PIN	Name	Description
1	SW	Internal Buck switching node
2	BST	Boot pin for internal Buck high side MOSFET driver
3	VIN	Internal Buck and LDO5 input, need ceramic capacitor from this pin to PGND
4	PVDD	Internal LDO5 output pin and internal LDO33/LDO18 input
5	SNSBP	Channel B high side current sense amplifier positive input terminal
6	SNSBN	Channel B high side current sense amplifier negative input terminal
7	VSNSP	Channel A high side current sense amplifier positive input terminal
8	VSNSN	Channel A high side current sense amplifier negative input terminal
9	SNSOUT	Channel A high side current sense amplifier output
10	GND	Analog GND and digital GND pin
11	DVDD	Internal 1.8V LDO for digital, need 2.2uF ceramic capacitor to GND
12	LDO33	Internal 3.3V LDO bypass pin, need 2.2uF capacitor to GND
13	CC1/GP0/ADC9	Type-C Connector Configuration Channel (CC1) pins -General purpose I/O port -ADC Input port
14	CC2/GP1/ADC10	Type-C Connector Configuration Channel (CC2) pins -General purpose I/O port -ADC Input port
15	TXD1/GP2/DN/ADC11	TXD of UART serial interface -General purpose I/O port -USB D- data line -ADC Input port
16	RXD1/GP3/ DP/ADC12	RXD of UART serial interface -General purpose I/O port -USB D+ data line -ADC Input port

PIN	Name	Description
17	XTAL_IN/GP4	External Crystal Input -General purpose I/O port
18	XTAL_OUT/GP5	External Crystal Output -General purpose I/O port
19	GP6/ADC13	General purpose I/O port -ADC Input port
20	SDA/OD0	SDA of I2C serial interface. -General purpose OD port
21	SCL/OD1	SCL of I2C serial interface. -General purpose OD port
22	TXD2/GP9	TXD of UART serial interface -General purpose I/O port
23	RXD2/GP10/ADC14	RXD of UART serial interface -General purpose I/O port -ADC Input port
24	GP11/PWMBN	-General purpose I/O port PWMBN output pin, it can be configured by firmware to drive external half bridge driver.
25	SWCLK/GP12/PWMCP/ADC15	SWCLK of SWD serial interface. -General purpose I/O port -PWMCP output pin -ADC Input port
26	SWDIO/GP13/PWMCN	SWDIO of SWD serial interface. -General purpose I/O port -PWMCN output pin
27	LED1/GP14	LED1 driver output, connect a LED from this pin to GND -General purpose I/O port
28	LED2/GP15/ DTEST	LED2 driver output, connect a LED from this pin to GND -General purpose I/O port - Internal digital test pin
29	NTCB/ ATEST/DAC_OUT	Channel B External thermal Resistor ADC input -Internal analog test pin. -DAC buffer output port

PIN	Name	Description
30	NTCA	Channel A External thermal Resistor ADC input
31	COMMB	Channel B ASKV(Non-coherent) Demodulation input
32	FODB	Channel B foreign Object detection input -ADC Input port
33	COMMA	Channel A ASKV(Coherent) Demodulation input
34	FODA	Channel A foreign Object detection input -ADC Input port
35	DRVH2	Half bridge driver 2 output for high side MOSFET
36	BST2	Bootstrap capacitor for SW2. Suggest place a 0.1uF capacitor between BST2 and SW2.
37	SW2	Half bridge driver 2 switching node
38	DRVL2	Half bridge driver 2 output for low side MOSFET
39	PGND	Power ground
40	DRVL1	Half bridge driver 1 output for low side MOSFET
41	SW1	Half bridge driver1 switching node
42	BST1	Bootstrap capacitor for SW1. Suggest place a 0.1uF capacitor between BST1 and SW1.
43	DRVH1	Half bridge driver 1 output for high side MOSFET
44	DRVH3	Half bridge driver 3 output for high side MOSFET /DC-DC converter high side MOSFET driver
45	BST3	Bootstrap capacitor for SW3. Suggest place a 0.1uF capacitor between BST3 and SW3.
46	SW3	Half bridge driver 3 switching node
47	DRVL3	Half bridge driver 3 output for low side MOSFET /DC-DC converter low side MOSFET driver
48	PGND	Power ground

2. Specification

2.1. Absolute maximum ratings

Table 2.1 Absolute maximum ratings

Pin	Min	Max	Unit
VIN,SW Note1	-0.6	26	V
CC1,CC2	-0.7	26	V
BST	-0.6	SW+5.5	V
VSNSP,VSNSN,SNSBP,SNSBN, SW1/2/3Note2, FODANote3, FODB Note3	-0.7	30	V
BST1/2/3 Note4, DRVH1/2/3 Note5	-0.6	SW1/2/3+5.5	V
DRVL1/2/3 Note5	-0.7	5.5	V
PVDD	-0.6	5.5	V
LDO33	-0.6	3.6	V
DVDD	-0.6	2	V
SNSOUT, COMMA Note6,COMMB Note6	-0.7	5.5	V
DN,DP	-0.6	5.5	V
NTCA, NTCB, XTAL_IN,XTAL_OUT, GP9, GP10	-0.7	3.6	V
GP6, SDA, SCL, GP11, GP12, GP13, GP14, GP15	-0.6	3.6	V

These are the stress ratings only. Stresses that exceeds the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at these or any other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Note1: The negative pulse (<100nS) voltage rating is -1.5V, the positive pulse voltage (<100nS) rating is 28V
Note2: The negative pulse (<100nS) voltage rating is -1.5V, the positive pulse voltage (<100nS) rating is 33V
Note3: The negative voltage rating is -1.5V with 2mA forward current, the positive pulse voltage (<10uS) rating is 41V with 200uA sink current
Note4: The positive pulse voltage (<100nS) rating is 36V
Note5: The negative pulse (<100nS) voltage rating is -1.5V
Note6: The positive pulse voltage rating is 6V (pulse width <5mS, duty cycle <1%)

2.2. Recommended Operation Conditions

Table 2.2 Recommended operation range

Parameter		Minimum	Typical	Maximum	Unit
V_{IN}	Input voltage range	3.9		24	V
VSNSP,VSNSN, SNSBP,SNSBN	Half bridge supply voltage range	2		26	V
DVDD	Digital supply voltage range	1.62	1.8	1.98	V
V_{GP}	GPIO port Voltage	0		3.3	V
V_{OD}	Open drain port Voltage	0		3.3	V
T_J	Junction temperature	-40	-	125	°C
T_A	Ambient Operation temperature	-40	-	105	°C
T_{STG}	Storage temperature	-55	-	155	°C
T_{BUMP}	Maximum Soldering Temperature			260	°C

2.3. ESD Ratings

Table 2.3 ESD Information

Parameter	Value	Unit	Note
ESD tolerance	±2000	V	Human Body Model (HBM)
	±1000	V	Charge Device Model (CDM)

2.4. Thermal Information

Table 2.4 Thermal Information

Parameter	**Description**	**QFN**	**Unit**
θ_{JA}	Thermal Resistance Junction to Ambient	28	℃/W
θ_{JC}	Thermal Resistance Junction to Case	14	℃/W
θ_{JB}	Thermal Resistance Junction to Board	5.5	℃/W
T_L	Lead Soldering Temperature	260	℃

2.5. Electronics Characteristics

VIN=9V, Typical values are at room temperature unless otherwise noted

Parameter	Min	Typ	Max	Unit	Note
Quiescent Current					
I_{VIN_SUPPLY}			10	mA	Operating supply current, MCU is disabled.
I_{Q_OFF}			20	uA	VIN below VIN_UVLO
I_{DLP}			60	uA	VIN=9V, Deep low power mode
Input Supply					
VIN	3.9		24	V	Input operating range
$VIN_{\_UVLO}$	3.2	3.45	3.7	V	Under Voltage Lock Out threshold (rising edge)，
$VIN_{\_UVLO\_HYS}$	0.3	0.45	0.6	V	Under Voltage Lock Out threshold Hysteresis
VIN UV warning Threshold	3.2		4.6	V	Falling edge, Programmable, 0.2V step
VIN UV warning Hysteresis	0.16	0.19	0.22	V	
VIN OV warning Threshold	6		26	V	Programmable,6V/7V/10V/11V/14V/17V/22V/26V
VIN OV warning Recovery	4		24	V	Programmable,4V/5V/6V/8V/9V/10V/12V/13V/15V/16V/20V/21V/24V
VPA OV warning Threshold	6		30	V	Programmable,6V/7V/10V/11V/14V/17V/22V/26V/27V/28V/29V/30V
VPA OV warning Recovery	4		27	V	Programmable,4V/5V/6V/8V/9V/10V/12V/13V/15V/16V/20V/21V/24V/25V/26V/27V
Internal Buck，C_{OUT}=10uF					
V_{PVDD}		5		V	BUCK output voltage
V_{PVDD} accuracy	-5%		+5%		BUCK output voltage accuracy
I_{PVDD}			300	mA	BUCK output current capability
I_{PVDD_LMT}	0.8		1.4	A	Cycle-by-cycle current limit, programmable, 0.2A/step
LDO5, C_{OUT}=10uF					
V_{LDO5}		4.6		V	LDO5 output voltage
V_{LDO5} accuracy	-5%		+5%		LDO5 output voltage accuracy

Parameter	Min	Typ	Max	Unit	Note
I_{LDO5_max}			50	mA	LDO5 output current capability
LDO33, C_{OUT}=2.2uF					
V_{LDO33}		3.3		V	LDO33 output voltage
V_{LDO33} accuracy	-2%		+2%		LDO33 output voltage accuracy
I_{LDO33_max}			50	mA	LDO33 output current capability
DVDD, C_{OUT}=2.2uF					
V_{DVDD}		1.8		V	LDO18 output voltage
V_{DVDD} accuracy	-5%		+5%		LDO18 output voltage accuracy
I_{DVDD_max}			50	mA	LDO18 output current capability
BGR					
V_{BGR} (post-trim)	2.433	2.457	2.481	V	-40 °C to 105 °C
OSC					
F_{CLOCK_50K}	49.25	50	50.75	kHz	-40°C to 105°C
F_{CLOCK_8M}	7.84	8	8.16	MHz	-40°C to 105°C
External Crystal					
C_L		15		pF	
F_{XTAL}		40		MHz	-40°C to 105°C
Start-up time		2		mS	
PWMA/PWMB					
F_{SW}	60	127.773	210	KHz	PWM switching frequency
Accuracy	-0.1%		+0.1%		-40°C to 105°C
Duty	0%		100%		PWM duty cycle
Accuracy	-0.1%		+0.1%		-40°C to 105°C
△Phase	0		180	degree	PWM phase difference
Accuracy	-0.2		+0.2	degree	-40°C to 105°C,F_{SW}=127.77KHz
PWMC					
F_{SW}	0.1	127.773	210	KHz	PWM switching frequency
Accuracy	-0.1%		+0.1%		-40°C to 105°C
Duty	0		100	%	PWM duty cycle
Accuracy	-0.1%		+0.1%		-40°C to 105°C
△Phase	0		180	degree	PWM phase difference
Accuracy	-0.2		+0.2	degree	-40°C to 105°C,F_{SW}=127.77KHz
HB Driver (DRV1,DRV2)					
T_{HS_R}		140		nS	High side rise time, CL=3nF.

Parameter	Min	Typ	Max	Unit	Note
T_{HS_F}	20		140	nS	High side fall time, CL=3nF. programmable, 40ns step
T_{LS_R}	20		140	nS	Low side rise time, CL=3nF. programmable, 40ns step
T_{LS_F}	20		140	nS	Low side fall time, CL=3nF. programmable, 40ns step
T_{DEAD_L2H}	40		320	ns	Low side to high side dead time, programmable, 40ns step
T_{DEAD_H2L}	40		320	ns	High side to low side dead time, programmable, 40ns step
HB Driver (DRV3)					
T_{HS_R}	30		180	nS	High side rise time, CL=3nF. Programmable, 30/50/90/180nS
T_{HS_F}	20		220	nS	High side fall time, CL=3nF. Programmable, 20/40/60/220nS
T_{LS_R}	20		140	nS	Low side rise time, CL=3nF. programmable, 40ns step
T_{LS_F}	20		140	nS	Low side fall time, CL=3nF. programmable, 40ns step
T_{DEAD_L2H}	10		80	ns	Low side to high side dead time, programmable, 10nS/step
T_{DEAD_H2L}	10		80	ns	High side to low side dead time, programmable, 10nS/step
IPA Current Sense					
AVG Current Sense Range	0		3.5	A	Rcs=20mohm
LSB_{IPA}		0.9375		mA	Rcs=20mohm
Accuracy	-1%		1%		I_{VIN}>500mA after trimming
	-5		5	mA	I_{VIN}≤500mA after trimming
$Av_{\_ADC}$	31	32	33		Gain to ADC
$Av_{\_ASK}$	48		64		Gain to ASK de-modulation programmable, x64 / x48
V_{OS} (post-trim)	**3**	5	7	mV	
VIN Voltage Sense					
VIN Sense Range	0		30	V	
LSB_{VPA}		8.5714		mV	
Accuracy	-1		+1	%	From 5V to 26V VIN
VPA Voltage Sense					
VPA Sense Range	0		30	V	
LSB_{VPA}		8.5714		mV	

Parameter	Min	Typ	Max	Unit	Note
Accuracy	-1		+1	%	From 5V to 30V VPA
DC-DC converter					
V_O Range (Boost)	1		30	V	Programmable, 17.143mV/step
V_O Range (Buck)	1		24.57	V	Programmable, 12mV/step
I_{LMT}	1.5		17.25	A	cycle-by-cycle current limit, Rcs=20mohm, Av_ocp=4, Av_cs=14, Programmable, step =250mA,
Fsw	200		1000	KHz	Switching frequency Programmable,200KHz/300KHz/500KHz/800KHz/1MHz
T_{ON_MIN}	140		300	nS	Minimum on time, Programmable, 140/220/300nS
$T_{OFF\_MIN\_BUCK}$	125		250	nS	Minimum off time cycle at BUCK mode, Programmable, 125nS/250nS
D_{MAX_BUCK}		97		%	Maximum duty cycle at BUCK mode, Fsw=200KHz
D_{MAX_BOOST}		85		%	Maximum duty cycle at BOOST mode
ADC Converter					
Resolution		12		bits	
ENOB		10		bits	Effective number of bits
F_{sample}		100	200	kSa/S	Max sampling speed
Channel		16			Number of channels
V_{FS}			2.457	V	ADC full scale input voltage
DAC Converter					
Resolution		11		bits	
DAC Output	0.04		2.457	V	Output voltage range
DAC output Step		1.2		mV	
DAC Output Slew-Rate	0.5		64	us/step	3 bit, Programmable
DP,DN					
V_{DP}	0		3.3	V	Programmable, 0V, 0.6V, 1.8V, 3.3V
Accuracy	-5		5	%	
V_{DN}	0		3.3		Programmable, 0V, 0.6V, 1.8V, 3.3V
Accuracy	-5		5	%	
T_{Rise}		1	3.6	us	DP/DN rise time, 10%-90%

Parameter	Min	Typ	Max	Unit	Note
T_{Fall}		1	3.6	us	DP/DN fall time, 90%-10%
$V_{IH\_SCP\_DN}$	1.4			V	Input high voltage
$V_{IL\_SCP\_DN}$			0.7	V	Input low voltage
$V_{OH\_SCP\_DN}$	0.9VDD				Source 5mA
$V_{OL\_SCP\_DN}$			0.36	V	Sink 5mA
Pulse Width Detector					
T_{b_SCP}	144	160	176	uS	SCP bit time
$T_{Pulse\_SCP\_DN}$	36		3000	uS	SCP pulse width range
Accuracy		1		uS	
T_{Pulse_ASK}	36		1000	uS	pulse width range
Accuracy		1		uS	
CC1,CC2					
$V_{TH\_CC\_USB}$	0.15	0.20	0.25	V	Threshold voltage for default current source capability DFP
$V_{TH\_CC\_MED}$	0.61	0.66	0.7	V	Threshold voltage for 1.5A DFP
$V_{TH\_CC\_HIGH}$	1.16	1.23	1.31	V	Threshold voltage for 3.0A DFP
Z_{DRIVER_CC}	33		75	ohm	Output impedance of CC1/CC2 during TX
Z_{BMCEX_CC}	1			Mohm	Receiver input impedance
V_{OH_CC}	1.05	1.125	1.2	V	Transmit high voltage when operating in PD mode
V_{OL_CC}	0		0.075	V	Transmit low voltage when operating in PD mode
V_{IH_CC}	0.65		1.53	V	Input high voltage when sinking power.
V_{IL_CC}	-0.33		0.23	V	Input low voltage when sinking power
f_{BMC}	270	300	330	kHz	BMC signal bit rate
t_{RISE_BMC}	300			ns	BMC signal rise time
t_{FALL_BMC}	300			ns	BMC signal fall time
t_{HOLD_BMC}	1			us	Time to cease driving the line after the final high to low transition
t_{IFG_BMC}	25			us	Time from the end of last bit of a frame until the start of the first bit of next preamble
t_{END_BMC}			23	us	Time to cease driving the line after the end of the last bit of frame

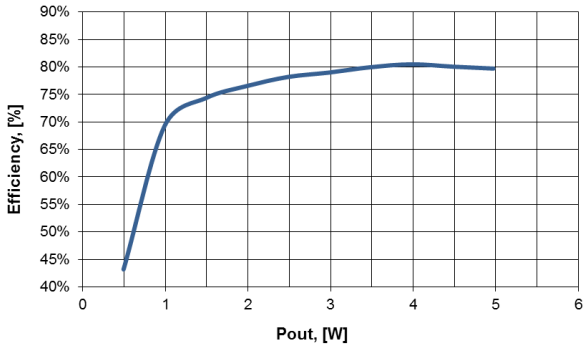
Parameter	Min	Typ	Max	Unit	Note
t_{RXFTR_BMC}	100			ns	BMC receiver bandwidth limiting filter
t_{NILDLE_BMC}	12		20	us	Time window for detecting non-idle
GPIO					
V_{IH}	1.4			V	Input high voltage
V_{IL}			0.7	V	Input low voltage
V_{OH}	0.9VDD			V	Source 5mA, VDD=3.3V
V_{OL}			0.36	V	Sink 5mA
I_{LKG}	-1		1	uA	Leakage current
SCL, SDA					
V_{IH}	1.4			V	Input high voltage
V_{IL}			0.7	V	Input low voltage
I_{LKG}	-1		1	uA	Leakage current
V_{OL}			0.36	V	Sink 5mA
C_B		150		pF	Capacitance load on bus
C_I		5		pF	Input capacitance
F_{SCL}			400	kHz	Clock frequency
T_{LOW}		1.3		uS	Clock low
T_{HIGH}		0.6		uS	Clock high
Internal Temperature Sensor					
Temperature Accuracy	-5		+5	^oC	T_J from -40^oC to 150 ^oC
Thermal protection					
T_{SD}		140		^oC	T_J shutdown temperature
T_{SD-HYS}		20		^oC	T_J shutdown hysteresis
T_{WN}	60		120	^oC	T_J thermal warning temperature, programmable, 20 ^oC step
T_{WN_HYS}		20		^oC	T_J thermal warning hysteresis
Vcoil OVP					
$V_{FOD\_OV\_TH}$	13		27	V	FODA/FODB OV warning Threshold, Programmable, 2V/step
$V_{FOD\_OV\_Hys}$		1		V	FODA/FODB OV warning Hysteresis
IPA OCP					
$I_{PA\_AVG\_OC\_TH}$	1.25		3.35	A	IPA average current OC

Parameter	Min	Typ	Max	Unit	Note
					warning threshold, R_{CS}=20mohm, V_{OS}=5mV, Programmable, 0.3A/step
LED					
Blink Frequency	0.1		100	Hz	
Accuracy	-2%		2%		-40 to 105 °C
Breathe Frequency	0.1		100	Hz	
Accuracy	-2%		2%		-40 to 105 °C

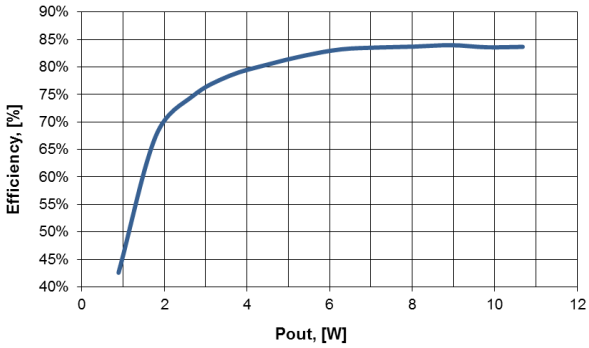
3. Typical Performance Characteristics

Test conditions: VIN=5V, VPA=12V, RX Output=5V/9V，TX coil use MP-A2, RX = CPS4037 RX module with ECM_52091500_V3.0 coil.

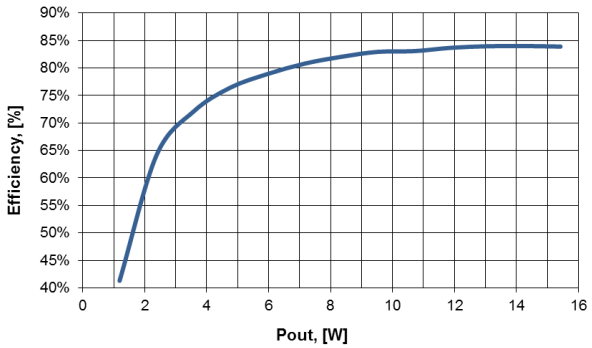
System Efficiency Vs Output Power@VOUT=5V



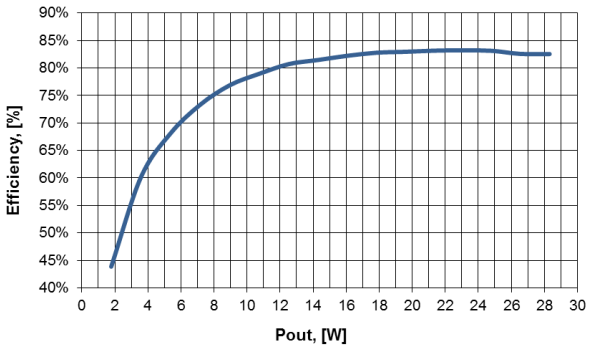
System Efficiency Vs Output Power@VOUT=9V



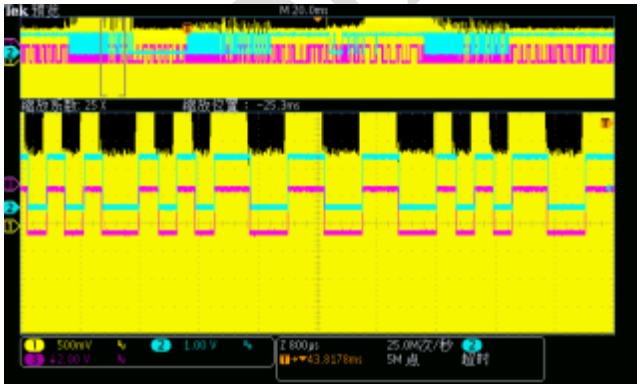
System Efficiency Vs Output Power@VOUT=12V



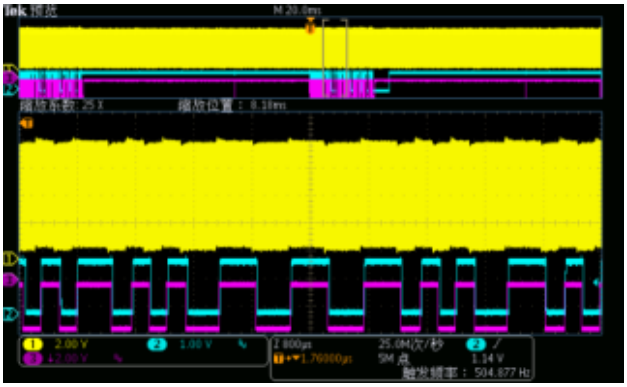
System Efficiency Vs Output Power@VOUT=18V



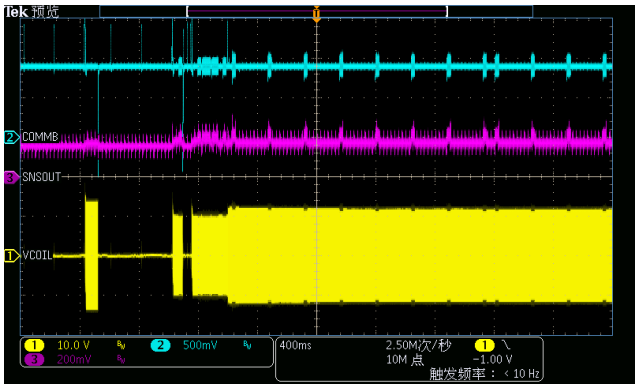
Voltage Demodulation Signal for ASK



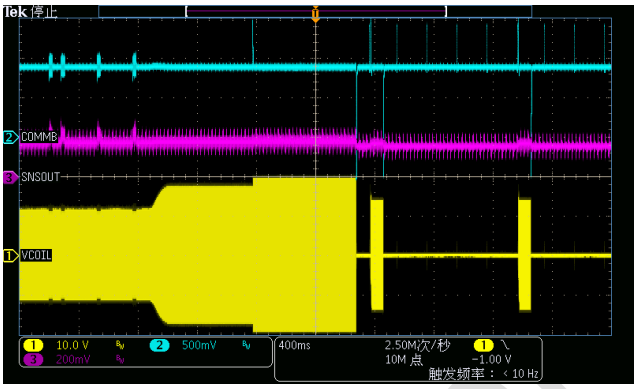
Current Demodulation Signal for ASK



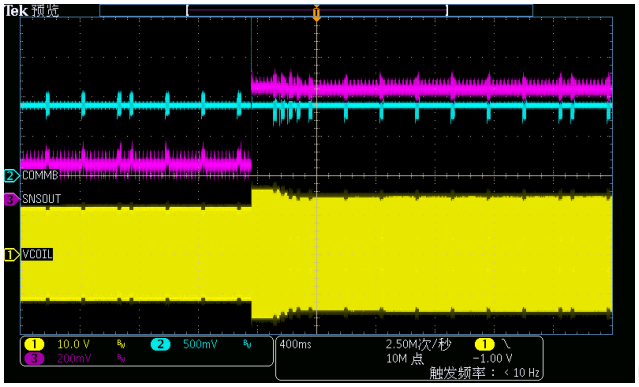
Start up



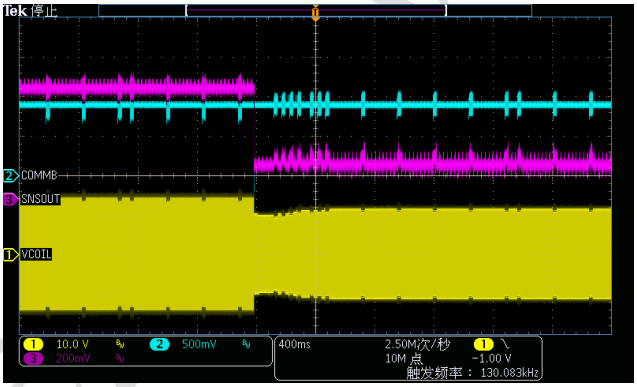
Rx Remove



Rx Load Transient from 0A to 1A



Rx Load Transient from 1A to 0A



4. Function Description

4.1. General Descriptions

CPS8100 is a highly efficient, Qi-compliant, magnetic inductive wireless power transmitter IC with wide input voltage range of 3.9V to 26V. It supports secure bi-directional communication with wireless power receiver (ASK/FSK), flexible communication interface ports, as well as reliable over-voltage/current/ temperature protection schemes.

It includes buck converter, low dropout linear regulator, DC-DC controller, full bridge drivers, communication modulator/de-modulator, foreign object detection (FOD), a multi-channel 12-bit ADC, and ARM processor core and on-chip MTP for maximize software flexibility while consuming extremely low standby power.

The CPS8100 is available in a Pb-free, small QFN 6mmx6mm, 48 pin package. This product is rated over an operating temperature range of -40 to 105°C.

4.2. Wireless Power Transfer System

The Qi wireless power transfer system uses magnetic induction to transfer power to a power receiver subsystem contained within the mobile device when it is placed on top of a power transmitter. Both the transmitter and receiver subsystems contain coils as well as circuitry that handle the communication and power transfer between them. The power transmitter make power available via DC to AC inverter and transmit the power over a coupled inductor pair to a receiver in a mobile device.

Power transfer from a power transmitter to a power receiver comprises four phases in BPP, namely selection, ping, identification & configuration, and power transfer. Figure 2 illustrates the relation between the phases. The solid arrows indicate transitions, which the power transmitter initiates; and the dash-dotted arrows indicate transitions that the power receiver initiates. The implementation and transition of each phase is accomplished by CPS8100 SW.

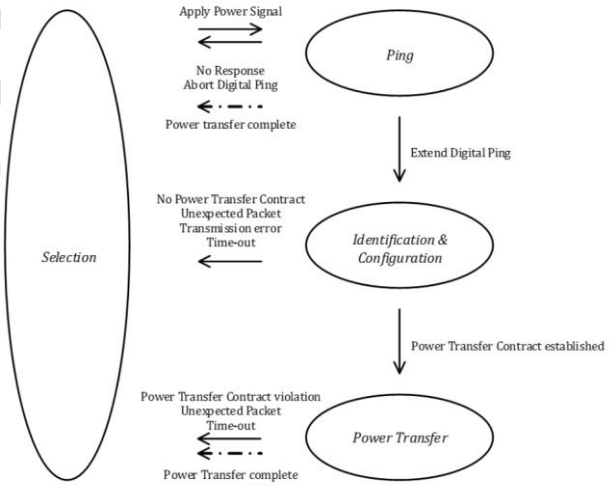


Figure 4.2-1 WPC Power Transfer Phases – Baseline Power Profile

On Tx system, CPS8100 periodically enters selection phase and ping phase to detect the presence of a receiver. If a receiver is detected, CPS8100 will enter power transfer phase (transfer power is limited),

monitor communication link, and prepare for handshake with the receiver. Once the receiver is identified and authenticated, CPS8100 starts to regulate transmitting power to the request of the power receiver.

4.3. UVLO

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage, the CPS8100 UVLO comparator monitors the input voltage (VIN). The UVLO rising threshold is 3.45V while its falling threshold is 3.0V.

4.4. BUCK and LDO

The internal analog control logic is powered by PVDD, and the digital core is powered by DVDD, CPS8100 integrated a buck converter for FET drivers, LDO33 and DVDD to improve the system efficiency.

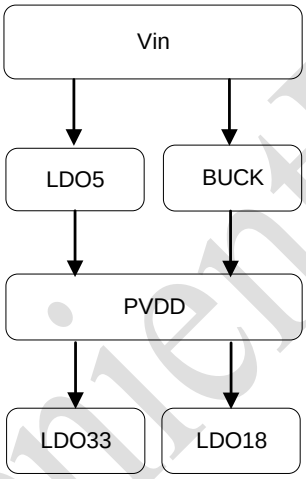


Figure 4.4-1 Power Domains

4.5. DC-DC Controller

CPS8100 integrates a DC-DC controller to regulate the VPA voltage. This DC-DC converter own perfect load transient, line transient, load regulation, line regulation, cycle-by-cycle current limit, over-current and short-circuit protect function.

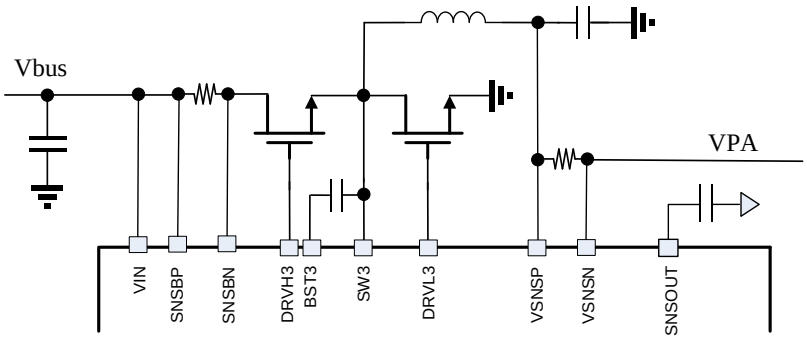


Figure 4.5-1 BUCK Converter

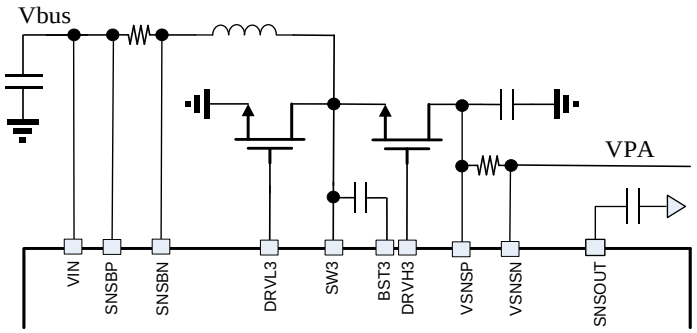


Figure 4.5-2 Boost converter

4.6. VIN/VPA Control

When VIN/VPA drops below the threshold voltage, an INT is sent to MCU. MCU can then increase operating frequency or reduces duty cycle and output power is lowered.

4.7. PWM Generator

CPS8100 provides up to 3 channels of PWMs which are clocked form main clock up to 144MHz. For each channel of PWM, the CPS8100 supports duty cycle mode and phase mode. In duty cycle mode, the PWM duty cycle varies from 0% to 100%. In phase mode, the PWM has duty cycle of 50% and the phase difference can be as low as 3 °

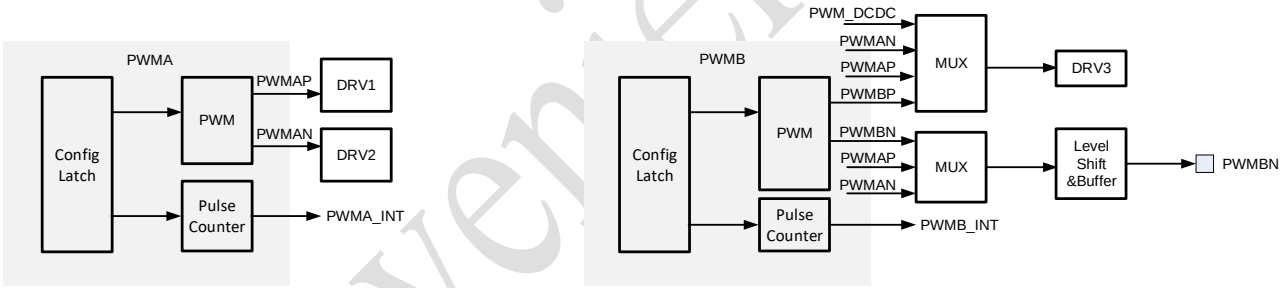


Figure 4.7-1PWMA&PWMB Diagram

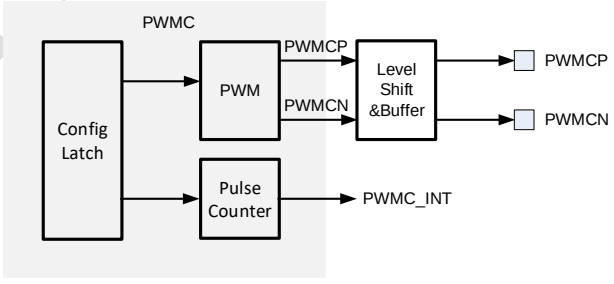


Figure 4.7-2 PWMC Diagram

4.8. MOSFET Driver

CPS8100 contains 3 Half-bridge drivers. MTP bits are used to tune the driving strength (turn-on/off separated control) of both the high and low side driver. MTP bits are also used to control the dead time of the drivers. The combination of these registers is used to accommodate different FETs.

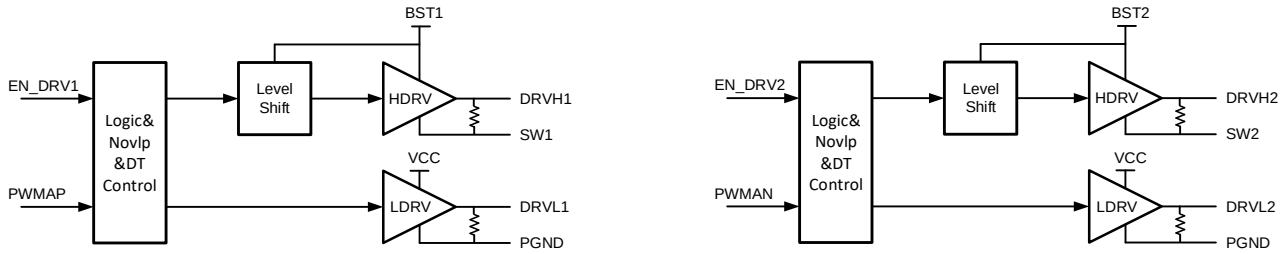


Figure 4.8-1 MOS DRV1&DRV2 Diagram

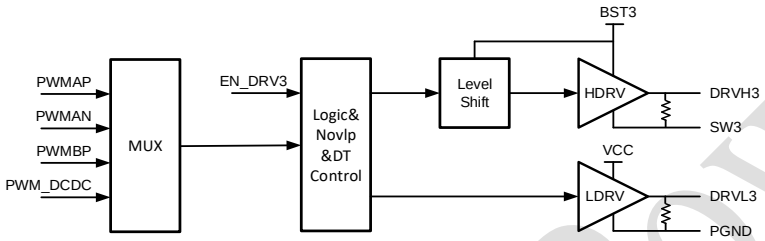


Figure 4.8-2 MOS DRV3 Diagram

4.9. Current Sense

Power FET current is sensed with external sense resistor of 20mOhm between, and amplified by a gain. This sensed current is used for safety protection and for communication with RX.

Details are described in section FOD and ASK. The current sense amplifier had to have a minimum bandwidth of 2MHz, enough to reflect inductor peak current (which switches at <200KHz).

4.10. Crystal Driver

CPS8100 integrates a low power consumption crystal driver for the high precision and steady clock. This module can also be disabled.

4.11. PLL

CPS8100 integrates a system clock PLL which max output clock frequency up to 144MHz. the PLL source can be selected from external 48 MHz high speed crystal or 8 MHz internal high speed RC oscillator.

4.12. Adaptor Support

CPS8100 supports fast charging power adaptors of different protocols, including USB PD, QC2.0, SCP, and AFC.

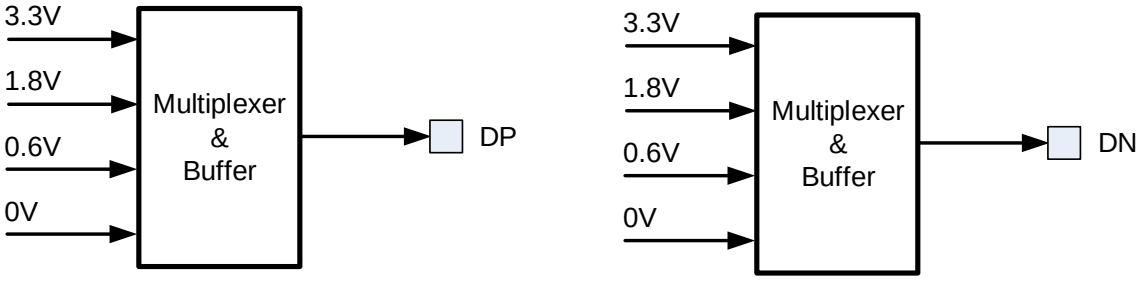


Figure 4.12-1 QC/SCP/AFC Diagram

4.13. Pulse Width Detector

CPS8100 contains three pulse width detector for ASK de-modulation and SCP adaptor support, the positive and negative pulse width data are stored in the correlated registers. An interrupt can be produced on rising edge and falling edge of input source for each pulse width detector

4.14. PD PHY

CPS8100 integrates a PD_PHY (PD3.0 sink) which supports adjust the output voltage of power supply in small increments over its range (PPS), transmit and receive buffer and comparators to recognize the CCx voltage. CPS8100 integrates patented adaptive engine of BMC receiver for robust communication with BMC transmitters. In BMC transmitter, MTP bits are used to tune the drive capacity of CC1/CC2 for match the BMC Mask spec.

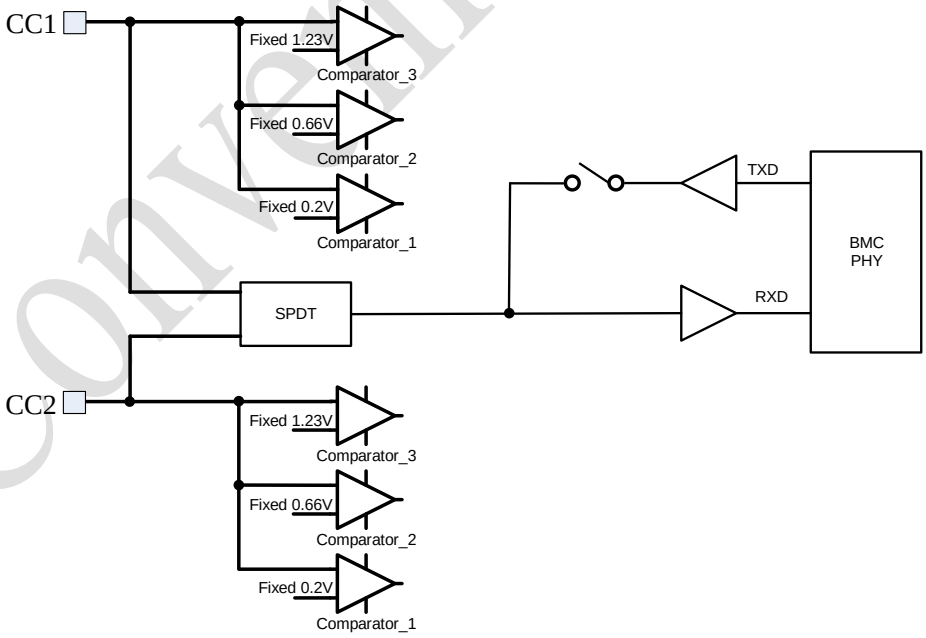


Figure 4.14-1 PD_PHY Diagram

4.15. Thermal Control

If the die temperature (Tj) exceeds safe limits which is defined by TOTS, all drivers in the device can be shut down by firm ware.

If the board temperature (monitored by NTC) exceeds warning limit which is defined by THTS, an INT is sent to MCU to lower output power by increasing operating frequency or reduce duty cycle.

4.16. Heat Sinking

For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat.

5. IO Interfaces

5.1. I2C

CPS8100 supports I2C master/slave interface that enables communication with other device over the standard two-wire I2C bus

5.2. UART

CPS8100 contains 2x standard UART interface. This UART is standard 2-wire interface (TXD and RXD), no hardware flow control (CTS, RTS).

5.3. GPIO and GPOD

CPS8100 contains 14x general purpose I/O and 2x open-drain I/O. All of GPIO are support push-pull mode and open-drain mode.

Table 5.3 GPIO Pin Sharing

Pin	Functions	Priority			
		0	1	2	3
13	CC1/GP0/ADC9	CC1	GP0	ADC9	
14	CC2/GP1/ADC10	CC2	GP1	ADC10	
15	TXD1/GP2/DN/ADC11	TXD1	GP2	DN	ADC11
16	RXD1/GP3/DP/ADC12	RXD1	GP3	DP	ADC12
17	XTAL_IN/GP4	XTAL_IN	GP4		
18	XTAL_OUT/GP5	XTAL_OUT	GP5		
19	GP6/ADC13	GP6		ADC13	
20	SDA/ OD0	SDA		OD0	
21	SCL/OD1	SCL		OD1	
22	GP9/TXD2	GP9	TXD2		
23	GP10/RXD2/ADC14	GP10	RXD2	ADC14	
24	GP11/ PWMBN	GP11	PWMBN		
25	SWCLK/GP12/PWMCP/ADC15	SWCLK	GP12	PWMCP	ADC15
26	SWDIO/GP13/PWMCN	SWDIO	GP13	PWMCN	
27	LED1/GP14	LED1	GP14		
28	LDE2/GP15/DTEST	LED2	GP15	DTEST	

5.4. ADC

CPS8100 integrates a 16 channels 12-bit SAR ADC for analog–digital conversion. This ADC contains auto-zero feature for offset cancellation and enhanced accuracy

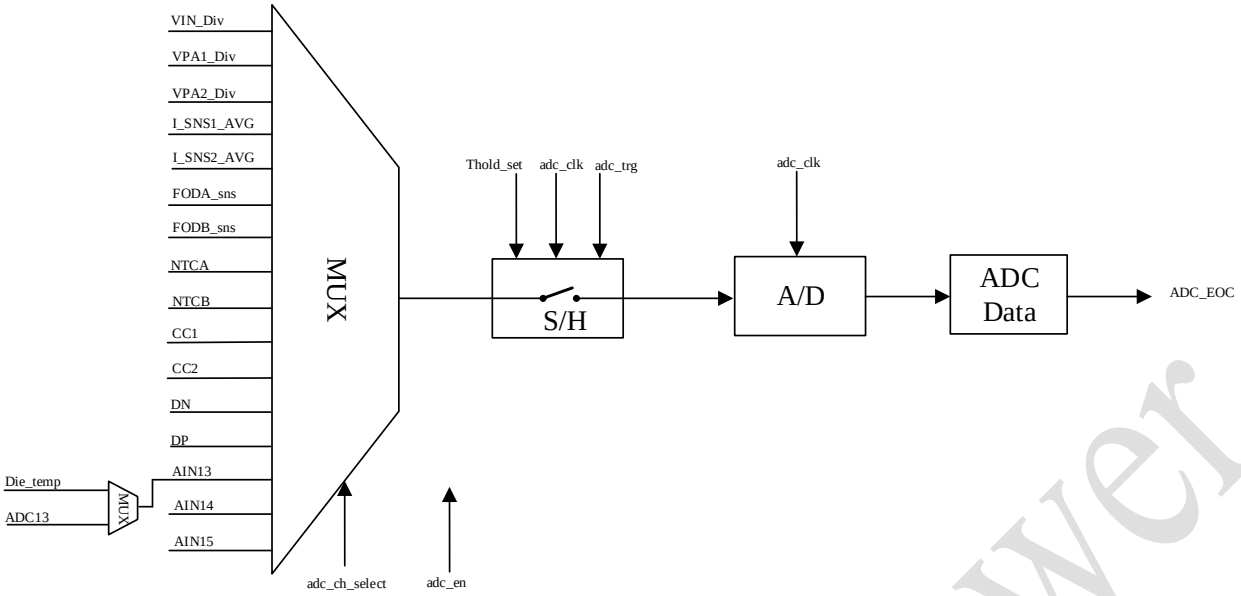


Figure 5.4-1 ADC Diagram

6. Communication

To set up power transfer and assist in its control, a power transmitter and power receiver execute a communication protocol with each other. The power receiver uses amplitude shift keying to communicate requests and other information to the power transmitter by modulating its reflected impedance. The power transmitter uses frequency shift keying (FSK) to provide synchronization and other information to the power receiver by modulating its operating frequency.

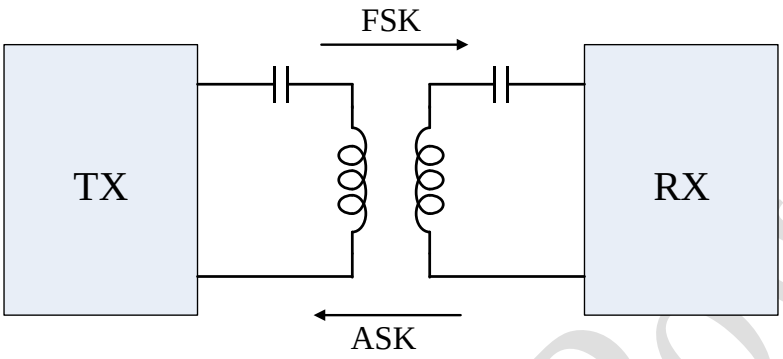


Figure 6.0-1 Example of WPT in-band communication (Bi-directional)

6.1. ASK

The Power receiver communicates to the power transmitter using backscatter modulation. For this purpose, the Power receiver modulates the amount of power that it draws from the power signal. The Power transmitter detects this as a modulation of the current through and/or voltage across the Primary Cell. In other words, the Power receiver and Power transmitter use a amplitude modulated Power Signal to provide a Power receiver to Power transmitter communications channel.

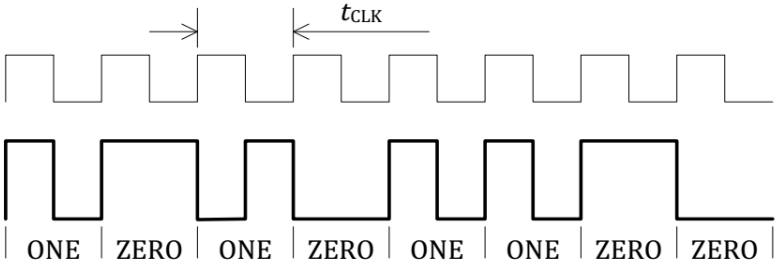


Figure 6.1-1 WPC ASK Bit-encoding scheme

CPS8100 has a variety of demodulation of ASK signals from Receiver. This analog signal is pre-processed before send to MCU/digital to decode signal packet.

Voltage Mode

For ASKV non-coherent demodulation, the envelop signal of Vcoil is first generated and attenuated, which is then AC coupled to precondition to be compared before it is sent to MCU.

For ASKV coherent demodulation, The Vcoil signal is attenuated, filtered, mixed and compared before it is

sent to MCU.

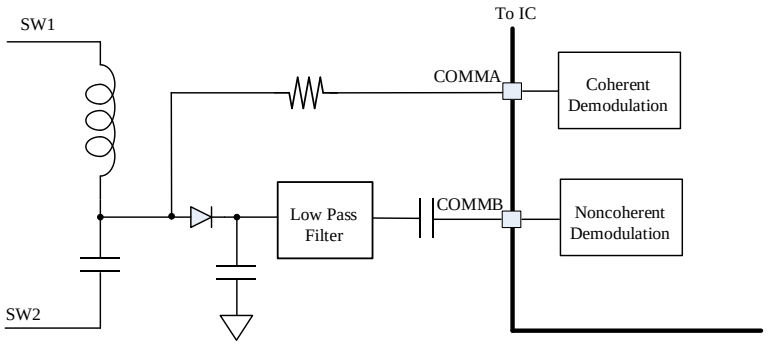


Figure 6.1-2 Voltage Mode ASK Diagram

Current Mode

IPA current is sensed through an external resistor. For ASKI non-coherent demodulation, the sensed current signals (average, peak, valley) are amplified and filtered before be compared to a threshold, and then it is sent to MCU.

For ASKI coherent demodulation, the sensed current signal is amplified, filtered, mixed and compared before it is sent to MCU.

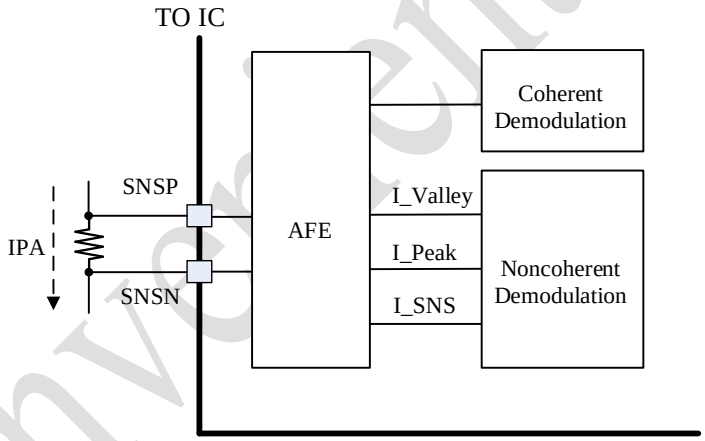


Figure 6.1-3 Current Mode ASK Diagram

6.2. FSK

The power transmitter communicates to the power receiver using frequency shift keying, in which the power transmitter modulates the operating frequency of the power signal.

CPS8100 can switch its operating frequency between the operating frequency f_{op} in the un-modulated state and the operating frequency f_{mod} in the modulated state. The difference between these two frequencies is characterized by two parameters:

- Polarity. This parameter determines whether the difference between f_{mod} and f_{op} is positive or negative.
- Depth. This parameter determines the magnitude of the difference between f_{op} and f_{mod}.

Table 6.2 WPC FSK States

Polarity	Depth	$\frac{1}{f_{mod}} - \frac{1}{f_{op}}$		Unit
		Minimum	Maximum	
positive	3	−282.00	−249.00	ns
positive	2	−157.00	−124.00	ns
positive	1	−94.50	−61.50	ns
positive	0	−63.25	−30.25	ns
negative	0	30.25	63.25	ns
negative	1	61.50	94.50	ns
negative	2	124.00	157.00	ns
negative	3	249.00	282.00	ns

Depth determines the magnitude of the difference between f_{op} and f_{mod}. Larger depth could result in large variation in the magnetic field, therefore, it tends to choose depth ‘0’ or ‘1’ to minimize system stability impact. The CPS8100 has a master clock of 48MHz/144MHz to meet the requirements of all the depth.

The power transmitter shall use a differential bi-phase encoding scheme to modulate data bits in the power signal. For this purpose, the power transmitter shall align each data bit to 512 cycles of the power signal frequency.

The power transmitter shall encode a ONE bit using two transitions in the power signal frequency. The first transition shall occur at the start of the bit and the second transition shall occur at 256 cycles into the bit. The transmitter shall encode a ZERO bit using a single transition in the power signal frequency at the start of the bit

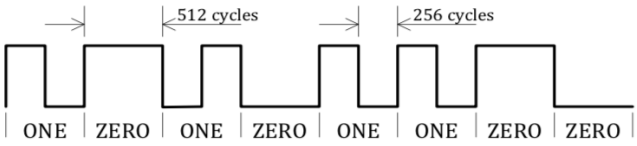


Figure 6.2-1 WPC FSK Bit-encoding scheme

7. Foreign Object Detection

Foreign object detection (FOD) feature and performance is critical for safety protection in wireless charging system. Metallic objects heating from being exposed to alternating magnetic fields will lead to unsafe situation. In WPC Extended Power Profile, there are two stages of FOD. One is by measuring the system quality factor (Q-factor) prior to entering the power-transfer phase, and the other is to measure the power loss difference between the received power and the transmitted power during the power-transfer phase.

CPS8100 features a fast and accurate time-domain Q-factor detection circuit. Before entering power-transfer stage, CPS8100 charges LC resonances circuit to 3.3V through internal LDO3P3, then connects the LC tank to GND for self-decaying. The ringing of coil voltage is processed by internal analog blocks to determine the time taken to decay to a pre-set voltage level. This can effectively measure Q factor of the system. Besides, self-resonance frequency is also process by internal digital block, which can be used for FOD optimization. MCU compares the measured Q-factor with reference Q-factor provided by the receiver. If the difference is higher than the pre-programmed threshold, CPS8100 will identify it as an FO and stop entering power-transfer.

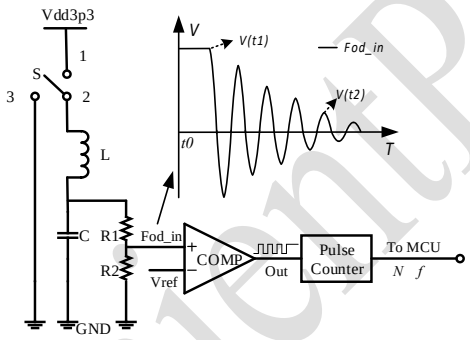
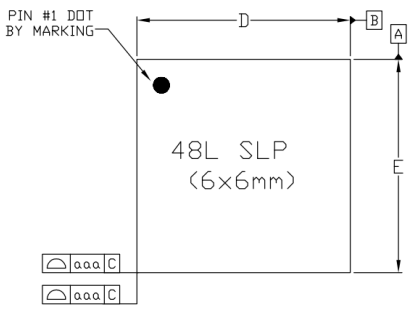


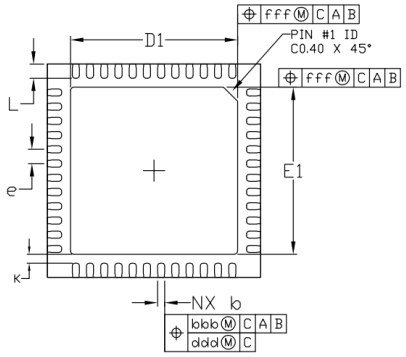
Figure 7.0-1 Q Detection

CPS8100 also features foreign object detection during power-transfer, where the power loss difference between the received power and transmitted power is constantly measured and compared to WPC specified threshold. The transmitted power accuracy is guaranteed by CPS8100's voltage / current sensing blocks. If the power loss difference is higher than threshold, the system will exit power-transfer stage to avoid over-heating.

8. Package Outline Dimensions

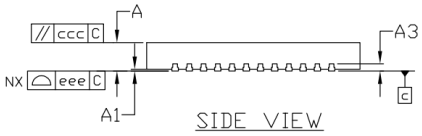


TOP VIEW



BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	---	0.050
A3	0.203 Ref.		
D	5.950	6.000	6.050
E	5.950	6.000	6.050
D1	4.650	4.700	4.750
E1	4.650	4.700	4.750
b	0.150	0.200	0.250
L	0.350	0.400	0.450
K	0.150 MIN		
e	0.400 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		



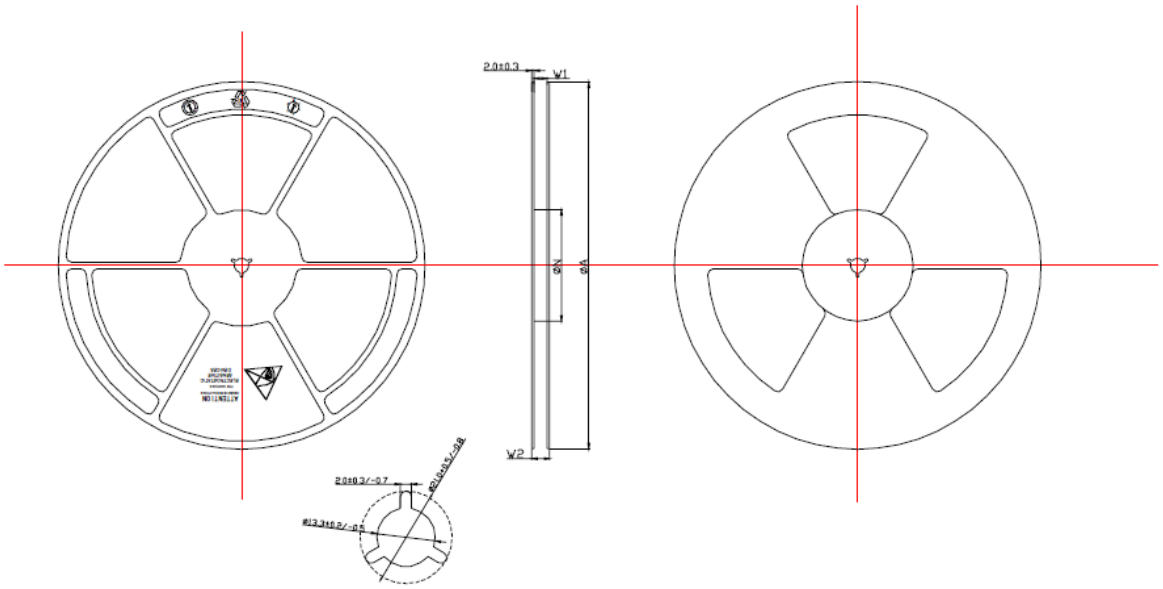
SIDE VIEW

Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

9. Tape and Reel Information

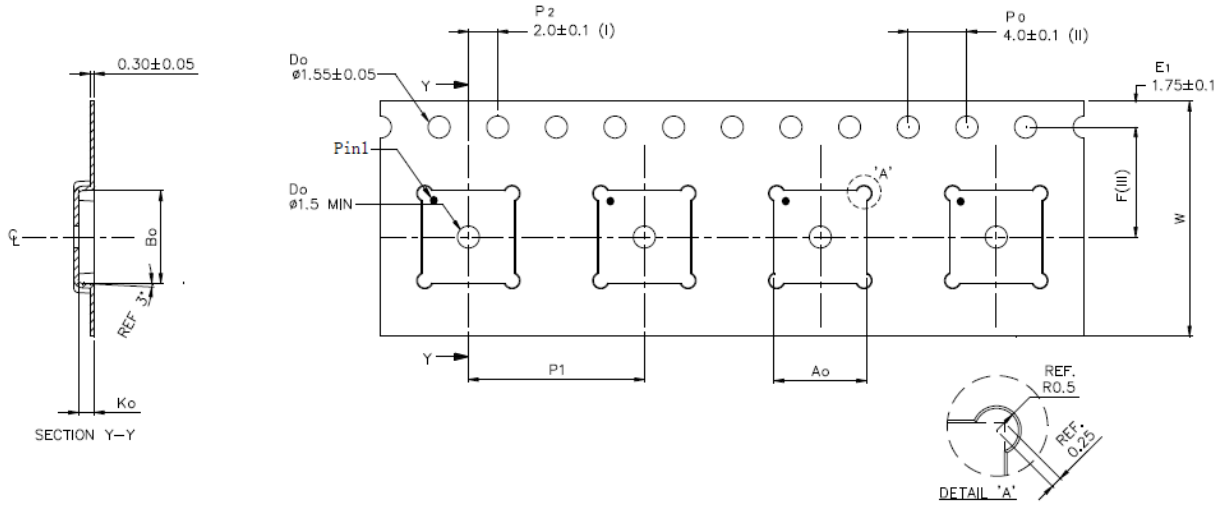
Reel Information



PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4

DRN. : ZHD	2005. 09. 23	TITLE:Platic Reel
CHK. : RPP	2005. 09. 24	13''Inch(Dia)×4''Inch(HUB)
RPP. : XGM	2005. 09. 27	Dwg NO:CM-REEL-05

Carrier Tape Information



Ao	6.30 +/−0.1
Bo	6.30 +/−0.1
Ko	1.10 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

P/N: 433113

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

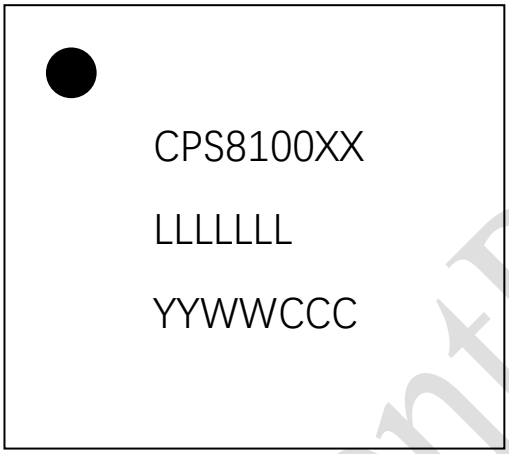
10. Order Information

Order Information

Device	Package	Shipping
CPS8100-XXXX*	QFN48 6mm x 6mm	3000/Tape & Reel

*Note – this field is a custom value that is specific to each customer application. Please contact your local sales team for your particular value for this field.

11. Marking Information



The first line: CPS8100XX: Part Number with package type suffix code

The second line: LLLLLL = Production Lot ID

The third line: YYWW= Production Date Code, consisting of Year (YY) and Week (WW)

CCC= Production Tracking Code defined and used by factory

12. Important Notice

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