1 DESCRIPTION

The MT5705 is a SoC (System on Chip) for magnetic induction based wireless power receiver.

It is fully compliant with the latest WPC Qi specification (Version 1.2.4) of BPP (Baseline Power Profile). It is capable of wireless charging for 5W of delivered power with fully programmable output voltage and current limit.

MT5705 has a very high overall AC to DC conversion efficiency (up to 95%), thanks to the optimized and adaptive full synchronous rectifier control, very small Rdson of power MOSFET's, and extremely low bias current.

With the exception of a few external passive components, this SoC integrates everything that is needed for a wireless power receiving function. It is composed of an ARM Cortex M0 processor with 2KB SRAM and 8KB OTP, full synchronous rectifier and special output LDO, robust and reliable over voltage, over current and over temperature protection circuits, various GPIO's and serial interfaces.

With the flexibility of SoC architecture and the unique implementation, the MT5705 is future proof in supporting WPC Qi specification's further updates and new proprietary protocols.

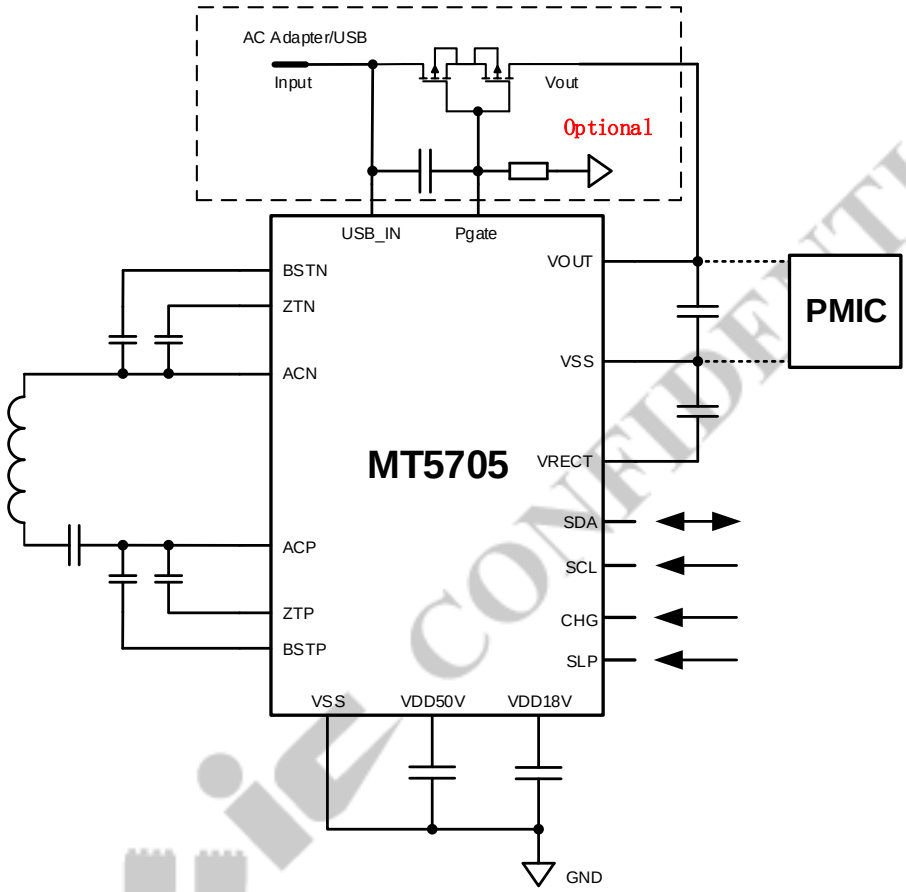
2 FEATURES

- 5W power delivery
- Fully programmable output voltage and current limit
- Embedded ARM Cortex M0 processor with 2KB SRAM and 8KB OTP
- Up to 95% AC input to DC output efficiency
- Reliable and unique over voltage, current, temperature protection
- Specially designed output LDO with output clamping and fast response to line and load transient
- WPC compliant and proprietary communication protocols support with hardware ASK modulation
- Independent I^2C slave interface with additional GPIO's
- Halogen free and RoHS compliant
- Available in 4.00mm x 4.00mm QFN32L package

3 APPLICATIONS

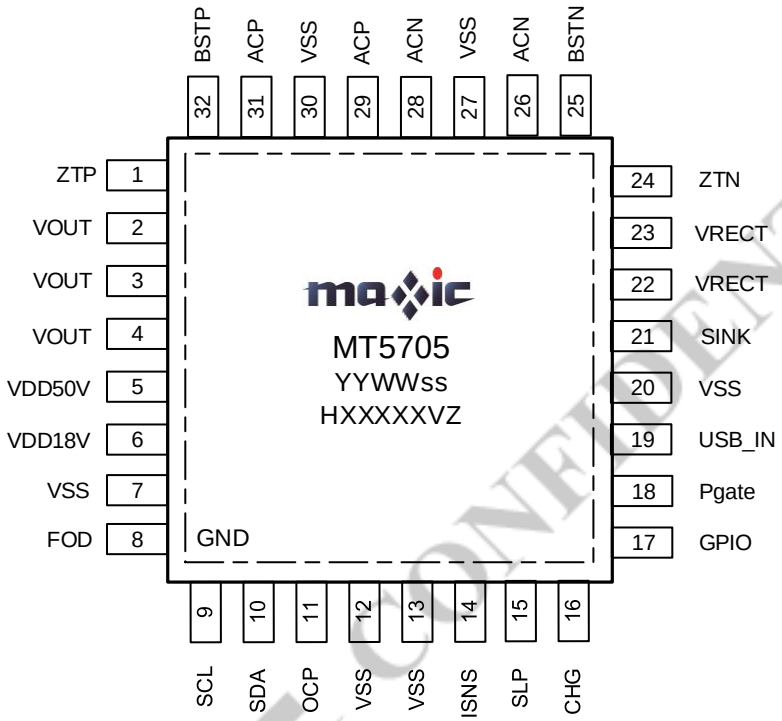
- Standard wireless charging for TWS
- Wireless charging for wearable devices with high integration and small form factor
- Rx function for power banks where they can be wirelessly charged
- Other wireless power applications

4 TYPICAL APPLICATION CIRCUIT



5 PIN CONFIGURATIONS AND FUNCTIONS

5.1 QFN32L Pin Configurations



5.2 Pin Functions

Pin Name	Pin No.	Description
ZTP	1	ASK Modulation FET at ACP. Connect a 33nF ceramic capacitor from ZTP to ACP.
ZTN	24	ASK Modulation FET at ACN. Connect a 33nF ceramic capacitor from ZTP to ACN.
VOUT	2, 3, 4	Output of LDO.
VDD50V	5	Internal 5V Power Supply. Connect to VSS with 1uF capacitor.
VDD18V	6	Internal 1.8V Power Supply. Connect to VSS with 1uF capacitor.
VSS	7, 12, 13, 20, 27, 30	Ground
Pgate	18	Gate control signal for external Over Voltage Protection P-MOSFET.
USB_IN	19	Adapter or USB input.
SINK	21	Providing sinking current. Usually shorted with VRECT. Connect a 50Ω/0.125W from SINK to VRECT at lager than 5W application.
ACN	26, 28	AC input.
ACP	29, 31	AC input.
GND	Thermal Pad	Power Ground.
VRECT	22, 23	Output of Synchronous Rectifier.
BSTP	32	Boost Capacitor for internal driver for synchronous bridge rectifier at ACP. Connect a 15nF ceramic capacitor from BSTP to ACP.
BSTN	25	Boost Capacitor for internal driver for synchronous bridge rectifier at ACN. Connect a 15nF ceramic capacitor from BSTN to ACN.
FOD	8	Foreign object detection function parameter setting by resistor divider. For details, please see the user guide.
OCP	11	OCP threshold setting by resistor divider. For details, please see the user guide.
SCL	9	I^2C slave SCL.
SDA	10	I^2C slave SDA.
ISNS	14	Current sense filter capacitor.
SLP	15	Default low level. High level indicates sleep mode, IC enters low power consumption.
CHG	16	Default low level. High level indicates charging is complete.
GPIO	17	NC, reserved pin.

6 SPECIFICATIONS

6.1 Absolute Maximum Ratings

ACN, ACP, ZTP, ZTN	-0.3V to 19.2V
BSTP, BSTN	-0.3V to ACP+6V, ACN+6V
VRECT, SINK	-0.3V to 19.2V
VOUT	-0.3V to 14.4V
VDD50V	-0.3V to 6V
FOD, OCP, SCL, SDA, ISNS, SLP, CHG, GPIO	-0.3V to 6V
VDD18V	-0.3V to 2V
PGATE	-0.3V to 8V
USB_IN	-0.3V to 8V
Storage Temperature	-55°C to 150°C
Maximum Soldering Temperature(Reflow, Pb-Free)	260°C

6.2 ESD Ratings

Test Model	Pins	Ratings
HBM	All pins	2000V
CDM	All pins	1000V
LU	USB_IN, Pgate	100mA
	The other pins	250mA

6.3 Recommended Operating Conditions

	Minimum	Typical	Maximum	Unit
Operating Temperature(Environment)	0		85	°C
Operating Current (Iout)	0	0.6	1	A
Operating Voltage (Vrect)	3		10	V

6.4 Thermal Information (Package Thermal Data)

Junction to ambient ($R_{\theta JA}$)	45°C /W
Junction to case ($R_{\theta JC}$)	22°C /W

6.5 Electrical Characteristics

(Test conditions: V_{RECT}=5.5V, T_A=25°C, unless otherwise stated.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up (VDD pin)						
UVLO	Under Voltage Lockout	VRECT rising from 0V		2.95		V
U_{VLO_HYS}	Under Voltage Lockout Hysteresis	VRECT falling		200		mV
Supply Current						
I_q	Quiescent Current			6		mA
Bridge Rectifier						
Rds(on)	Rds(on) of Power MOSFETs			90		mΩ
Over-Voltage Protection						
VOVP-DC	DC Over-Voltage Protection (programmable)	Rising voltage			12	V
LSB_Vovp	Least Significant Bitat OVP			500		mV
LDO						
VOUT	Output Voltage Regulation	Vrect = 5.5V, Iout = 0A		5		V
LSB_VOUT	Least Significant Bit when programming output voltage			25		mV
Programming _Range				3~10		V
OCP	Output Current Protection (programmable)				1.1	A
LSB_OCP	Least Significant Bit when programming output current protection			25		mA
ADC						
N	Resolution			12		Bit
f_{Sample}	Sampling Rate			100		kS/s
Channel	Number of Channels			8		
Miscellaneous						
VDD50V	VDD50V Output Voltage			5		V
VDD18V	VDD18V Output Voltage			1.8		V

6.6 Typical Operating Characteristics

The following performance characteristics were taken using MT5815 wireless power transmitter at T_A=25℃, unless otherwise noted.

Figure1. Efficiency vs. Output Load：Vout=5V

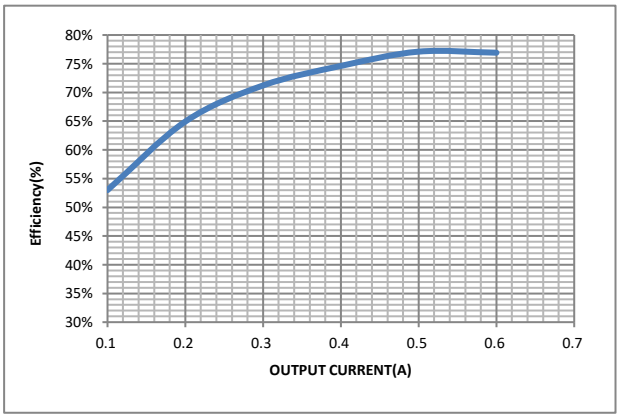


Figure2. Load Reg. vs. Output Load：Vout=5V

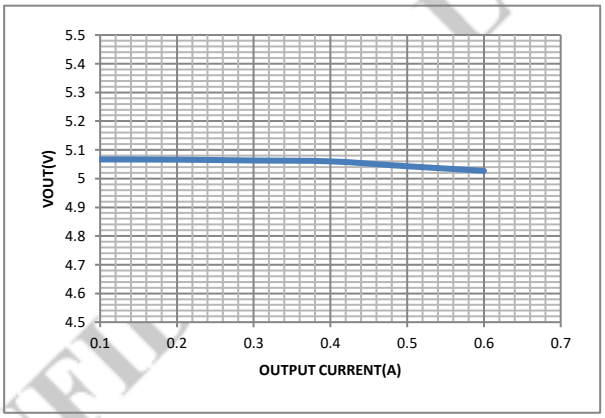


Figure3. Enable Startup: V_{OUT}=5V; I_{OUT}=0.6A

Figure4. Transient Resp: Vout=5V; I_{OUT}=0 to 0.6A

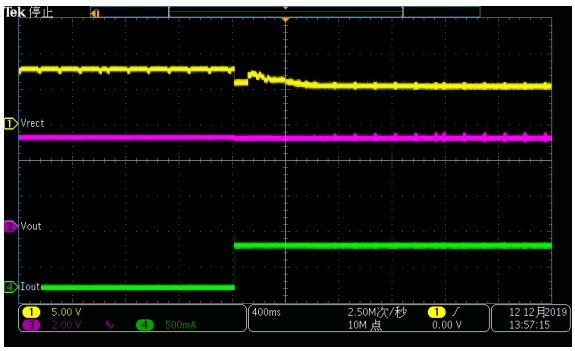
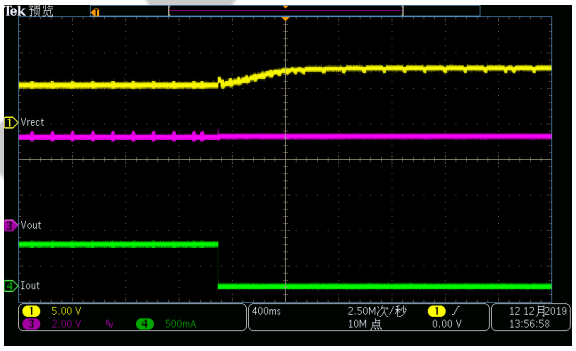


Figure5. Transient Resp: Vout=5V; I_{OUT}=0.6 to 0A



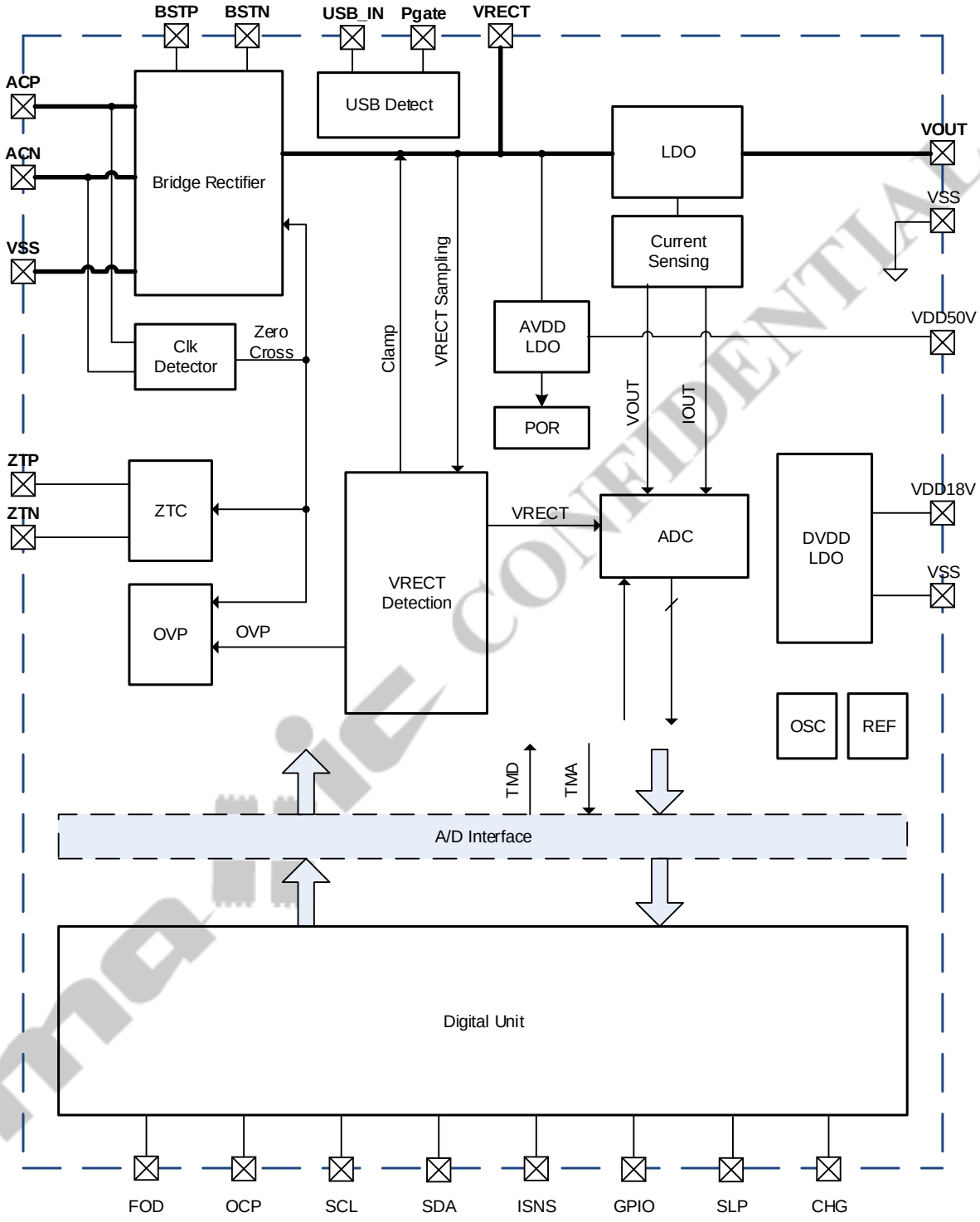
7 DETAILED DESCRIPTIONS

7.1 Overview

MT5705 is a SoC (System on Chip) for wireless power receiver. It only needs several passive components like power receiving coils, resonant tank capacitors, decoupling capacitors and pull up/down resistors to build a complete wireless power receiver system. When coupled with a wireless power transmitter, this system can provide all the functions for wireless power transfer, including power receiving and rectification, output regulation, communication for power control and data exchange, and abnormal condition (over voltage, current, temperature, etc.) protection.

MT5705 is by default programmed to be fully compliant with the latest WPC Qi Specification Version 1.2.4 with support of BPP (Baseline Power Profile).

7.2 Functional Block Diagram



7.3 Theory of Operation

MT5705 is composed of several major functional blocks which together achieve the wireless power receiving function.

Bridge Rectifier, which is also called Full Synchronous Rectifier. This block converts the received AC power from the resonant tank to DC power with the help of the capacitors connected on its output.

LDO, which is also called Main LDO or Output LDO. This block functions as a load switch (connecting and disconnecting the external load), output voltage and current regulation and output clamping when fast load/line transient happens.

VDD50V and DVDD LDO and POR. These blocks provide the necessary regulated power supplies from rectifier output for the operation of the chip.

OVP and Vrect Detection. These blocks are for the rectifier output voltage detection and over voltage protection when Vrect is too high.

OSC and REF. These blocks provide the timing reference and voltage reference for the whole chip.

ADC. This block is one of the key blocks that convert various measured analog variables (voltages, currents, temperature, external analog inputs, etc.) to digital domain such that the embedded micro controller can use the information for follow up actions.

Digital Unit. This block contains all the digital circuits, which include embedded micro controller, volatile and nonvolatile memories, I^2C interface, peripherals, DMA (Direct Memory Access), internal buses, and other digital functional blocks. This block is the brain of the whole chip which dynamically configures chip for different functions in different state, communicate with the outside world (power transmitter external host), and perform necessary data processing for proper operation (like target Vrect and Vout calculation, etc.)

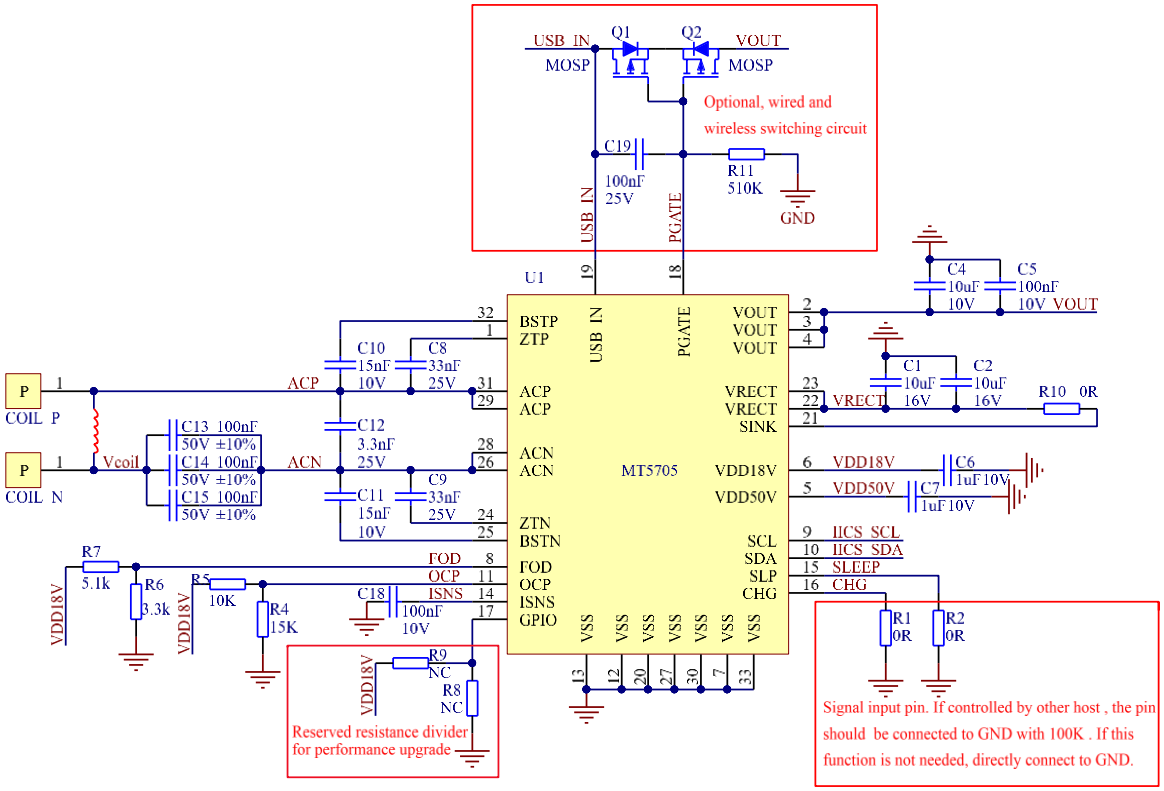
7.4 Device Function Modes

MT5705 can be programmed to operate in different modes. The switching among these modes can be made automatically based on the types of the transmitter or the instruction from the transmitter the receiver is coupled with. The operation modes can also be programmed by an external host (e.g., an Application Processor in a smart phone) via I^2C interface. Here are some of these modes:

- WPC BPP only receiver mode
- WPC BPP and proprietary receiver mode
- WPC proprietary only receiver mode

8 APPLICATIONS AND IMPLEMENTIONS

8.1 Reference Schematic

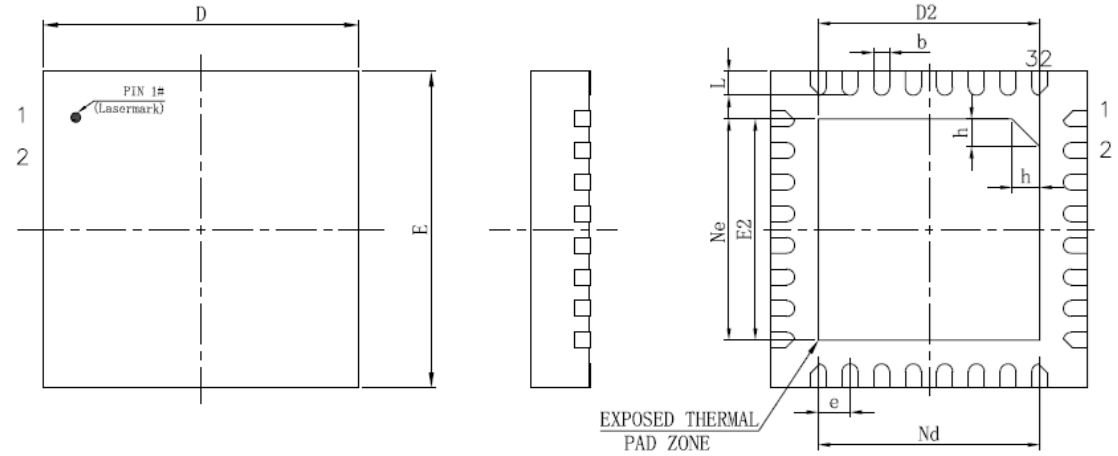


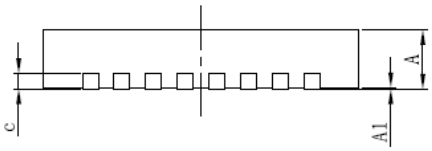
8.2 BOM

#	Reference	Value	Description	Footprint	Quantity
1	R4	15K	RES SMD 15K 5%	0402	1
2	R5	10K	RES SMD 10K 5%	0402	1
3	R6	3.3K	RES SMD 3.3K 5%	0402	1
4	R7	5.1K	RES SMD 5.1K 5%	0402	1
5	C1, C2	10uF	CAP CER 10UF 16V X7R	0603	2
6	C4	10uF	CAP CER 10UF 10V X7R	0603	1
7	C5, C18	0.1uF	CAP CER 0.1UF 10V X7R	0402	2
8	C6, C7	1uF	CAP CER 1UF 10V X7R	0402	2
9	C8, C9	33nF	CAP CER 0.033UF 25V	0402	2
10	C10, C11	15nF	CAP CER 0.015UF 10V	0402	2
11	C12	3.3nF	CAP CER 3.3NF 25V X7R	0402	1
12	C13, C14, C15	100nF	CAP CER 0.1UF 50V X7R	0603	3
13	U1	MT5705	Wireless power receiver IC	QFN32L	1
				Notes	20

9 DETAILED PACKAGING AND PCB INFORMATIONS

QFN32L Package Outline and Dimensions



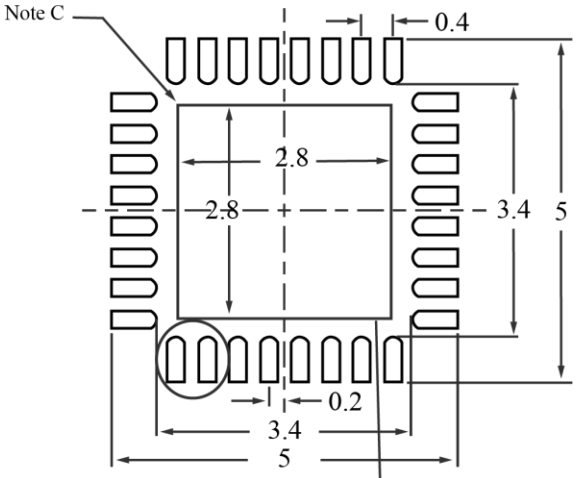


SIDE VIEW

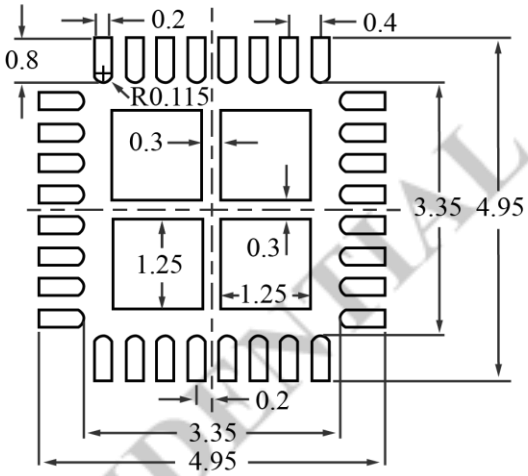
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F	122X122		

PCB Footprint Design

Example Board Layout

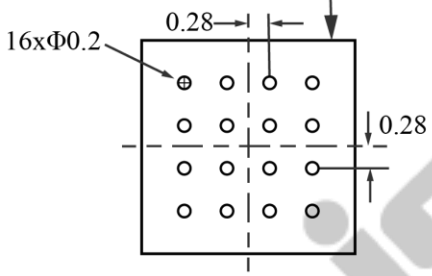


Example Stencil Design
0.125 Thick Stencil
(Note D)



(71% Printed Solder Coverage By Area)

Example Via Layout Design
may vary depending on constraints
(Note C)



Notes

A. All linear dimension are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board.
D. Laser cutting apertures with trapezoidal walls and also routing corners will offer better paste release. Customer should contact their board assembly site for stencil design recommendations.

10 ORDERING INFORMATION

Part No.	Package Information	Package Quantity	Moisture Sensitivity Level	Chip Mark
MT5705	4.00 x 4.00mm QFN32L	3000/Tape & Reel	MSLIII	MT5705 YYWWss HXXXXXVZ

11 REVISION HISTORY

Revision	Date	Description
1.00	2020-1-10	Initial release.
1.10	2020-3-16	Complete the chapter 6.2 and 6.4.
1.15	2020-5-25	Add PCB Footprint Design.
1.20	2020-06-06	Add Halogen and RoHS test results.
1.25	2020-08-24	Update ESD test result and Ordering Information.
1.26	2020-09-30	Modify absolute maximum ratings.

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