R1LP5256E Series

256Kb Advanced LPSRAM (32k word x 8bit)

R10DS0268EJ0200
Rev.2.00
2019.10.29

Description

The R1LP5256E Series is a family of low voltage 256-Kbit static RAMs organized as 32,768-word by 8-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies. The R1LP5256E Series has realized higher density, higher performance and low power consumption. The R1LP5256E Series is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. It has been packaged in 28-pin SOP and 28-pin TSOP.

Features

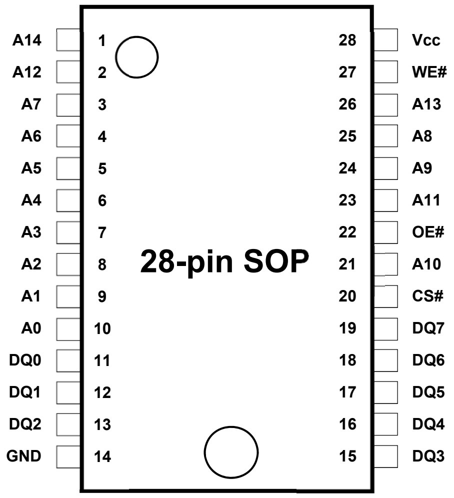
- Single 4.5V~5.5V power supply
- Small stand-by current: 0.6µA (5.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS#
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

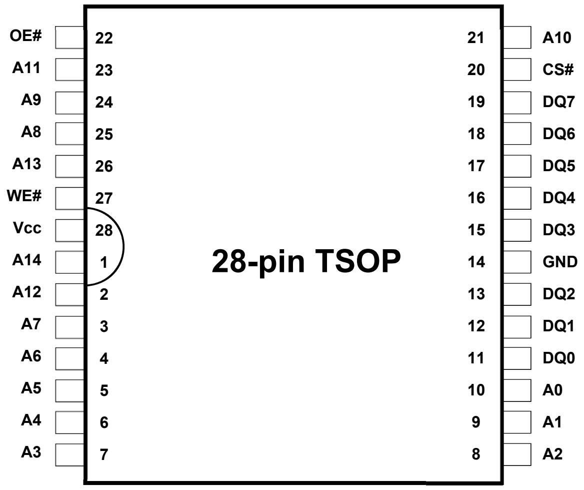
Ordering Information

Orderable part name	Access time	Temperature range	Package	Shipping container
R1LP5256ESP-5SI#B*	55 ns	-40 ~ +85°C	450-mil 28-pin plastic SOP	Tube (Magazine)
R1LP5256ESP-5SI#S*				Embossed tape
R1LP5256ESA-5SI#B*			8mm×13.4mm 28-pin plastic TSOP	Tray
R1LP5256ESA-5SI#S*				Embossed tape

Note 1. * = Revision code for Assembly site change, etc. (* = 0, 1, etc.)

Pin Arrangement

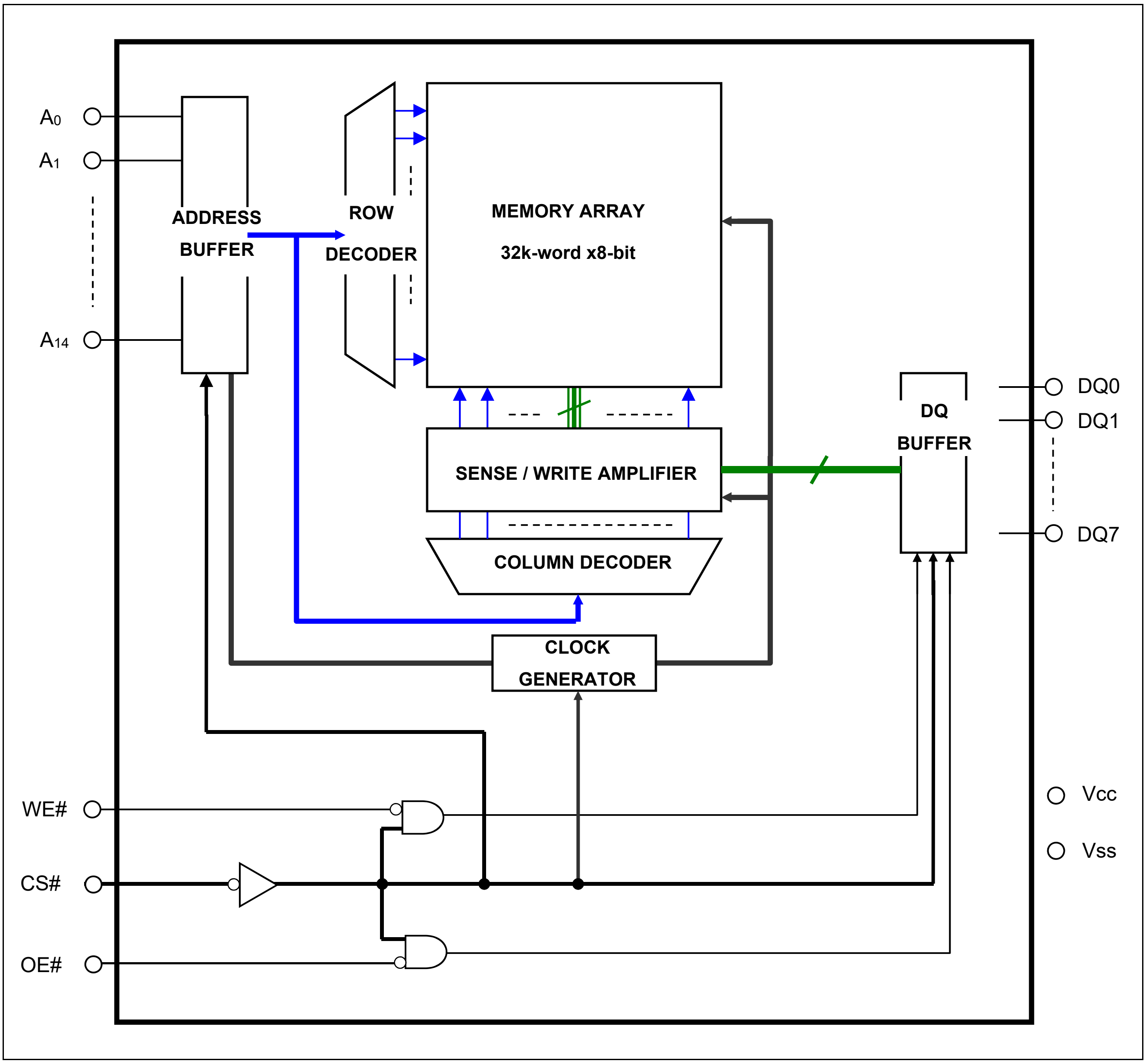




Pin Description

Pin name	Function
Vcc	Power supply
Vss (GND)	Ground
A0 to A14	Address input
DQ0 to DQ7	Data input/output
CS#	Chip select
WE#	Write enable
OE#	Output enable

Block Diagram



Operation Table

CS#	WE#	OE#	DQ0~7	Operation
H	X	X	High-Z	Stand-by
L	L	X	Din	Write
L	H	L	Dout	Read
L	H	H	High-Z	Output disable

Note 1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	Vcc	-0.3 to +7.0	V
Terminal voltage on any pin relative to Vss	V_T	-0.3[*1] to Vcc+0.3[*2]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 1. –3.0V for pulse ≤ 30ns (full width at half maximum)
2. Maximum voltage is +7.0V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	
	Vss	0	0	0	V	
Input high voltage	V_{IH}	2.2	-	Vcc+0.3	V	
Input low voltage	V_{IL}	-0.3	-	0.8	V	1
Ambient temperature range	Ta	-40	-	+85	°C	

Note 1. –3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	$\mid I_{LI} \mid$	-	-	1	μA	Vin = Vss to Vcc	
Output leakage current	$\mid I_{LO} \mid$	-	-	1	μA	CS# =V_{IH} or OE# =V_{IH}, VI/O =Vss to Vcc	
Average operating current	I_{CC1}	-	25	35	mA	Min. cycle, duty =100%, II/O = 0mA, CS# =V_{IL}, Others = V_{IH}/V_{IL}	
	I_{CC2}	-	2	4	mA	Cycle =1μs, duty =100%, II/O = 0mA, CS# ≤ 0.2V, V_{IH} ≥ Vcc-0.2V, V_{IL} ≤ 0.2V	
Standby current	I_{SB}	-	-	3	mA	CS# =V_{IH}, Others = Vss to Vcc	
Standby current	I_{SB1}	-	0.6[*1]	2	μA	~+25°C	Vin = Vss to Vcc, CS# ≥ Vcc-0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -1mA	
	V_{OH2}	Vcc - 0.5	-	-	V	I_{OH} = -0.1mA	
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA	

Note 1. Typical parameter indicates the value for the center of distribution at 5.0V (Ta= 25ºC), and not 100% tested.

Capacitance

(Vcc = 4.5V ~ 5.5V, f = 1MHz, Ta = -40 ~ +85°C)

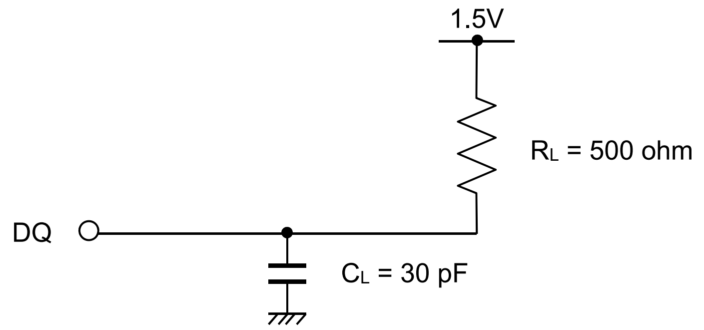
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	6	pF	Vin =0V	1
Input / output capacitance	$C_{I/O}$	-	-	8	pF	VI/O =0V	1

Note 1. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 4.5V ~ 5.5V, Ta = -40 ~ +85°C)

- Input pulse levels: VIL = 0.6V, VIH = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	55	-	ns	
Address access time	t_{AA}	-	55	ns	
Chip select access time	t_{ACS}	-	55	ns	
Output enable to output valid	t_{OE}	-	30	ns	
Output hold from address change	t_{OH}	10	-	ns	
Chip select to output in low-Z	t_{CLZ}	5	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ}	0	20	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2,3

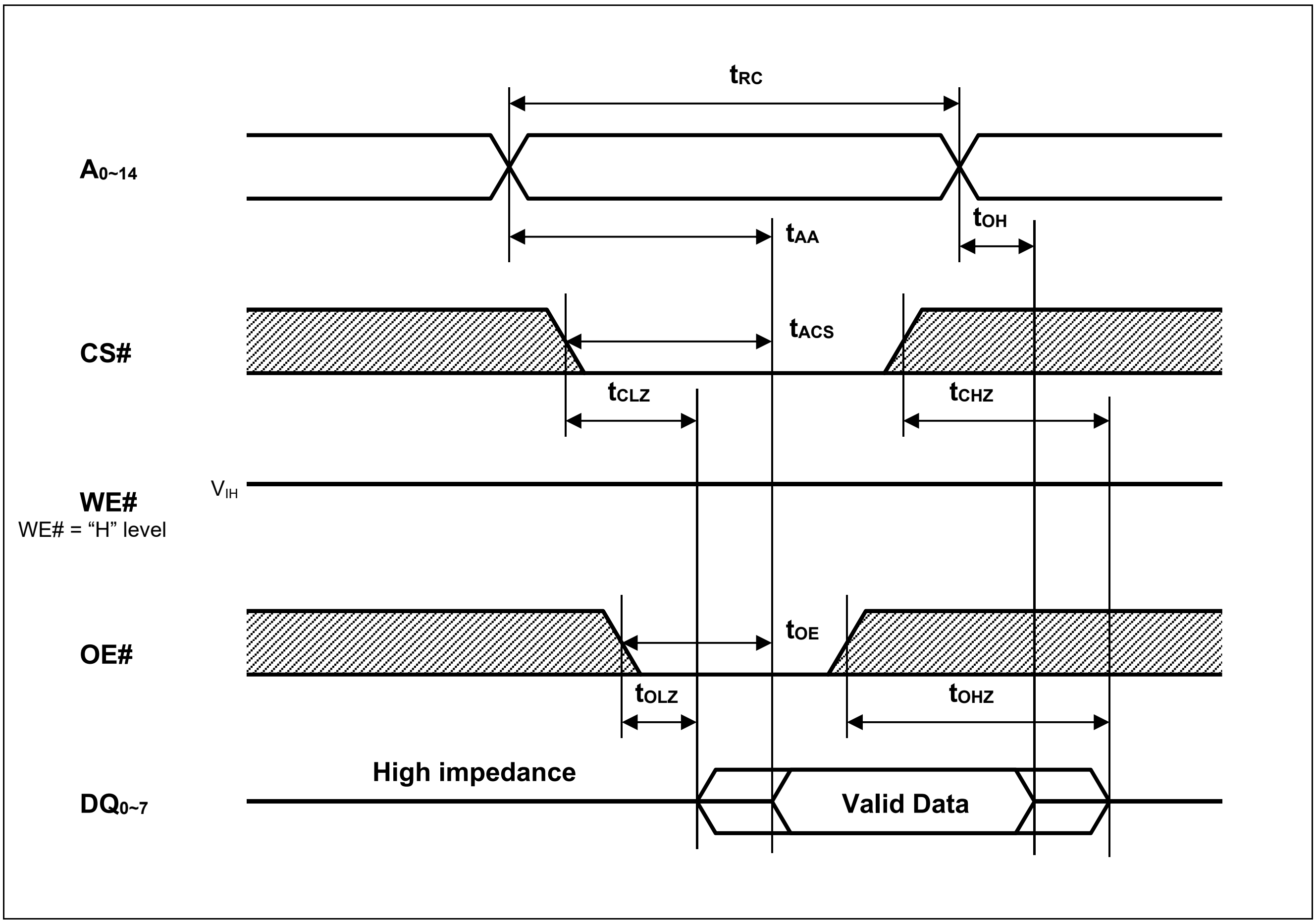
Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	55	-	ns	
Address valid to end of write	t_{AW}	50	-	ns	
Chip select to end of write	t_{CW}	50	-	ns	5
Write pulse width	t_{WP}	40	-	ns	4
Address setup time	t_{AS}	0	-	ns	6
Write recovery time	t_{WR}	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	ns	
Data hold from write time	t_{DH}	0	-	ns	
Output enable from end of write	t_{OW}	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	ns	1,2

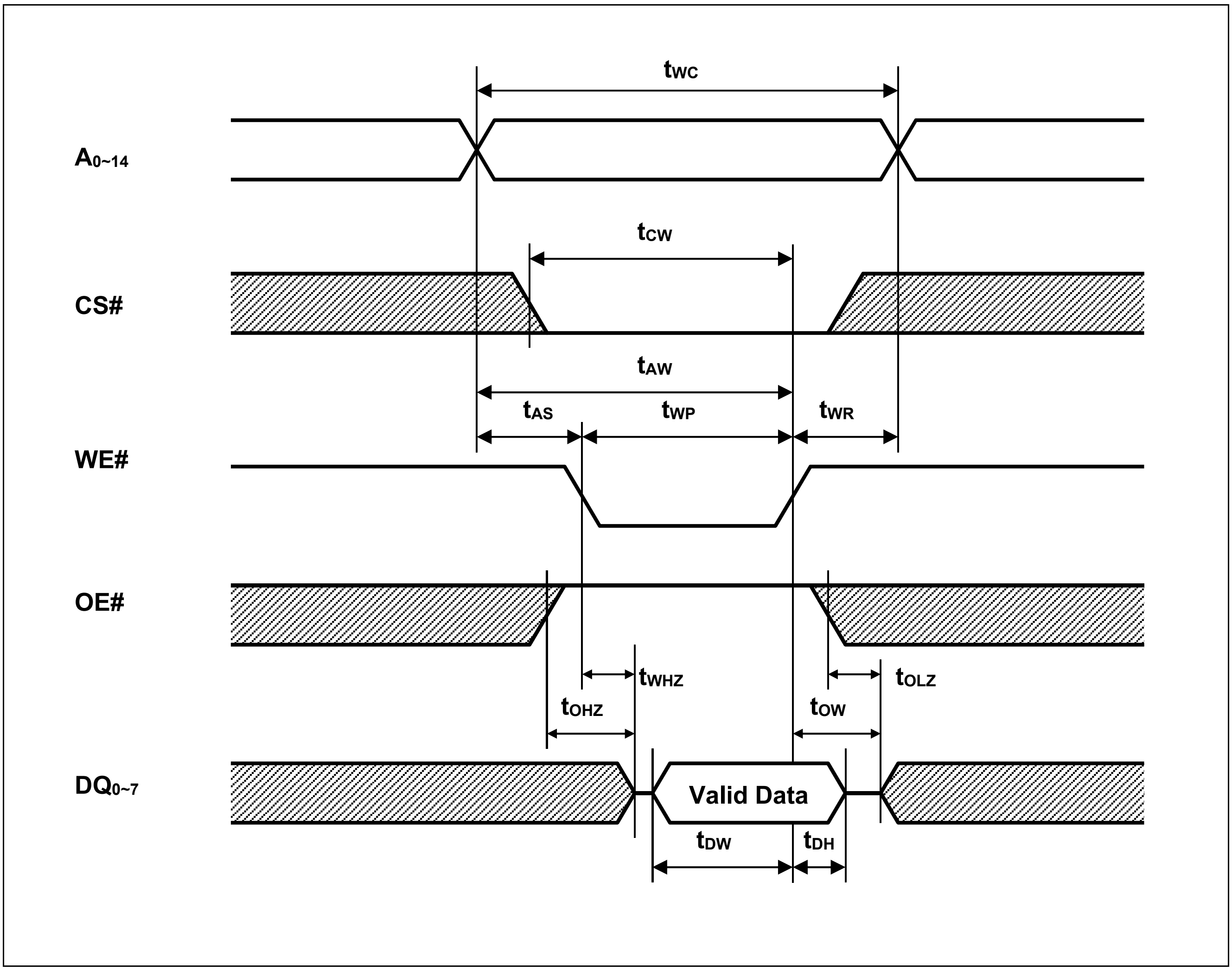
Note
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low CS#, a low WE#.
   A write begins at the latest transition among CS# going low and WE# going low.
   A write ends at the earliest transition among CS# going high and WE# going high.
   t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS# going low to end of write.
6. t_{AS} is measured the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS# or WE# going high to the end of write cycle.
8. Don’t apply inverted phase signal externally when DQ pin is output mode.

Timing Waveforms

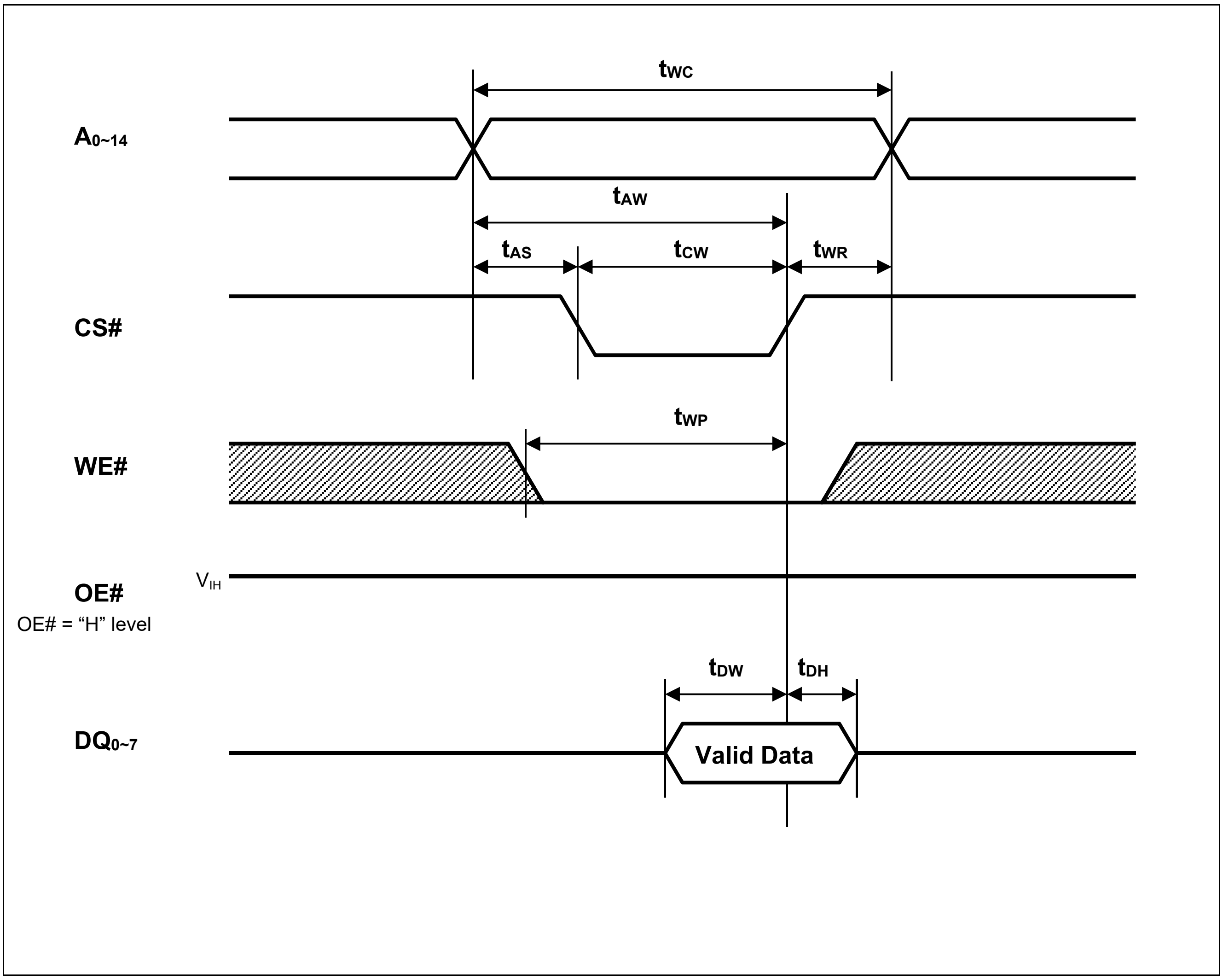
Read Cycle



Write Cycle (1) (WE# CLOCK)



Write Cycle (2) (CS# CLOCK)



Low Vcc Data Retention Characteristics

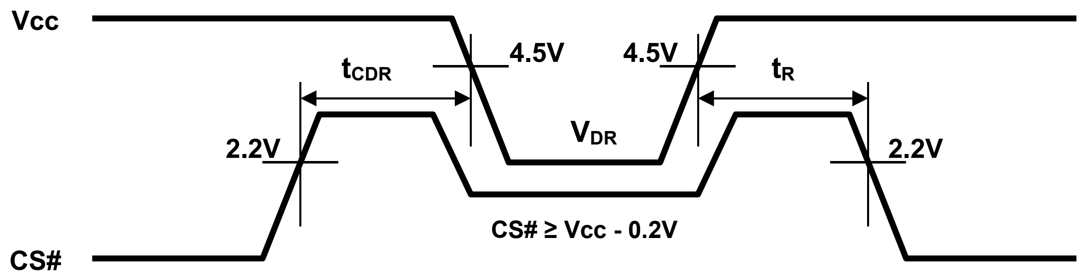
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions*2	
Vcc for data retention	V_{DR}	2.0	-	5.5	V	Vin ≥ 0V, CS# ≥ Vcc-0.2V	
Data retention current	I_{CCDR}	-	0.6*1	2	μA	~+25°C	Vcc=3.0V, Vin ≥ 0V, CS# ≥ Vcc-0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Chip deselect time to data retention	t_{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t_R	5	-	-	ms		

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.

2. CS# controls address buffer, WE# buffer, OE# buffer and Din buffer. If CS# controls data retention mode, Vin levels (address, WE#, OE#, DQ) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms

CS# Controlled



Revision History	R1LP5256E Series Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	2017.1.27	-	First Edition issued
2.00	2019.10.29	p.1	Revised orderable part name information.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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