Low Power 3-Port HDMI/MHL Receiver with Scaler and CCIR 656 Output

EP9555E

Data Sheet

V0.3

Revised Date: Nov. 14, 2013
Original Release Date: Nov. 07, 2012

Explore

1.1 Overview

EP9555E is a 3-Port Low Power HDMI/MHL receiver with video up/down Scaler and CCIR 601/656 digital video output. The chip is compliant with HDMI 1.4, MHL 2.0 and HDCP 1.4 specifications. The chip supports 1 HDMI/MHL dual mode port (Port 1) and 2 MHL ports (Port 0 and Port 2). The chip supports Video Output up to 1080p 60 Hz. The chip also supports 2-channel IIS and S/PDIF Audio Outputs. The chip integrates Equalizer Switches, HDMI/MHL core, HDCP engine, Video Scaler and EDID RAM in a single chip.

The on-chip Video Scaler is able to scale the input video up or down to any resolution within the range of 0.5X to 2X in both Horizontal and Vertical direction. This is useful for converting an EIA standard video to fit an LCD panel in different resolution.

EP9555E is also integrated with an 8-bit MCU on-chip for HDMI/MHL/HDCP/Scaler control and CEC/RCP applications. With this embedded MCU user is not required to develop the firmware and it is very easy for user to use the chip.

1.2 Features

- On-chip MCU for HDMI/MHL/HDCP/Scaler control and CEC/RCP applications.
- On-chip HDMI/MHL dual mode Receiver core which is compliant with HDMI 1.4 and MHL 2.0 specifications
- On-chip HDCP Engine which is compliant with HDCP 1.4 specification
- On-chip Video Up/Down Scaler
- Support 1 HDMI/MHL dual mode port (Port 1) and 2 MHL ports (Port 0 and Port 2).
- On-chip EDID RAM
- Supports video resolution up to 1080p 60 Hz in both input and output
- On-chip Audio Decoder which support 2-channel IIS and S/PDIF audio outputs
- Support audio soft mute
- Support SPDIF Channel Status extraction
- On-chip YCC422 to YCC444 conversion and YCC444 to YCC422 conversion
- On-chip YCC to RGB and RGB to YCC conversion in ITU-R BT.601 and 709 color space
- Support 24-bit RGB, 24-bit YCC444, 16-bit YCC422 non-multiplexed digital video output
- Support 8-bit YCC422 multiplexed video output in CCIR 601/656
- Support Bit Sequence Reverse and Port Swapping in video output pins to ease PCB layout
- Support DDR clocking in digital video output

- Register-programmable via slave IIC interface
- Flexible interrupt registers with interrupt pin
- Link On and Valid DE Detection
- Controllable tri-state for output pins
- Low Power operation
- Low stand-by current (< 1mA) at power down mode
- 128-pin LQFP for EP9555E

2.2 EP9555E Pin Diagram (LQFP-128)

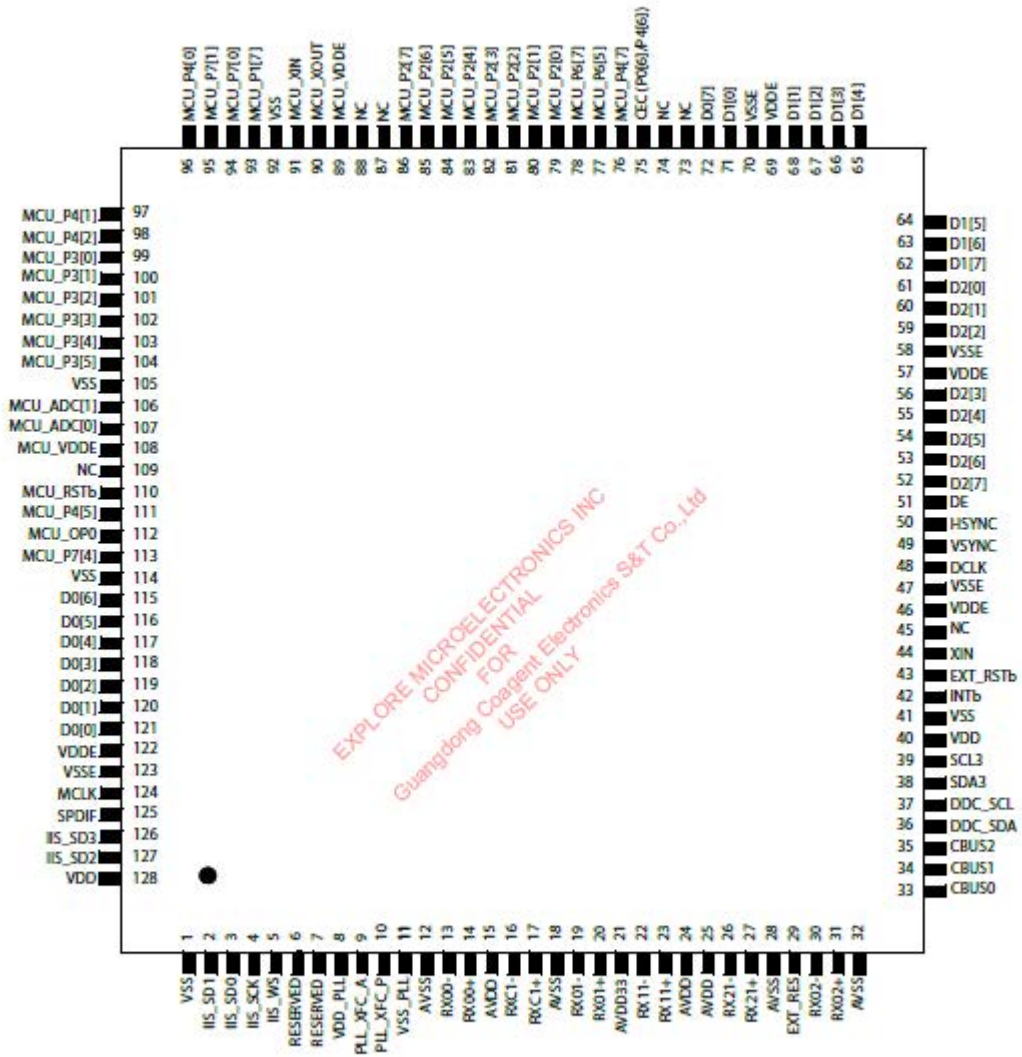
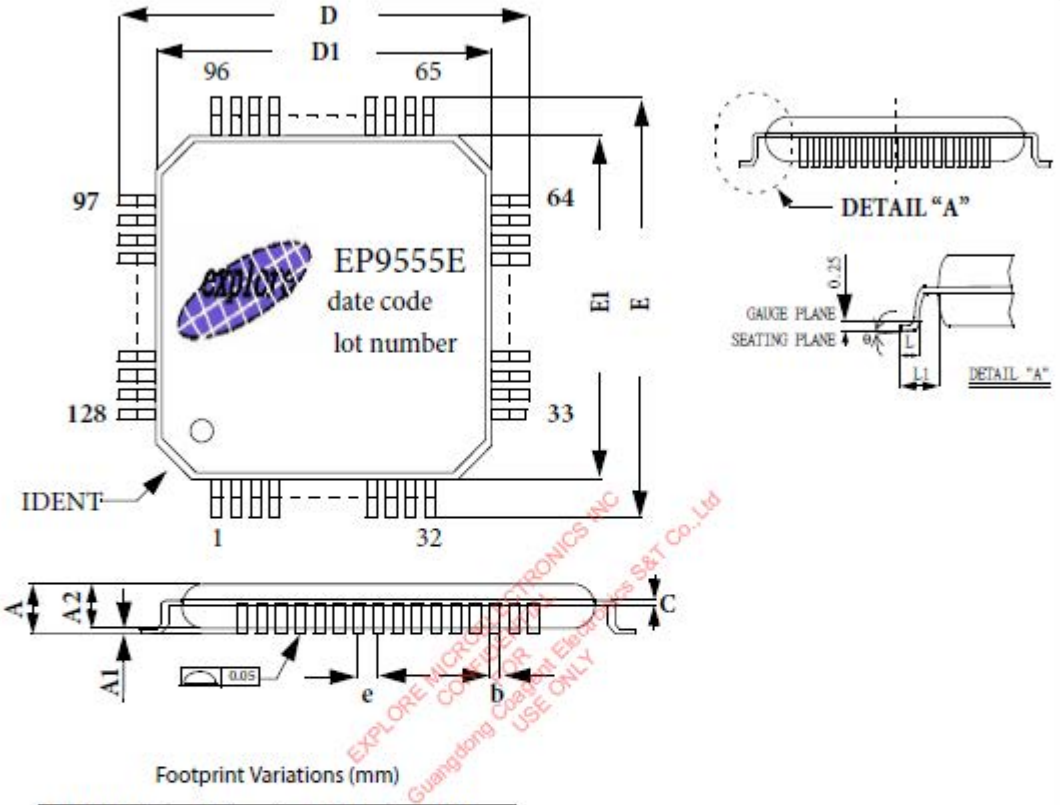


Figure 2-2 EP9555E Pin Diagram

Appendix A

Figure A-1 EP9555E Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.6
A1	0.05	0.1	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
C	0.09	-	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:
1. JEDEC OUTLINE : N/A
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.