HS-3182

ARINC 429 Bus Interface Line Driver Circuit

FN2963
Rev 3.00
May 30, 2008

The HS-3182 is a monolithic dielectric ally isolated bipolar differential line driver designed to meet the specifications of ARINC 429. This device is intended to be used with a companion chip, HS-3282 CMOS ARINC Bus Interface Circuit, which provides the data formatting and processor interface function.

All logic inputs are TTL and CMOS compatible. In addition to the DATA (A) and DATA (B) inputs, there are also inputs for CLOCK and SYNC signals which are AND'd with the DATA inputs. This feature enhances system performance and allows the HS-3182 to be used with devices other than the HS-3182.

Three power supplies are necessary to operate the HS-3182: +V = +15V ±10%, -V = -15V ±10%, and V1 = 5V ±5%. V_{REF} is used to program the differential output voltage swing such that V_{OUT} (DIFF) = ±2VREF. Typically, V_{REF} = V1 = 5V ±5%, but a separate power supply may be used for VREF which should not exceed 6V.

The driver output impedance is 75Ω ±20% at +25°C. Driver output rise and fall times are independently programmed through the use of two external capacitors connected to the CA and CB inputs. Typical capacitor values are CA = CB = 75pF for high-speed operation (100kBPS), and CA = CB = 300pF for low-speed operation (12kBPS to 14.5kBPS). The outputs are protected against overvoltage and short circuit as shown in the Block Diagram. The HS-3182 is designed to operate over an ambient temperature range of -55°C to +125°C, or -40°C to +85°C.

TABLE 1. TRUTH TABLE

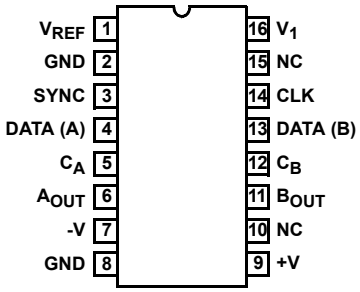
SYNC	CLK	DATA (A)	DATA (B)	A_{OUT}	B_{OUT}	COMMENTS
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	$-V_{REF}$	$+V_{REF}$	Low
H	H	H	L	$+V_{REF}$	$-V_{REF}$	High
H	H	H	H	0V	0V	Null

Features

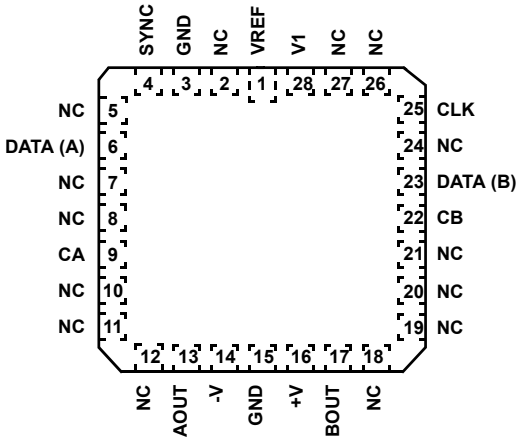
- RoHS/Pb-free Available for SBDIP Package (100% Gold Termination Finish)
- TTL and CMOS Compatible Inputs
- Adjustable Rise and Fall Times via Two External Capacitors
- Programmable Output Differential Voltage via V_{REF} Input
- Operates at Data Rates Up to 100k Bits/s
- Output Short Circuit Proof and Contains Overvoltage Protection
- Outputs are Inhibited (0V) If DATA (A) and DATA (B) Inputs are Both in the "Logic One" State
- DATA (A) and DATA (B) Signals are "AND'd" with Clock and Sync Signals
- Full Military Temperature Range

Pinouts

HS-3182
(16 LD SBDIP)
TOP VIEW



HS-3182
(28 LD CLCC)
TOP VIEW

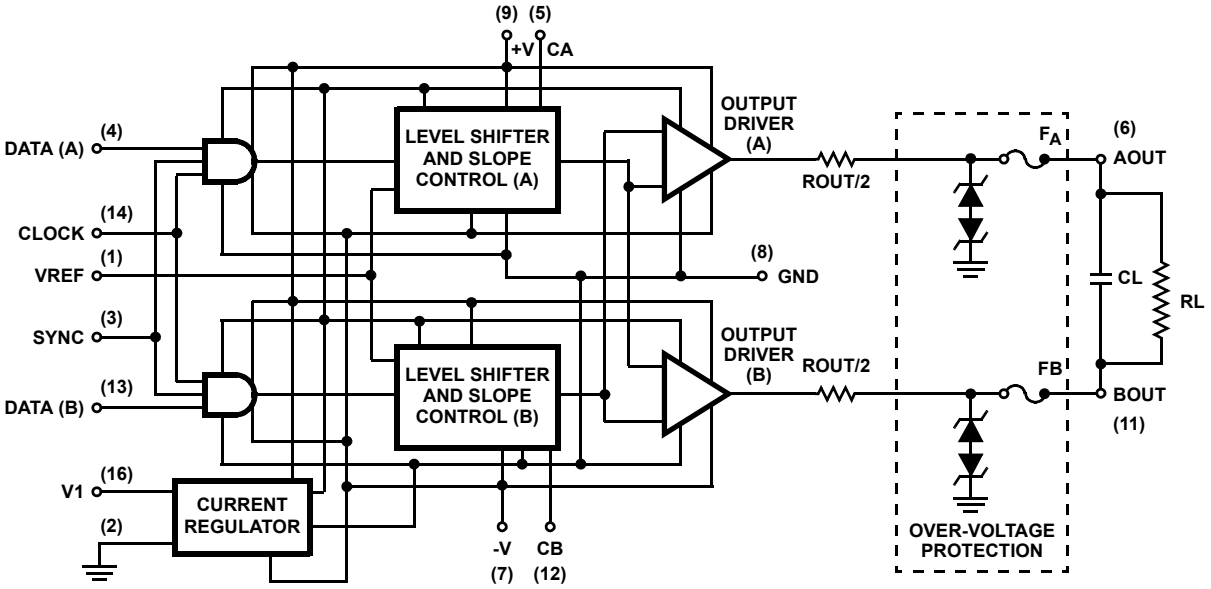


Ordering Information

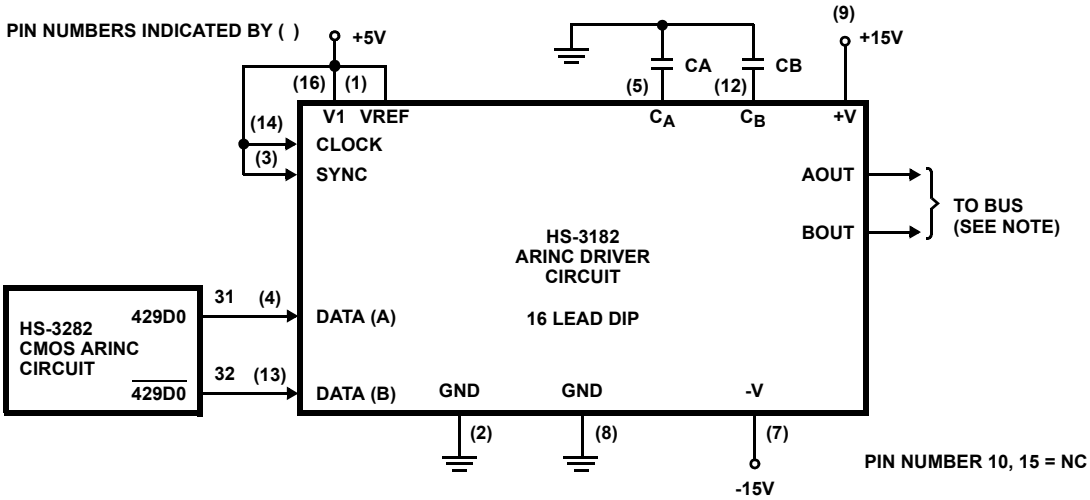
PART NUMBER	ORDERING NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HS1-3182-8	5962-8687901EA	HS1-3182-8 RD	-55 to +125	16 Ld SBDIP, Solder Seal (Pb-free)	D16.3
HS1-3182-9+	HS1-3182-9+	HS1-3182-9+ RD	-40 to +85	16 Ld SBDIP, Solder Seal (Pb-free)	D16.3
HS4-3182-8	5962-86879013A	HS4- 3182-8 RD	-55 to +125	28 Ld TER CLCC, Solder Seal	J28.A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Block Diagram



Typical Application



NOTE: The rise and fall time of the outputs are set to ARINC specified values by C_A and C_B. Typical $C_A = C_B = 75pF$ for high speed and 300pF for low speed operation. The output HI and low levels are set to ARINC specifications by V_{REF}.

Absolute Maximum Ratings

Voltage Between +V and -V Terminals 40V
V1. . . . . .7V
VREF 6V
Logic Input Voltage . . . . . GND -0.3V to V1 +0.3V
Output Short Circuit Duration. . . . . (Note 3)
Output Overvoltage Protection. . . . . (Note 4)

Operating Conditions

Operating Voltage
+V . . . . . +15V ±10%
-V . . . . . -15V ±10%
V1. . . . . 5V ±5%
VREF (For ARINC 429) . . . . . 5V ±5%
Operating Temperature Range
HS-3182-9+ . . . . . .-40°C to +85°C
HS-3182-8 . . . . . .-55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	68	12
CLCC Package	54	10

Storage Temperature Range . . . . . .-65°C to +150°C
Maximum Junction Temperature . . . . . .+175°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Die Characteristics

Number of Transistors or Gates 133

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JC}, the “case temp” location is the center of the package underside.
3. Heat sink may be required for 100k bits/s at +125°C and output short circuit at +125°C.
4. The fuses used for output overvoltage protection may be blown by a fault at each output of greater than ±6.5V relative to GND.

DC Electrical Specifications

Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

DC PARAMETER	SYMBOL	CONDITIONS (Note 5)	MIN	MAX	UNITS
Supply Current +V (Operating)	I_{CCOP} (+V)	No Load (0k to 100k bits/s)	-	16	mA
Supply Current -V (Operating)	I_{CCOP} (-V)	No Load (0k to 100k bits/s)	-16	-	mA
Supply Current V_1 (Operating)	I_{CCOP} (V_1)	No Load (0k to 100k bits/s)	-	975	µA
Supply Current V_{REF} (Operating)	I_{CCOP} (V_{REF})	No Load (0k to 100k bits/s)	-1.0	-	mA
Logic “1” Input Voltage	V_{IH}		2.0	-	V
Logic “0” Input Voltage	V_{IL}		-	0.5	V
Output Voltage High (Output to GND)	V_{OH}	No Load (0k to 100k bits/s)	V_{REF} (-250mV)	V_{REF} (+250mV)	
Output Voltage Low (Output to GND)	V_{OL}	No Load (0k to 100k bits/s)	$-V_{REF}$ (-250mV)	$-V_{REF}$ (+250mV)	
Output Voltage Null	V_{NULL}	No Load (0k to 100k bits/s)	-250	+250	mV
Input Current (Input Low)	I_{IL}		-20	-	mA
Input Current (Input High)	I_{IH}		-	10	mA
Output Short Circuit Current (Output High)	I_{OHSC}	Short to GND	-	-80	mA
Output Short Circuit Current (Output Low)	I_{OLSC}	Short to GND	80	-	mA
Output Impedance	Z_O	T_A = +25°C	60	90	Ω

NOTES:

5. +V = +15V ±10%, -V = -15V ±10%, V_1 = V_{REF} = 5V ±5%, unless otherwise specified T_A = -40°C to +85°C for HS-3182-9+ and T_A = -55°C to +125°C for HS-3182-8.

AC Electrical Specifications

AC PARAMETER	SYMBOL	CONDITIONS (Note 6)	MIN	MAX	UNITS
Rise Time (A_{OUT}, B_{OUT})	t_R	$C_A = C_B = 75pF$, (Note 7)	1	2	µs
		(at T_A = -55°C Only)	0.9	2.4	µs
		$C_A = C_B = 300pF$, (Note 7)	3	9	µs
Fall Time (A_{OUT}, B_{OUT})	t_F	$C_A = C_B = 75pF$, (Note 8)	1	2	µs
		(at T_A = -55°C Only)	0.9	2.4	µs
		$C_A = C_B = 300pF$, (Note 8)	3	9	µs
Propagation Delay Input to Output	t_{PLH}	$C_A = C_B = 75pF$, No Load	-	3.3	µs
Propagation Delay Input to Output	t_{PHL}	$C_A = C_B = 75pF$, No Load	-	3.3	µs

NOTES:

6. +V = +15V, -V = -15V, $V_1 = V_{REF}$ = 5V, unless otherwise specified T_A = -40°C to +85°C for HS-3182-9+ and T_A = -55°C to +125°C for HS-3182-8.
7. t_R measured 50% to 90% x 2, no load.
8. t_F measured 50% to 10% x 2, no load.

Electrical Specifications

PARAMETER	SYMBOL	CONDITIONS (NOTE 9)	MIN	MAX	UNITS
Input Capacitance	C_{IN}	T_A = +25°C	-	15	pF
Supply Current +V (Short Circuit)	I_{SC} (+V)	Short to GND, T_A = +25°C	-	150	mA
Supply Current -V (Short Circuit)	I_{SC} (-V)	Short to GND, T_A = +25°C	-150	-	mA

NOTES:

9. Limits established by characterization and are not production tested.

Power Specifications

Nominal Power at +25°C, +V = +15V, -V = -15V, V1 = VREF = 5V, Notes 10, 12

DATA RATE (k BITS/s)	LOAD	+V	V-	V_1	CHIP POWER	POWER DISSIPATION IN LOAD
0 to 100	No Load	11mA	-10mA	600µA	325mW	0
12.5 to 14	Full Load, Note 11	24mA	-24mA	600µA	660mW	60mW
100	Full Load, Note 11	46mA	-46mA	600µA	1 Watt	325mW

NOTES:

10. Heat sink may be required for 100k bits/s at +125°C and output short circuit at +125°C.

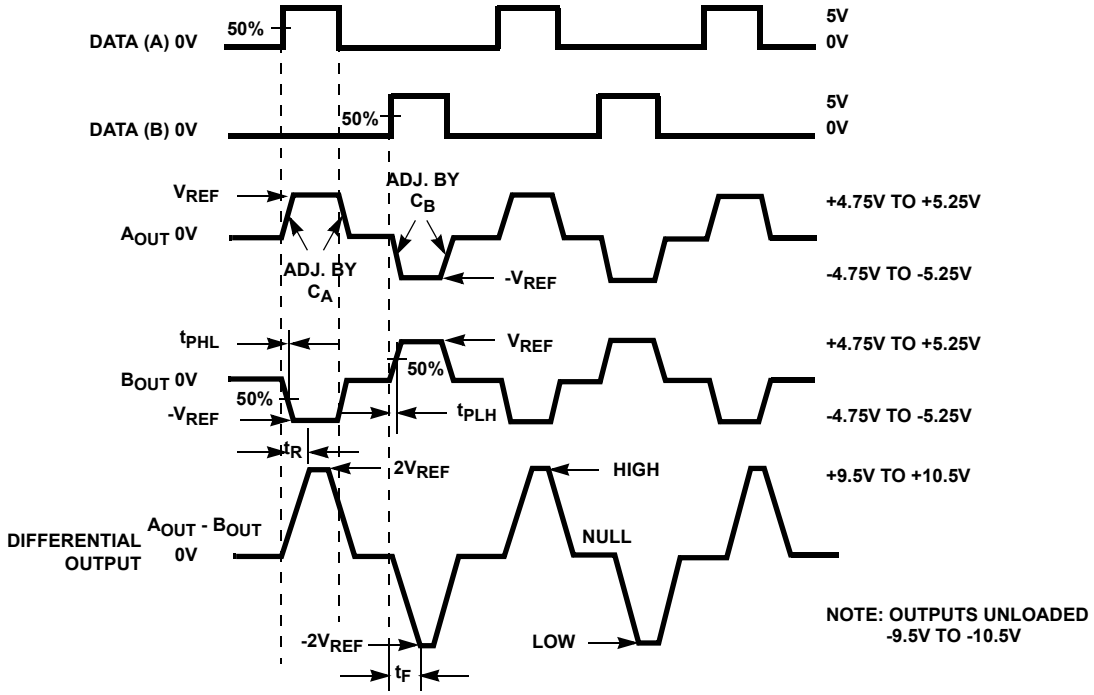
    Thermal characteristics: $T_{(CASE)} = T_{(Junction)} - \theta_{(Junction - Case)} P_{(Dissipation)}$.

    Where: $T_{(Junction\ Max)}$ = +175°C

    $\theta_{(Junction - Case)}$ = 10.9°C/W (6.1°C/W for LCC)

    $\theta_{(Junction - Ambient)}$ = 73.5°C/W (54.0°C/W for LCC)
11. Full Load for ARINC 429: $R_L = 400\Omega$ and C_L = 30,000pF in parallel between A_{OUT} and B_{OUT} (See “Block Diagram” on page 2).
12. Output Overvoltage Protection: The fuses used for output overvoltage protection may be blown by a fault at each output of greater than ±6.5V relative to GND.

Driver Waveforms



NOTES:

t_R measured 50% to 90% x 2

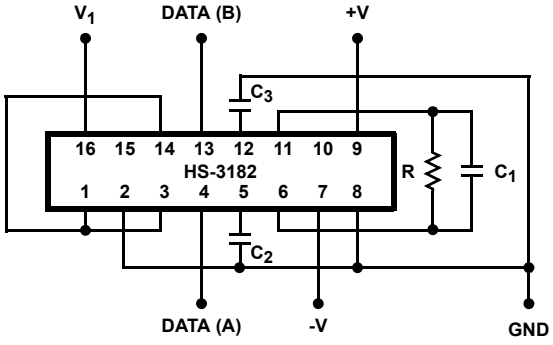
t_F measured 50% to 10% x 2

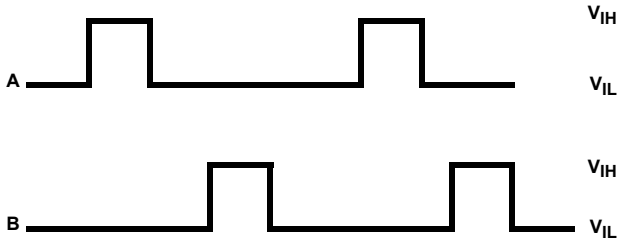
V_{IH} = 5V V_{OL} = -4.75V to -5.25V

V_{IL} = 0V V_{OH} = 4.75V to 5.25V

When the Data (A) input is in the Logic One state and the Data (B) input is in the Logic Zero state, A_{OUT} is equal to V_{REF} and B_{OUT} is equal to $-V_{REF}$. This constitutes the Output High state. Data (A) and Data (B) both in the Logic Zero state causes both A_{OUT} and B_{OUT} to be equal to 0V which designates the output Null state. Data (A) in the Logic Zero state and Data (B) in the Logic One state causes A_{OUT} to be equal to $-V_{REF}$ and B_{OUT} to be equal to V_{REF} which is the Output Low state.

Burn-In Schematic





NOTES:

R = 400Ω ± 5%

C_1 = 0.03mF ± 20%

C_2 = C_3 = 500pF, NPO

+V = +15.5V ± 0.5V

-V = -15.5V ± 0.5V

V_1 = +5.5V ± 0.5V

A 0.0mF decoupling capacitor is required on each of the three supply lines (+V, -V and V_1) at every 3rd Burn-In socket.

Ambient Temp. Max. = +125°C.

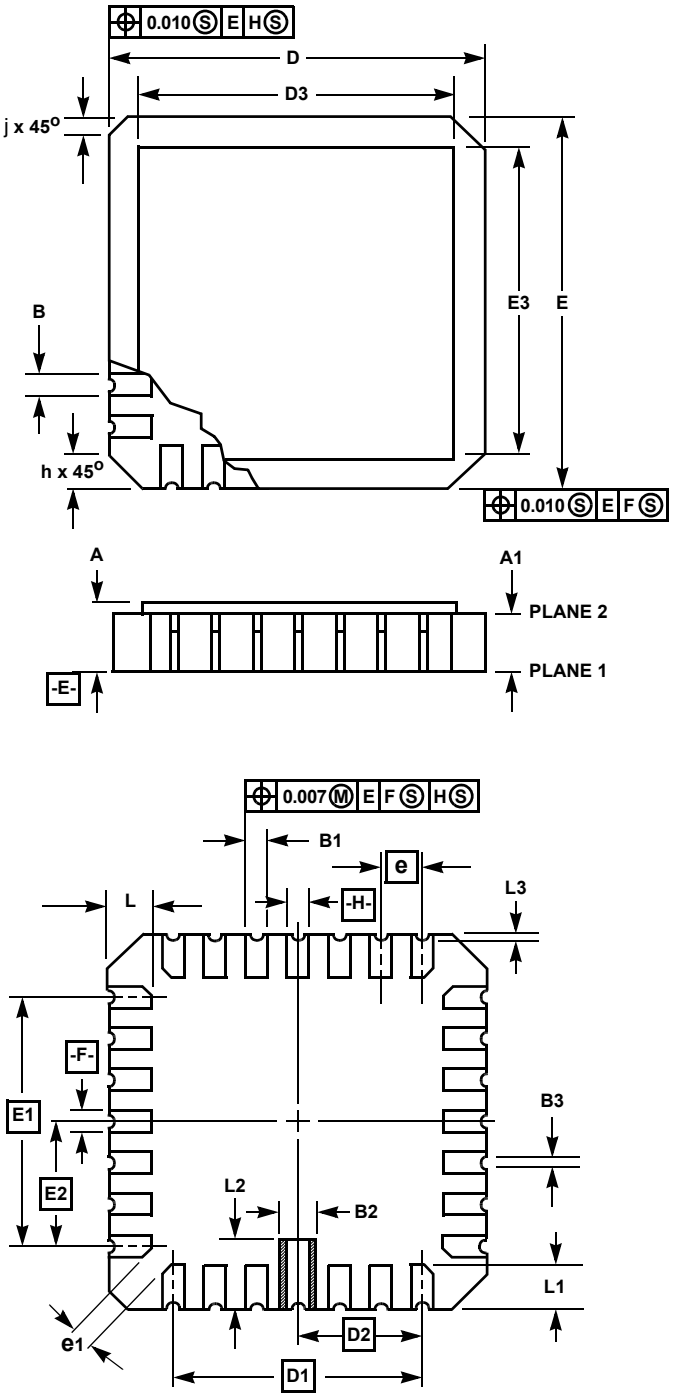
Package = 16 Lead Side Brazed DIP.

Pulse Conditions = A & B = 6.25kHz ±10%. B is delayed one-half cycle and in sync with A.

V_{IH} = 2.0V Min.

V_{IL} = 0.5V Max.

Ceramic Leadless Chip Carrier Packages (CLCC)



J28.A MIL-STD-1835 CQCC1-N28 (C-4)
28 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

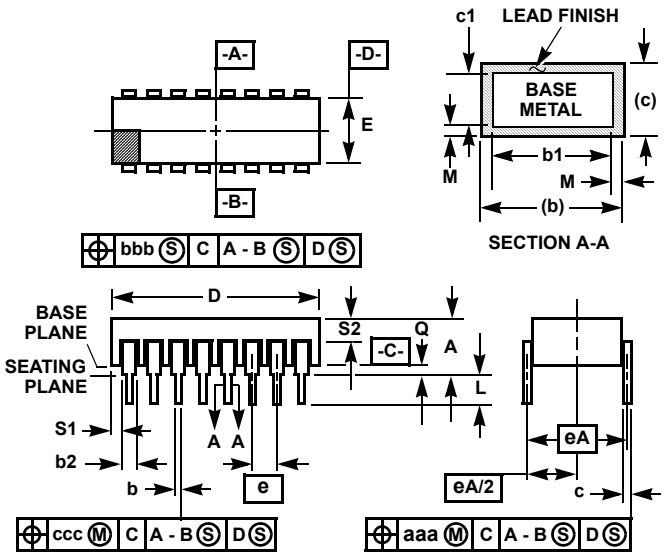
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.442	0.460	11.23	11.68	-
D1	0.300 BSC		7.62 BSC		-
D2	0.150 BSC		3.81 BSC		-
D3	-	0.460	-	11.68	2
E	0.442	0.460	11.23	11.68	-
E1	0.300 BSC		7.62 BSC		-
E2	0.150 BSC		3.81 BSC		-
E3	-	0.460	-	11.68	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.038	-
ND	7		7		3
NE	7		7		3
N	28		28		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94