MP2672
Boost Charger with Cell Balance for 2-Cell Series Lithium-Ion Battery

DESCRIPTION

The MP2672 is a highly integrated, flexible switch-mode battery charger IC for a Lithium-ion battery with two cells in series, which is used in a wide range of portable applications.

When the input power supply is present, the MP2672 operates in boost mode to charge the battery with two cells in series. When charging is enabled, the MP2672 automatically detects the battery voltage and charges the battery in three phases: pre-charge, constant-current charge, and constant-voltage charge. Other features include charge termination and auto-recharge.

The MP2672 also has a narrow voltage DC (NVDC) power structure. When the battery is weak, the MP2672 regulates the system output at the minimum voltage level to power the system instantly and charge the battery via the battery FET simultaneously.

The MP2672 also has cell balance function. It monitors the voltage across each cell and equalizes cell voltages once the difference exceeds the mismatch threshold.

The MP2672 has two configuration modes: standalone mode and host control mode. In standalone mode, the charging parameters can be configured by the hardware pins. In host control mode, the charging parameter can be configured by the I²C registers.

The MP2672 has diversified and robust protections. It has a thermal regulation loop to decrease the charge current if the junction temperature exceeds the thermal loop threshold. It also has battery temperature protection compliant with JEITA standards. Other safety features include input over-voltage protection, battery over-voltage protection, thermal shutdown, battery temperature monitoring, a watchdog timer, and a programmable back-up timer to prevent prolonged charging of a dead battery.

FEATURES

- 4.0V to 5.75V Input Operation Voltage
- Up to 14V Sustainable Voltage
- Up to 2A Programmable Charge Current for Battery with 2 Cells in Series
- Compatible with Host Control and Standalone Mode
- NVDC Power Path Management
- Programmable Input Voltage Limit
- Programmable Charge Voltage with 0.5% Accuracy
- No External Sense Resistor Required
- Integrated Cell Balancing Circuit for Cell Mismatch
- Preconditioning for Fully Depleted Battery
- Flexible New Charging Cycle Initiation
- Charging Operation Indicator in Standalone Mode
- Missing Battery Detection
- I²C Port for Flexible System Parameter Setting and Status Reporting in Host Control Mode
- Negative Temperature Coefficient Pin for Temperature Monitoring Compliant with JEITA Standards
- Built-In Charging Protection and Programmable Safety Timer
- MOSFET Cycle-by-Cycle Over-Current Protection
- Thermal Regulation and Thermal Shutdown
- Available in a QFN-18 (2mmx3mm) Package

APPLICATIONS

- Portable Handheld Solutions
- POS Machines
- Bluetooth Speakers
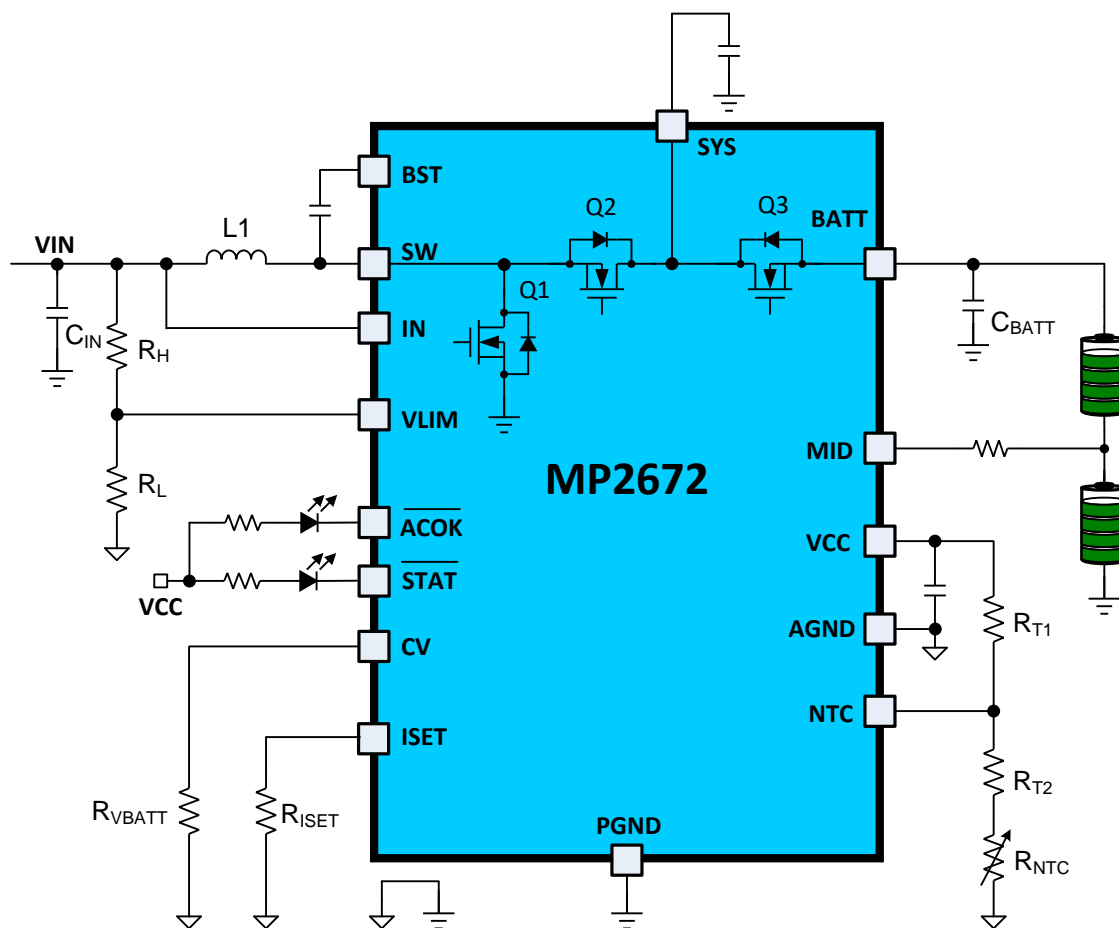- E-Cigarettes
- General 2-Cell Applications

TYPICAL APPLICATION

Standalone Mode:

Connect the CV pin to AGND via a resistor. Set the battery-full voltage according to Table 1.

Table 1: Battery Voltage Settings

R_{VBATT} Range	V_{BATT_REG}
30kΩ to 35kΩ	8.4V
70kΩ to 75kΩ	8.6V
100kΩ to 105kΩ	8.7V
130kΩ to 135kΩ	8.8V

TYPICAL APPLICATION

Host Control Mode

Connect the CV pin to VCC. Set the battery-full voltage according to the register.
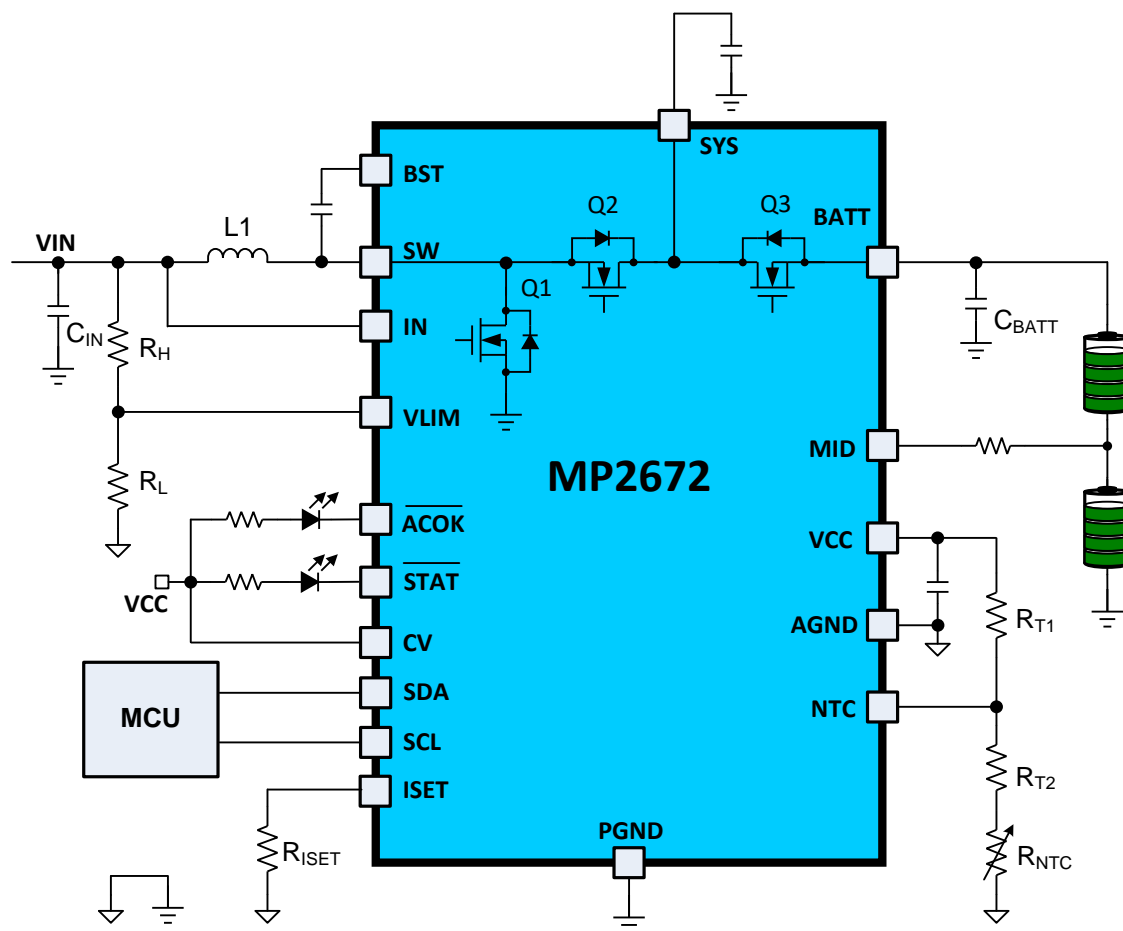
ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2672GD-xxxx**	QFN-18 (2mmx3mm)	*See Below*	1
EVKT-MP2672	Evaluation kit		

*For Tape & Reel, add suffix –Z (e.g. MP2672GD–xxxx-Z).

**"xxxx" is the register setting option. The factory default is "0000". This content can be viewed in the I^{2}C Register Map section on page 28. For customer options, contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

‾‾‾
BHA
YWW
LLL

BHA: Product code
Y: Year code
WW: Week code
LLL: Lot number

EVALUATION KIT EVKT-MP2672

EVKT-MP2672 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2672-D-01A	MP2672 evaluation board	1
2	EVKT-USBI2C-02-bag	Includes one USB to I^{2}C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

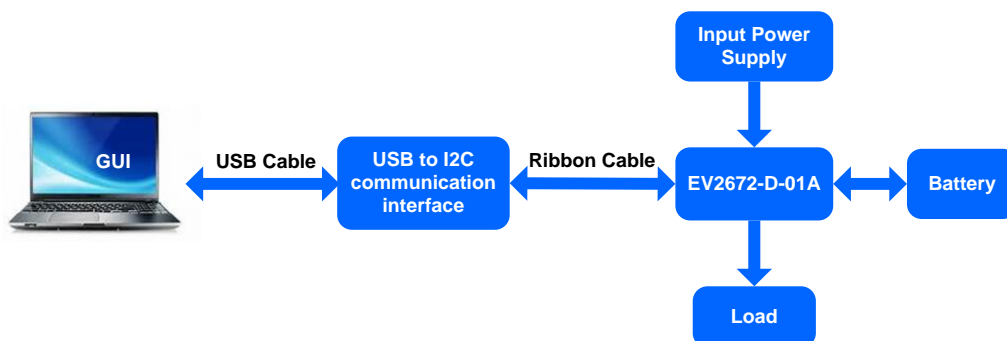**Order direct from MonolithicPower.com or our distributors.**

Figure 1: EVKT-MP2672 Evaluation Kit Set-Up

PACKAGE REFERENCE

Pin	Name
18	ACOK
17	CV
16	STAT
15	SDA
14	SCL
1	IN
2	SW
3	BST
4	VCC
13	PGND
12	SW
11	SYS
10	BATT
5	ISET
6	AGND
7	VLIM
8	NTC
9	MID

QFN-18 (2mmx3mm)
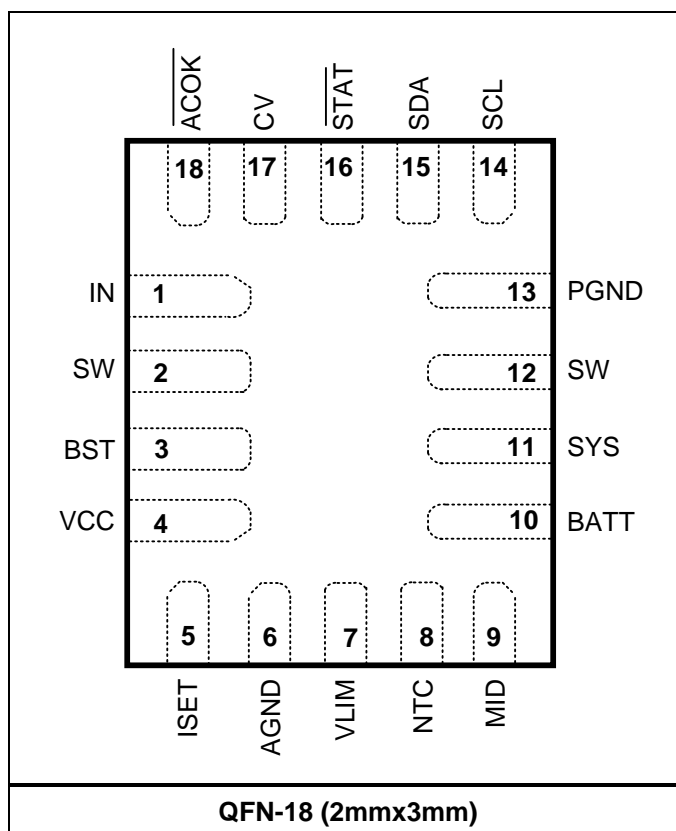
PIN FUNCTIONS

Pin #	Name	Type[1]	Description
1	IN	Power	**Input power pin.**
2, 12	SW	Power	**Switching node.** Middle point of the high-side and low-side FET of the boost.
3	BST	Power	**Bootstrap.** Connect a bootstrap capacitor between BST and SW to provide a floating supply to the high-side FET driver.
4	VCC	Power	**Internal LDO output pin.** Bypass a 1µF ceramic capacitor from this pin to AGND. It is recommended to pull no more than 20mA current from this pin.
5	ISET	AI	**Charge current set.** Connect an external resistor to AGND to program the charge current, which also limits the maximum charge current in host control mode.
6	AGND	Power	**Analog ground.**
7	VLIM	AI	**Input voltage limit feedback pin.** Connect a voltage divider from IN to AGND to program the minimum input voltage limit threshold.
8	NTC	AI	**Battery temperature sense input.** See the NTC protection details on page 23.
9	MID	Power	**Middle point of the high-side and low-side cells.** Used to measure the voltage and provide a balance path for each cell. Connect MID to AGND to disable the cell balance function.
10	BATT	Power	**Battery positive terminal.** Connect the capacitor from BATT to PGND as close as possible to the IC.
11	SYS	Power	**System output.** Connect the capacitor from SYS to PGND as close as possible to the IC.
13	PGND	Power	**Power ground.**
14	SCL	DI	**I²C interface clock pin.** Only valid if the CV pin is connected to VCC.
15	SDA	DIO	**I²C interface data pin.** Only valid if the CV pin is connected to VCC.
16	$\overline{\text{STAT}}$	DO	**Charging operation indicator.** Open-drain output. It can also be used as INT in host control mode.
17	CV	AI	**Operation mode and battery voltage control pin.** Pull CV to VCC to configure the IC to host control mode. Connect an external resistor to AGND to configure the IC to standalone mode and program the battery-full voltage via the resistor value.
18	$\overline{\text{ACOK}}$	DO	**Valid input supply indicator.** Open-drain output. Pulled to low when the input voltage is greater than V_{IN_UVLO} and below V_{IN_OVLO}.

Note:
1) AI = Analog input, DI = Digital input, DO = Digital output, DIO = Digital input output, P = Power

ABSOLUTE MAXIMUM RATINGS [2]

BATT, SYS, IN .... -0.3V to +14V
SW .... -0.3V (-2V for 50ns) to +14V
MID .... -0.3V to +12V
BST to SW…………….................... -0.3V to +5V
All other pins to GND .... -0.3V to +5V
Continuous power dissipation .... (T_A = 25°C) [3]
.... 1.78W
Junction temperature .... 150°C
Lead temperature (solder) .... 260°C
Storage temperature…. .... -65°C to +150°C

Recommended Operating Conditions [4]

IN to GND…………………………. ..4V to 5.75V
BATT to GND...................................... Up to 9V
I_{CC}... Up to 2A
I_{DSCHG}.. Up to 3A
I_{SYS} .... Up to 2A
Operating junction temp (T_J) .... -40°C to +125°C

ESD Rating

Human body model (HBM)[5] 2000V
Charged device model (CDM)[6] 250V

Thermal Resistance [7] θ_{JA} θ_{JC}

QFN-18 (2mmx3mm).............. 70 ...... 15... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Per ANSI/ESDA/JEDEC JS-001.
6) Per JESD22-C101.
7) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
Input over-voltage lockout threshold	V_{IN_OVLO}	V_{IN} rising	5.75	6.0	6.25	V
Input over-voltage lockout threshold hysteresis				150		mV
Input under-voltage lockout threshold	V_{IN_UVLO}	V_{IN} falling	3.25	3.45	3.65	V
Input under-voltage lockout threshold hysteresis				150		mV
Boost Converter						
VCC LDO output	V_{VCC}	V_{IN} = 5V, I_{VCC} = 20mA	3.5	3.6	3.7	V
Low-side NFET on resistance	R_{ON_Q1}			54	70	mΩ
High-side NFET on resistance	R_{ON_Q2}			28	40	mΩ
Peak current limit for low-side NFET	I_{LS_PK}	Boost mode	6	7		A
Valley current limit for high-side NFET	I_{HS_VL}	Boost mode	5	6		A
Operating frequency	f_{SW}	REG07H bit [7] = 1	1100	1270	1440	kHz
System regulation minimum voltage (V_{BATT_PRE} + V_{TRACK})		REG00H bit [3:1] = 100, V_{BATT} = 5V	6.55	6.7	6.85	V
Battery track regulation voltage	V_{TRACK}			300		mV
Battery Charger						
Pre-charge threshold	V_{BATT_PRE}	REG00H bit [3:1] = 000	5.9	6.05	6.2	V
		REG00H bit [3:1] = 100	6.25	6.4	6.55	
		REG00H bit [3:1] = 111	6.6	6.75	6.9	
Pre-charge threshold hysteresis		V_{BATT} falling		250		mV
Pre-charge current	I_{PRE}	V_{BATT} = 5.9V	230	300	370	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Fast charge current	I_{CC}	REG01H bit [3:0] = 0101, R_{ISET} = 6kΩ	0.9	1	1.1	A
		REG01H bit [3:0] = 1111, R_{ISET} = 6kΩ	1.8	2	2.2	A
Termination charge current	I_{TERM}	If I_{CC} > 1.5A, as the percentage of I_{CC}	8	11	14	%
		If I_{CC} ≤ 1.5A (setting)	130	160	190	mA
Input minimum voltage regulation reference	$V_{IN\_MIN\_REF}$		1.18	1.2	1.22	V
Battery charge voltage regulation	$V_{BATT\_REG\_ACC}$	V_{BATT_REG} = 8.3V, host control mode, REG00H bit [7:5] = 000	-0.5		+0.5	%
		V_{BATT_REG} = 8.4V, host control mode, REG00H bit [7:5] = 001, standalone mode, R_{VBATT} = 30kΩ				
		V_{BATT_REG} = 8.8V, host control mode, REG00H bit [7:5] = 101, standalone mode, R_{VBATT} = 135kΩ				
		V_{BATT_REG} = 9.0V, host control mode, REG00H bit [7:5] = 111				
Recharge threshold below V_{BATT_REG}	V_{RECH}			450		mV
Battery pack over-voltage protection threshold	V_{BATT_OVP}	As the percentage of the V_{BATT_REG}	102	104	105	%
Battery pack over-voltage protection hysteresis		REG00H bit [0] = 0		150		mV
SYS to BATT NFET on resistance	R_{ON_Q3}			31	40	mΩ
Battery quiescent current	I_{BATT_Q}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 8.4V, system no load		31	42	µA
ACOK, STAT, pin output low voltage		Sinking 1.5mA			400	mV
ACOK, STAT, pin leakage current		Connected to 5V			1	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

| Parameter	Symbol	Condition	Min	Typ	Max	Units
Termination deglitch time	t_{TERM_DGL}			180		ms
Recharge deglitch time	t_{RECH_DGL}			180		ms
Battery Temperature Monitoring (JEITA)						
NTC low temp rising threshold	V_{COLD}	As percentage of V_{CC}	70	71	72	%
NTC low temp rising threshold hysteresis		As percentage of V_{CC}		2.4		%
NTC cool temp rising threshold	V_{COOL}	As percentage of V_{CC}	62	63	64	%
NTC cool temp rising threshold hysteresis		As percentage of V_{CC}		2.2		%
NTC warm temp falling threshold	V_{WARM}	As percentage of V_{CC}	39.4	40.4	41.4	%
NTC warm temp falling threshold hysteresis		As percentage of V_{CC}		2.5		%
NTC hot temp falling threshold	V_{HOT}	As percentage of V_{CC}	33.5	34.5	35.5	%
NTC hot temp falling threshold hysteresis		As percentage of V_{CC}		2.5		%
Thermal Regulation and Protection						
Thermal shutdown temperature	T_{J_SHDN}	Rising threshold		150		°C
Thermal shutdown hysteresis		Temperature falling		20		°C
Cell Balance Function						
Internal balance FET on resistance	R_{ON_BHS}			2.1		Ω
	R_{ON_BLS}			1.3		Ω
Cell balance start voltage threshold	V_{CELL_BAL}	I^{2}C programmable, REG01H bit [6] = 0	3.35	3.5	3.65	V
Cell voltage high to low cell mismatch threshold	$V_{CELL\_DIFF\_HTL}$	REG01H bit [5] = 0		50	70	mV
Cell voltage high to low cell mismatch threshold hysteresis				52		mV
Cell voltage low to high cell mismatch threshold	$V_{CELL\_DIFF\_LTH}$	REG01H bit [4] = 0		50	70	mV
Cell voltage low to high cell mismatch threshold hysteresis				58		mV
HS_cell over-voltage protection threshold	V_{HCELL_OVP}	As percentage of the battery full voltage	101	103.5	104.5	%
LS_cell over-voltage protection threshold	V_{LCELL_OVP}	As percentage of the battery full voltage	102	103.9	104.8	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Communication Interface						
Input high threshold level	V_{IH}	$V_{PULL\ UP}$ = 1.8V	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Timing Characteristic						
Clock frequency	f_{CLK}			131		kHz
Watchdog timer	t_{WTD}	REG02H bit [5:4] = 01		40		s
Safety charge timer	t_{TMR}	I²C programmable, REG02H bit [2:1] = 11	16	20		hours
Pre-charge timer				1		hours

TYPICAL CHARACTERISTICS

I_{PRE} vs. Temperature
V_{BATT} = 5V
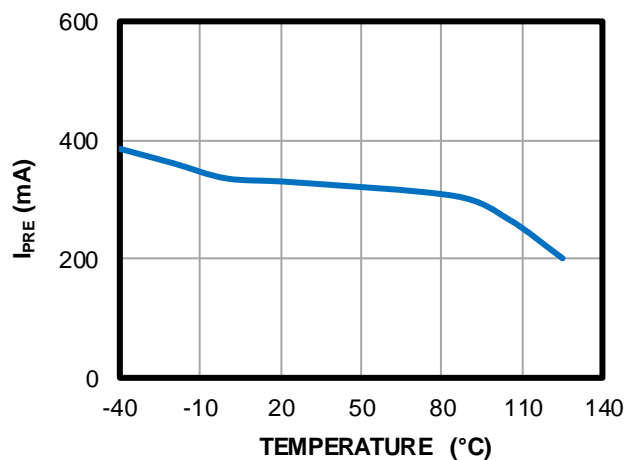
I_{CC} vs. Temperature
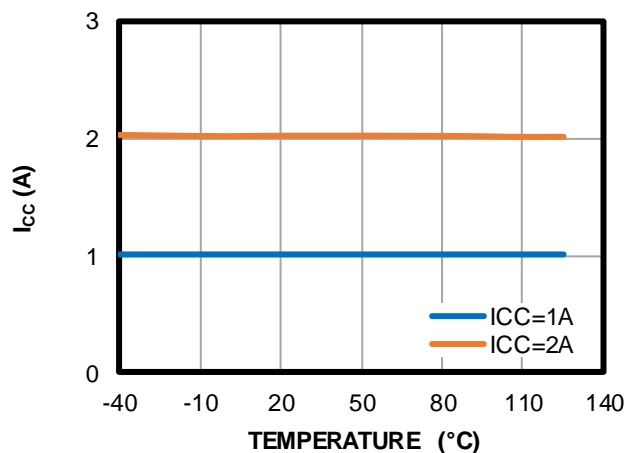
I_{TERM} vs. Temperature
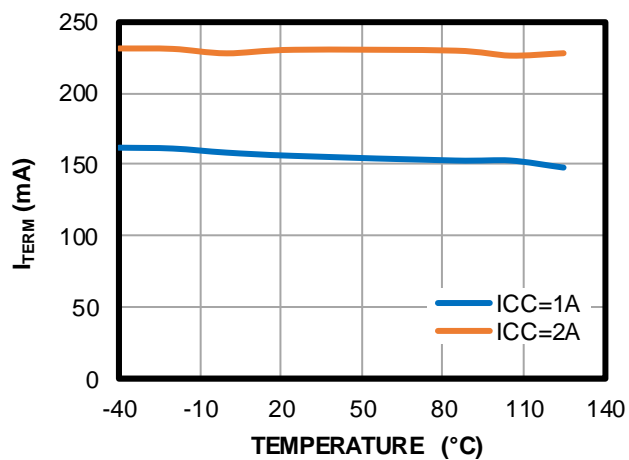
V_{BATT_REG} (8.4V) vs. Temperature
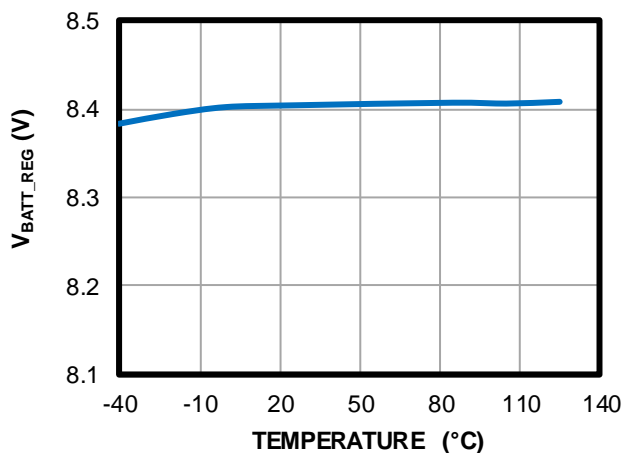
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

CC Charge Efficiency
V_{IN} = 5V, f_{SW} = 1200kHz, L = 1.5µH
(DCR = 10mΩ), I_{SYS} = 0A
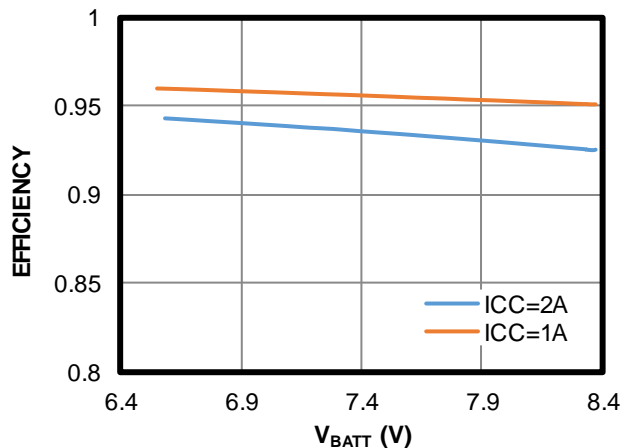
CV Charge Efficiency
V_{IN} = 5V, f_{SW} = 1200kHz, L = 1.5µH
(DCR = 10mΩ), V_{BATT} = 8.4V, I_{SYS} = 0A
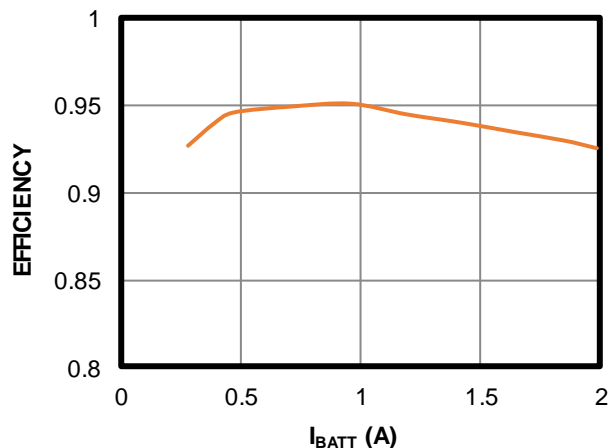
**Programmable Charge Current
Standalone Mode**
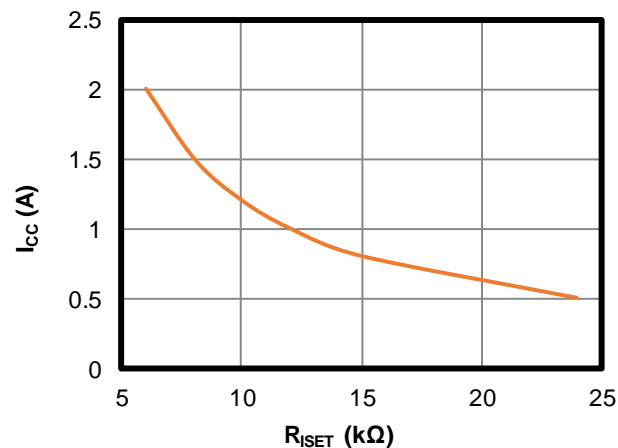
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT_PRE} = 6.4V, I_{CC} = 2A, I_{SYS} = 0A, V_{BATT} = 0V to 8.4V, C_{IN} = 10µF, C_{SYS} = 44µF, C_{BATT} = 22µF, L = 1.5µH, f_{SW} = 1200kHz, temp = 25°C, unless otherwise noted.

Battery Charge Curve
V_{BATT_REG} = 8.4V

CH2: V_{SYS}
2V/div.

CH1: V_{BATT}
2V/div.

CH4: I_{BATT}
500mA/div.

CH3: $\overline{STAT}$
2V/div.

4s/div.
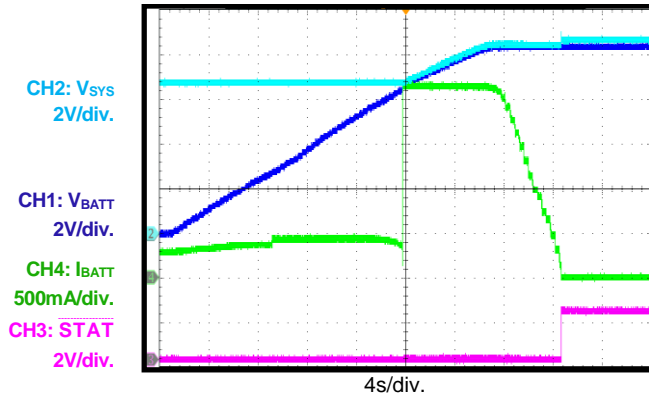
Auto-Recharge
V_{BATT_REG} = 8.4V
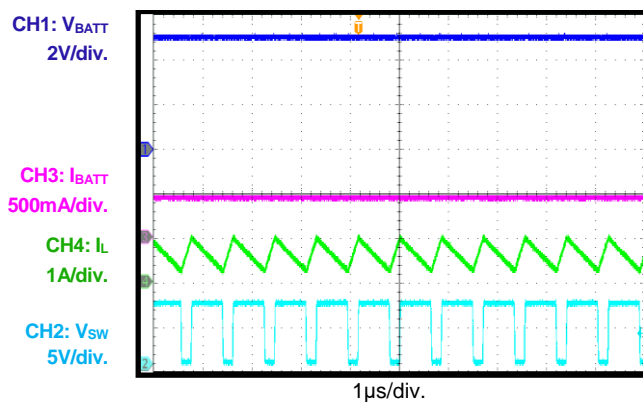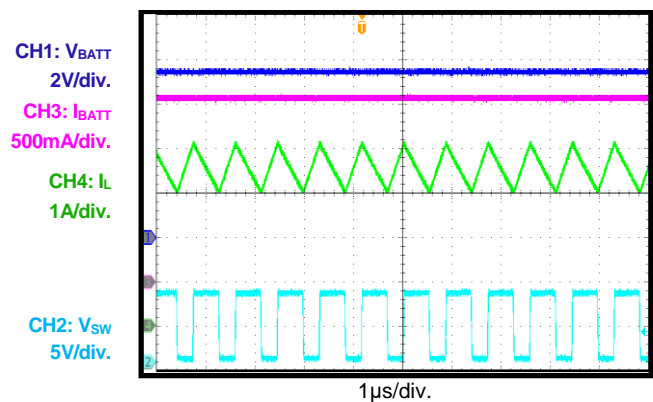
CH2: V_{SYS}
2V/div.

CH1: V_{BATT}
2V/div.

CH4: I_{BATT}
500mA/div.

CH3: $\overline{STAT}$
2V/div.

2s/div.

TC Charge Steady
V_{BATT} = 5V

CH1: V_{BATT}
2V/div.

CH3: I_{BATT}
500mA/div.

CH4: I_L
1A/div.

CH2: V_{SW}
5V/div.

1µs/div.

CC Charge Steady
V_{BATT} = 7.4V

CH1: V_{BATT}
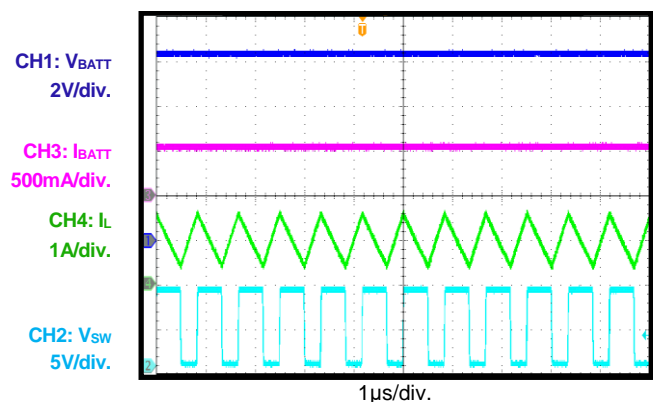2V/div.
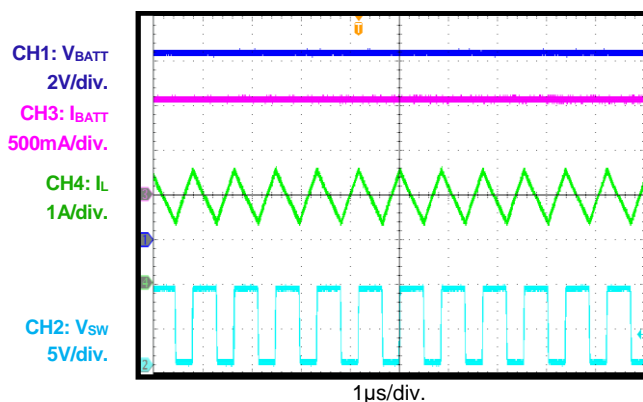
CH3: I_{BATT}
500mA/div.

CH4: I_L
1A/div.

CH2: V_{SW}
5V/div.

1µs/div.

CV Charge Steady
V_{BATT} = 8.4V (1A)

CH1: V_{BATT}
2V/div.

CH3: I_{BATT}
500mA/div.

CH4: I_L
1A/div.

CH2: V_{SW}
5V/div.

1µs/div.

CV Charge Steady
V_{BATT} = 8.4V (0.5A)

CH1: V_{BATT}
2V/div.

CH3: I_{BATT}
500mA/div.

CH4: I_L
1A/div.

CH2: V_{SW}
5V/div.

1µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT_PRE} = 6.4V, I_{CC} = 2A, I_{SYS} = 0A, V_{BATT} = 0V to 8.4V, C_{IN} = 10µF, C_{SYS} = 44µF, C_{BATT} = 22µF, L = 1.5µH, f_{SW} = 1200kHz, temp = 25°C, unless otherwise noted.

VIN Power On
V_{BATT} = 7.4V

VIN Power Off
V_{BATT} = 7.4V

Boost Enable
V_{BATT} = 7.4V

Boost Disable
V_{BATT} = 7.4V

CC Charge Enable
V_{BATT} = 7.4V

CC Charge Disable
V_{BATT} = 7.4V
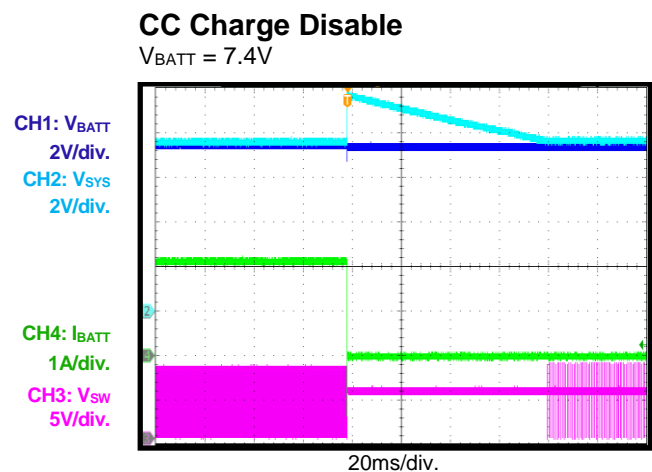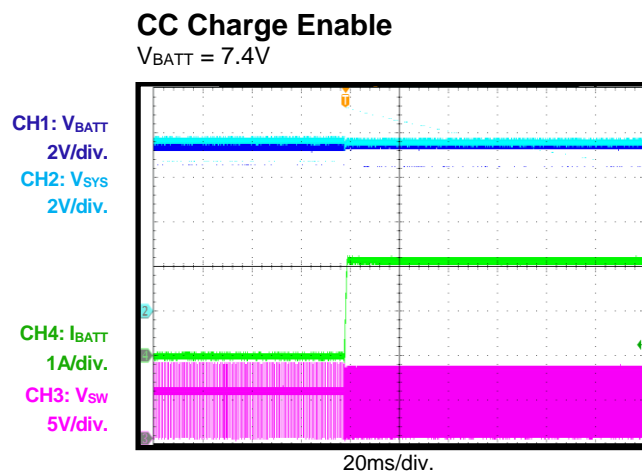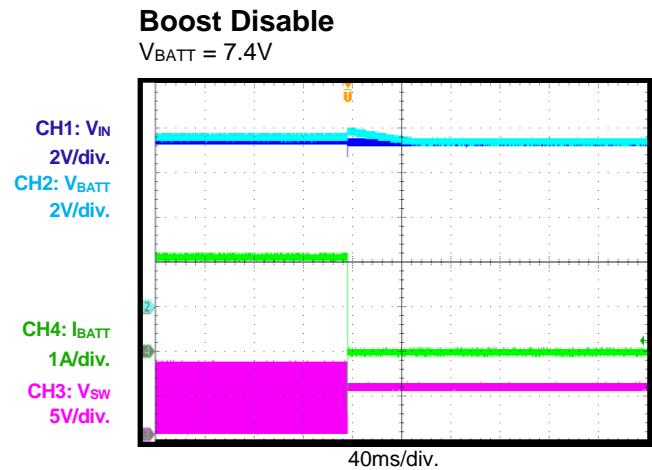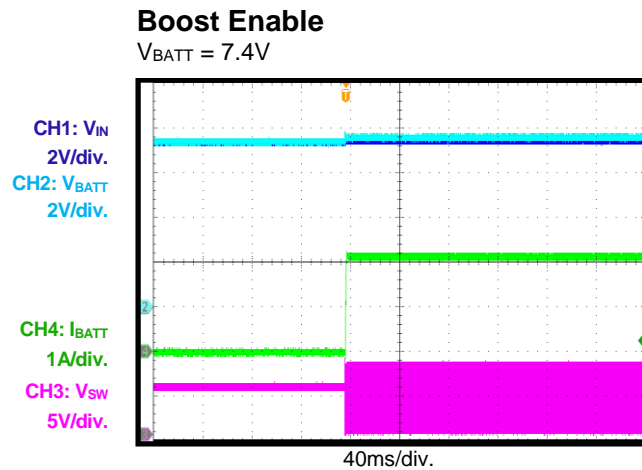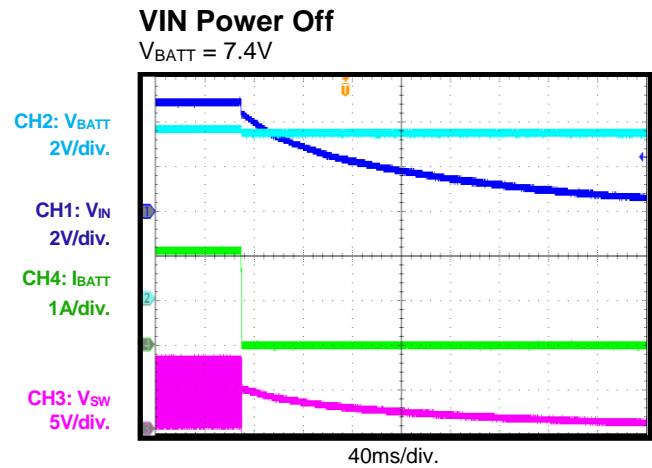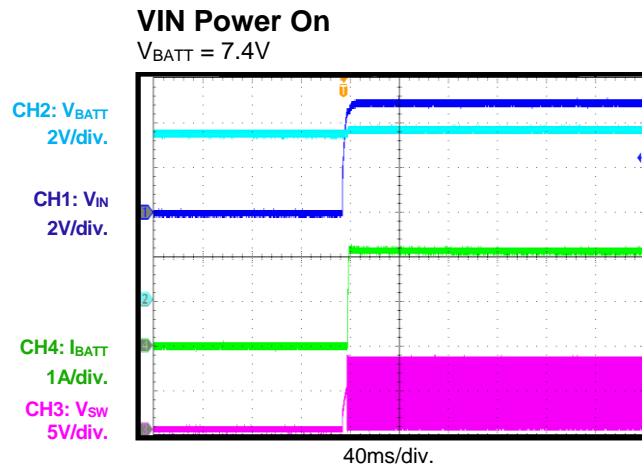
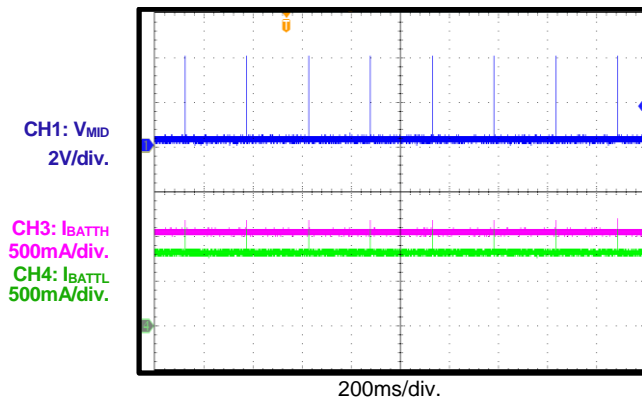# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 0V to 8.4V, C_{IN} = 10µF, C_{SYS} = 44µF, C_{BATT} = 22µF, f_{SW} = 1200kHz, temp = 25°C, unless otherwise noted.

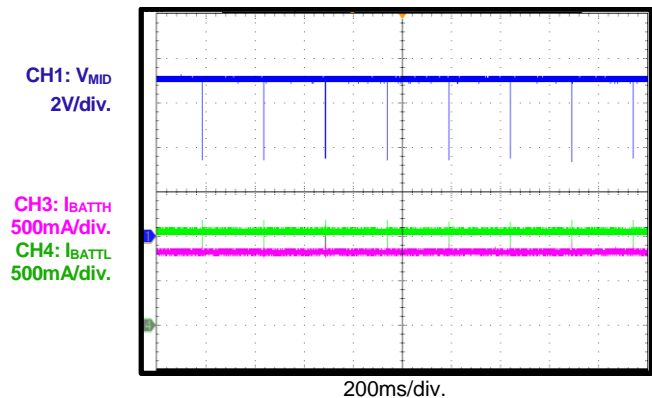**LS Cell Balance**

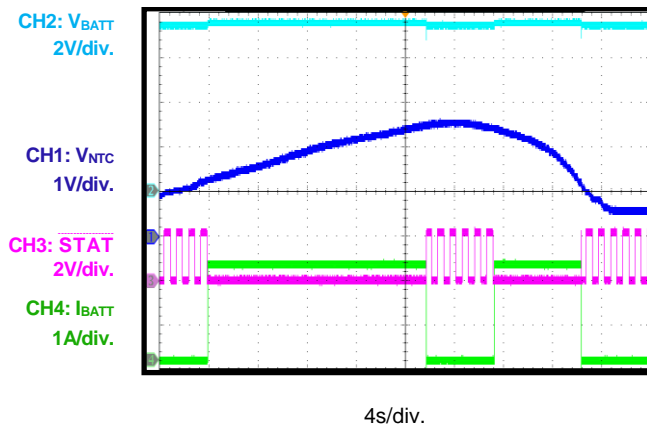I_{CC} = 1A, I_{SYS} = 0A, HS cell is 3.6V and LS cell is 3.8V, enable balance, balance resistor is 17mΩ

CH1: V_{MID}
2V/div.

CH3: I_{BATTH}
500mA/div.
CH4: I_{BATTL}
500mA/div.

200ms/div.

HS Cell Balance

I_{CC} = 1A, I_{SYS} = 0A, HS cell is 3.8V and LS cell 3.6V, enable balance, balance resistor is 17mΩ

CH1: V_{MID}
2V/div.

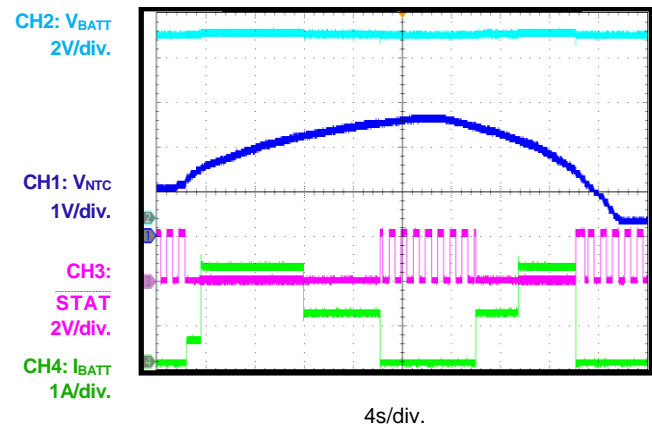CH3: I_{BATTH}
500mA/div.
CH4: I_{BATTL}
500mA/div.

200ms/div.

Standard NTC Protection

V_{BATT} = 7.4V, standard NTC, I_{CC} = 2A, vary V_{NTC}

CH2: V_{BATT}
2V/div.

CH1: V_{NTC}
1V/div.

CH3: $\overline{STAT}$
2V/div.
CH4: I_{BATT}
1A/div.

4s/div.

JEITA NTC Protection

V_{BATT} = 8.15V, JEITA NTC, I_{CC} = 2A, vary V_{NTC}

CH2: V_{BATT}
2V/div.

CH1: V_{NTC}
1V/div.

CH3:
$\overline{STAT}$
2V/div.

CH4: I_{BATT}
1A/div.

4s/div.

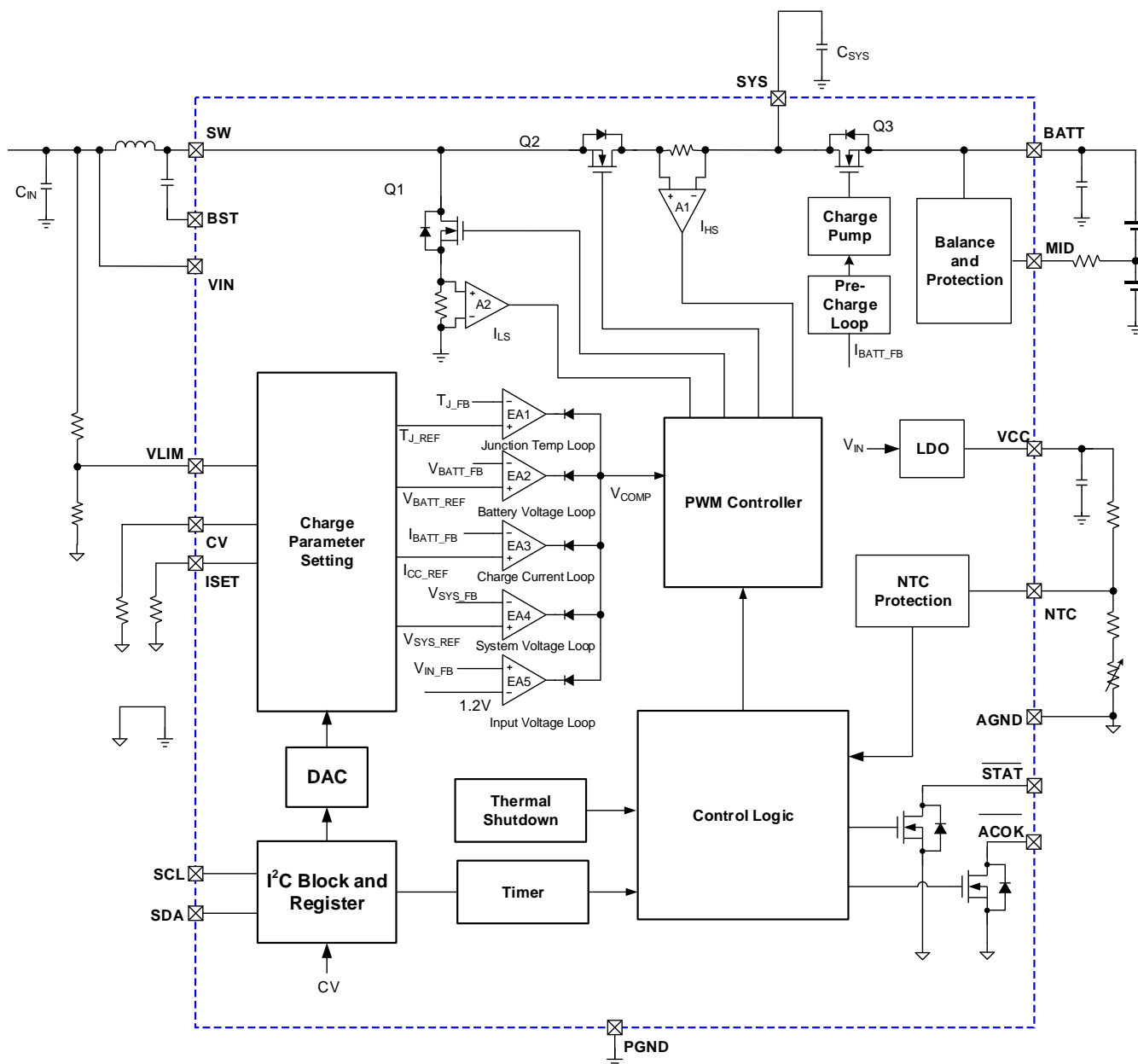# FUNCTIONAL BLOCK DIAGRAM

Figure 2: Functional Block Diagram

OPERATION

The MP2672 is a highly integrated, switch-mode battery charger to charge Lithium-ion battery with two cells in series from a 5V input power supply, which could be an adapter or USB input.

Host Control Mode and Standalone Mode

The MP2672 can operate in either host control mode or standalone mode. After input power-on, the MP2672 checks the CV status first.

*   If CV is pulled up to logic high, the MP2672 works in host control mode

*   If CV is connected to ground through a resistor, the MP2672 works in standalone mode

In host control mode, charging parameters can be programmed by the I²C registers. In standalone mode, V_{BATT_REG} and I_{CC} can be set by hardware pins.

Table 2: Host Control Mode and Standalone Mode

CV Pin	Mode	V_{BATT_REG}	I_{CC}
Connect resistor to AGND	Standalone	Set by CV resistor	Set by ISET resistor
Pull up to VCC	Host control	Set by I²C register	Set by I²C register*

*Note: Maximum charge current is limited by the ISET setting.

Internal Power Supply

The VCC LDO is powered by the input power supply, and is used to power the internal circuit and MOSFET driver. When the input is absent, the VCC LDO is off. An external capacitor is required to be connected from VCC pin to AGND. The VCC output is regulated at 3.6V typically when V_{IN} is 5V. When the V_{IN} is lower than 3.6V, the LDO enters into dropout state and the LDO FET is fully turned on. The VCC output is not able to carry a current load greater than 20mA.

Input Voltage vs. System Voltage Limitation

To avoid the MP2672 entering open-loop operation due to the minimum on time of the low-side FET, the boost converter turns off when $V_{SYS} < 1.1 * V_{IN}$. It restarts, then checks the input voltage and system voltage again. The boost turns off again after a 1ms soft-start time if V_{SYS} is still below $1.1 * V_{IN}$.

As a result, it is recommended to choose V_{BATT_PRE} and V_{TRACK} to ensure that the minimum output voltage of boost is greater than 1.1 times the maximum DC input voltage.

Input Power Start-Up

When the input voltage is below V_{IN_UVLO}, SYS is powered by the battery via Q3, which is fully turned on at this time. When the input power is connected, Q3 exits fully on mode and enters virtual diode mode once V_{IN} exceeds V_{IN_UVLO}. At the same time, the boost starts up with a soft start of the system voltage loop. When the system voltage rises to about 20mV higher than the battery voltage, Q3 is turned off. It turns on again with a soft start of charge current after system voltage soft start completes.

NVDC Power Structure

The MP2672 employs a narrow VDC (NVDC) power structure, which is composed of a front-end boost converter and a rear-end battery FET between SYS and BATT pins. This allows for separate control between the system and the battery. The system is given the priority to start up even with a deeply discharged or missing battery. Therefore, when the input power is available and a depleted battery is connected, the system voltage is regulated at the minimum system voltage V_{SYS_MIN}, which is set by I²C register REG00 bit [3:1].

Figure 3 shows the system voltage control:

(1) When the battery voltage is below V_{BATT_PRE}, the system voltage is regulated at $V_{SYS\_REG\_MIN} = V_{BATT\_PRE} + V_{TRACK}$, and the battery FET works linearly to charge the battery with pre-charge current.

(2) When the battery voltage is above V_{BATT_PRE}, the battery FET is fully turned on and the system voltage is always $I_{BATT} * R_{ON\_Q3}$ higher than the battery voltage. Once battery charging is completed, the system output (V_{SYS}) is regulated to $V_{BATT} + V_{TRACK}$.
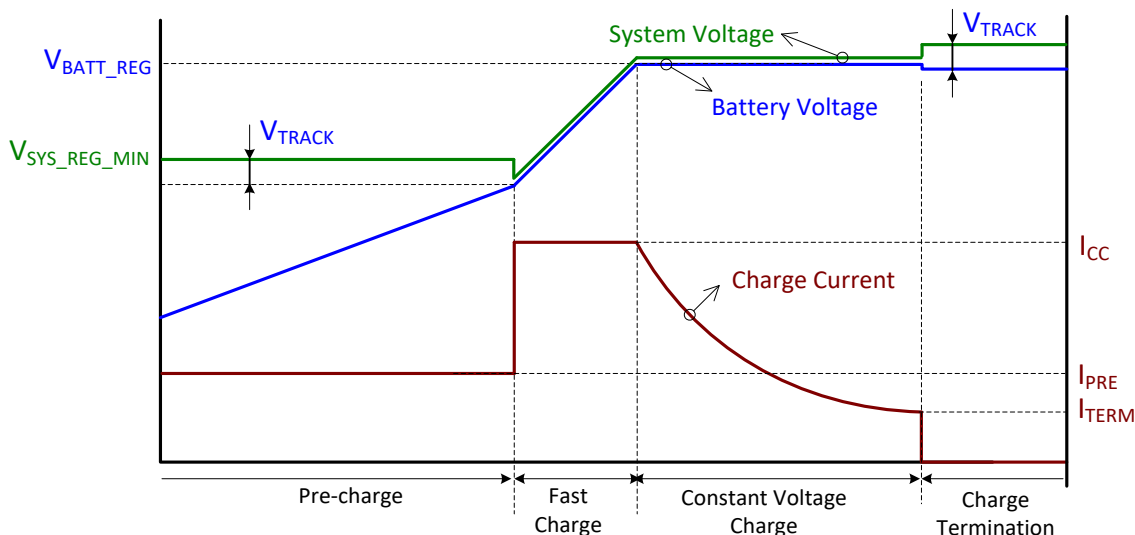
Figure 4: Battery Charge Profile

(3) When charging is disabled, REG00H bit [4] = 0, V_{SYS} is also regulated to V_{TRACK} higher than real battery voltage.
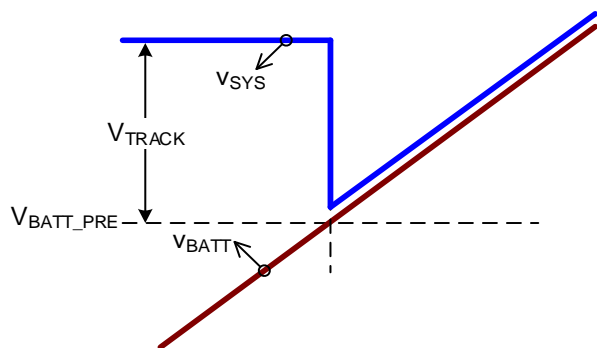

Figure 3: V$_{SYS}$ Variation with V$_{BATT}$

Battery Charge Profile

The MP2672 provides three main charging phases: pre-charge, constant-current charge and constant-voltage charge (see Figure 4).

Phase 1 (Pre-Charge)

When the battery voltage is below V_{BATT_PRE}, the MP2672 regulates the system voltage at $V_{SYS\_REG\_MIN}$ and applies a safe pre-charge current I_{PRE} to charge the deeply depleted battery until the battery voltage reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer (60mins) expires, the charge cycle ceases and a corresponding timeout fault signal is asserted.

### *Phase 2 (Constant-Current Charge)*

When the battery voltage exceeds V_{BATT_PRE}, the MP2672 stops the pre-charge phase and enters the fast charge phase. The fast charge current can be programmed via the ISET pin in standalone mode or I^{2}C register in host control mode.

Phase 3 (Constant-Voltage Charge)

As depicted in Figure 5, when the battery voltage rises to the battery regulation voltage V_{BATT_REG}, the charge current begins to decrease. The charge cycle is considered complete when the CV loop is dominant and the charge current drops below the charge termination current threshold for a 200ms deglitch time. This 200ms deglitch time is also designed for starting each charge cycle; after 200ms expires, the charge full signal is allowed to assert if termination conditions are met.
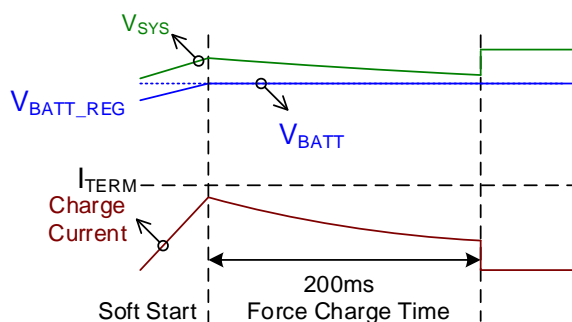
(a) Force Charge Time
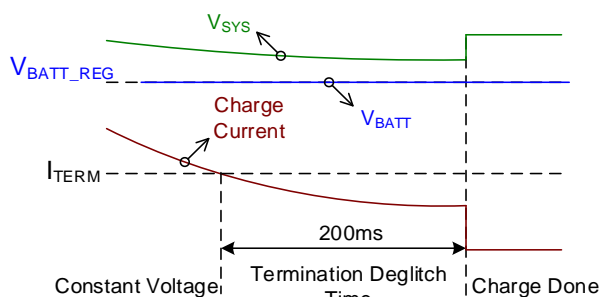
(b) Termination Deglitch Time
Figure 5: Force Charge Time and Termination Deglitch Time

If I_{TERM} is not reached before the safety charge timer expires (see the Safety Timer section on page 22), the charge cycle ceases and the corresponding timeout fault signal is asserted.

A new charge cycle starts when the following conditions are valid:

- The input power is re-plugged in
- Auto-recharge
- No thermistor fault at the NTC pin
- No safety timer fault
- No battery over-voltage
- No thermal shutdown

The charge termination can be disabled manually by pulling the NTC pin up to VCC.

Auto-Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged for system consumption or self-discharge (see Figure 6). The MP2672 automatically starts another new charging cycle without the requirement of manually restarting a charging cycle when the battery voltage drops below the recharge threshold for 200ms.
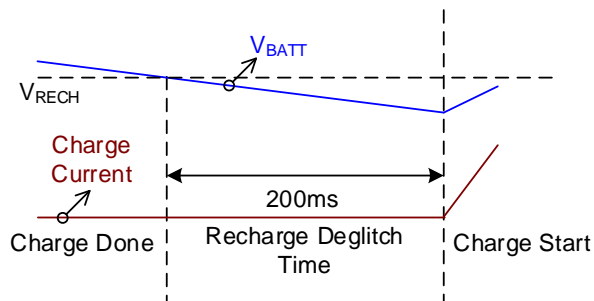

Figure 6: Recharge Profile

Charge Enable Default Setting

In case the battery is not expected to be charged frequently during high-SOC conditions, the MP2672 has an OTP option (REG05H bit[7]) to disable charging when the input power is on and the battery voltage is higher than the recharge voltage threshold. Charging is enabled until the battery voltage falls below the recharge threshold.

Battery-Full Voltage Setting

The MP2672 has a CV pin to program the battery regulation voltage.

When CV is pulled up to VCC, the MP2672 operates in host control mode. The battery regulation voltage is programmed through the I²C.

When CV is connected to AGND via a resistor, the MP2672 operates in standalone mode. The battery regulation voltage is set according to Table 3. Figure 7 shows the simplified diagram.

Table 3: V$_{BATT\_REG}$ vs. R$_{VBATT}$ Resistor

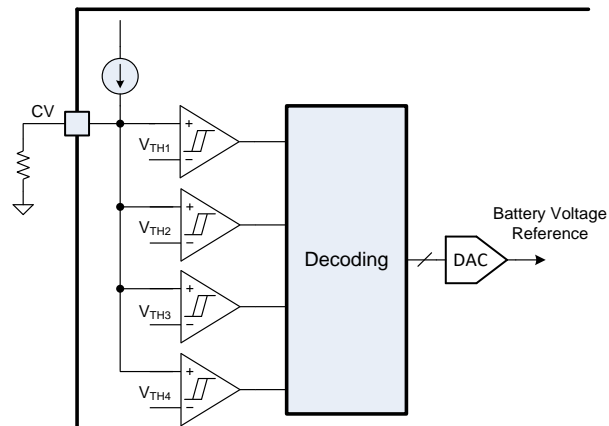| Resistor Range	V$_{BATT\_REG}$
30kΩ to 35kΩ	8.4V
70kΩ to 75kΩ	8.6V
100kΩ to 105kΩ	8.7V
130kΩ to 135kΩ	8.8V

Figure 7: Simplified Diagram of the V$_{BATT\_REG}$ Setting in Standalone Mode

Charge Current Setting

In standalone mode, the charge current is programmed via the ISET pin. Calculate the setting formula with Equation (1):

$$I_{CC} = \frac{12k\Omega}{R_{ISET}}(A) \qquad (1)$$

In host mode, the charge current can be programmed via REG01H bit [3:0] together with R_{ISET}. R_{ISET} determines the full-scale value of the register. For example, if R_{ISET} is 6kΩ, then the REG01H bit [3:0] programmable range is 500mA to 2000mA with 100mA per step. If R_{ISET} is 24kΩ, then the REG01H bit [3:0] programmable range is 125mA to 500mA with 25mA per step. R_{ISET} is recommended to be between 6kΩ and 24kΩ.

Minimum Input Voltage Limit

To avoid overloading the adapter, the MP2672 implements input voltage based power management by continuously monitoring the input voltage. When the minimum input voltage limit is reached, the charge current is reduced to prevent the input voltage from dropping further. The minimum input voltage limit can be programmed by a voltage divider on the VLIM pin.

The internal reference of the input voltage loop is 1.2V, and the minimum input voltage limit can be set with Equation (2):

$$V_{IN\_MIN} = 1.2 \times \frac{R_H + R_L}{R_L} \qquad (2)$$

Battery Supplement Mode and Virtual Diode Mode

When the minimum input voltage limit is reached, the charge current is reduced to keep the input voltage from dropping further. However, if the charge current is reduced to zero and the input source is still overloaded due to heavy system load, the system voltage will continue dropping.

Once the system voltage falls below the battery voltage, the MP2672 enters battery supplement mode. The battery starts to supplement the system load together with the boost converter. In supplement mode, the battery FET operates as a virtual diode.

When the system voltage falls 30mV below the battery voltage, the battery FET turns on, and its source-to-drain voltage is regulated at 24mV. As the battery discharge current rises, the virtual diode loop is saturated and the battery FET is fully turned on. The source-to-drain voltage is the discharge current times the on resistance of the battery FET.

Battery Missing Detection

The MP2672 is capable of detecting whether a battery is connected or not. The following conditions initiate battery missing detection:

- Charging is enabled
- Auto-recharge is triggered
- Recovery from any faults

If a battery absence is detected, 1Hz blinking on the $\overline{STAT}$ pin indicates that, BATTFLOAT_STAT is set at 1 in host control mode. Figure 8 shows the battery missing detection flowchart.

Battery Over-Voltage Protection

The MP2672 is designed with a built-in battery over-voltage protection threshold, which is 104% of V_{BATT_REG}. When a battery over-voltage event occurs, the MP2672 turns off the battery FET (Q3) and suspends charging. At this time, the boost converter continues operating and the system voltage tracks the battery voltage with additional V_{TRACK}.
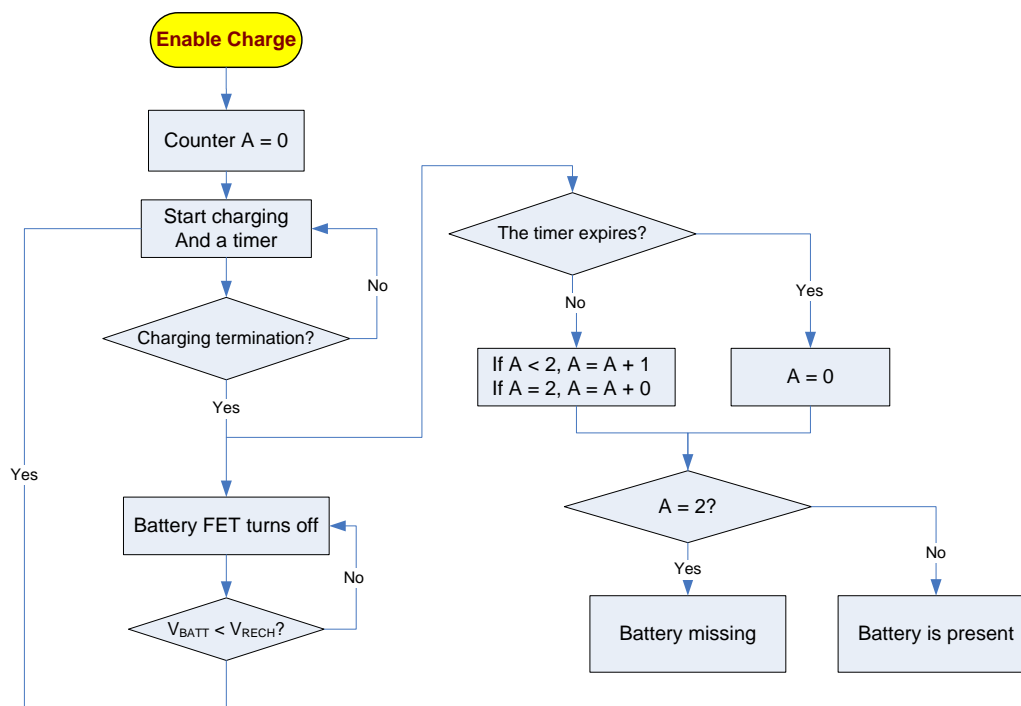
Figure 8: Battery Missing Detection Flowchart

When the balance function is enabled (the MID pin is not pulled down to AGND), the MP2672 also has a MID pin to monitor each cell's voltage. If any one of the cell voltages exceeds 104% of V_{BATT_REG} / 2, the MP2672 stops charging the battery.

Safety Timer

The MP2672 provides both pre-charge and fast charge cycle safety timers to avoid an extended charging cycle due to abnormal battery conditions. The safety timer for pre-charge is 60 minutes when the battery is below V_{BATT_PRE}. The fast charge cycle safety timer starts when the battery enters fast charge. The fast charge safety timer can be programmed by the I²C. This feature can also be disabled via the I²C.

The safety timer is reset at the beginning of a new charging cycle. It can also be reset by writing 0 and 1 sequentially to REG00H bit[4]. The following actions restart the safety timer:

- Beginning a new charge cycle

- Write REG00H bit 4 from 0 to 1 (charge enable)

- Write REG02H bit [2:1] from 00 to 01/10/11 (safety timer enable)

- Write REG02H bit [3] from 0 to 1 (software reset)

In the event of an NTC hot or cold fault, the charging timer is suspended. Once the NTC fault is removed, the timer continues to count from the value before the NTC fault.

Watchdog Timer

When the MP2672 operates in host control mode, a watchdog timer is provided to reset all the registers to their default values if the watchdog timer is not reset periodically. By doing this, the register values of the MP2672 go back to default when no action occurs on the I²C bus for a certain time. The watchdog timer duration can be programmed and disabled through the register.

NTC (Negative Temperature Coefficient) Thermistor

"Thermistor" is the generic name given to thermally sensitive resistors. An negative temperature coefficient (NTC) thermistor is generally called a thermistor. Depending on the manufacturing method and the structure, there are many shapes and characteristics for various purposes. The thermistor resistance values, unless otherwise specified, are classified at a standard temperature of 25°C. The resistance of a temperature is solely a function of its absolute temperature.

Refer to the datasheet of the thermistor for the mathematic expression that relates the resistance and the absolute temperature of the thermistor, or calculate it with Equation (3):

$$R_1 = R_2 \times e^{\beta \bullet \left(\frac{1}{T1} - \frac{1}{T2} \right)} \qquad (3)$$

Where R1 is the resistance at absolute temperature T1, R2 is the resistance at absolute temperature T2, and β is a constant that depends on the material of the thermistor.

The MP2672 continuously monitors the battery's temperature by measuring the voltage on the NTC pins. This voltage is determined by the voltage divider whose ratio is produced by different resistance of the NTC thermistor under a different ambient temperature of the battery.

The MP2672 internally sets a predetermined upper and lower bound of the range. If the voltage at the NTC pin goes out of the hot/cold threshold, the temperature is outside safe operating limits. At this time, charging ceases until the operating temperature returns to within the safe range.

To satisfy JEITA requirements, the MP2672 monitors four temperature thresholds: the cold battery threshold (e.g. $T_{NTC} < 0°C$), the cool battery threshold (e.g. $0°C < T_{NTC} < 10°C$), the warm battery threshold (e.g. $45°C < T_{NTC} < 60°C$), and the hot battery threshold (e.g. $T_{NTC} > 60°C$). For a given NTC thermistor, these temperatures correspond to V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}.

See Figure9, it is the typical JEITA operation when the battery temperature is in different temperature window.

1) When $V_{NTC} < V_{HOT}$ or $V_{NTC} > V_{COLD}$, charging is suspended and timers are suspended.

2) When $V_{HOT} < V_{NTC} < V_{WARM}$, the battery regulation voltage V_{BATT_REG} is reduced by 120mV/cell from the programmable threshold.

3) When $V_{COOL} < V_{NTC} < V_{COLD}$, the charging current is reduced to half of the programmable charge current.
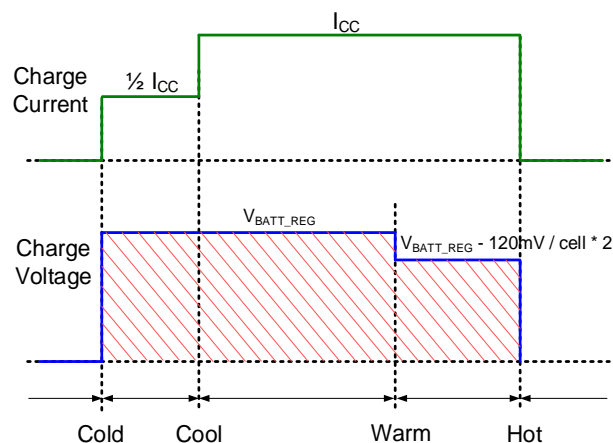
Figure 9: JEITA Compatible NTC Window

For a given thermistor, two of four temperature thresholds can be selected to calculate the values of R_{T1} and R_{T2}. See the Resistor Selection for the NTC Sensor on page 35.

Thermal Regulation and Thermal Shutdown

To guarantee safe operation, the MP2672 limits the die temperature. When the internal junction temperature reaches the preset threshold, the MP2672 starts to reduce the charge current to prevent higher power dissipation.

When $V_{BATT} > V_{BATT\_PRE}$, the die temperature limit is always set to 120°C. When $V_{BATT} < V_{BATT\_PRE}$, the die temperature limit has four options (60°C/80°C/100°C/120°C), which can be programmed by the OTP (one-time programmable) register, REG05H bit[4:3].

When the junction temperature reaches 150°C, the boost converter goes into shutdown mode.

Indications

The MP2672 has two open-drain pins ($\overline{ACOK}$ and $\overline{STAT}$) to indicate the input power and charging status. Table 4 shows the behavior for each of these indications.

Table 4: Indication in Different Cases

Charging State	$\overline{ACOK}$	$\overline{STAT}$
Charging	Low	Low
Charging complete, charging disabled	Low	Open drain
Charging suspended due to: • Battery OVP • Timer fault • NTC hot fault • NTC cold fault • Battery float	Low	1Hz Blinking
Thermal shutdown	Low	Open drain

Battery Cell Balance and Protection

The MP2672 provides battery cell balance and protection for dual-cell applications (see Figure 10). It is able to sense the voltage across each cell. If these two cell voltages mismatch by more than 50mV (typically), the internal discharge path is turned on to discharge the cell with the higher voltage until the two cell voltages mismatch by less than 30mV.

If battery OVP occurs before the two cells are equalized, charging is suspended.

The MP2672 integrates the balance path and control circuit. An external power dissipation resistor is also required to limit the balance current.

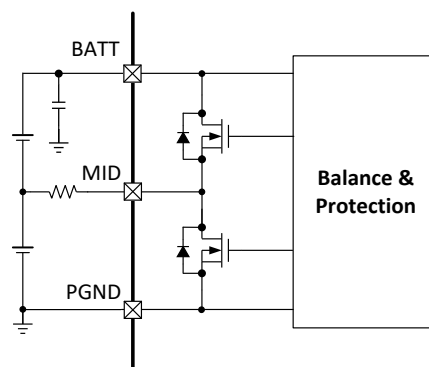If the cell balance function is not used, connect MID to PGND directly.

Figure 10: Block Diagram of the Battery Balance

Balancing Algorithm

Balance block only operates in charge mode. Balance starts when any cell voltage exceeds the balance start point (V_{CELL_BAL}).

The voltage difference between cells should be greater than V_{CELL_DIFF}. The MP2672 detects the cell voltages in the pack, then checks the voltage difference between two cells. If the differential voltage is greater than V_{CELL_DIFF}, the corresponding balance MOSFET turns on.

To measure the open-circuit voltage of the cell, balancing is frequently suspended for a short duration. Charging always operates independently of the balance algorithm if no other charge fault occurs. The cell voltage measurement works for 200μs when cell balance suspends, and then cell balance works for 249.8ms of each 250ms cycle (see Figure 11). Figure 12 shows the battery balance flowchart.
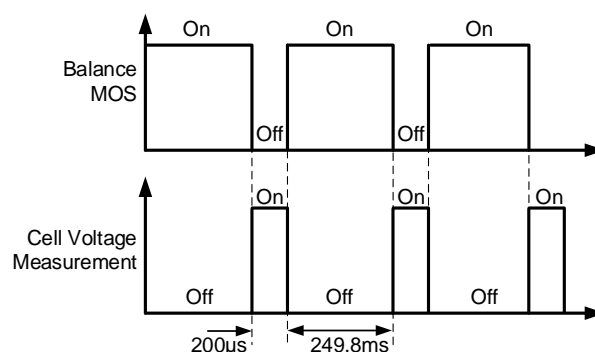

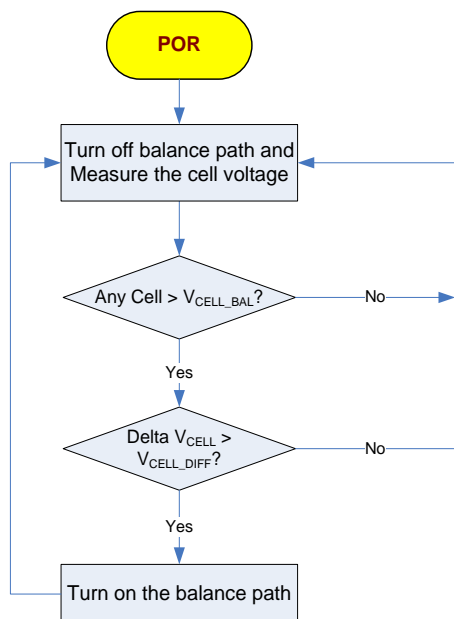
Figure 11: Battery Balance Clock

Figure 12: Flowchart of the Battery Balance

For extremely unbalanced dual-cell batteries, the charger takes a few cycles to make the two battery voltages balanced. For some applications, such as removable dual-cell batteries, a charger is required to balance dual cells in one charge cycle. In this case, an external cell balance circuit is recommended (see Figure 13).

The MP2672 also has an option to automatically disable termination if the cell balance is active. By doing this, the two cells are matched better when charging is terminated.

The cell voltage measured within the 200µs time is also delivered to the battery cell OVP block, and charging is suspended (the battery FET turns off) until the measured cell voltage drops below the recovery threshold, which is set by REG00H bit[0].

Suspend Mode

The MP2672 has a suspend mode to turn off the boost switcher even when the input is present. In this mode, the SYS pin is powered by the battery through the internal battery FET and the input quiescent current is optimized. The MP2672 enters this mode by setting REG02H bit [0] to 0.

Series Interface

The IC uses two wires: serial data (SDA) and serial clock (SCL). All I^2C master and slave devices are connected with only those two wires. The master, such as a microcontroller or a digital signal processor, generates the bus clock and initiates communication on the bus. The slaves receive and respond to the commands on the bus from the master device. In order to communicate with a specific device, each slave device must have a unique address on the bus.

The I^2C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). The SDA and SCL pins are open drain. Both SDA and SCL are connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are high. MP2672's SDA is a bidirectional line, but the SCL is a unidirection line.
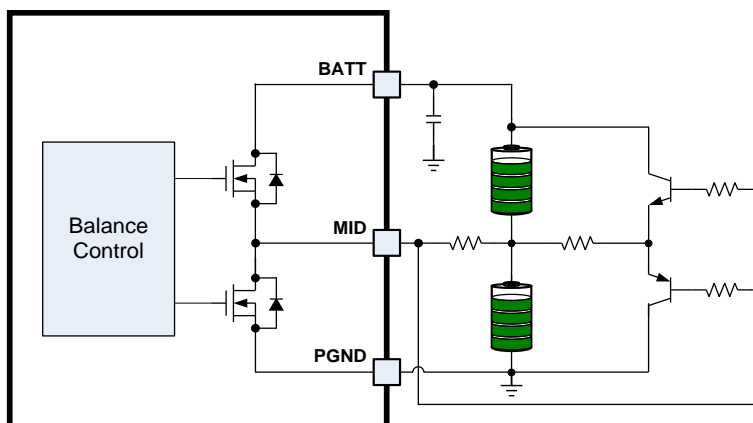

Figure 13: External Cell Balance Circuit

The data on the SDA line must be stable during the high period of the clock (see Figure 14). The high or low state of the data line can only change when the clock signal on the SCL line is low. One clock pulse is generated for each data bit transferred.
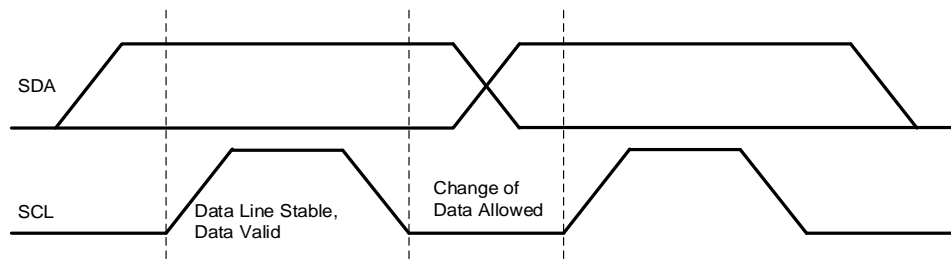

Figure 14: Bit Transfer on the I²C Bus

All the transactions begin with a start (S) and can be terminated by a stop (P). A high to low transition on the SDA line while SCL is HIGH defines a start condition. A low to high transition on the SDA line when the SCL is high defines a stop condition (see Figure 15). Start and stop conditions are always generated by the master. The bus is considered busy after the start condition, and free after the stop condition.
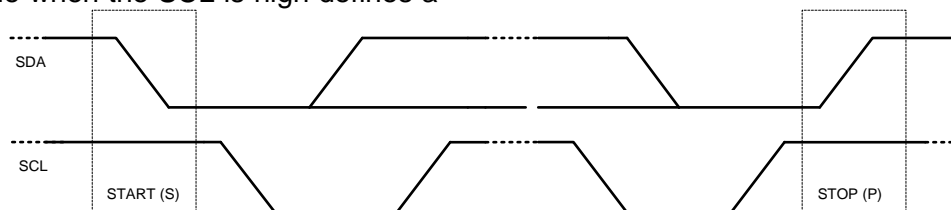

Figure 15: Start and Stop Conditions

Data on the I²C bus is transferred in 8-bit packets (bytes) (see Figure 16). Each byte has to be followed by an acknowledge bit (ACK). Data is transferred with the most significant bit (MSB) first.

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low, and it remains high during the 9th clock pulse. This is the not acknowledge (NACK) signal. The master can then generate either a stop to abort the transfer or a repeated start to begin a new transfer.

After the start, a slave address is sent. This address is 7 bits long followed by an 8th data direction bit (R/W). 0 indicates a transmission (write), and 1 indicates a request for data (read). Figure 17 shows the complete data transfer.

If the register address is not defined, the charger IC sends back NACK and returns to its idle state.
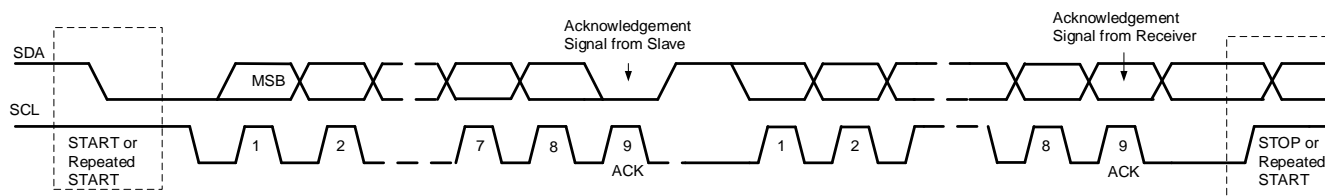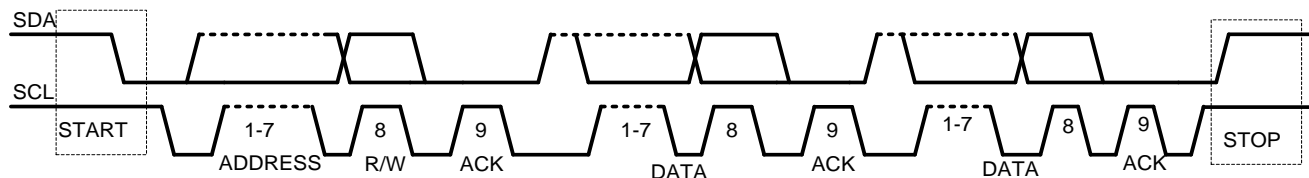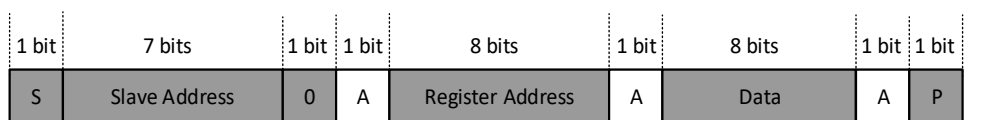
The MP2672 operates as a slave device with the address 4BH. The MP2672 supports single byte R/W (see Figure 18 and Figure 19).

Figure 16: Data Transfer on the I²C BUS

Figure 17: Complete Data Transfer

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit
S	Slave Address	0	A	Register Address	A	Data	A	P

From Master to Slave   From Slave to Master   A = Acknowledge (SDA LOW)   S = Start   P = Stop

Figure 18: Single Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit
S	Slave Address	0	A	Register Address	A	S	Slave Address	1	A	Data	/A	P

From Master to Slave   A = Acknowledge (SDA LOW)   S = Start
From Slave to Master   /A = not Acknowledge (SDA HIGH)   P = Stop

Figure 19: Single Read

I²C Register MAP

IC Address 4BH

Register Name	Address	R/W	Description	Default
REG00H	0x00	R/W	Battery regulation voltage, charge configuration, and SYS voltage setting	0011 1000
REG01H	0x01	R/W	Balance setting and charge current setting	1000 1111
REG02H	0x02	R/W	Timer setting	1001 0101
REG03H	0x03	R	Status register	0000 0000
REG04H	0x04	R	Fault register	0000 0000

REG 00H (Default: 0011 1000)

Bit	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Notes
7	V_{BATT_REG} [2]	0	Y	Y	R/W	000: 8.3V 001: 8.4V 010: 8.5V 011: 8.6V 100: 8.7V 101: 8.8V 110: 8.9V 111: 9.0V	**Battery Regulation Voltage** Default: (8.4V) OTP programmable
6	V_{BATT_REG} [1]	0	Y	Y	R/W		
5	V_{BATT_REG} [0]	1	Y	Y	R/W		
4	CHG CONFIG	1	Y	Y	R/W	0: Charge disabled 1: Charge enabled	Default: Charge enabled
3	V_{BATT_PRE} [2]	1	Y	N	R/W	0.4V	**System Minimum Voltage Offset** Offset: 6.0V Range: 6.0V to 6.7V Default: 6.4V This threshold is also used as the pre-charge battery voltage threshold. OTP programmable
2	V_{BATT_PRE} [1]	0	Y	N	R/W	0.2V	
1	V_{BATT_PRE} [0]	0	Y	N	R/W	0.1V	
0	CELL_OVP_HYS	0	Y	N	R/W	0: 80mV 1: 0mV	**Cell OVP Hysteresis**

REG 01H (Default: 1000 1111)

Bit	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Notes
7	NTC_TYPE	1	Y	Y	R/W	0: Standard 1: JEITA	Default: JEITA OTP programmable
6	V_{CELL_BAL}	0	Y	Y	R/W	0: 3.5V 1: 3.7V	**Cell Balance Start Point** Default: 3.5V OTP programmable
5	Balance Threshold_H2L	0	Y	Y	R/W	0: 50mV 1: 70mV	**Cell Balance Threshold** Default: 50mV OTP programmable
4	Balance Threshold_L2H	0	Y	Y	R/W	0: 50mV 1: 70mV	**Cell Balance Threshold** Default: 50mV OTP programmable
3	I_{CC} [2]	1	Y	Y	R/W	800mA	**Fast Charge Current Setting** If R_{ISET} is 6kΩ: Offset: 500mA Range: 500mA to 2000mA Default: 2000mA (1111) If R_{ISET} is 24kΩ: Offset: 125mA Range: 125mA to 500mA Default: 500mA (1111) OTP programmable
2	I_{CC} [2]	1	Y	Y	R/W	400mA	
1	I_{CC} [1]	1	Y	Y	R/W	200mA	
0	I_{CC} [0]	1	Y	Y	R/W	100mA	

REG 02H (Default: 1001 0101)

Bit	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Notes
7	FSW	1	Y	Y	R/W	0: 600kHz 1: 1200kHz	Default: (1) 1200kHz OTP programmable
6	I²C WD Timer Reset	0	Y	N	R/W	0: Normal 1: Reset	Default: 0 (normal)
5	WD Timer [1]	0	Y	N	R/W	00: Disable timer 01: 40s	**I²C WD Timer Limit** Default: 40s (01)
4	WD Timer [0]	1	Y	N	R/W	10: 80s 11: 160s	OTP programmable
3	Register Reset	0	Y	N	R/W	0: Keep current setting 1: Reset	Default: 0 After reset, this bit goes back to 0 automatically.
2	CHG_TMR [1]	1	Y	Y	R/W	00: Disable CHG timer 01: 8hrs	Default: 10 (20hrs)
1	CHG_TMR [0]	0	Y	Y	R/W	10: 20hrs 11: 12hrs	
0	EN_SUSP	1	Y	Y	R/W	0: Enable suspend mode (disable boost) 1: Disable suspend mode (enable boost)	Default: 1

REG 03H (Default: 0000 0000)

Bit	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Notes
7	Reserved	N/A	N/A	N/A	R	Reserved	Reserved
6	Reserved	N/A	N/A	N/A	R	Reserved	Reserved
5	CHG_STAT [1]	0	N/A	N/A	R	00: Not charge 01: Pre-charge 10: Constant-current/constant-voltage charge 11: Charge done	Default: 00
4	CHG_STAT [0]	0	N/A	N/A	R		
3	PPM_STAT	0	N/A	N/A	R	0: Not PPM 1: VINPPM	Default: 0
2	BATTFLOAT_STAT	0	N/A	N/A	R	0: Battery present 1: Battery missing	Default: 0
1	THERM_STAT	0	N/A	N/A	R	0: Normal 1: Thermal regulation	Default: 0
0	VSYS_STAT	0	N/A	N/A	R	0: Not in VSYSMIN regulation 1: In VSYSMIN regulation	Default: 0

REG 04H (Default: 0000 0000)

Bit	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Notes
7	WD_FAULT	0	N/A	N/A	R	0: Normal 1: WD timer expiration	Default: 0
6	INPUT_FAULT	0	N/A	N/A	R	0: Normal 1: Input fault (OVP)	Default: 0
5	THERM SD_FAULT	0	N/A	N/A	R	0: Normal 1: Thermal shutdown	Default: 0
4	TIMER_FAULT	0	N/A	N/A	R	0: Normal 1: Safety timer expiration	Default: 0
3	BAT_FAULT	0	N/A	N/A	R	0: Normal 1: Battery OVP	Default: 0
2	NTC_FAULT [2]	0	N/A	N/A	R	000: Normal 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot	Default: 000
1	NTC_FAULT [1]	0	N/A	N/A	R		
0	NTC_FAULT [0]	0	N/A	N/A	R		

REG 05H (Default: 1110 0000) [8]

Bit	Bit Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Notes
7	RCHG	1	N/A	N/A	N/A	0: No charging after input power-on when $V_{BATT} > V_{RECH}$ 1: Automatic charging after input power-on when $V_{BATT} > V_{RECH}$	Default: 1
6	Reserved	1	N/A	N/A	N/A	Reserved	
5	BALANCE_EOC_EN	1	N/A	N/A	N/A	0: Does not suspend termination when cell balance is active 1: Suspends termination when cell balance is active	Default: 1
4	T_{J_REG} [1]	0	N/A	N/A	N/A	00: 120°C 01: 100°C 10: 80°C 11: 60°C	Default: 00
3	T_{J_REG} [0]	0	N/A	N/A	N/A		
2	Reserved	0	N/A	N/A	N/A	Reserved	Reserved
1	Reserved	0	N/A	N/A	N/A	Reserved	Reserved
0	Reserved	0	N/A	N/A	N/A	Reserved	Reserved

Note:

(8) This register is for OTP only and not accessible to customers.

OTP MAP

#	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	V_{BATT_REG}: 8.3V to 9.0V			N/A	V_{BATT_PRE}: 6.0V to 6.7V			N/A
01	NTC type	V_{CELL_BAL}	$V_{CELL\_DIFF\_HL}$	$V_{CELL\_DIFF\_LH}$	I_{CC}: 500mA to 2000mA / 100mA step (R_{ISET} = 6kΩ)			
02	FSW	N/A	Watchdog		N/A	N/A	N/A	N/A
05 [6]	RCHG	N/A	BALANCE _EOC_EN	T_{J_REG}: 60°C/80°C/ 100°C/120°C	N/A	N/A	N/A	N/A

OTP DEFAULT

OTP Items	Default
V_{BATT_REG}	8.4V
V_{BATT_PRE}	6.4V
NTC type	JEITA
V_{CELL_BAL}	3.5V
Balance threshold H2L	50mV
Balance threshold L2H	50mV
I_{CC}	2000mA
SW FREQ	1200kHz
Watchdog	40s
RCHG	New charge cycle starts when V_{BATT} > V_{RECH} after power-on
BALANCE_EOC_EN	Enable (if two cells are not balanced, EOC is not asserted even if all other conditions are met)
Thermal regulation threshold	120°C

APPLICATION INFORMATION

Setting the Charge Current in Standalone Mode

In standalone mode, the charge current of the MP2672 can be set by an external resistor (R_{ISET}) using Equation (4):

$$I_{CC} = \frac{12k\Omega}{R_{ISET}}(A) \qquad (4)$$

The charge current can be programmed up to 2A. Table 5 shows the expected R_{ISET} for a typical charge current.

Table 5: Charge Current Setting Table

R_{ISET} (kΩ)	I_{CC} (A)
24	0.5
12	1
6	2

Setting the Input Minimum Voltage Limit

In charge mode, connect a voltage divider from IN to AGND tapped to VLIM to program the input minimum voltage using Equation (5):

$$V_{IN\_MIN} = 1.2V \times \frac{R_H + R_L}{R_L} \qquad (5)$$

Where 1.2V is the reference of the input minimum voltage loop.

With given R_L, R_H can be calculated with Equation (6):

$$R_H = R_L \times \frac{V_{IN\_MIN} - 1.2V}{1.2V} \qquad (6)$$

For example, if a 4.675V input minimum voltage limit is expected, $R_L = 10k\Omega$ and $R_H = 28.7k\Omega$.

Resistor Selection for the NTC Sensor

Figure 20 shows an internal voltage divider reference circuit that limits the high and low temperature thresholds at V_{HOT} and V_{COLD}, respectively.

For a given NTC thermistor, select the appropriate R_{T1} and R_{T2} values to set the NTC window. Determine R_{T1} and R_{T2} using Equation (7) and Equation (8), respectively:

$$R_{T1} = \frac{(1-V_{COLD})(1-V_{HOT})(R_L - R_H)}{(1-V_{HOT}) \cdot V_{COLD} - (1-V_{COLD}) \cdot V_{HOT}} \qquad (7)$$

$$R_{T2} = \frac{V_{COLD} \cdot R_{T1}}{1 - V_{COLD}} - R_L \qquad (8)$$

Where, V_{HOT} and V_{COLD} are the high and low temperature thresholds, respectively.

R_H is the value of the NTC resistor at high temperatures of the required temperature operation range, and R_L is the value of the NTC resistor at low temperatures.
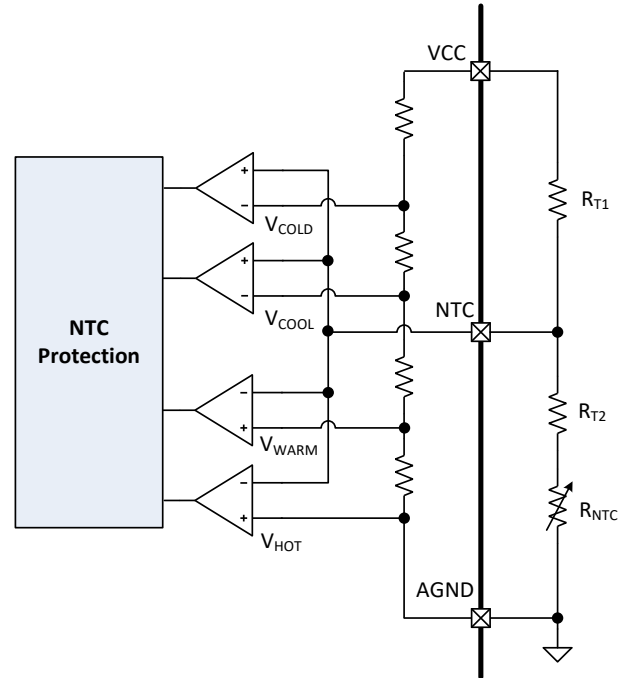

Figure 20: NTC Protection Block

R_{T1} and R_{T2} allow the high temperature limit and low temperature limit to be programmed independently. With this feature, the MP2672 can fit most types of NTC resistors and different temperature operation range requirements.

R_{T1} and R_{T2} values depend on the type of the NTC resistor. For example, for the 103AT thermistor, it has the following electrical characteristics:

At 0°C, $R_{NTC\_COLD} = 27.28k\Omega$

At 60°C, $R_{NTC\_HOT} = 3.02k\Omega$

Based on Equation (7) and Equation (8), V_{HOT}

www.MonolithicPower.com

and V_{COLD} from the EC table to calculate R_{T1} = 12.62kΩ and R_{T2} = 3.63kΩ. Apply the spread sheet for R_{T1} and R_{T2} calculation if required.

Selecting the Inductor

Inductor selection is the tradeoff between cost, size, and efficiency. A lower inductance value results in lower DCR for the same component size, but results in higher current ripple, higher magnetic hysteretic losses, and higher output capacitance. The inductor ripple current must not exceed 30% of maximum input current under worst-case conditions.

Choose an inductor that does not saturate under worst-case load conditions. The saturation current of the inductor should be greater than the peak current limit of the low-side FET.

When the MP2672 works in charge mode, estimate the required inductance with Equation (9), Equation (10), and Equation (11):

$$L = \frac{V_{IN} \cdot (V_{SYS} - V_{IN})}{V_{SYS} \cdot f_{SW} \cdot \Delta I_{L\_MAX}} \qquad (9)$$

$$\Delta I_{L\_MAX} = 2 \times \left(I_{L\_PK} - I_{IN(MAX)} \right) \qquad (10)$$

$$I_{IN(MAX)} = \frac{V_{SYS} \times I_{SYS(MAX)}}{V_{IN} \times \eta} \qquad (11)$$

Where V_{SYS} is the system minimum regulation voltage, f_{SW} is the switching frequency, ΔI_{L_MAX} is the peak-to-peak inductor ripple current, $I_{IN(MAX)}$ is maximum input current, I_{L_PK} is the expected inductor peak current, $I_{SYS(MAX)}$ is the maximum boost output current, and η is the boost efficiency.

With an 8.4V battery voltage, 2A maximum charge current, 8.7V system voltage, typical input voltage (V_{IN} = 5V), 1.2MHz switching frequency, 90% efficiency, and expected 4.5A inductor peak current, the inductance is calculated close to 1.5µH.

A 1.5µH inductor with 5A saturation current is recommended for a 1.2MHz switching frequency. A 2.5µH inductor with >5A saturation current is recommended for a 600kHz switching frequency.

Selecting the Input Capacitor

C_{IN} is the input capacitor of the boost converter during charge mode. Calculate its values with Equation (12) and Equation (13):

$$\frac{\Delta V_{IN}}{V_{IN}} = \frac{1 - V_{IN}/V_{SYS}}{8 \cdot C_{IN} \cdot f_{SW}^2 \cdot L} \qquad (12)$$

$$C_{IN} = \frac{1 - V_{IN}/V_{SYS}}{8 \cdot f_{SW}^2 \cdot L \cdot \Delta V_{IN}/V_{IN}} \qquad (13)$$

Assume the maximum input voltage ripple is 1%. When V_{SYS} is 9.25V, V_{IN} is 5V, L is 1µH, and f_{SW} is 1200kHz, then C_{IN} is 4.7µF.

Place one ceramic capacitor greater than 4.7µF with X5R or X7R at the IN terminal.

Selecting the System Capacitor

In charge mode, C_{SYS} is the output capacitor of the boost converter. C_{SYS} keeps the V_{SYS} ripple small (<0.5%) and ensures feedback loop stability. Select the system capacitors based on the ripple current. For best results, use X5R or X7R dielectric ceramic capacitors with low ESR and small temperature coefficients. For most applications, two 22µF capacitors and one 1µF capacitor are sufficient. Be sure to place them as close to the IC as possible.

PCB Layout Guidelines

Efficient PCB layout is critical for meeting specified noise, efficiency, and stability requirements. For best results, follow the guidelines below:

1. Place the output capacitor as close to SYS and PGND as possible.

2. Place the local power input capacitors connected from IN to PGND as close as possible.

3. Minimize the length of the high-side switching node (SW, inductor) trace that carries the high current.

4. Keep the switching node short and away from all control signals, especially the feedback network.

5. Route the power stages adjacent to their grounds.
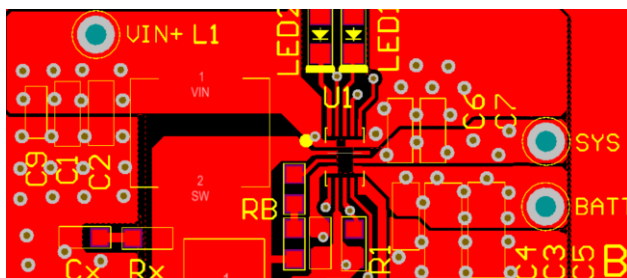
TOP Layer
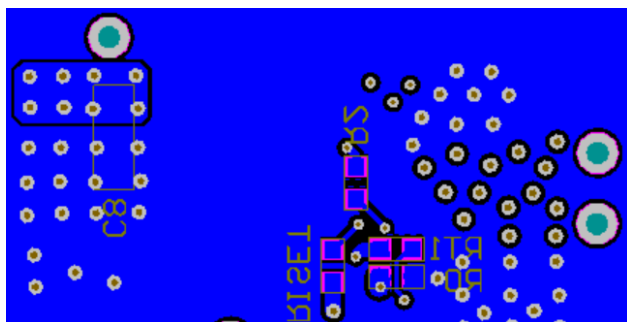
Bottom Layer

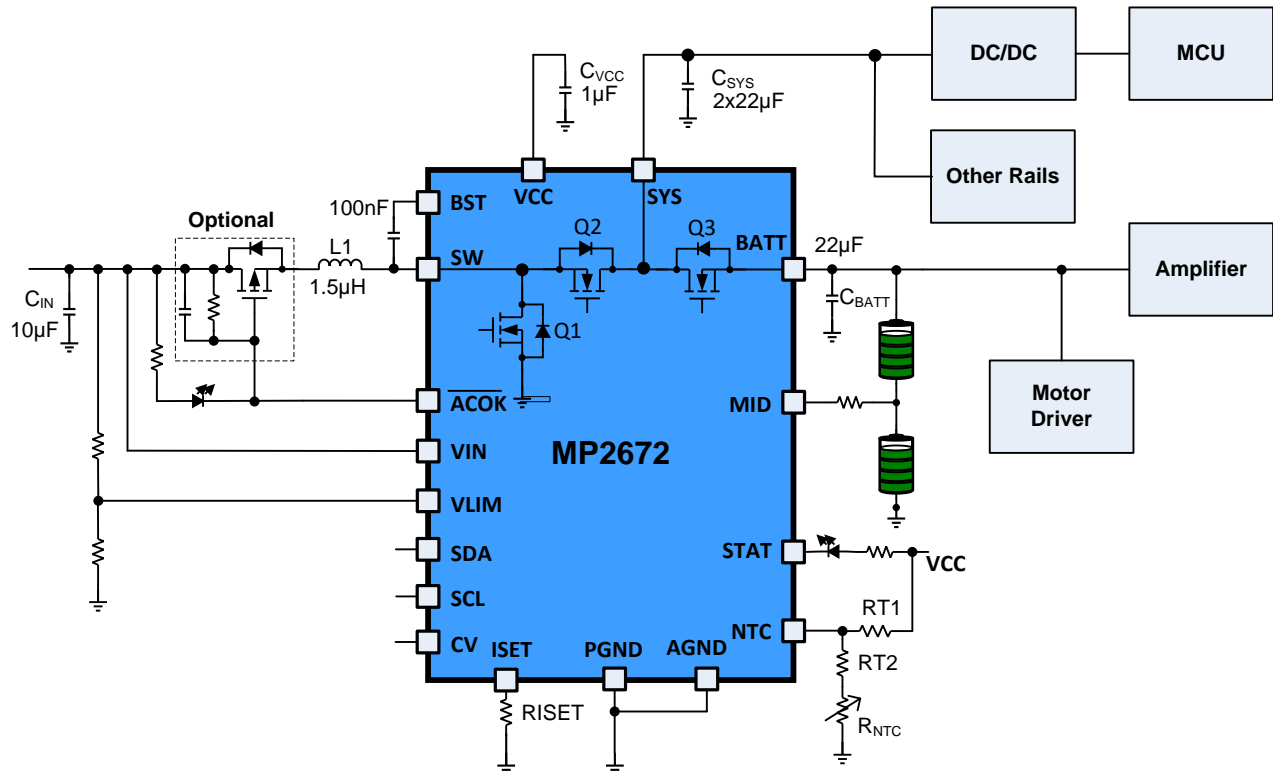**Figure 21 Recommended PCB Layout**

TYPICAL APPLICATION CIRCUITS

Figure 22: MP2672-0000 Application Reference Circuit for NVDC Application

Table 6: Key BOM of Figure 22

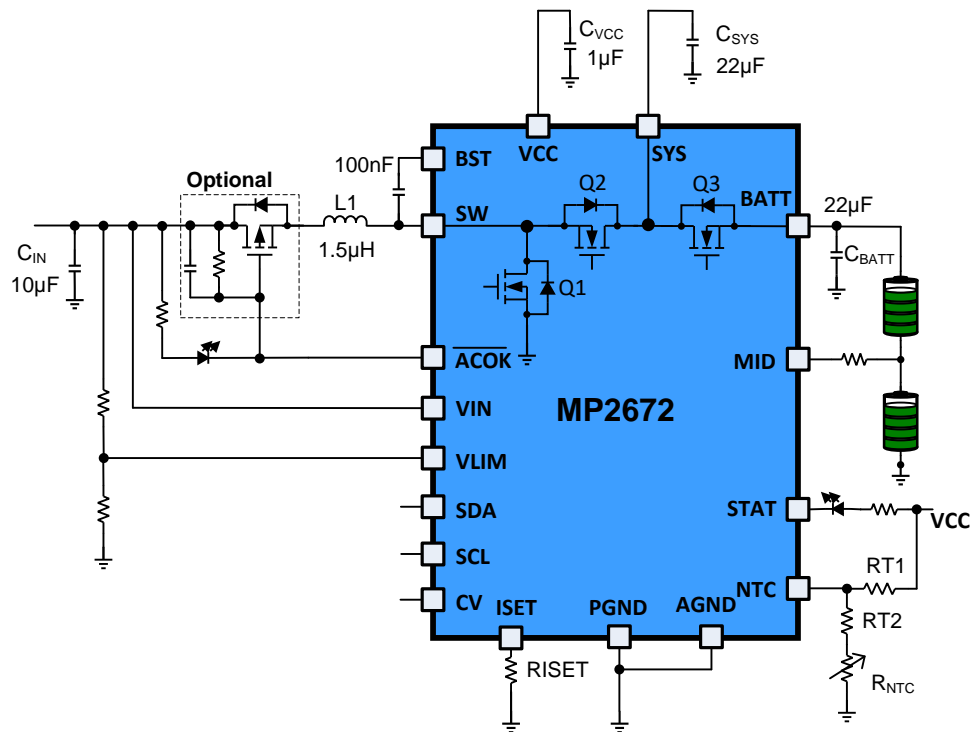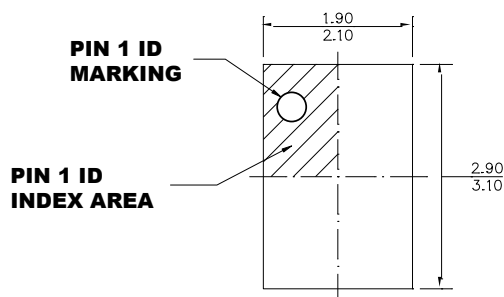| Qty	Ref	Value	Description	Package	Manufacture
1	C_{IN}	10µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
2	C_{SYS}	22µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{BATT}	22µF	Ceramic capacitor, 16V, X5R or X7R	1206	Any
1	C_{VCC}	1µF	Ceramic capacitor, 6.3V, X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1.5µH	Inductor, 1.5µH, saturation current > 8A, low DCR	SMD	Any

TYPICAL APPLICATION CIRCUITS

Figure 23: MP2672-000D Application Reference Circuit for Charge Only Application
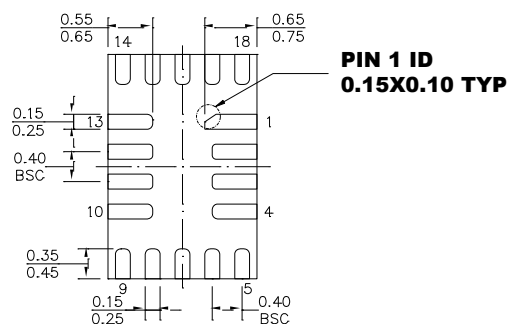
Table 7: Key BOM of Figure 23

Qty	Ref	Value	Description	Package	Manufacture
1	C_{IN}	10μF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{SYS}	22μF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{BATT}	22μF	Ceramic capacitor, 16V, X5R or X7R	1206	Any
1	C_{VCC}	1μF	Ceramic capacitor, 6.3V, X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1.5μH	Inductor, 1.5μH, saturation current > 8A, low DCR	SMD	Any

PACKAGE INFORMATION

QFN-18 (2mmx3mm)

PIN 1 ID MARKING

PIN 1 ID INDEX AREA

1.90
2.10

2.90
3.10

TOP VIEW

0.55
0.65

14

18

0.65
0.75

PIN 1 ID 0.15X0.10 TYP

0.15
0.25

13

1

0.40
BSC

10

4

0.35
0.45

9

5

0.15
0.25

0.40
BSC

BOTTOM VIEW

0.20 REF

0.80
1.00

0.00
0.05

SIDE VIEW

1.70

0.15X0.10

1.00

0.20

0.40

0.90

0.70

2.90

0.20

0.40
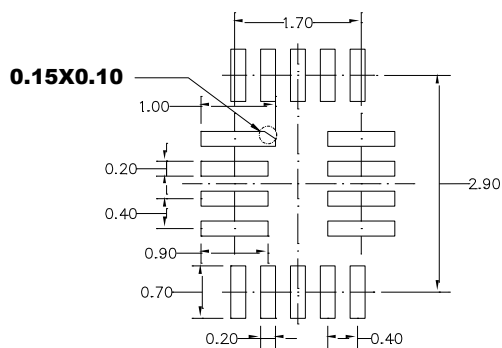
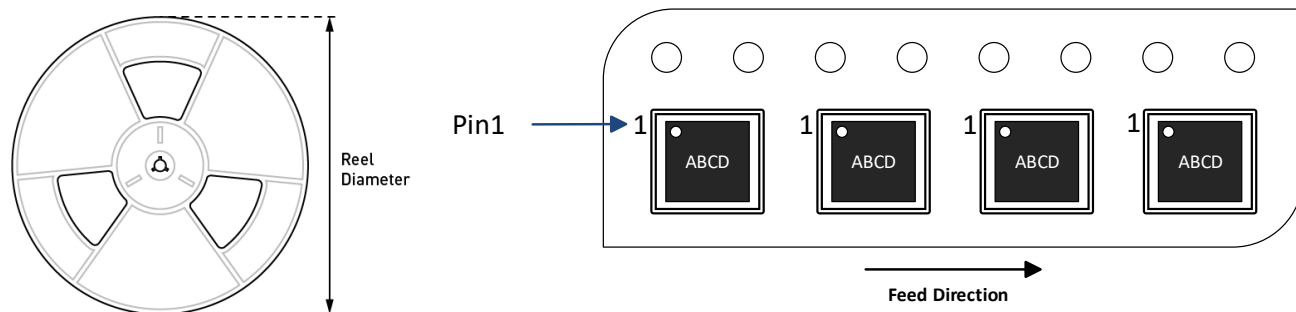**RECOMMENDED LAND PATTERN**

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION

Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2672GD-xxxx-Z	QFN-18 (2mmx3mm)	5000	N/A	N/A	13 in.	12 mm	8 mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	7/17/2020	Initial Release	-