

# AP1023

# 2ch H-Bridge Constant Voltage Control Motor Driver IC

# 1. General Description

The AP1023 is 2ch H-Bridge Motor Driver corresponding to motor operating voltage range from 1.6 to 6.5V. The AP1023 is capable of driving two motor or one stepper motor. The AP1023 is suitable for battery drive application, and realizes to the battery life by PWM constant voltage control. The AP1023 is housed in a small  $4 \times 4$ mm 24pin QFN package with good heat dissipation performance, and therefore contributes to downsize Printed Circuit Board.

	2. Features							
•	PWM Constant Voltage Control							
•	Motor Operating Voltage	1.6V~6.5V						
•	Control Supply Voltage	2.7V~5.5V						
•	Maximum Output Current	1.45A(Ta=25°C, 2ch simultaneously)						
•	H-Bridge On-Resistance (High+Low)	0.54Ω (Ta=25°C)						
•	Built-in Charge Pump block							
•	Under Voltage Lockout Circuit (UVLO)							
•	Thermal Shutdown Circuit (TSD)							
•	Operating Temperature Range	-30°C~85°C						
•	Package	24pin QFN (4mm×4mm, with Ex-posed PAD)						

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# 4. Block Diagram and Functions

# ■Block Diagram



Figure 1. Block Diagram

#### ■Functions

	lictions	
No	Block Name	Function
1	Charge Pump	Generate High side Gate drive Voltage.
2	VREF	Output Reference Voltage. It uses PWM Constant Voltage Setting pin, VSET.
3	Saw-Tooth OSC	According to input signal and VSET setting Voltage, VM voltage, the AP1023 generates PWM control signal and supplies H-Bridge Control Circuit.
4	UVLO	If VC voltage is lower than 2.2V (typ.) at the starting, the H-Bridge output is the Hi-Z.
5	TSD	If the internal temperature of the IC (Tj) reaches 175 °C (typ.), the H-Bridge outputs Hi-Z.
6	Control Circuit	Every block is controlled by signal of Input terminal. When UVLO and TSD operate at the abnormal operation, every block is stopped.
7		According to information from Control Circuit and PWM control setting (M0, M1), PWM Constant Voltage (VSET), the AP1023 generates signal to drive H-Bridge.
8	LDMOS H-Bridge1, 2	H-Bridge is configured by Hi-Side(TOP) and Lo-Side(BOT) Nch-MOSFET.

#### 5. Ordering Guide

AP1023AEN

-30°C~85°C

6.

24-pin QFN

#### Pin Configurations and Functions

#### ■Pin Configurations



Exposed PAD must be connected to GND.

#### ■Functions

Function	113			
Pin Number	Pin Name	I/O	Functions	Notes
1,2	OUT1B	0	Motor Driver Output	
3	VG	I/O	Connect Terminal for Stabilizing Capacitor.	
4	СН	I/O	Connect Terminal for Charge Pump Capacitor.	
5	CL	I/O	Connect Terminal for Charge Pump Capacitor.	
6	VC	Р	Control Power Supply	
7	IN1	Ι	Control Signal Input	Built-in 200kΩ Pull-down
8	IN2	Ι	Control Signal Input	Built-in 200kΩ Pull-down
9	IN3	Ι	Control Signal Input	Built-in 200kΩ Pull-down
10	IN4	Ι	Control Signal Input	Built-in 200kΩ Pull-down
11	VREF	0	Output Terminal of Reference Voltage	
12	VSET	Ι	Constant Voltage Analog input	
13	GND	Р	Ground	
14	EN	Ι	Enable Signal Input	Built-in 200kΩ Pull-down
15	M0	Ι	Constant Voltage magnification setting Input (x1, x2)	Built-in 200kΩ Pull-down
16	M1	Ι	Driver control setting Input (Two Phase-excitation, Generic)	Built-in 200k $\Omega$ Pull-down
17,18	OUT2B	0	Motor Driver Output	
19,20	OUT2A	0	Motor Driver Output	
21,22	VM	Р	Motor Power Supply	
23,24	OUT1A	0	Motor Driver Output	
EP	PGND	Р	Power Ground, Ex-posed Pad	PGND and EP are shorted on the frame.

Note 1. I(Input pin), O(Output pin), P(Power pin), I/O(Input/Output pin)

Parameter	Symbol	min	max	Unit	Condition
Control Supply Voltage	VC	-0.5	6.0	V	
Motor Operating Voltage	VM	-0.5	7.0	V	
VC Level Terminal Voltage (INn,VREF,VSET,M1,M0,EN)	Vterm1	-0.5	VC	V	
VM Level Terminal Voltage (OUTnA, OUTnB,CL)	Vterm2	-0.5	VM	V	
VC+VM Level Terminal Voltage (CH,VG)	Vterm3	-0.5	13.0	V	
		-	1.35	А	Ta=85°C, 1ch (Note 3)
Maximum Output Current	Iload	-	0.95	A/ch	Ta=85°C, 2ch simultaneously (Note 3,Note 4)
Power Dissipation	PD	-	3.125	W	Thermal shutdown detection Temperature: Tj=150°C , (Note 3,Note 4)
Junction Temperature	Tj	-	150	°C	
Storage Temperature	Tstg	-40	150	°C	

## 7. Absolute Maximum Ratings

Note 2.All above voltages are with respect to GND=PGND=0V. GND and PGND must be connected to a ground plane.

Note 3. For Power Dissipation, the output current rating may be limited by duty cycle, Ta, and PCB board heat sinking design.

Note 4.A 4-layer board is used.  $R_{\theta JA} = 40^{\circ}C/W$ .



Figure 2. Maximum Power Dissipation

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

# 8. Recommended Operating Conditions

				(12	1-25 C,	unless otherwise specified.)
Parameter	Symbol	min	typ	max	Unit	Condition
Motor Operating Voltage	VM	1.6	5.0	6.5	V	
Control Supply Voltage	VC	2.7	3.0	5.5	V	
Input Frequency Range	Fin	-	-	1	kHz	M1="L",IN1,2
VSET terminal Voltage	VSET	0.5	-	VC	V	
Operating Temperature Range	Та	-30	-	85	°C	

(Ta=25°C, unless otherwise specified.)

WARNING: The maximum ratings are the absolute limitation values with the possibility of the IC breakage. When the operation exceeds this standard quality cannot be guaranteed.

9. Electrical Characteristics									
		(Ta=+25°C, VM=3.0V,VC=3.3V,	unless c	otherwise	e specifie	d.)			
Parameter	Symbol	Condition	min	typ	max	Unit			
Quiescent Current									
VC Quiescent Current at the time	т	TNT A 11 (17 )			1				
of Power Save	I <sub>VCOFF</sub>	IN=All "L"	-	-	1	μA			
VM Quiescent Current at the time									
of Power Save	I <sub>VMOFF</sub>	IN=All "L"	-	-	1	μA			
VC Quiescent Current at the time of									
Operating	I <sub>VC</sub>		-	0.45	1.0	mA			
Charge Pump									
Charge Pump Voltage	VG	VG = VM + VC, $Iload = 0A$	-	-	6.3	V			
Charge Pump Rise Time	tVGON	Charge-Pump: $VC > VC_{UV}$	-	0.3	3.0	ms			
H-Bridge									
Driver on resistance 1	R <sub>ON</sub>	Iload 1ch/2ch = $0.1A/0.1A$	-	0.54	0.70	Ω			
(H-Bridge High+Low)	KON	10001701/2011 = 0.174/0.174	-	0.34	0.70	32			
Driver on resistance 2	R <sub>ONTj</sub>	Iload $1ch/2ch = 0.1A/0.1A$	_	0.72	0.86	Ω			
(H-Bridge High+Low)(Note 6)	NONTj	$Tj = 150^{\circ}C$	_	0.72	0.00	32			
H-Bridge Driver	V <sub>F</sub>	$I_{\rm F} = 100 {\rm mA}$	_	0.8	1.2	v			
Body diode forward voltage	۴F	$r_{\rm F} = 100 {\rm mm}$ V		0.0	1.2	•			
Delay Time	1			1		1			
Output Delay Time	tPDLH	Connected to $1k\Omega$ between		_	1.0				
("L"→"H")	IFDLI	OUTA and OUTB.(Figure 3)	-	-	1.0	μs			
		IN1=IN3="L", VM=3.6V							
Output Delay Time	tPDHL	IN2=IN4=200kHz VC=3V, VSET=1.9V	_	_	1.0	μs			
("H"→"L")	u DIIL	N=2 (M0="H"), M1="H"		i I		μο			
		Connected to $20\Omega$ between							
Output Pulse Width	tPW	OUTA and OUTB.	0.6	1.0	1.4	μs			
Sulput I uise Widui		Input Pulse Width : 1µs(Figure 3)	0.0	1.0	1.4	μο			
Control Logic		input l'une vitaur : 1µs(11gure 3)							
Input High Level Voltage	V <sub>IH</sub>		0.7×VC	-	_	V			
Input Low Level Voltage	V <sub>IL</sub>		-	_	0.3×VC	V			
Input Pulse Rise Time	t <sub>R</sub>		_	_	1.0	μs			
Input Pulse Fall Time	t <sub>F</sub>		-	_	1.0	μs			
Input High Level Current	I <sub>IH</sub>	VC=3.0V	7.5	15	30	μA			
Input Low Level Current	I <sub>IH</sub> I <sub>IL</sub>		-1.0	-	1.0	μΑ			
Constant Voltage Control	▲IL	L	1.0	I	1.0	µ11			
VREF Output Voltage	V <sub>REF</sub>	Iref=0.1mA	2.25	2.5	2.75	V			
PWM Frequency1	f <sub>PWM</sub> 1	VM=1.6V~6.5V	10	-	160	kHz			
PWM Frequency2	f <sub>PWM</sub> 2	VM=1.8V~3.6V	25	_	140	kHz			
Constant Voltage Control									
Accuracy1	Duty <sub>OUT</sub> 1	VM=3.6V、VSET=1.8V,M0="L"	45	50	55	%			
Constant Voltage Control			~ <b>-</b>		100				
Accuracy2	Duty <sub>OUT</sub> 2	VM=1.8V、 VSET=1.8V,M0="L"	95	-	100	%			
Voltage between the OUT terminal	V <sub>OUT</sub>	VM=2.0V、Iout=200mA VSET=1.85V	1.65	1.75	1.85	v			
Protection Circuit				•		•			
VC Under Voltage Detect Voltage	VC <sub>UV</sub>		1.9	2.2	2.5	V			
Thermal Shutdown Temperature						00			
(Note 6)	T <sub>TSD</sub>		150	175	200	°C			
Temperature Hysteresis (Note 6)	T <sub>TSDHYS</sub>		-	30	-	°C			

Note 5.All above voltage is defined to GND=0V. Note 6.Not tested under mass-production.



(a) Delay Time

(b) Pulse Width

Figure 3.Timming Chart (Delay Time, Pulse Width)

## **10. Functional Descriptions**

#### 10.1 Operation Outline

The AP1023 can adjust the PWM duty of the output signal so that the average voltage of the H-Bridge output is about "VSET  $\times$  N".

Ex. N=1, VSET =1.8V, VM=3.6V→50% duty PWM signal Output,

H-Bridge Output average Voltage=1.8V

N=1, VSET =1.8V, VM=1.8V $\rightarrow$ 100% duty PWM signal Output,

H-Bridge Output average Voltage=1.8V

H-Bridge Output average voltage can be hold without depending VM.

Ex.VREF  $\times$  N>VM $\rightarrow$ 100% duty, H-Bridge Output average Voltage=1.8V

It should be noted that this average output voltage does not include the voltage loss due to the load current and the on-resistance of the H-Bridge. Please note that different from the actual voltage applied to the load.

Calculation of Output signal duty : PWM duty = VSET  $\times$  N /VM

Table 1.Selection of the Setting voltage magnification (N) by the M0 signal

M0	Ν
L	1 (PWM Constant Voltage Control)
Н	2 (PWM Constant Voltage Control)

Table 2.Selection of the Input Logic by the M1 signal (Input Logic of M1 = "L" is the best in the case of a Two-phase excitation.)

M1	Input Logic
L	Two-phase excitation
Н	Generic

Table 3. M1="L"

		INPUT				OUT	Mode		
EN	IN1	IN2	IN3	IN4	OUT1A	OUT1B	OUT2A	OUT2B	widde
L	-	-	-	-	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Save(Note 7)
Н	L	-	-	-	L	H(PWM)	-	-	CCW(Reverse)
Н	Н	-	-	-	H(PWM)	L	-	-	CW(Forward)
Н	-	L	-	-	-	-	L	H(PWM)	CCW(Reverse)
Н	-	Н	-	-	-	-	H(PWM)	L	CW(Forward)

Table 4. M1="H"

		INPUT	ר			OUT	Mode		
EN	IN1	IN2	IN3	IN4	OUT1A	OUT1B	OUT2A	OUT2B	widde
L	-	-	-	-	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Save(Note 7)
Н	L	L	I	-	L	L	-	-	Brake
Н	Η	L	I	-	H(PWM)	L	-	-	CW(Forward)
Н	L	Н	I	-	L	H(PWM)	-	-	CCW(Reverse)
Н	Η	Н	-	-	Hi-Z	Hi-Z	-	-	Standby
Н	-	-	L	L	-	-	L	L	Brake
Н	-	-	Н	L	-	-	H(PWM)	L	CW(Forward)
Н	-	-	L	Н	-	-	L	H(PWM)	CCW(Reverse)
Н	-	-	Н	Н	-	-	Hi-Z	Hi-Z	Standby

Note 7. Charge Pump block and TSD, UVLO don't operate at the Power Save.

# **10.2 Motor Driver Block Configuration**

The N-ch LDMOS FET of the output stage is layout on both sides of the high-side and low-side, and therefore the AP1023 possible to be housed in a small package.

Hi-side FET is driven by VG. "VG=VM+VC" is generated by Charge-Pump. Lo-side FET is driven by VC.



Figure 4.Driver Block Equivalent circuit

# **10.3 Protection Circuits**

• Under Voltage Lockout(UVLO) If VC voltage is lower than 2.2V (typ.) at the starting, the H-Bridge output is the Hi-Z.

• Thermal Shutdown(TSD)

When the internal temperature of the IC reaches the specified temperature ( $T_{TSD}(min)=150^{\circ}C$ ), and the H-Bridge driver outputs Hi-Z. When the internal temperature after the detection is lowered about 30°C ( $T_{TSDHYS}$ ), drivers will start the operation.

Restart Temperature =  $T_{TSD}$  -  $T_{TSDHYS}$ 









Note 8. There is no restriction to the power-up sequence of VM and VC.

### 11. Recommended External Circuits

#### ■Recommended External Circuits

• Driving Stepper Motor(External VREF)



• Driving DC Motor(External VREF)



Driving Stepper Motor(Internal VREF)



Figure 7.Recommended External Circuits

Table 5. Parts Li	Table 5. Parts List							
Item	Value	Unit	Note					
CVM1	22	μF	stabilization capacitors					
CVM2	1.0	μF	de-coupling capacitor					
CVC	0.1	μF						
CHL	0.1	μF						
CVG	0.1	μF						
CVR	0.1	μF						
CVS	100	pF						
COUT	0.1	μF						
R1	130k	ohm	$R1+R2 \ge 50k\Omega$					
R2	370k	ohm	$K1+K2 \leq 30KM$					

Note 9.Above values are examples. Please choose appropriate external components for your system board. Note 10.Capacitance of CVM and CVC should be determined in consideration of the load current profile, the load capacitance, the line resistance and etc. of the actual system board.

Note 11.Please layout the large ground plane on the PCB.

Note 12.Exposed Pad (heat sink) is common to the ground terminal. Please connect it to the ground of the PCB.

# 12. Package

# ■Outline Dimensions

• 24-pin QFN (Unit : mm)



■Recommended Land Pattern



#### ■Marking



- (1) 1pin Indication
- (2) Market No.
- (3) Year code (last digit)
- (4) Week code
- (5) Management code

13. Revise History	
IS. REVISE THSIDLY	

Date (YY/MM/DD)	Revision	Page	Contents
16/03/24	00	-	First Edition

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