

**HCPL-0600**

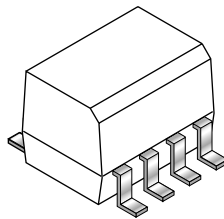
**HCPL-0601**

**DESCRIPTION**

The HCPL-0600/0601 optocouplers consist of a 870 nm AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. The devices are housed in a compact small-outline package. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8). An internal noise shield provides superior common mode rejection of typically 10 kV/μs.

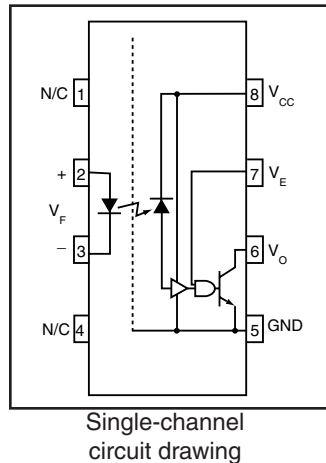
**FEATURES**

- Compact SO8 package
- Very high speed-10 MBit/s
- Superior CMR-10 kV/μs
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700)

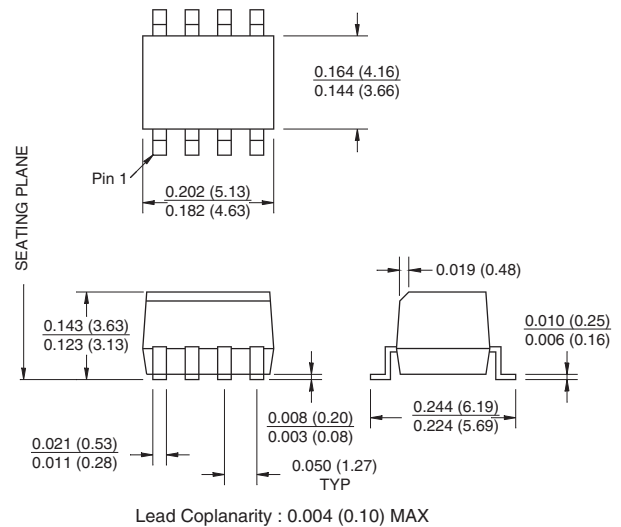


**APPLICATIONS**

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface



**PACKAGE DIMENSIONS**



**NOTE**  
All dimensions are in inches (millimeters)

**TRUTH TABLE  
(Positive Logic)**

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

A 0.1 μF bypass capacitor must be connected between pins 8 and 5. (See note 1)

**HCPL-0600**

**HCPL-0601**

<b>ABSOLUTE MAXIMUM RATINGS</b> (No derating required up to 85°C)			
Parameter	Symbol	Value	Units
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C
Operating Temperature	T <sub>OPR</sub>	-40 to +85	°C
Lead Solder Temperature	T <sub>SOL</sub>	260 for 10 sec	°C
<b>EMITTER</b>			
DC/Average Forward Input Current	I <sub>F</sub>	50	mA
Enable Input Voltage Not to exceed VCC by more than 500 mV	V <sub>E</sub>	5.5	V
Reverse Input Voltage	V <sub>R</sub>	5.0	V
Power Dissipation	P <sub>I</sub>	45	mW
<b>DETECTOR</b>			
Supply Voltage	V <sub>CC</sub> (1 minute max)	7.0	V
Output Current	I <sub>O</sub>	50	mA
Output Voltage	V <sub>O</sub>	7.0	V
Collector Output Power Dissipation	P <sub>O</sub>	85	mW

<b>RECOMMENDED OPERATING CONDITIONS</b>				
Parameter	Symbol	Min	Max	Units
Input Current, Low Level	I <sub>FL</sub>	0	250	μA
Input Current, High Level	I <sub>FH</sub>	*6.3	15	mA
Supply Voltage, Output	V <sub>CC</sub>	4.5	5.5	V
Enable Voltage, Low Level	V <sub>EL</sub>	0	0.8	V
Enable Voltage, High Level	V <sub>EH</sub>	2.0	V <sub>CC</sub>	V
Operating Temperature	T <sub>A</sub>	-40	+85	°C
Fan Out (TTL load)	N		8	

\*6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less

**HCPL-0600**

**HCPL-0601**

**ELECTRICAL CHARACTERISTICS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  Unless otherwise specified.)

**INDIVIDUAL COMPONENT CHARACTERISTICS**

Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit
<b>EMITTER</b> Input Forward Voltage	( $I_F = 10\text{ mA}$ )	$V_F$			1.8	V
	$T_A = 25^\circ\text{C}$				1.75	
Input Reverse Breakdown Voltage	( $I_R = 10\ \mu\text{A}$ )	$B_{VR}$	5.0			V
Input Capacitance	( $V_F = 0$ , $f = 1\text{ MHz}$ )	$C_{IN}$		60		pF
Input Diode Temperature Coefficient	( $I_F = 10\text{ mA}$ )	$\Delta V_F/\Delta T_A$		-1.4		mV/ $^\circ\text{C}$
<b>DETECTOR</b>						
High Level Supply Current	( $V_{CC} = 5.5\text{ V}$ , $I_F = 0\text{ mA}$ ) ( $V_E = 0.5\text{ V}$ )	$I_{CCH}$		7	10	mA
Low Level Supply Current	( $V_{CC} = 5.5\text{ V}$ , $I_F = 10\text{ mA}$ ) ( $V_E = 0.5\text{ V}$ )	$I_{CCL}$		9	13	mA
Low Level Enable Current	( $V_{CC} = 5.5\text{ V}$ , $V_E = 0.5\text{ V}$ )	$I_{EL}$		-0.8	-1.6	mA
High Level Enable Current	( $V_{CC} = 5.5\text{ V}$ , $V_E = 2.0\text{ V}$ )	$I_{EH}$		-0.6	-1.6	mA
High Level Enable Voltage	( $V_{CC} = 5.5\text{ V}$ , $I_F = 10\text{ mA}$ )	$V_{EH}$	2.0			V
Low Level Enable Voltage	( $V_{CC} = 5.5\text{ V}$ , $I_F = 10\text{ mA}$ ) (Note 2)	$V_{EL}$			0.8	V

**SWITCHING CHARACTERISTICS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $I_F = 7.5\text{ mA}$  Unless otherwise specified.)

AC Characteristics	Test Conditions	Device	Symbol	Min	Typ	Max	Unit
Propagation Delay Time to Output High Level	(Note 3) ( $T_A = 25^\circ\text{C}$ ) ( $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ ) (Fig. 12)	All	$T_{PLH}$	20	45	75 100	ns
Propagation Delay Time to Output Low Level	(Note 4) ( $T_A = 25^\circ\text{C}$ ) ( $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ ) (Fig. 12)	All	$T_{PHL}$	25	45	75 100	ns
Pulse Width Distortion	( $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ ) (Fig. 12)	All	$ T_{PHL} - T_{PLH} $		3	35	ns
Output Rise Time (10-90%)	( $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ ) (Note 5) (Fig. 12)	All	$t_r$		50		ns
Output Fall Time (90-10%)	( $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ ) (Note 6) (Fig. 12)	All	$t_f$		12		ns
Enable Propagation Delay Time to Output High Level	( $I_F = 7.5\text{ mA}$ , $V_{EH} = 3.5\text{ V}$ ) ( $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ ) (Note 7) (Fig. 13)	All	$t_{ELH}$		20		ns
Enable Propagation Delay Time to Output Low Level	( $I_F = 7.5\text{ mA}$ , $V_{EH} = 3.5\text{ V}$ ) ( $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ ) (Note 8) (Fig. 13)	All	$t_{EHL}$		20		ns
Common Mode Transient Immunity (at Output High Level)	( $R_L = 350\ \Omega$ ) ( $T_A = 25^\circ\text{C}$ ) ( $I_F = 0\text{ mA}$ , $V_{OH}(\text{Min.}) = 2.0\text{ V}$ ) (Note 9)(Fig. 14)	$ V_{CM}  = 10\text{ V}$	HCPL-0600		10,000		V/ $\mu\text{s}$
		$ V_{CM}  = 50\text{ V}$	HCPL-0601	5000	10,000		
Common Mode Transient Immunity (at Output Low Level)	( $R_L = 350\ \Omega$ ) ( $T_A = 25^\circ\text{C}$ ) ( $I_F = 7.5\text{ mA}$ , $V_{OL}(\text{Max.}) = 0.8\text{ V}$ ) (Note 10)(Fig. 14)	$ V_{CM}  = 10\text{ V}$	HCPL-0600		10,000		V/ $\mu\text{s}$
		$ V_{CM}  = 50\text{ V}$	HCPL-0601	5000	10,000		

**HCPL-0600**

**HCPL-0601**

<b>TRANSFER CHARACTERISTICS</b> ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Unless otherwise specified.)						
DC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
High Level Output Current	( $V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$ ) ( $I_F = 250\ \mu\text{A}$ , $V_E = 2.0\text{ V}$ ) (Note 2)	$I_{OH}$			100	$\mu\text{A}$
Low Level Output Voltage	( $V_{CC} = 5.5\text{ V}$ , $I_F = 5\text{ mA}$ ) ( $V_E = 2.0\text{ V}$ , $I_{OL} = 13\text{ mA}$ ) (Note 2)	$V_{OL}$		.35	0.6	V
Input Threshold Current	( $V_{CC} = 5.5\text{ V}$ , $V_O = 0.6\text{ V}$ , $V_E = 2.0\text{ V}$ , $I_{OL} = 13\text{ mA}$ )	$I_{FT}$		3	5	mA

<b>ISOLATION CHARACTERISTICS</b> ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Unless otherwise specified.)						
Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-Output Insulation Leakage Current	(Relative humidity = 45%) ( $T_A = 25^\circ\text{C}$ , $t = 5\text{ s}$ ) ( $V_{I-O} = 3000\text{ VDC}$ ) (Note 11)	$I_{I-O}$			1.0*	$\mu\text{A}$
Withstand Insulation Test Voltage	( $R_H < 50\%$ , $T_A = 25^\circ\text{C}$ ) (Note 11) ( $t = 1\text{ min.}$ )	$V_{ISO}$	2500			$V_{RMS}$
Resistance (Input to Output)	( $V_{I-O} = 500\text{ V}$ ) (Note 11)	$R_{I-O}$		$10^{12}$		$\Omega$
Capacitance (Input to Output)	( $f = 1\text{ MHz}$ ) (Note 11)	$C_{I-O}$		0.6		pF

\*\* All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

**NOTES**

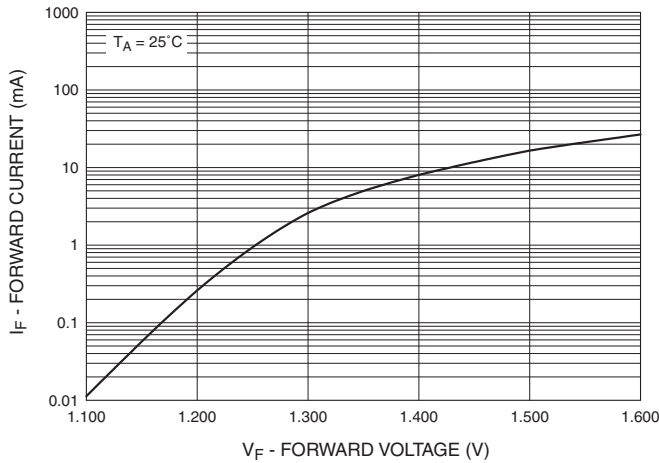
1. The  $V_{CC}$  supply to each optoisolator must be bypassed by a  $0.1\ \mu\text{F}$  capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package  $V_{CC}$  and GND pins of each device.
2. Enable Input - No pull up resistor required as the device has an internal pull up resistor.
3.  $t_{PLH}$  - Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
4.  $t_{PHL}$  - Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
5.  $t_r$  - Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
6.  $t_f$  - Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
7.  $t_{ELH}$  - Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
8.  $t_{EHL}$  - Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
9.  $CM_H$  - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e.,  $V_{OUT} > 2.0\text{ V}$ ). Measured in volts per microsecond (V/ $\mu\text{s}$ ).
10.  $CM_L$  - The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e.,  $V_{OUT} < 0.8\text{ V}$ ). Measured in volts per microsecond (V/ $\mu\text{s}$ ).
11. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.

**HCPL-0600**

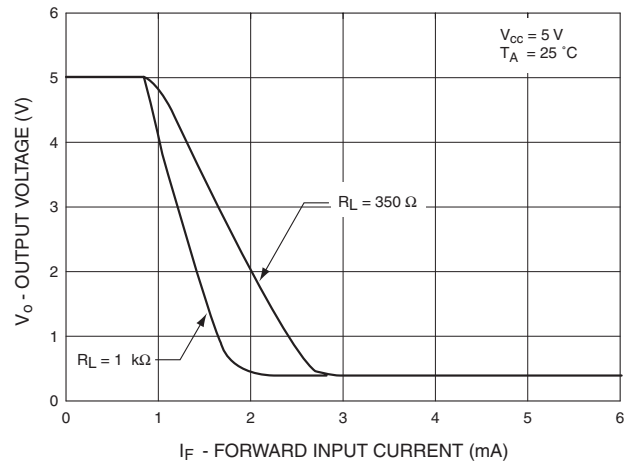
**HCPL-0601**

**TYPICAL PERFORMANCE CURVES**

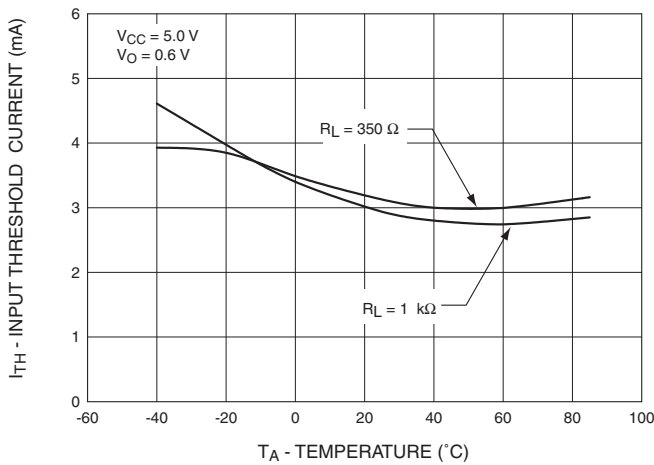
**Fig. 1 Forward Current vs. Input Forward Voltage**



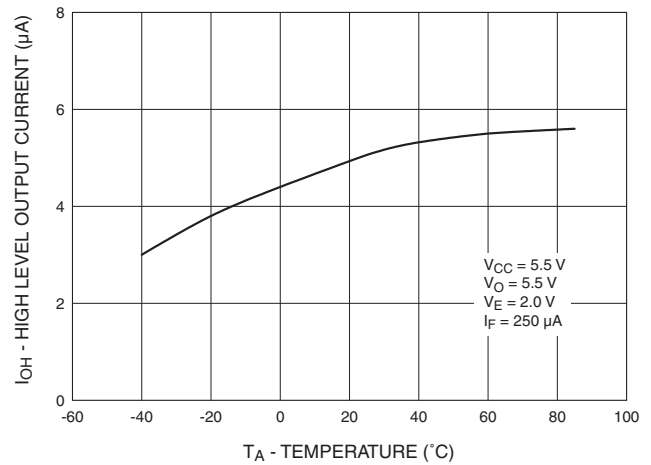
**Fig. 2 Output Voltage vs. Forward Current**



**Fig. 3 Input Threshold Current vs. Temperature**



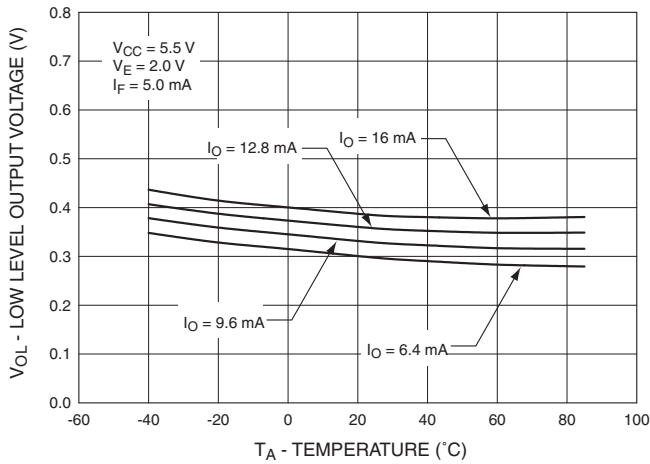
**Fig. 4 High Level Output Current vs. Temperature**



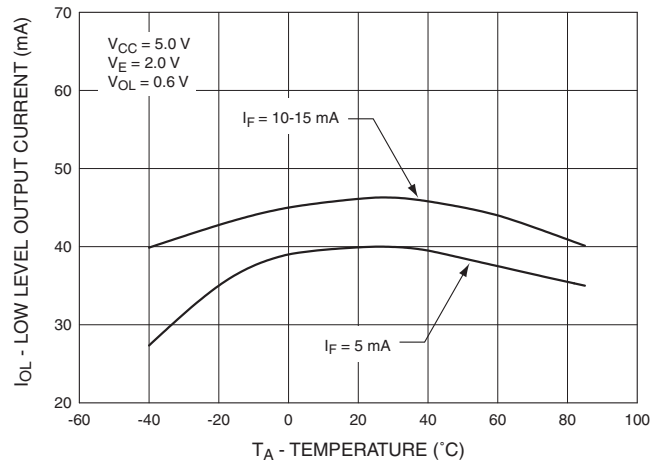
**HCPL-0600**

**HCPL-0601**

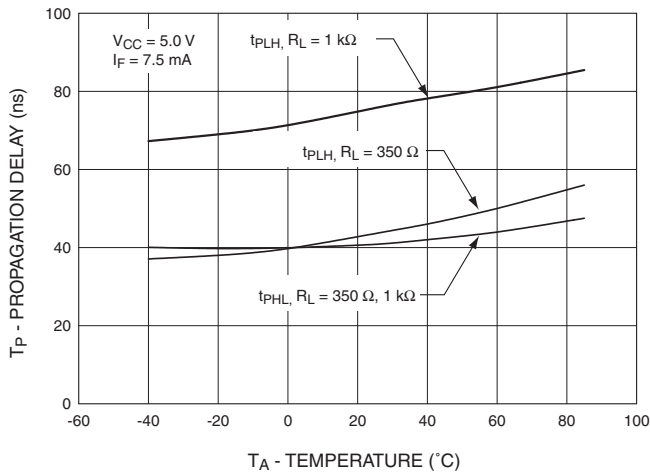
**Fig. 5 Low Level Output Voltage vs. Temperature**



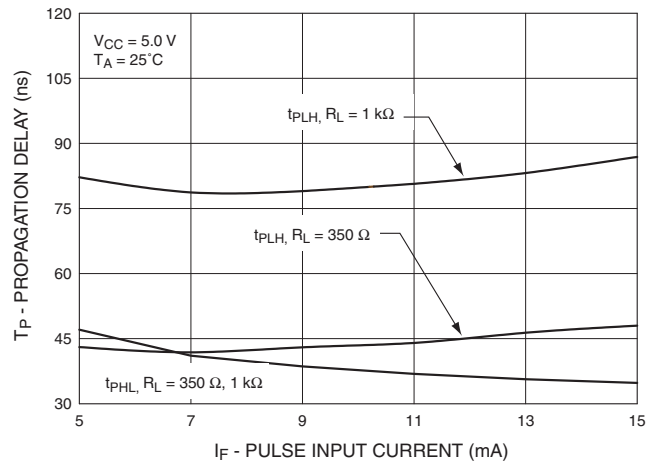
**Fig. 6 Low Level Output Current vs. Temperature**



**Fig. 7 Propagation Delay vs. Temperature**



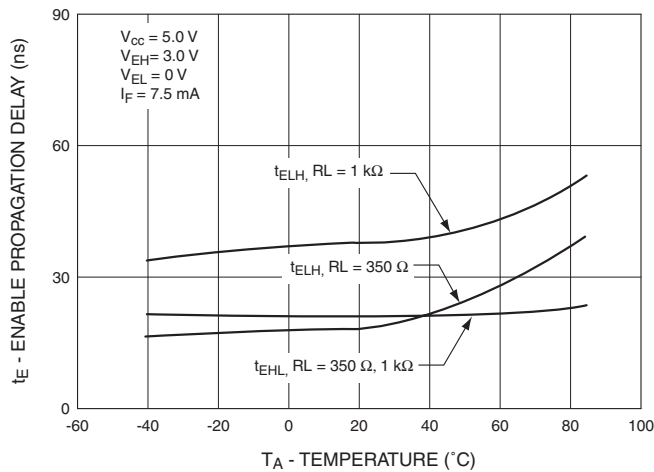
**Fig. 8 Propagation Delay vs. Pulse Input Current**



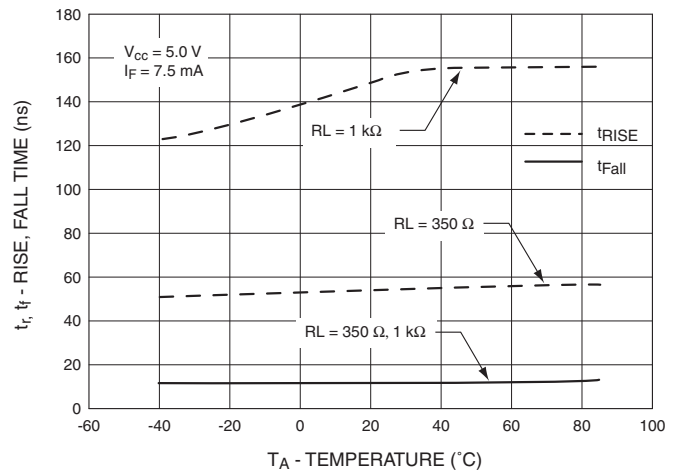
**HCPL-0600**

**HCPL-0601**

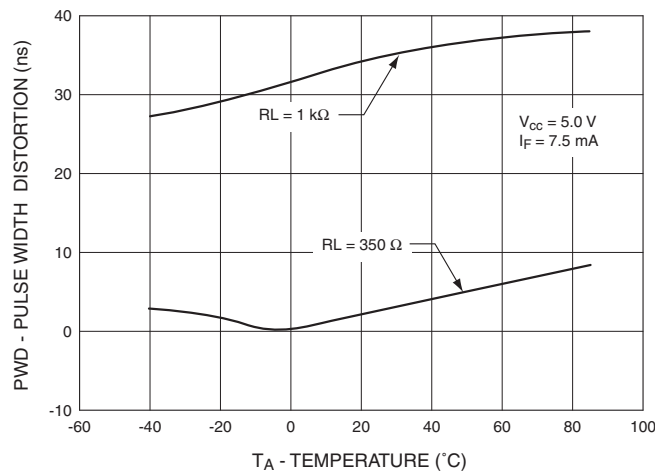
**Fig. 9 Typical Enable Propagation Delay vs. Temperature**



**Fig. 10 Typical Rise and Fall Time vs. Temperature**

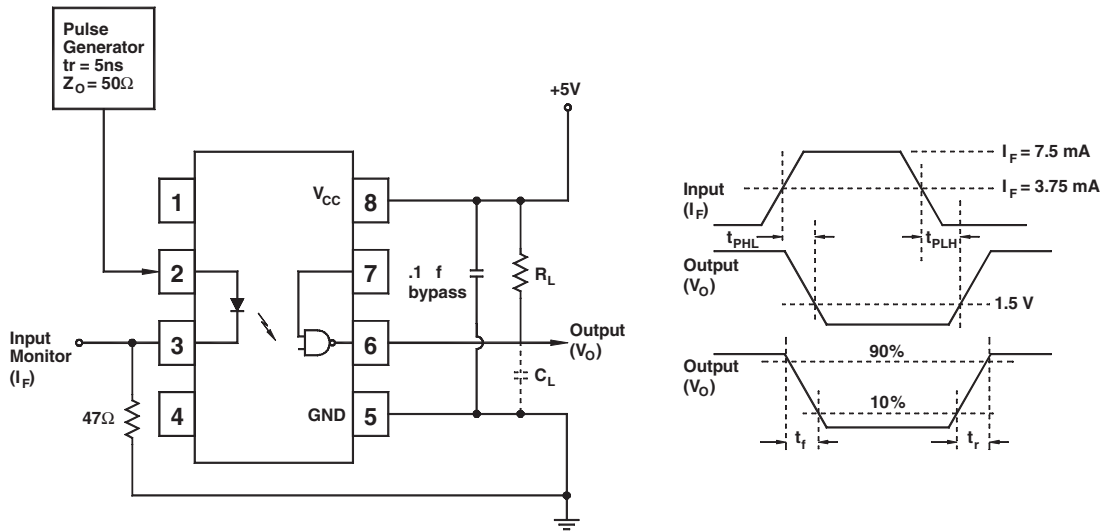


**Fig. 11 Typical Pulse Width Distortion vs. Temperature**

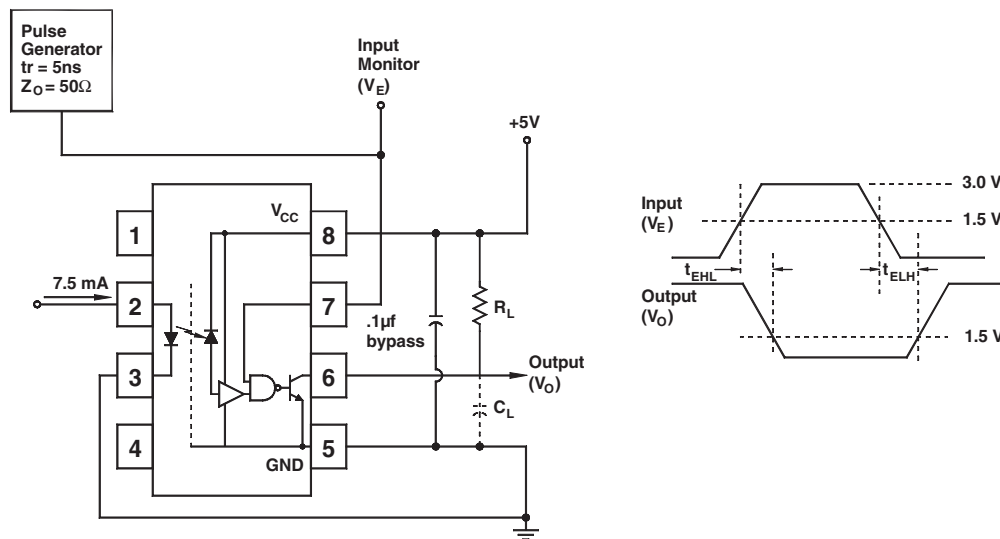


**HCPL-0600**

**HCPL-0601**



**Fig. 12 Test Circuit and Waveforms for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$ .**

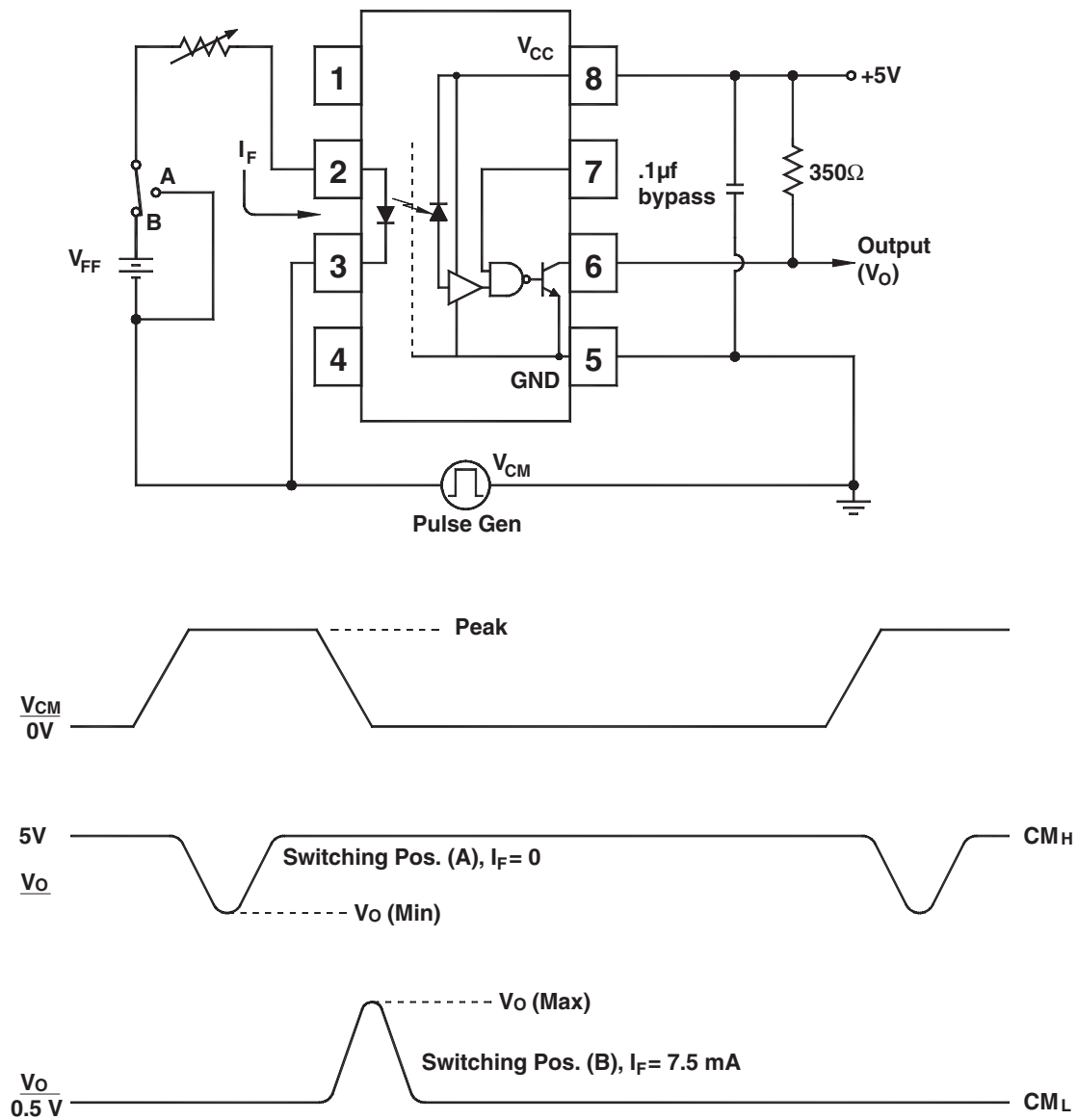


**Fig. 13 Test Circuit  $t_{EHL}$  and  $t_{ELH}$ .**



**HCPL-0600**

**HCPL-0601**



**Fig. 14 Test Circuit Common Mode Transient Immunity**

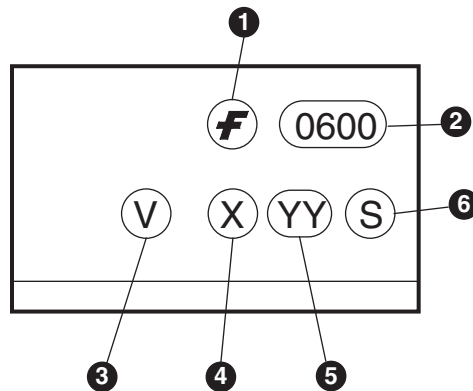
**HCPL-0600**

**HCPL-0601**

**ORDERING INFORMATION**

Option	Order Entry Identifier	Description
R1	.R1	Tape and Reel (500 per Reel)
R2	.R2	Tape and Reel (2500 per Reel)

**MARKING INFORMATION**

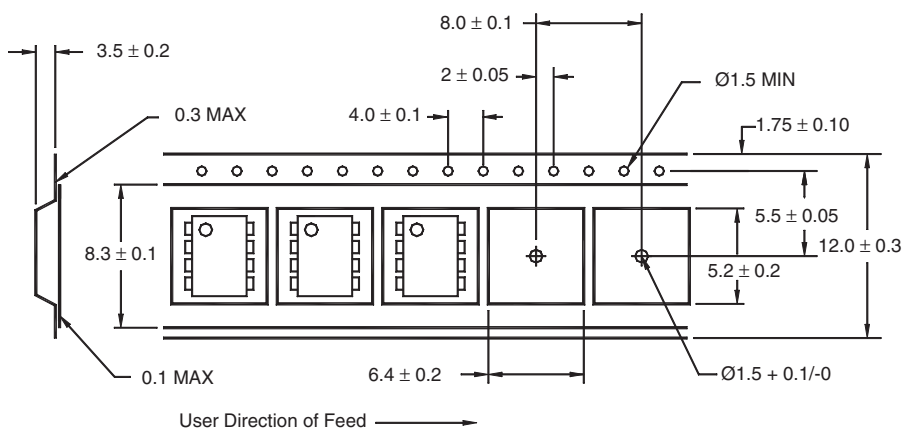


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

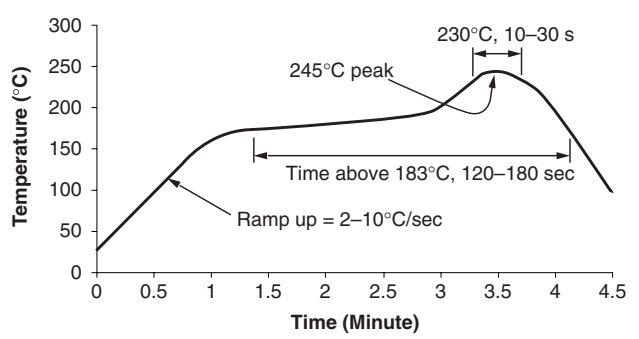
**HCPL-0600**

**HCPL-0601**

**Carrier Tape Specifications**



**Reflow Profile**



- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120-180 seconds
- One time soldering reflow is recommended

---

**HCPL-0600**

**HCPL-0601**

---

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.