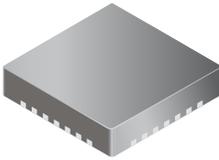


## Single Phase Fan Pre-Driver

### FEATURES AND BENEFITS

- Synchronous rectification for low power dissipation
- Drives four N-channel MOSFETs
- Internal UVLO and thermal shutdown circuitry
- Hall element input
- PWM current limiting
- Dead time protection
- FG output
- RD output
- Lock detect protection
- High  $V_{BB}$  absolute maximum
- Soft start
- A4930GETTR-T AEC-Q100 qualified

**PACKAGE: 28-pin QFN with exposed thermal pad (suffix ET)**



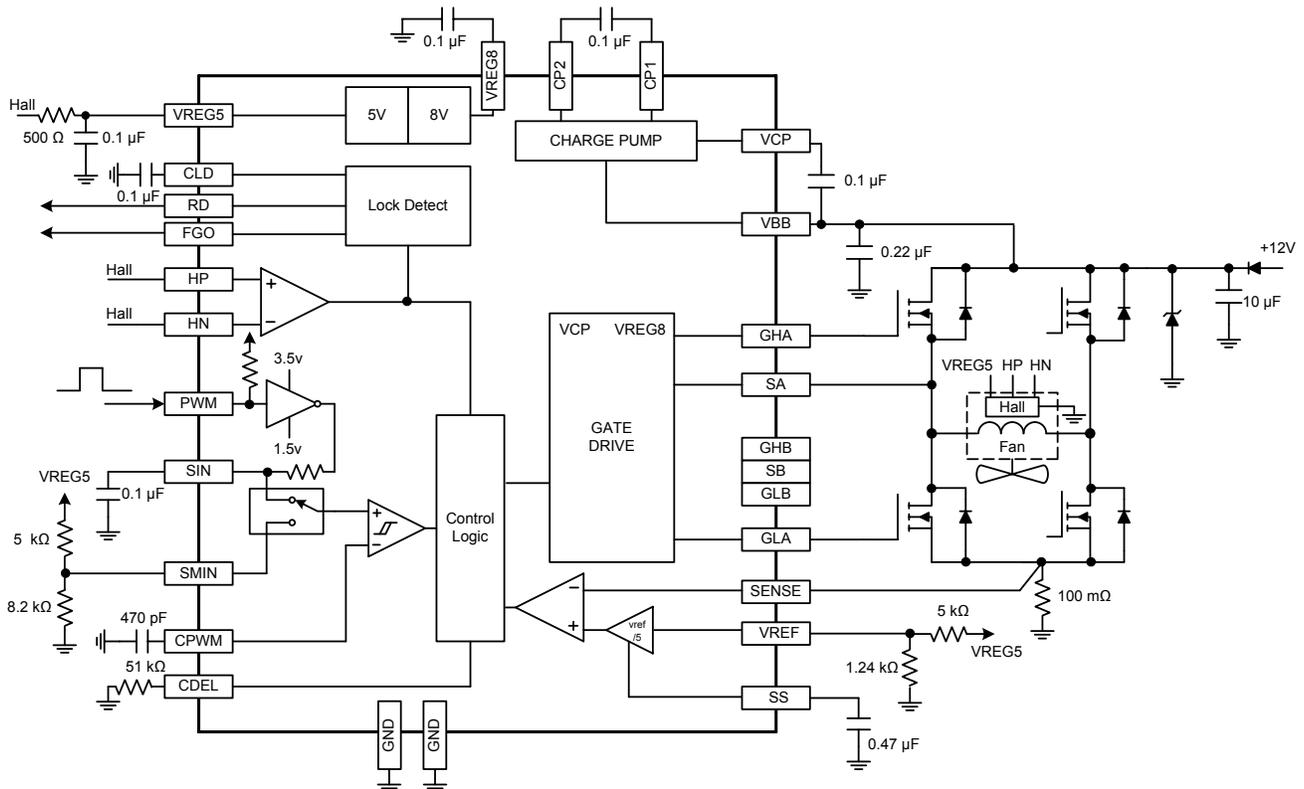
Approximate footprint

### DESCRIPTION

Designed for pulse width modulated (PWM) current control of single phase brushless fans, the A4930 minimizes external component count and integrates all the key features required for high-current fans. Internal synchronous rectification control circuitry is provided to improve power dissipation in the external MOSFETs during PWM operation. Internal circuit protection includes thermal shutdown with hysteresis, rotor lock, and dead time protection.

The A4930 is supplied in a 0.90 nominal overall height, 5 mm × 5 mm, 28-pin QFN with exposed thermal pad, (suffix ET). It is lead (Pb) free with 100% matte tin leadframe plating.

### Functional Block Diagram



## Selection Guide

Part Number	Ambient Operating Temperature, $T_A$ (°C)	Packing
A4930GETTR-T	-40 to 105	1500 pieces per 7-in. reel
A4930GETTR-C-T	-20 to 105	

## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	$V_{BB}$		36	V
Hall Input	$V_{Hx}$		-0.3 to 6	V
Logic Input Voltage Range	$V_{IN}$		-0.3 to 6	V
Operating Temperature Range	$T_A$	A4930GETTR-T	-40 to 105	°C
		A4930GETTR-C-T	-20 to 105	°C
Junction Temperature	$T_J(\max)$		150	°C
Storage Temperature Range	$T_{stg}$		-55 to 150	°C

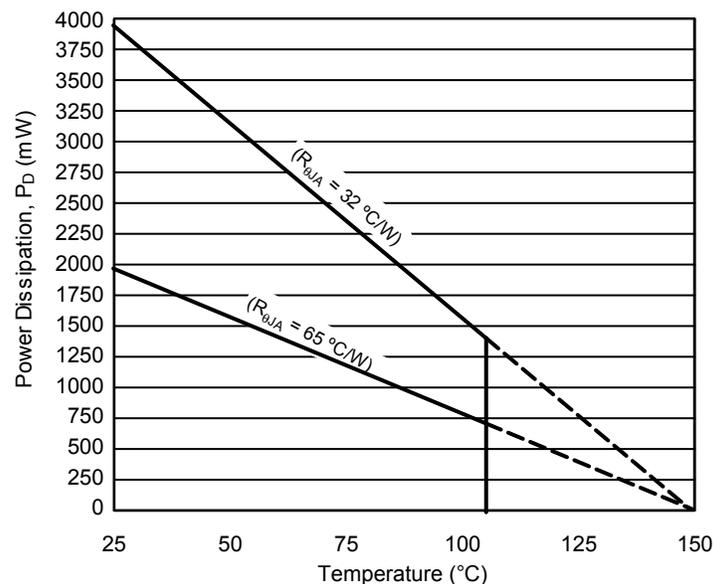
**THERMAL CHARACTERISTICS** may require derating at maximum conditions

Characteristic	Symbol	Test Conditions <sup>a</sup>	Value	Units
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	32	°C/W
		2-layer PCB with 0.7 in. <sup>2</sup> copper area	65	°C/W
Package Thermal Resistance (Junction to Case)	$R_{\theta JC}$		20 <sup>b</sup>	°C/W

<sup>a</sup>Additional thermal information available on Allegro™ website.

<sup>b</sup>Estimated.

**Power Dissipation versus Ambient Temperature**



**ELECTRICAL CHARACTERISTICS<sup>1</sup> valid at  $T_A = 25^\circ\text{C}$ ,  $V_{BB} = 12\text{ V}$ , unless noted otherwise**

Characteristic	Symbol	Test Conditions	Min.	Typ. <sup>2</sup>	Max.	Units
Load Supply Voltage Range	$V_{BB}$	Operating	8	12	36	V
Motor Supply Current	$I_{BB}$	$f_{PWM} < 30\text{ kHz}$ , $C_{load} = 1000\text{ pf}$	–	5	7	mA
VREG5	$V_5$	$I_{load} = 10\text{ mA}$	4.7	5	5.3	V
VREG5 Current Limit	$I_{REG5}$		15	–	–	mA
VREG5 Load Regulation	$V_{REG5}$	$I_{REG5} = 1\text{ to }10\text{ mA}$	–	12	30	mV
<b>Control Logic</b>						
Logic Input Voltage	$V_{IN(1)}$		2	–	–	V
	$V_{IN(0)}$		–	–	0.8	V
PWM Pin Input Current	$I_{IN(0)}$	$V_{IN} = 0$ , 50 k $\Omega$ pull-up	–	–100	–	$\mu\text{A}$
Other Logic Pin Input Current	$I_{IN(1)}$	$V_{IN} = 3.3$	–	–34	–	$\mu\text{A}$
<b>Gate Drive</b>						
High Side Gate Drive Output	$V_{GHx}$	Relative to $V_{BB}$ , $V_{BB} = 12\text{ V}$	7	–	–	V
Low Side Gate Drive Output	$V_{GLx}$		7	–	8.5	V
Gate Drive Current Turn-on	$I_G$	$GHx = GLx = 4\text{ V}$	–	20	–	mA
Gate Drive Pulldown	$R_{DS}$		–	40	–	$\Omega$
Dead Time	$t_{DEAD}$		700	1000	1300	ns
<b>Control</b>						
Soft Start Time	$t_{SS}$	$C_{LD} = 0.47\text{ }\mu\text{F}$	–	300	–	ms
Internal PWM Frequency	$f_{PWM}$	$C_{PWM} = 470\text{ pF}$	15	21	27	kHz
CPWM Output Voltage	$V_{PP}$	$C_{PWM} = 470\text{ pF}$	–	2	–	V
CPWM Low Threshold	$V_{LO}$		–	1.5	–	V
CPWM High Threshold	$V_{HI}$		–	3.5	–	V
SIN Input Impedance	$Z_{IN}$		–	200	–	k $\Omega$
<b>Protection</b>						
Thermal Shutdown Temperature	$T_{JTSD}$		–	165	–	$^\circ\text{C}$
Thermal Shutdown Hysteresis	$T_{JTSDhys}$		–	15	–	$^\circ\text{C}$

Continued on the next page...

**ELECTRICAL CHARACTERISTICS<sup>1</sup> (continued) valid at  $T_A = 25^\circ\text{C}$ ,  $V_{BB} = 12\text{ V}$ , unless noted otherwise**

Characteristic	Symbol	Test Conditions	Min.	Typ. <sup>2</sup>	Max.	Units
VBB Undervoltage Lockout Enable Threshold	$V_{BBUV}$	Rising $V_{BB}$	–	7.5	7.85	V
VBB Undervoltage Lockout Hysteresis	$V_{BBUVhys}$		0.3	0.8	–	V
VCP Undervoltage Lockout Enable Threshold	$V_{CPIUV}$	Relative to $V_{BB}$ , $V_{BB}$ rising	–	5.4	–	V
Lock Detect On-Time	$t_{LDoN}$	$C_{LD} = 0.1\ \mu\text{F}$	–	1	–	s
Lock Detect Off-Time	$t_{LDoff}$	$C_{LD} = 0.1\ \mu\text{F}$	–	15	–	s
<b>Hall Logic</b>						
Hall Input Current	$I_{HALL}$	$V_{IN} = 1.2\text{ V}$	–1	0	1	$\mu\text{A}$
Common Mode Input Range	$V_{CMR}$		0.2	–	3	V
AC Input Voltage Range	$V_{HALL}$		60	–	–	$\text{mV}_{p-p}$
Hall Threshold	$V_{th}$	Difference in Halls at FG transition	–	10	–	mV
Hysteresis Width	$V_{HYS}$		5	20	35	mV
Pulse Reject Filter	$t_{CD}$		1	2	3	$\mu\text{s}$
Commutation Delay	$V_{PU}$	$R_{CDEL} = 50\ \text{k}\Omega$	–	50	–	mV
<b>FG and RD Outputs</b>						
Output Saturation Voltage	$V_{OL}$	$I = 2\ \text{mA}$	–	0.27	0.4	V
Leakage Current	$V_{OH}$	$V = 5\ \text{V}$	–	–	1	$\mu\text{A}$

<sup>1</sup>For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

<sup>2</sup>Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

## Functional Description

**VREG5** This pin should be decoupled with a 0.1  $\mu\text{F}$  capacitor to ground. VREG5 can supply up to 15 mA, which can be used to power the external Hall element.

**VREG8** This pin should be decoupled with a 0.1  $\mu\text{F}$  capacitor to ground. VREG8 is used to power the low-side gate drive circuits.

**Charge Pump** The charge pump is used to generate a supply above  $V_{\text{BB}}$  to drive the high-side MOSFETs. The VCP voltage is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

**Lock Detect** The IC detects a locked rotor condition by checking to ensure that the FG output signal is continuously changing. The length of time allowed for a stoppage before evaluating a locked condition,  $t_{\text{LD}}$ , is set by a capacitor connected to the CLD pin.  $C_{\text{LD}}$  produces a triangle waveform with a frequency that is linearly related to the capacitor value. The definition of  $t_{\text{LD}}$  is defined as 8 cycles of this triangle waveform, and its value can be calculated as:

$$t_{\text{LD}} = C_{\text{LD}} \times (10 \text{ s} / \mu\text{F}) \quad (1)$$

If an FG transition is not detected within  $t_{\text{LD}}$ , the IC will disable the appropriate source driver and hold both sink drivers on. The circuit will automatically retry with a 15:1 ratio of off-time to on-time. An RD pin logic high indicates this fault condition.

**Current Limit and Soft Start** To minimize demand on the power supply, peak current is controlled. Initially, with the fan at a stand-still, the turn-on of the bridge results in current rising according to the L/R time constant of the motor. To prevent over-stress, this peak current is regulated by an internal PWM control circuit. When the outputs of the full-bridge are turned on, current increases in the motor winding until it reaches a value given by:

$$I_{\text{TRIP}} = V_{\text{REF}} / 5 \times R_{\text{SENSE}} \quad (2)$$

The  $R_{\text{SENSE}}$  value should be chosen to keep the peak sense voltage within the range of 200 to 500 mV, according to the relationship:

$$R_{\text{SENSE}} < 500 \text{ mV} / I_{\text{TRIP}} \quad (3)$$

At the trip point, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for 50  $\mu\text{s}$ .

A soft start capacitor,  $C_{\text{SS}}$ , can be connected to the SS pin to set the rate for slowly ramping-up the load current to the maximum value, according to the relationship:

$$t_{\text{SS}} = (C_{\text{SS}} \times V_{\text{REF}}) / 3.3\text{E-}6 \quad (4)$$

In this case the current limit will likely not be achieved and there will be less demand on the input power supply. If this feature is not utilized, the SS pin should be left open.

**Synchronous Rectification** When a PWM off-cycle is triggered, load current recirculates. The A4930 synchronous rectification feature turns on the appropriate MOSFETs during current decay, and effectively shorts out the body diodes of the low  $R_{\text{DS(on)}}$  driver.

**TSD** If the die temperature exceeds approximately 165°C, the outputs will be disabled until the internal temperature falls below a hysteresis level of 15°C.

**Shutdown** In the event of a fault due to excessive junction temperature, or low voltage on VCP or VBB, the outputs of the device are disabled until the fault condition is removed. At power-up the UVLO circuit disables the drivers until the UVLO threshold is reached.

**CPWM** This capacitor sets the frequency of the internal PWM circuit. The value is typically from 15 to 30 kHz.

**PWM** The IC accepts a direct input PWM signal with a level in the range from 0 to 6 V. The duty cycle, DC, of the input to this pin is converted to an analog voltage that is output on the SIN terminal as follows:

$$V_{\text{SIN}} = 3.5 \text{ V} - 2 \times \text{DC} \quad (5)$$

If the PWM input is not used, then leave this pin open circuit. Direct external PWM control can be utilized by applying the signal to the SIN input (refer to the Applications Information section). This can be implemented to create different PWM input to PWM output transfer functions.

**SIN** An analog voltage input to this pin sets the duty cycle applied to the fan winding. For temperature-based systems, connect SIN to a thermistor output. For systems with direct input to the PWM pin, the pin should be decoupled with a 0.1  $\mu\text{F}$  capacitor. If variable fan speed is not required, for 100% duty cycle, connect this pin to GND. The input impedance is 200  $\text{k}\Omega$  (referenced to a 3.5 or 1.5 V rail).

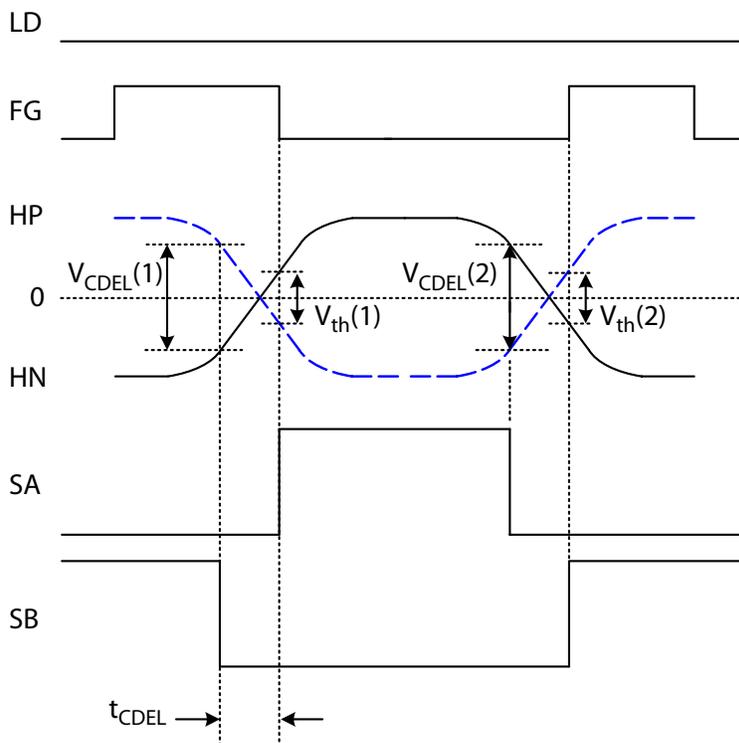
**SMIN** An analog voltage input to this pin sets the minimum speed duty cycle to the fan winding. The PWM comparator chooses either SIN or SMIN to determine the output duty cycle, which-

ever is set to a lower voltage. For 100% duty cycle applications, connect this pin to GND.

**CDEL** A resistor connected between this pin and GND sets the level at which the A4930 switches to slow decay mode in advance of the Hall zero crossing as shown here:

$$V_{\text{CDEL}} = (2950 / R_{\text{CDEL}}) - 7 \text{ mV} \quad (\text{mV}) \quad (6)$$

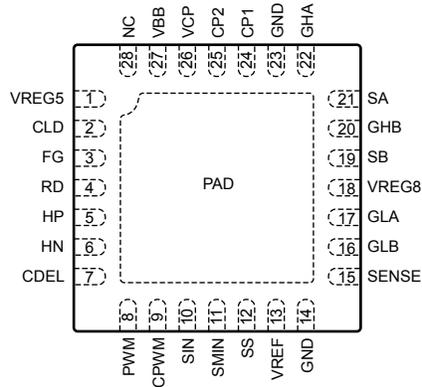
The resistor should be 25 to 100  $\text{k}\Omega$ . If this feature is not used, the CDEL pin should be pulled up to  $V_{\text{REG5}}$  with a 5  $\text{k}\Omega$  resistor.



$$\begin{aligned} V_{\text{th}}(1) &= V_{\text{HP}} - V_{\text{HN}} = 10 \text{ mV (Typical)} \\ V_{\text{th}}(2) &= V_{\text{HN}} - V_{\text{HP}} = 10 \text{ mV (Typical)} \\ V_{\text{HYS}} &= V_{\text{th}}(1) + V_{\text{th}}(2) = 20 \text{ mV (Typical)} \end{aligned}$$



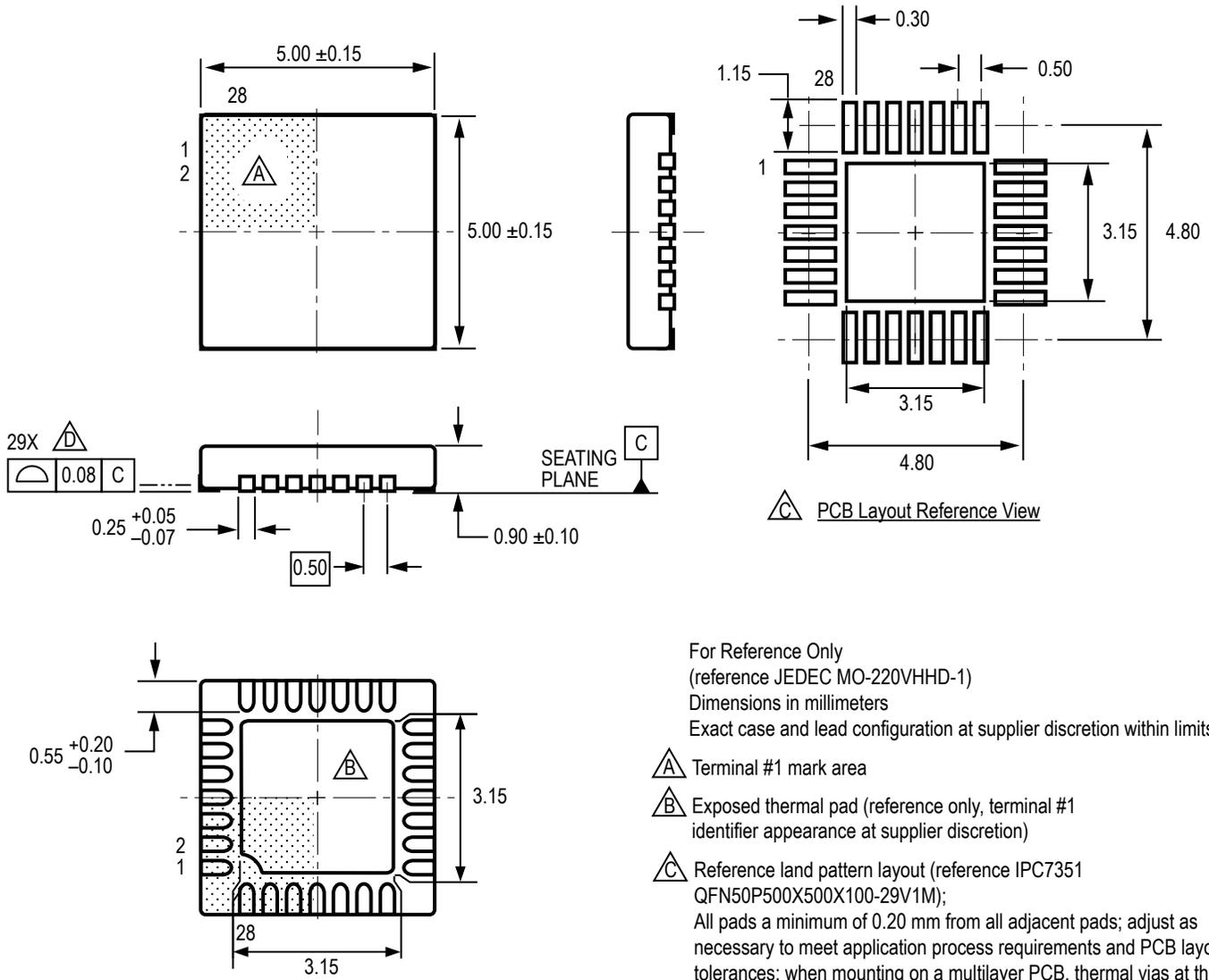
Pinout Diagram



Terminal List

Number	Name	Description	Number	Name	Description
1	VREG5	Regulator decoupling terminal	16	GLB	Low-side drive for external N-channel MOSFET
2	CLD	Capacitor to set Lock Detect Time	17	GLA	Low-side drive for external N-channel MOSFET
3	FG	FG output, fan speed indicator (open drain)	18	VREG8	Gate drive supply
4	RD	RD output, high for locked rotor condition (open drain)	19	SB	High-side source connection
5	HP	Hall input positive	20	GHB	High-side drive for external N-channel MOSFET
6	HN	Hall input negative	21	SA	High-side source connection
7	CDEL	Commutation delay	22	GHA	High-side drive for external N-channel MOSFET
8	PWM	PWM input	23	GND	Ground
9	CPWM	Capacitor to set internal frequency	24	CP1	Charge pump capacitor terminal
10	SIN	Speed analog input/adjusted PWM output	25	CP2	Charge pump capacitor terminal
11	SMIN	Minimum speed analog input	26	VCP	Reservoir capacitor terminal
12	SS	Connection for soft start capacitor	27	VBB	Supply voltage
13	VREF	Current limit setpoint	28	NC	Not connected
14	GND	Ground	-	Pad	Thermal pad, connect to GND plane with vias to bottom of PCB
15	SENSE	Sense resistor connection			

Package ET 28-Pin QFN with Exposed Thermal Pad



For Reference Only  
 (reference JEDEC MO-220VHHD-1)  
 Dimensions in millimeters  
 Exact case and lead configuration at supplier discretion within limits shown

- A** Terminal #1 mark area
- B** Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- C** Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- D** Coplanarity includes exposed thermal pad and terminals

Revision	Change	Pages	Responsible	Date
2	Revised Operating Temperature Range	2	R. Fennelly	February 26, 2014
3	Revised Features and Benefits	1	R. Fennelly	March 12, 2014
4	Minor editorial updates	All	R. Couture	February 10, 2020

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