AUTOMOTIVE, 125°C OPERATION, CMOS OPERATIONAL AMPLIFIER

Rev.1.1_00

This IC incorporates a general purpose analog circuit in a small package. This is a CMOS type operational amplifier with phase compensation circuit, which operates at a low voltage and low current consumption.
The S-19610AB is a dual operational amplifier (2 circuits).

Caution   This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.

■ Features

- Low input offset voltage: V_{IO} = +6.0 mV max. (Ta = −40°C to +125°C)
- Operation power supply voltage range: V_{DD} = 2.70 V to 5.50 V
- Low current consumption (Per circuit): I_{DD} = 1.00 mA typ.
- Internal phase compensation: No external parts required
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified[1]

   [1].   Contact our sales office for details.

■ Applications

- Current sensing
- Signal amplification
- Buffer
- Active filter

■ Package
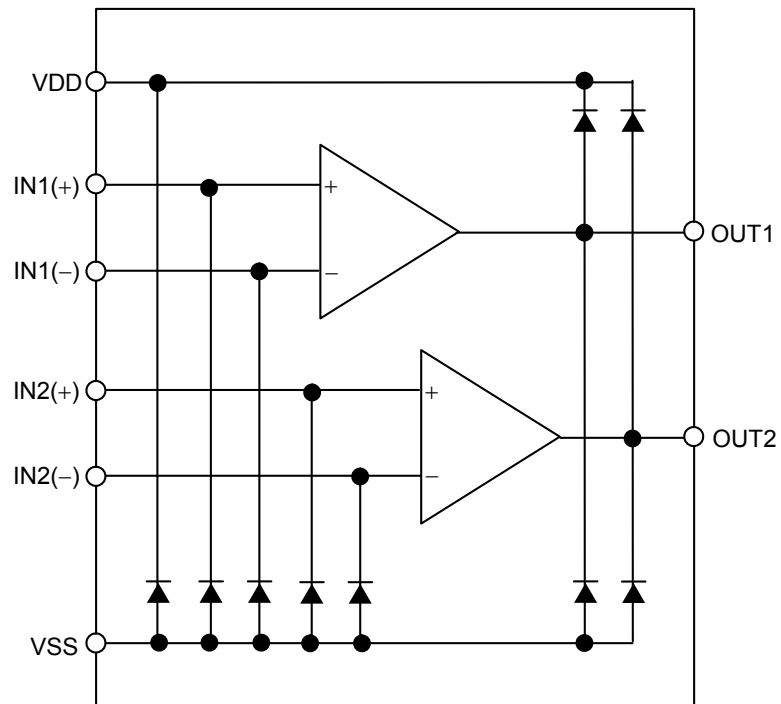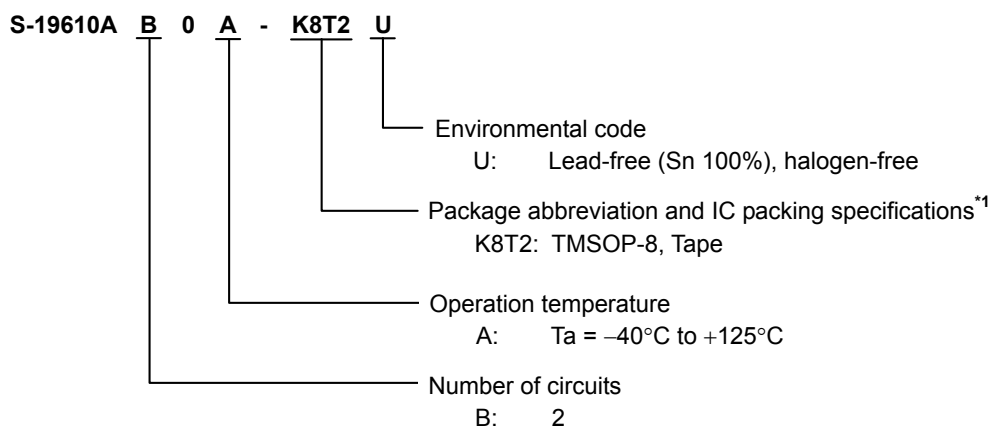
- TMSOP-8

■ **Block Diagram**

Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for the operation temperature grade 1.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

Refer to "**1.   Product name**" regarding the contents of product name, "**2.   Package**" regarding the package drawings and "**3.   Product name list**" regarding the product type.

1.   Product name

S-19610A B 0 A - K8T2 U

Environmental code
    U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications[1]
    K8T2: TMSOP-8, Tape

Operation temperature
    A: Ta = −40°C to +125°C

Number of circuits
    B: 2

*1.   Refer to the tape drawing.

2.   Package

Table 1   Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3.   Product name list

Table 2

Product Name	Package
S-19610AB0A-K8T2U	TMSOP-8

■ Pin Configuration

1. TMSOP-8

Top view
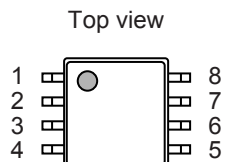
Figure 2

Table 3

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

■ Absolute Maximum Ratings

Table 4

(Ta = −40°C to +125°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Input voltage	$V_{IN(+)}$, $V_{IN(-)}$	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Output voltage	V_{OUT}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Differential input voltage	V_{IND}	± 7.0	V
Output pin current	I_{SOURCE}	20.0	mA
	I_{SINK}	20.0	mA
Operation ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−55 to +150	°C

Caution   **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance[1]	θ_{JA}	TMSOP-8	Board A	–	160	–	°C/W
			Board B	–	133	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

[1]. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Recommended operation condition

Table 6

(Ta = −40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation power supply voltage range	V_{DD}	−	2.70	5.00	5.50	V	−

2. V_{DD} = 5.0 V

Table 7

DC Electrical Characteristics   (Ta = −40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (2 circuits)	I_{DD}	$V_{CMR} = V_{OUT} = \dfrac{V_{DD}}{2}$, Ta = +25°C	−	2.00	2.50	mA	5
Input offset voltage	V_{IO}	$V_{CMR} = \dfrac{V_{DD}}{2}$	−6.0	±3.0	+6.0	mV	1
Input offset voltage drift	$\dfrac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = \dfrac{V_{DD}}{2}$	−	±3	−	μV/°C	1
Input bias current	I_{BIAS}	Ta = +25°C	−	1	−	pA	−
Input offset current	I_{IO}	Ta = +25°C	−	1	−	pA	−
Common-mode input voltage range	V_{CMR}	Ta = +25°C	−0.1	−	3.8	V	2
Voltage gain (open loop)	A_{VOL}	$V_{OUT} = V_{SS} + 0.5$ V to $V_{DD} − 0.5$ V, $V_{CMR} = \dfrac{V_{DD}}{2}$, $R_L = 1.0$ MΩ, Ta = +25°C	88	110	−	dB	8
Maximum output swing voltage	V_{OH}	$R_L = 1.0$ MΩ	4.9	−	−	V	3
	V_{OL}	$R_L = 1.0$ MΩ	−	−	0.1	V	4
Common-mode input signal rejection ratio	CMRR	$V_{CMR} = V_{SS} − 0.1$ V to $V_{DD} − 1.2$ V, Ta = +25°C	70	85	−	dB	2
Power supply voltage rejection ratio	PSRR	2.70 V ≤ V_{DD} ≤ 5.50 V, Ta = +25°C	70	90	−	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} − 0.12$ V, Ta = +25°C	5.0	−	−	mA	6
Sink current	I_{SINK}	$V_{OUT} = 0.12$ V, Ta = +25°C	5.0	−	−	mA	7

Table 8

AC Electrical Characteristics   (Ta = −40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Slew rate	SR	$R_L = 1.0$ MΩ, $C_L = 15$ pF (Refer to **Figure 11**)	−	2.00	−	V/μs
Gain-bandwidth product	GBP	$C_L = 0$ pF	−	3.00	−	MHz

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■ Test Circuits (Per Circuit)

1. Power supply voltage rejection ratio, input offset voltage

V_{DD}

R_F

R_S

R_S

R_F

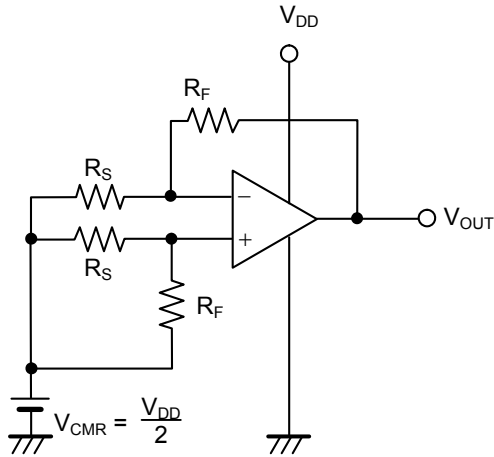V_{OUT}

$V_{CMR} = \dfrac{V_{DD}}{2}$

Figure 3   Test Circuit 1

● **Power supply voltage rejection ratio (PSRR)**

The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with V_{OUT} measured at each V_{DD}.

Test conditions:
   V_{DD} = 2.70 V: V_{DD} = V_{DD1}, V_{OUT} = V_{OUT1}
   V_{DD} = 5.50 V: V_{DD} = V_{DD2}, V_{OUT} = V_{OUT2}

$$\text{PSRR} = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{\left(V_{OUT1} - \frac{V_{DD1}}{2}\right) - \left(V_{OUT2} - \frac{V_{DD2}}{2}\right)} \right| \times \frac{R_F + R_S}{R_S} \right)$$

● **Input offset voltage (V_{IO})**

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

2. Common-mode input signal rejection ratio, common-mode input voltage range

V_{DD}

R_F

R_S

R_S

R_F

V_{OUT}

V_{IN}

$\dfrac{V_{DD}}{2}$
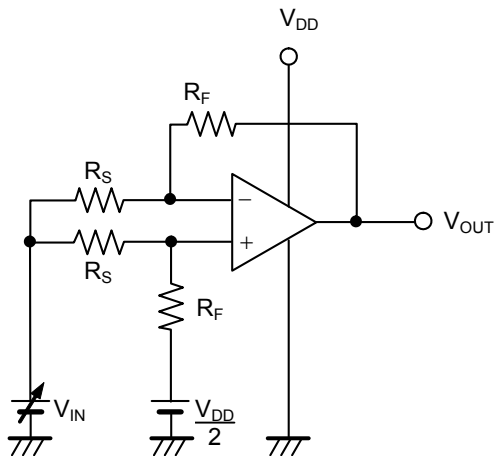
Figure 4   Test Circuit 2

● **Common-mode input signal rejection ratio (CMRR)**

The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with V_{OUT} measured at each V_{IN}.

Test conditions:
   V_{IN} = $V_{CMR\ Max.}$: V_{IN} = V_{IN1}, V_{OUT} = V_{OUT1}
   V_{IN} = $V_{CMR\ Min.}$: V_{IN} = V_{IN2}, V_{OUT} = V_{OUT2}

$$\text{CMRR} = 20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

● **Common-mode input voltage range (V_{CMR})**

The common-mode input voltage range is the range of V_{IN} in which V_{OUT} satisfies the common-mode input signal rejection ratio specifications when V_{IN} is changed.
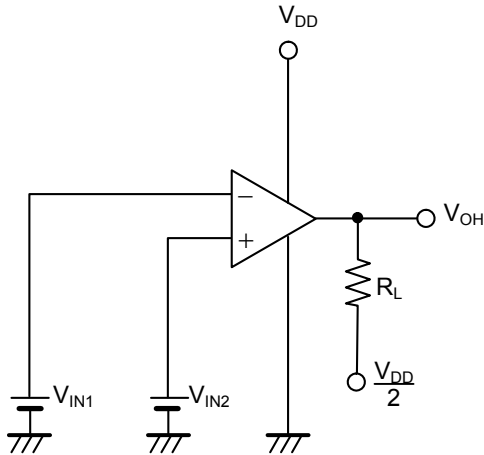
3. Maximum output swing voltage (V_{OH})

Figure 5   Test Circuit 3

- **Maximum output swing voltage (V_{OH})**

  Test conditions
  $$V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$
  $$V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$
  $$R_L = 1 \text{ M}\Omega$$
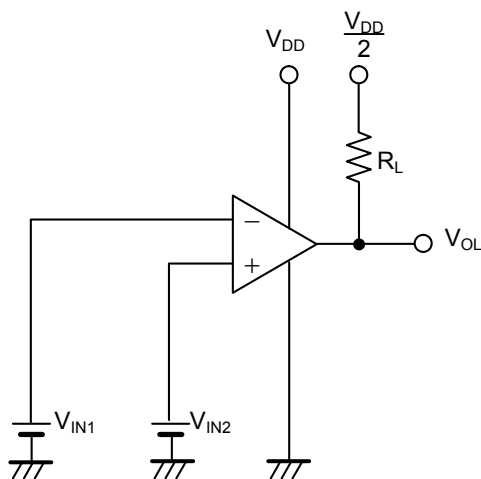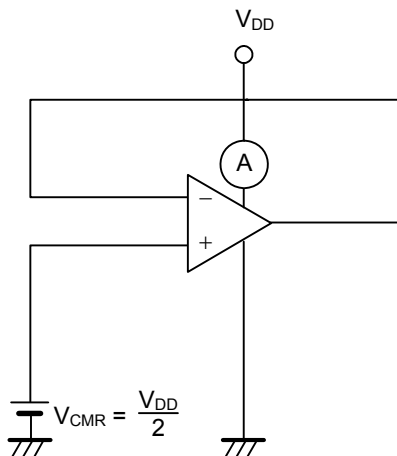
4. Maximum output swing voltage (V_{OL})

Figure 6   Test Circuit 4

- **Maximum output swing voltage (V_{OL})**

  Test conditions:
  $$V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$
  $$V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$
  $$R_L = 1 \text{ M}\Omega$$

5. Current consumption

Figure 7   Test Circuit 5

- **Current consumption (I_{DD})**

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6. Source current

V$_{DD}$

−

+

A
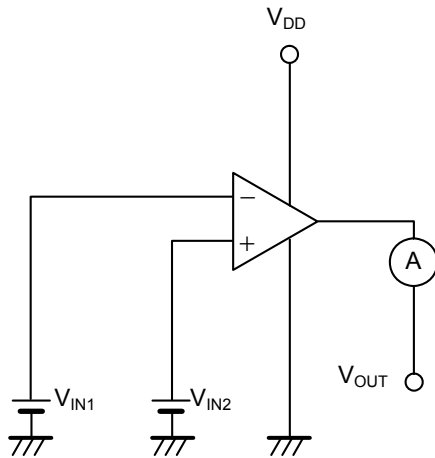
V$_{OUT}$

V$_{IN1}$

V$_{IN2}$

Figure 8   Test Circuit 6

● **Source current (I$_{SOURCE}$)**

Test conditions:
$$V_{OUT} = V_{DD} - 0.12 \text{ V}$$
$$V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$
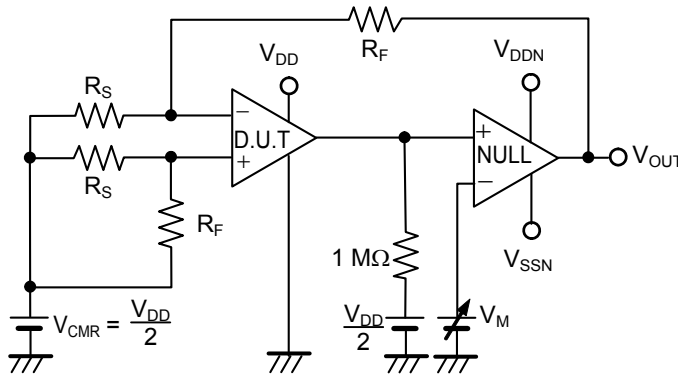$$V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

7. Sink current

V$_{DD}$ V$_{OUT}$

A

−

+
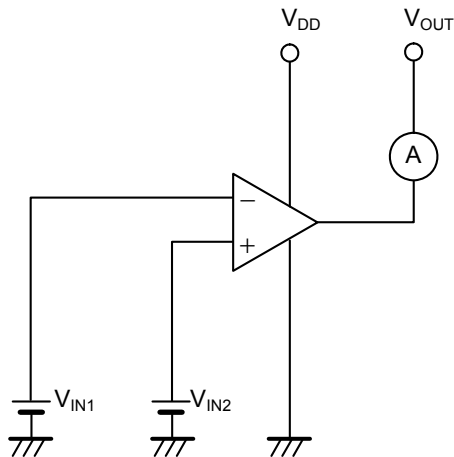
V$_{IN1}$

V$_{IN2}$

Figure 9   Test Circuit 7

● **Sink current (I$_{SINK}$)**

Test conditions:
$$V_{OUT} = V_{SS} + 0.12 \text{ V}$$
$$V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$
$$V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

8. Voltage gain

Figure 10 Test Circuit 8

• **Voltage gain (open loop) (A$_{VOL}$)**

The voltage gain (A$_{VOL}$) can be calculated by the following expression, with V$_{OUT}$ measured at each V$_M$.

Test conditions:
V$_M$ = V$_{DD}$ − 0.5 V: V$_M$ = V$_{M1}$, V$_{OUT}$ = V$_{OUT1}$
V$_M$ = 0.5 V: V$_M$ = V$_{M2}$, V$_{OUT}$ = V$_{OUT2}$

$$A_{VOL} = 20 \log \left(\left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

9. Slew rate (SR)

Measured by the voltage follower circuit.
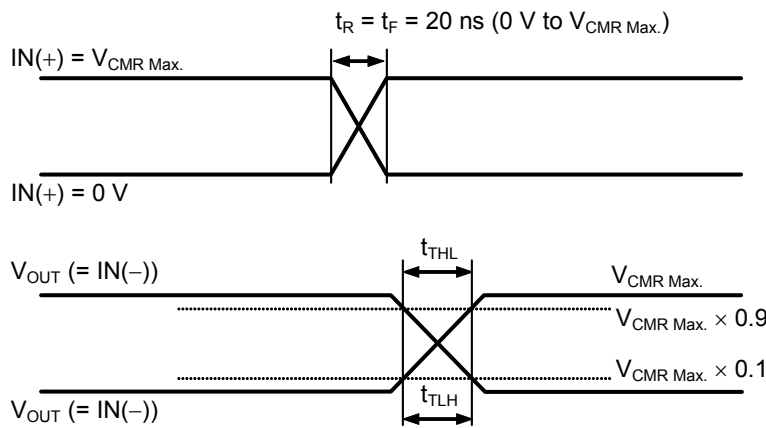
Figure 11

• **Slew rate (SR)**

$$SR = \frac{V_{CMR \ Max.} \times 0.8}{t_{TLH}}$$

$$SR = \frac{V_{CMR \ Max.} \times 0.8}{t_{THL}}$$

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■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

- Use this IC with the output current of 20 mA or less.

- This IC operates stably even directly connecting a load capacitance of 100 pF or less to the output pin, as shown in **Figure 12**. When connecting a load capacitance of 100 pF or more, connect a resistor of 47 Ω or more as shown in **Figure 13**. In case of connecting a filter for noise prevention, and connecting a load capacitance of 100 pF or more, also connect a resistor of 47 Ω or more as shown in **Figure 14**.
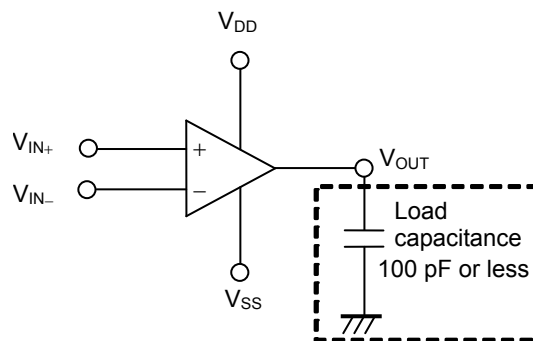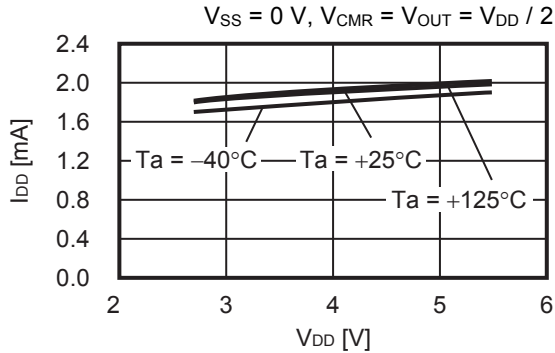

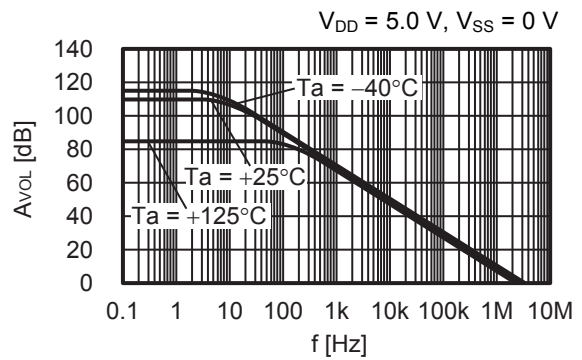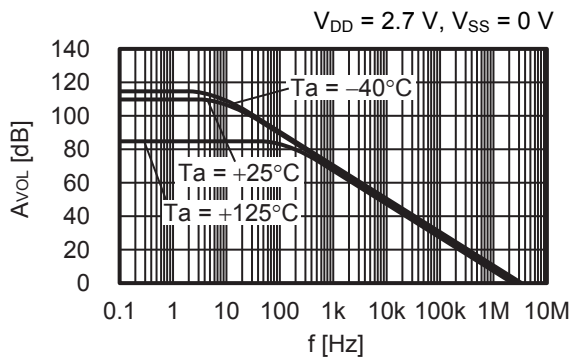**Figure 12**
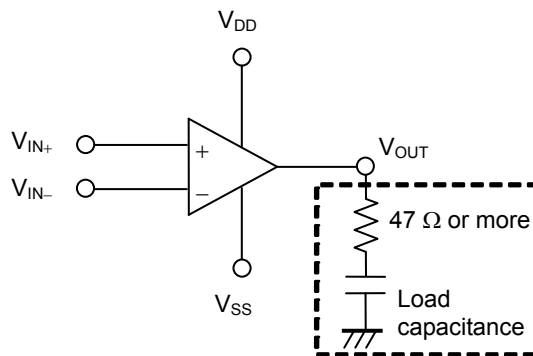
Figure 13
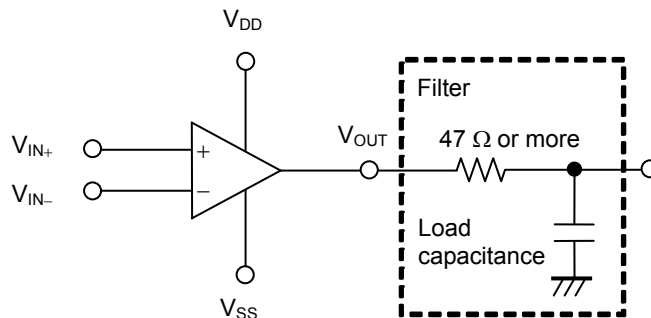
Figure 14

Caution   **The above connection diagrams and constants will not guarantee successful operation.**
Perform thorough evaluation using the actual application to set the constants.

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■ Characteristics (Typical Data)

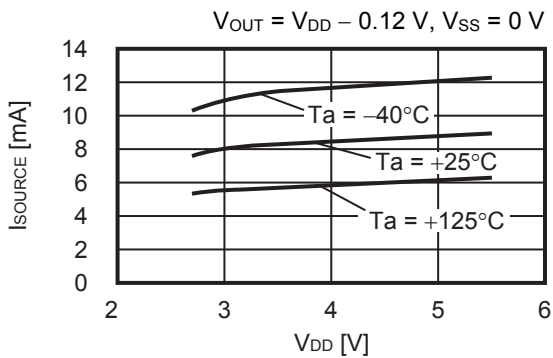### 1. Current consumption (I_{DD}) (2 circuits) vs. Power supply voltage (V_{DD})

$V_{SS} = 0$ V, $V_{CMR} = V_{OUT} = V_{DD} / 2$

2. Voltage gain (A_{VOL}) vs. Frequency (f)

$V_{DD} = 2.7$ V, $V_{SS} = 0$ V
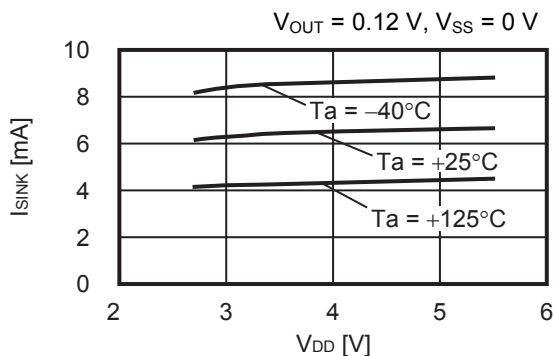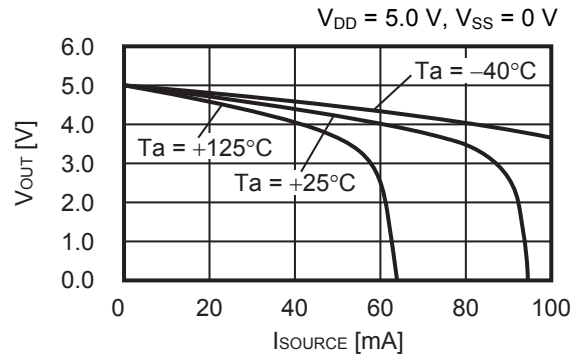
$V_{DD} = 5.0$ V, $V_{SS} = 0$ V

3. Output current

3. 1 Source current (I_{SOURCE}) vs. Power supply voltage (V_{DD})
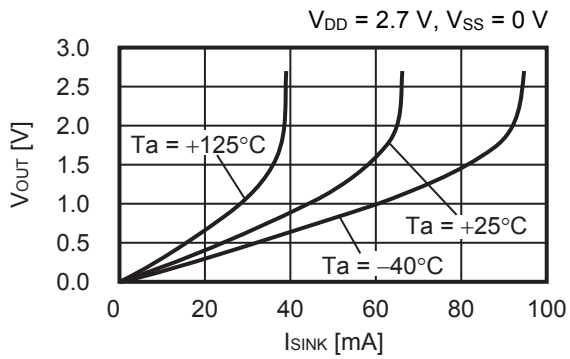
$V_{OUT} = V_{DD} - 0.12$ V, $V_{SS} = 0$ V

3. 2 Sink current (I_{SINK}) vs. Power supply voltage (V_{DD})

$V_{OUT} = 0.12$ V, $V_{SS} = 0$ V

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3. 3 Output voltage (V_OUT) vs. Source current (I_SOURCE)

V_{DD} = 2.7 V, V_{SS} = 0 V

V_{DD} = 5.0 V, V_{SS} = 0 V
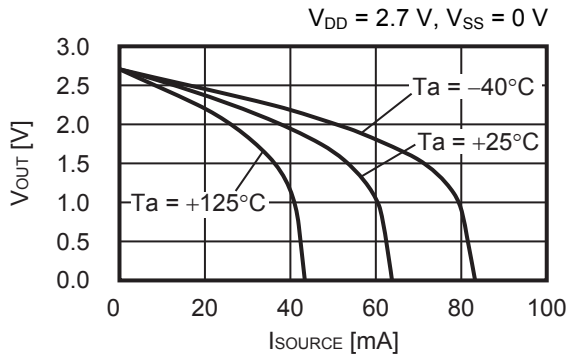
3. 4 Output voltage (V_OUT) vs. Sink current (I_SINK)

V_{DD} = 2.7 V, V_{SS} = 0 V

V_{DD} = 5.0 V, V_{SS} = 0 V
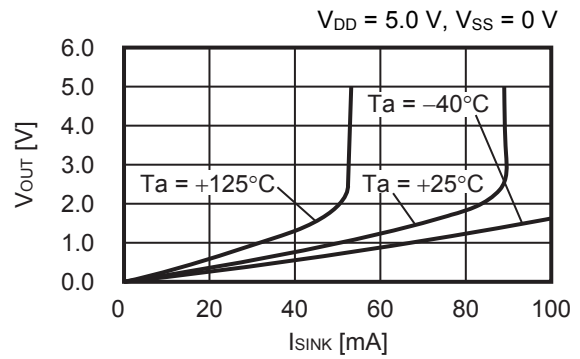
4. Input bias current (I_BIAS) vs. Temperature (Ta)

V_{DD} = 5.0 V, V_{SS} = 0 V, V_{CMR} = V_{DD} / 2
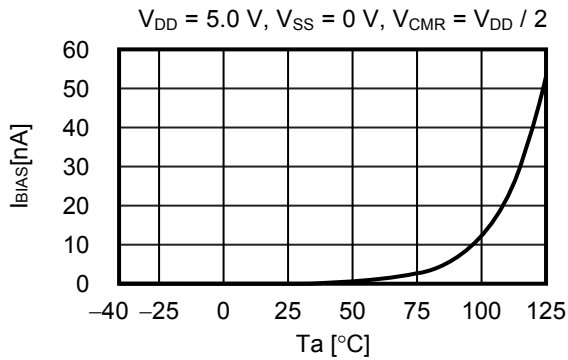
■ Power Dissipation

TMSOP-8

$T_j = +150°C$ max.
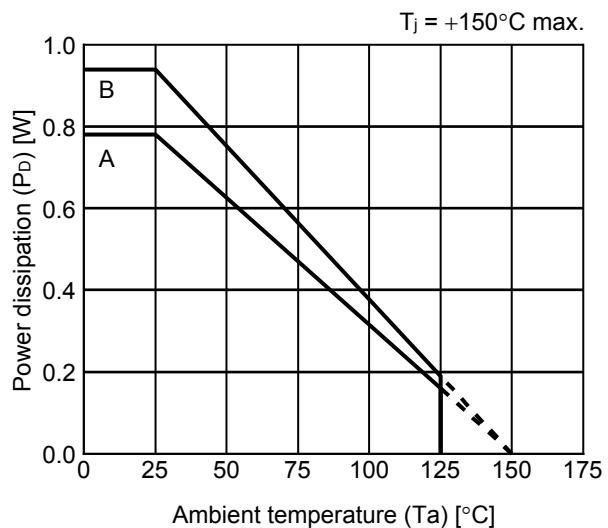
Board	Power Dissipation (P_D)
A	0.78 W
B	0.94 W
C	–
D	–
E	–

TMSOP-8 Test Board

(1) Board A

◯ IC Mount Area
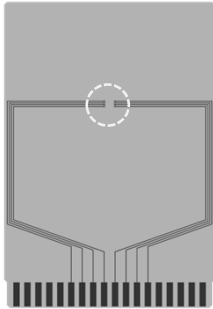
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B
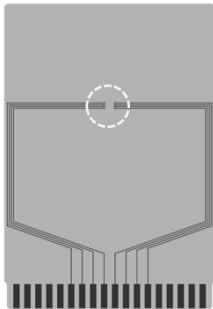
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. TMSOP8-A-Board-SD-1.0

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2.90±0.2

8   5

1   4

2.8±0.2

4.0±0.2

0.45±0.2

0.13±0.1

0.6±0.1

0.8max.

0.08±0.05

0.2±0.1

0.65±0.1
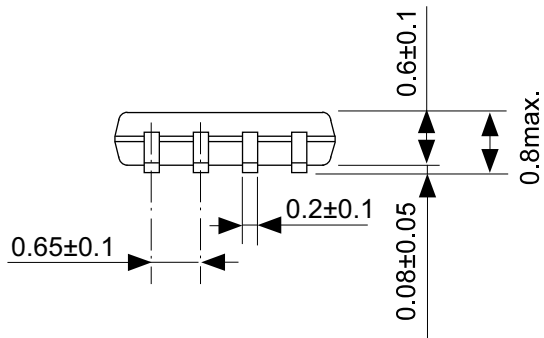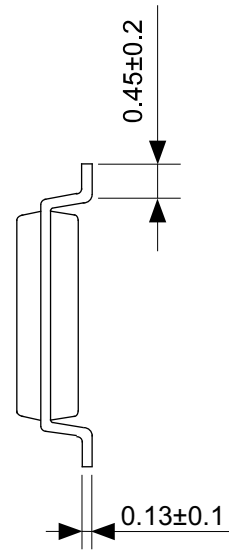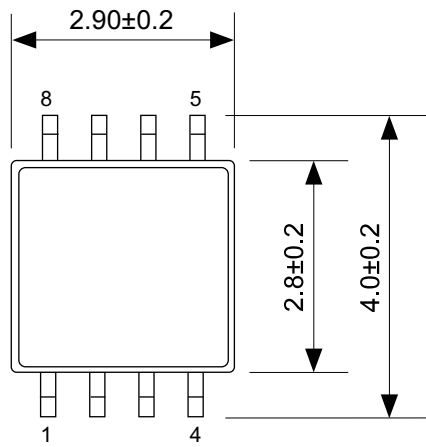
No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	⊕ ⊏
UNIT	mm

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2.00±0.05

4.00±0.1 | 4.00±0.1

1.5 +0.1 -0

1.75±0.1

1.00±0.1

5.50±0.05

12.0 +0.2 -0.1

4.25±0.05

1.05±0.05

0.30±0.05

3.25±0.05

4 1

5 8

Feed direction
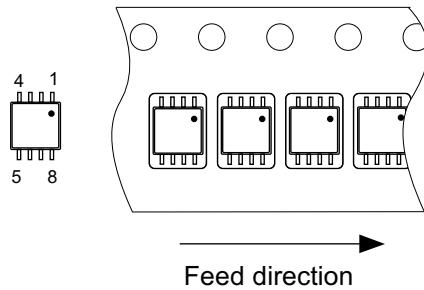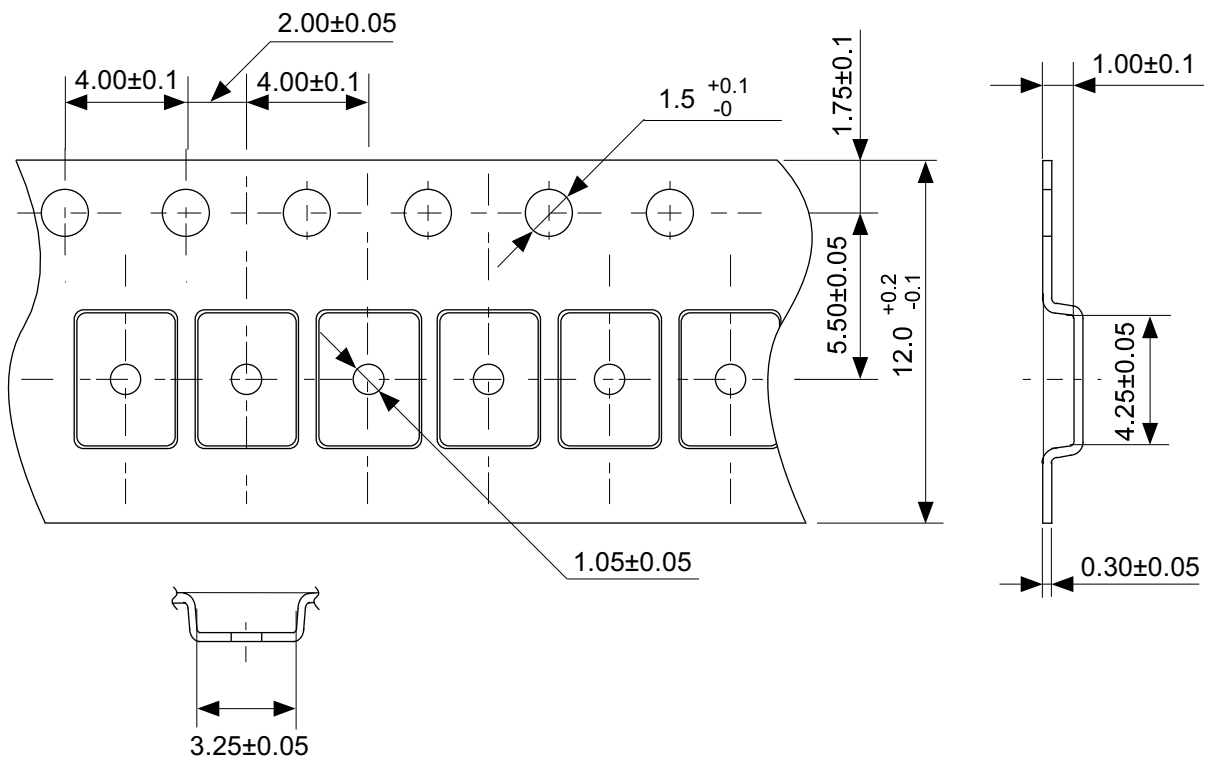
No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

16.5max.

$\varnothing 60 \, ^{+1}_{-0}$

$\varnothing 180 \, ^{+0}_{-3}$

13.0±0.3
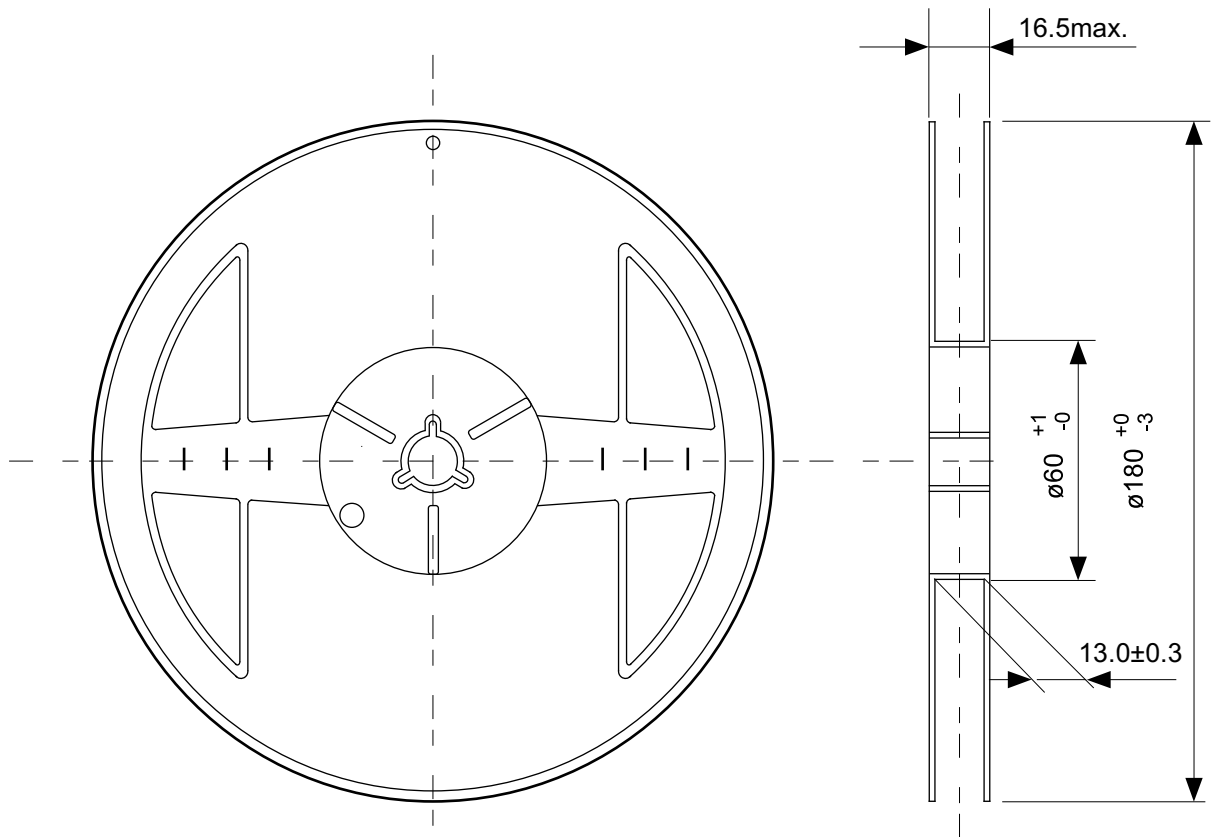
Enlarged drawing in the central part

21±0.8

13±0.2

2±0.5

(60°) (60°)
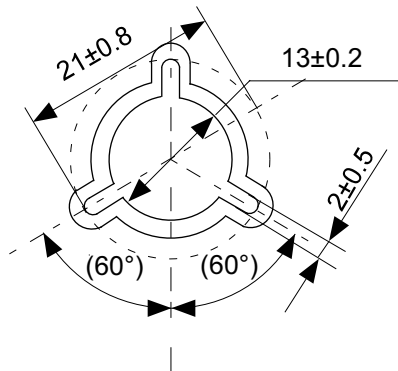
No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.

2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
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