S-809xxC Series

ULTRA-SMALL PACKAGE HIGH-PRECISION VOLTAGE DETECTOR WITH DELAY CIRCUIT (EXTERNAL DELAY TIME SETTING)

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The S-809xxC Series is a high-precision voltage detector developed using CMOS process. The detection voltage is fixed internally with an accuracy of ±2.0 %. A time delayed reset can be accomplished with the addition of an external capacitor. Two output forms, Nch open-drain and CMOS output, are available.

■ Features

- Ultra-low current consumption 1.0 μA typ. (Detection voltage ≤ 1.4 V, at V_{DD}=2.0 V)
  1.1 μA typ. (Detection voltage ≥ 1.5 V, at V_{DD}=3.5 V)
- High-precision detection voltage ±2.0 %
- Operating voltage range 0.7 V to 10.0 V
- Hysteresis characteristics 5 % typ.
- Detection voltage 1.3 V to 6.0 V (0.1 V step)
- Output forms Nch open-drain output (Active Low)
  CMOS output (Active Low)
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

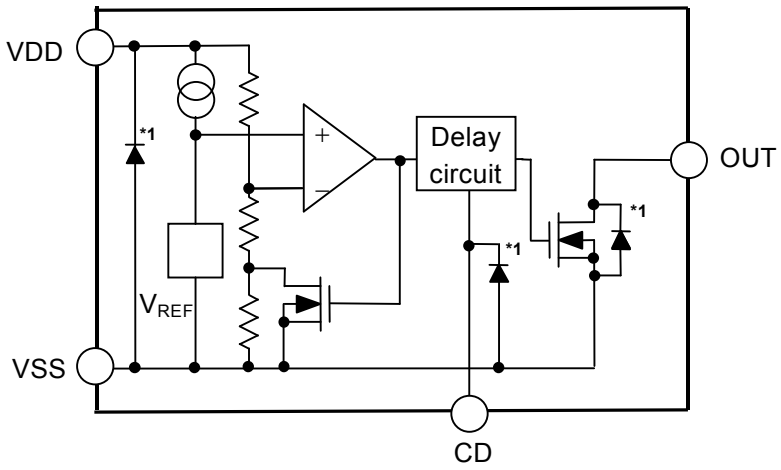
- Power supply monitor for portable equipment such as notebook PCs, digital still cameras, PDAs and cellular phones
- Constant voltage power monitor for cameras, video equipment and communication equipment
- Power monitor and reset for CPUs and microcomputers

■ Packages

- SC-82AB
- SOT-23-5
- SNT-4A

■ Block Diagrams

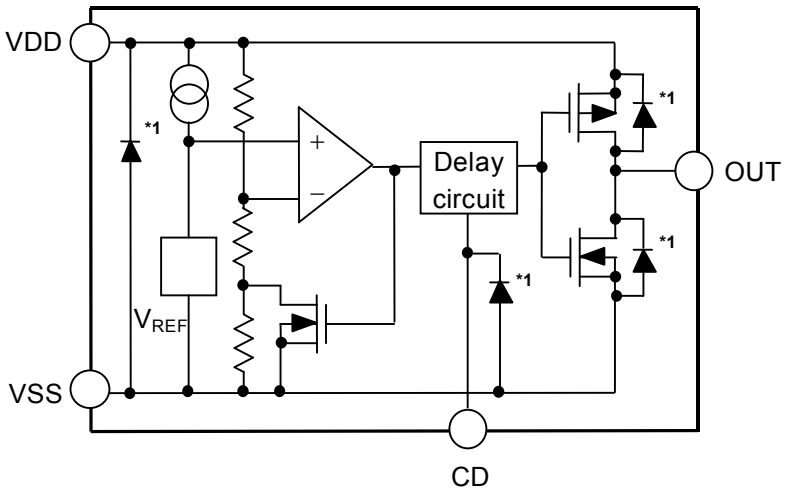
1. Nch Open-drain Output Products



***1.** Parasitic diode

Figure 1

2. CMOS Output Products



***1.** Parasitic diode

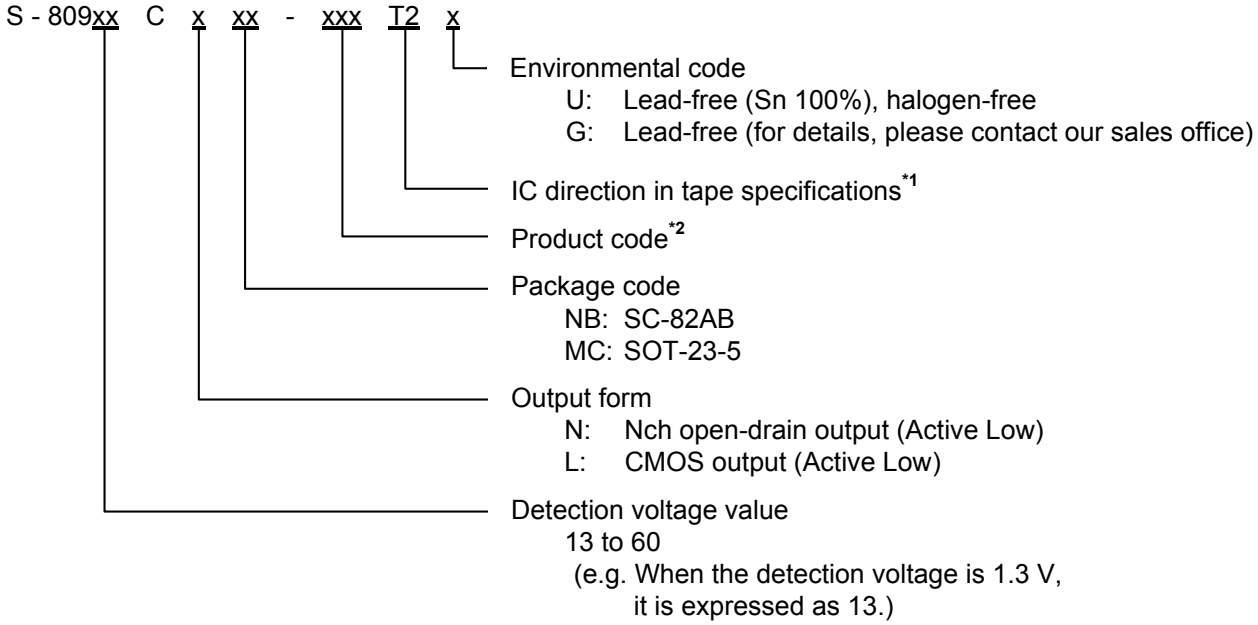
Figure 2

■ Product Name Structure

The detection voltage, output form and packages for S-809xxC Series can be selected at the user's request. Refer to the "**1. Product Name**" for the construction of the product name, "**2. Packages**" regarding the package drawings and "**3. Product Name List**" for the full product names.

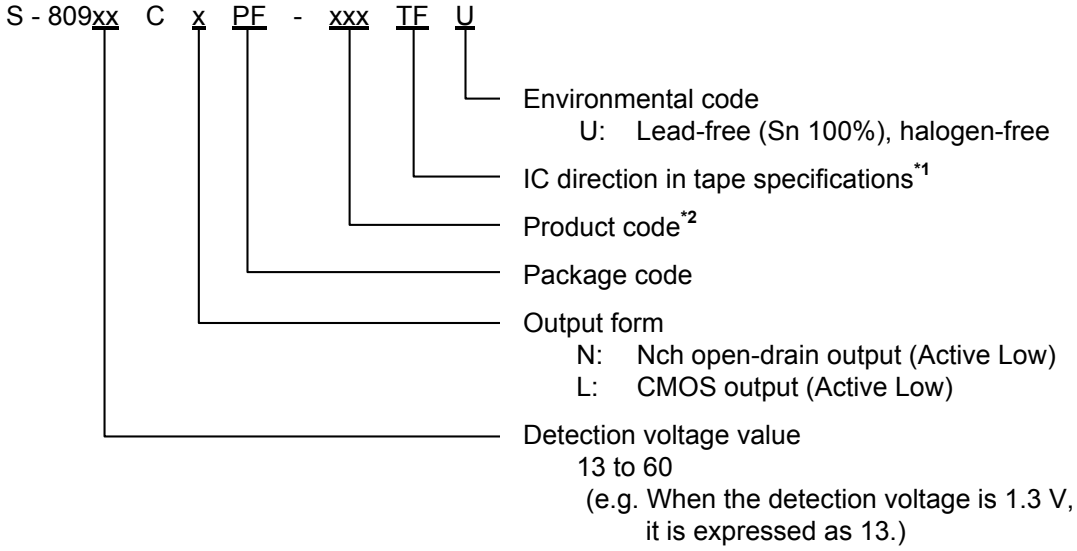
1. Product Name

1-1. SC-82AB, SOT-23-5



***1.** Refer to the taping specifications at the end of this book.
***2**. Refer to the **Table 1 to 2** in the "**3. Product Name List**"

1-2. SNT-4A



***1.** Refer to the taping specifications at the end of this book.
***2**. Refer to the **Table 1 to 2** in the "**3. Product Name List**"

2. Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD	—
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	—
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product Name List

3-1. Nch Open-drain Output Products

Table 1

Detection voltage range	Hysteresis width (Typ.)	SC-82AB	SOT-23-5	SNT-4A
1.3 V ±2.0 %	0.065 V	S-80913CNNB-G8HT2x	S-80913CNMC-G8HT2x	S-80913CNPF-G8HTFU
1.4 V ±2.0 %	0.070 V	S-80914CNNB-G8JT2x	S-80914CNMC-G8JT2x	S-80914CNPF-G8JTFU
1.5 V ±2.0 %	0.075 V	S-80915CNNB-G8KT2x	S-80915CNMC-G8KT2x	S-80915CNPF-G8KTFU
1.6 V ±2.0 %	0.080 V	S-80916CNNB-G8LT2x	S-80916CNMC-G8LT2x	S-80916CNPF-G8LTFU
1.7 V ±2.0 %	0.085 V	S-80917CNNB-G8MT2x	S-80917CNMC-G8MT2x	S-80917CNPF-G8MTFU
1.8 V ±2.0 %	0.090 V	S-80918CNNB-G8NT2x	S-80918CNMC-G8NT2x	S-80918CNPF-G8NTFU
1.9 V ±2.0 %	0.095 V	S-80919CNNB-G8PT2x	S-80919CNMC-G8PT2x	S-80919CNPF-G8PTFU
2.0 V ±2.0 %	0.100 V	S-80920CNNB-G8QT2x	S-80920CNMC-G8QT2x	S-80920CNPF-G8QTFU
2.1 V ±2.0 %	0.105 V	S-80921CNNB-G8RT2x	S-80921CNMC-G8RT2x	S-80921CNPF-G8RTFU
2.2 V ±2.0 %	0.110 V	S-80922CNNB-G8ST2x	S-80922CNMC-G8ST2x	S-80922CNPF-G8STFU
2.3 V ±2.0 %	0.115 V	S-80923CNNB-G8TT2x	S-80923CNMC-G8TT2x	S-80923CNPF-G8TTFU
2.4 V ±2.0 %	0.120 V	S-80924CNNB-G8UT2x	S-80924CNMC-G8UT2x	S-80924CNPF-G8UTFU
2.5 V ±2.0 %	0.125 V	S-80925CNNB-G8VT2x	S-80925CNMC-G8VT2x	S-80925CNPF-G8VTFU
2.6 V ±2.0 %	0.130 V	S-80926CNNB-G8WT2x	S-80926CNMC-G8WT2x	S-80926CNPF-G8WTFU
2.7 V ±2.0 %	0.135 V	S-80927CNNB-G8XT2x	S-80927CNMC-G8XT2x	S-80927CNPF-G8XTFU
2.8 V ±2.0 %	0.140 V	S-80928CNNB-G8YT2x	S-80928CNMC-G8YT2x	S-80928CNPF-G8YTFU
2.9 V ±2.0 %	0.145 V	S-80929CNNB-G8ZT2x	S-80929CNMC-G8ZT2x	S-80929CNPF-G8ZTFU
3.0 V ±2.0 %	0.150 V	S-80930CNNB-G80T2x	S-80930CNMC-G80T2x	S-80930CNPF-G80TFU
3.1 V ±2.0 %	0.155 V	S-80931CNNB-G81T2x	S-80931CNMC-G81T2x	S-80931CNPF-G81TFU
3.2 V ±2.0 %	0.160 V	S-80932CNNB-G82T2x	S-80932CNMC-G82T2x	S-80932CNPF-G82TFU
3.3 V ±2.0 %	0.165 V	S-80933CNNB-G83T2x	S-80933CNMC-G83T2x	S-80933CNPF-G83TFU
3.4 V ±2.0 %	0.170 V	S-80934CNNB-G84T2x	S-80934CNMC-G84T2x	S-80934CNPF-G84TFU
3.5 V ±2.0 %	0.175 V	S-80935CNNB-G85T2x	S-80935CNMC-G85T2x	S-80935CNPF-G85TFU
3.6 V ±2.0 %	0.180 V	S-80936CNNB-G86T2x	S-80936CNMC-G86T2x	S-80936CNPF-G86TFU
3.7 V ±2.0 %	0.185 V	S-80937CNNB-G87T2x	S-80937CNMC-G87T2x	S-80937CNPF-G87TFU
3.8 V ±2.0 %	0.190 V	S-80938CNNB-G88T2x	S-80938CNMC-G88T2x	S-80938CNPF-G88TFU
3.9 V ±2.0 %	0.195 V	S-80939CNNB-G89T2x	S-80939CNMC-G89T2x	S-80939CNPF-G89TFU
4.0 V ±2.0 %	0.200 V	S-80940CNNB-G9AT2x	S-80940CNMC-G9AT2x	S-80940CNPF-G9ATFU
4.1 V ±2.0 %	0.205 V	S-80941CNNB-G9BT2x	S-80941CNMC-G9BT2x	S-80941CNPF-G9BTFU
4.2 V ±2.0 %	0.210 V	S-80942CNNB-G9CT2x	S-80942CNMC-G9CT2x	S-80942CNPF-G9CTFU
4.3 V ±2.0 %	0.215 V	S-80943CNNB-G9DT2x	S-80943CNMC-G9DT2x	S-80943CNPF-G9DTFU
4.4 V ±2.0 %	0.220 V	S-80944CNNB-G9ET2x	S-80944CNMC-G9ET2x	S-80944CNPF-G9ETFU
4.5 V ±2.0 %	0.225 V	S-80945CNNB-G9FT2x	S-80945CNMC-G9FT2x	S-80945CNPF-G9FTFU
4.6 V ±2.0 %	0.230 V	S-80946CNNB-G9GT2x	S-80946CNMC-G9GT2x	S-80946CNPF-G9GTFU
4.7 V ±2.0 %	0.235 V	S-80947CNNB-G9HT2x	S-80947CNMC-G9HT2x	S-80947CNPF-G9HTFU
4.8 V ±2.0 %	0.240 V	S-80948CNNB-G9JT2x	S-80948CNMC-G9JT2x	S-80948CNPF-G9JTFU
4.9 V ±2.0 %	0.245 V	S-80949CNNB-G9KT2x	S-80949CNMC-G9KT2x	S-80949CNPF-G9KTFU
5.0 V ±2.0 %	0.250 V	S-80950CNNB-G9LT2x	S-80950CNMC-G9LT2x	S-80950CNPF-G9LTFU
5.1 V ±2.0 %	0.255 V	S-80951CNNB-G9MT2x	S-80951CNMC-G9MT2x	S-80951CNPF-G9MTFU
5.2 V ±2.0 %	0.260 V	S-80952CNNB-G9NT2x	S-80952CNMC-G9NT2x	S-80952CNPF-G9NTFU
5.3 V ±2.0 %	0.265 V	S-80953CNNB-G9PT2x	S-80953CNMC-G9PT2x	S-80953CNPF-G9PTFU
5.4 V ±2.0 %	0.270 V	S-80954CNNB-G9QT2x	S-80954CNMC-G9QT2x	S-80954CNPF-G9QTFU
5.5 V ±2.0 %	0.275 V	S-80955CNNB-G9RT2x	S-80955CNMC-G9RT2x	S-80955CNPF-G9RTFU
5.6 V ±2.0 %	0.280 V	S-80956CNNB-G9ST2x	S-80956CNMC-G9ST2x	S-80956CNPF-G9STFU
5.7 V ±2.0 %	0.285 V	S-80957CNNB-G9TT2x	S-80957CNMC-G9TT2x	S-80957CNPF-G9TTFU
5.8 V ±2.0 %	0.290 V	S-80958CNNB-G9UT2x	S-80958CNMC-G9UT2x	S-80958CNPF-G9UTFU
5.9 V ±2.0 %	0.295 V	S-80959CNNB-G9VT2x	S-80959CNMC-G9VT2x	S-80959CNPF-G9VTFU
6.0 V ±2.0 %	0.300 V	S-80960CNNB-G9WT2x	S-80960CNMC-G9WT2x	S-80960CNPF-G9WTFU

Remark 1. x: G or U

2. Please select products of environmental code = U for Sn 100%, halogen-free products.

3-2. CMOS Output Products

Table 2

Detection voltage range	Hysteresis width (Typ.)	SC-82AB	SOT-23-5	SNT-4A
1.3 V ±2.0 %	0.065 V	S-80913CLNB-G6HT2x	S-80913CLMC-G6HT2x	S-80913CLPF-G6HTFU
1.4 V ±2.0 %	0.070 V	S-80914CLNB-G6JT2x	S-80914CLMC-G6JT2x	S-80914CLPF-G6JTFU
1.5 V ±2.0 %	0.075 V	S-80915CLNB-G6KT2x	S-80915CLMC-G6KT2x	S-80915CLPF-G6KTFU
1.6 V ±2.0 %	0.080 V	S-80916CLNB-G6LT2x	S-80916CLMC-G6LT2x	S-80916CLPF-G6LTFU
1.7 V ±2.0 %	0.085 V	S-80917CLNB-G6MT2x	S-80917CLMC-G6MT2x	S-80917CLPF-G6MTFU
1.8 V ±2.0 %	0.090 V	S-80918CLNB-G6NT2x	S-80918CLMC-G6NT2x	S-80918CLPF-G6NTFU
1.9 V ±2.0 %	0.095 V	S-80919CLNB-G6PT2x	S-80919CLMC-G6PT2x	S-80919CLPF-G6PTFU
2.0 V ±2.0 %	0.100 V	S-80920CLNB-G6QT2x	S-80920CLMC-G6QT2x	S-80920CLPF-G6QTFU
2.1 V ±2.0 %	0.105 V	S-80921CLNB-G6RT2x	S-80921CLMC-G6RT2x	S-80921CLPF-G6RTFU
2.2 V ±2.0 %	0.110 V	S-80922CLNB-G6ST2x	S-80922CLMC-G6ST2x	S-80922CLPF-G6STFU
2.3 V ±2.0 %	0.115 V	S-80923CLNB-G6TT2x	S-80923CLMC-G6TT2x	S-80923CLPF-G6TTFU
2.4 V ±2.0 %	0.120 V	S-80924CLNB-G6UT2x	S-80924CLMC-G6UT2x	S-80924CLPF-G6UTFU
2.5 V ±2.0 %	0.125 V	S-80925CLNB-G6VT2x	S-80925CLMC-G6VT2x	S-80925CLPF-G6VTFU
2.6 V ±2.0 %	0.130 V	S-80926CLNB-G6WT2x	S-80926CLMC-G6WT2x	S-80926CLPF-G6WTFU
2.7 V ±2.0 %	0.135 V	S-80927CLNB-G6XT2x	S-80927CLMC-G6XT2x	S-80927CLPF-G6XTFU
2.8 V ±2.0 %	0.140 V	S-80928CLNB-G6YT2x	S-80928CLMC-G6YT2x	S-80928CLPF-G6YTFU
2.9 V ±2.0 %	0.145 V	S-80929CLNB-G6ZT2x	S-80929CLMC-G6ZT2x	S-80929CLPF-G6ZTFU
3.0 V ±2.0 %	0.150 V	S-80930CLNB-G60T2x	S-80930CLMC-G60T2x	S-80930CLPF-G60TFU
3.1 V ±2.0 %	0.155 V	S-80931CLNB-G61T2x	S-80931CLMC-G61T2x	S-80931CLPF-G61TFU
3.2 V ±2.0 %	0.160 V	S-80932CLNB-G62T2x	S-80932CLMC-G62T2x	S-80932CLPF-G62TFU
3.3 V ±2.0 %	0.165 V	S-80933CLNB-G63T2x	S-80933CLMC-G63T2x	S-80933CLPF-G63TFU
3.4 V ±2.0 %	0.170 V	S-80934CLNB-G64T2x	S-80934CLMC-G64T2x	S-80934CLPF-G64TFU
3.5 V ±2.0 %	0.175 V	S-80935CLNB-G65T2x	S-80935CLMC-G65T2x	S-80935CLPF-G65TFU
3.6 V ±2.0 %	0.180 V	S-80936CLNB-G66T2x	S-80936CLMC-G66T2x	S-80936CLPF-G66TFU
3.7 V ±2.0 %	0.185 V	S-80937CLNB-G67T2x	S-80937CLMC-G67T2x	S-80937CLPF-G67TFU
3.8 V ±2.0 %	0.190 V	S-80938CLNB-G68T2x	S-80938CLMC-G68T2x	S-80938CLPF-G68TFU
3.9 V ±2.0 %	0.195 V	S-80939CLNB-G69T2x	S-80939CLMC-G69T2x	S-80939CLPF-G69TFU
4.0 V ±2.0 %	0.200 V	S-80940CLNB-G7AT2x	S-80940CLMC-G7AT2x	S-80940CLPF-G7ATFU
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4.5 V ±2.0 %	0.225 V	S-80945CLNB-G7FT2x	S-80945CLMC-G7FT2x	S-80945CLPF-G7FTFU
4.6 V ±2.0 %	0.230 V	S-80946CLNB-G7GT2x	S-80946CLMC-G7GT2x	S-80946CLPF-G7GTFU
4.7 V ±2.0 %	0.235 V	S-80947CLNB-G7HT2x	S-80947CLMC-G7HT2x	S-80947CLPF-G7HTFU
4.8 V ±2.0 %	0.240 V	S-80948CLNB-G7JT2x	S-80948CLMC-G7JT2x	S-80948CLPF-G7JTFU
4.9 V ±2.0 %	0.245 V	S-80949CLNB-G7KT2x	S-80949CLMC-G7KT2x	S-80949CLPF-G7KTFU
5.0 V ±2.0 %	0.250 V	S-80950CLNB-G7LT2x	S-80950CLMC-G7LT2x	S-80950CLPF-G7LTFU
5.1 V ±2.0 %	0.255 V	S-80951CLNB-G7MT2x	S-80951CLMC-G7MT2x	S-80951CLPF-G7MTFU
5.2 V ±2.0 %	0.260 V	S-80952CLNB-G7NT2x	S-80952CLMC-G7NT2x	S-80952CLPF-G7NTFU
5.3 V ±2.0 %	0.265 V	S-80953CLNB-G7PT2x	S-80953CLMC-G7PT2x	S-80953CLPF-G7PTFU
5.4 V ±2.0 %	0.270 V	S-80954CLNB-G7QT2x	S-80954CLMC-G7QT2x	S-80954CLPF-G7QTFU
5.5 V ±2.0 %	0.275 V	S-80955CLNB-G7RT2x	S-80955CLMC-G7RT2x	S-80955CLPF-G7RTFU
5.6 V ±2.0 %	0.280 V	S-80956CLNB-G7ST2x	S-80956CLMC-G7ST2x	S-80956CLPF-G7STFU
5.7 V ±2.0 %	0.285 V	S-80957CLNB-G7TT2x	S-80957CLMC-G7TT2x	S-80957CLPF-G7TTFU
5.8 V ±2.0 %	0.290 V	S-80958CLNB-G7UT2x	S-80958CLMC-G7UT2x	S-80958CLPF-G7UTFU
5.9 V ±2.0 %	0.295 V	S-80959CLNB-G7VT2x	S-80959CLMC-G7VT2x	S-80959CLPF-G7VTFU
6.0 V ±2.0 %	0.300 V	S-80960CLNB-G7WT2x	S-80960CLMC-G7WT2x	S-80960CLPF-G7WTFU

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configurations

SC-82AB
Top view

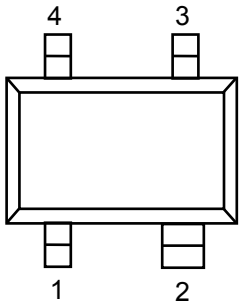


Figure 3

Table 3

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Voltage input pin
3	CD	Connection pin for delay capacitor
4	OUT	Voltage detection output pin

SOT-23-5
Top view

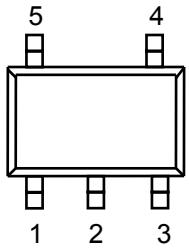


Figure 4

Table 4

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	VSS	GND pin
4	NC*1	No connection
5	CD	Connection pin for delay capacitor

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

SNT-4A
Top view

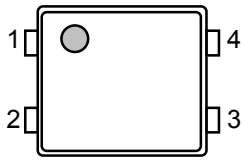


Figure 5

Table 5

Pin No.	Symbol	Description
1	VSS	GND pin
2	OUT	Voltage detection output pin
3	CD	Connection pin for delay capacitor
4	VDD	Voltage input pin

■ Absolute Maximum Ratings

Table 6

(Ta=25°C unless otherwise specified)

Item		Symbol	Absolute maximum ratings	Unit
Power supply voltage		V_{DD}–V_{SS}	12	V
CD pin input voltage		V_{CD}	V_{SS}–0.3 to V_{DD}+0.3	
Output voltage	Nch open-drain output products	V_{OUT}	V_{SS} –0.3 to V_{SS}+12	
	CMOS output products		V_{SS}–0.3 to V_{DD}+0.3	
Output current		I_{OUT}	50	mA
Power dissipation	SC-82AB	P_D	150 (When not mounted on board)	mW
			350*1	
	SOT-23-5		250 (When not mounted on board)	
			600*1	
	SNT-4A		140 (When not mounted on board)	
			300*1	
Operating ambient temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–40 to +125	

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

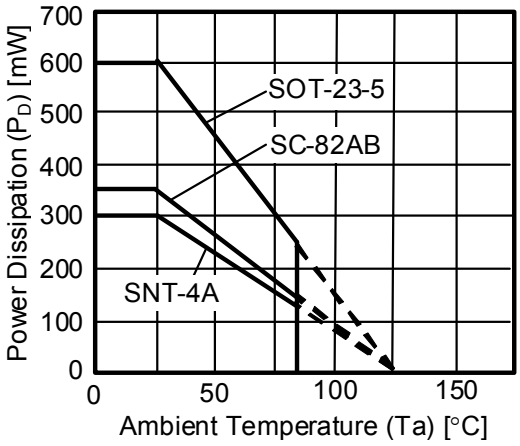


Figure 6 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Nch Open-drain Output Products

Table 7

(Ta=25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage*1	$-V_{DET}$	—		$-V_{DET(S)}$ ×0.98	$-V_{DET(S)}$	$-V_{DET(S)}$ ×1.02	V	1
Hysteresis width	V_{HYS}	S-80913 to 14		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08		
		S-80915 to 60		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.07		
Current consumption	I_{SS}	V_{DD}=2.0 V	S-80913 to 14	—	1.0	2.5	μA	2
		V_{DD}=3.5 V	S-80915 to 26	—	1.1	2.8		
		V_{DD}=4.5 V	S-80927 to 39	—	1.2	3.0		
		V_{DD}=6.0 V	S-80940 to 54	—	1.3	3.3		
		V_{DD}=7.5 V	S-80955 to 60	—	1.4	3.5		
Operating voltage	V_{DD}	—		0.7	—	10.0	V	1
Output current	I_{OUT}	Output transistor Nch, V_{DS}=0.5 V	V_{DD}=0.95 V S-80913 to 14	0.23	0.64	—	mA	3
			V_{DD}=1.2 V S-80915 to 60	0.59	1.36	—		
			V_{DD}=2.4 V S-80927 to 60	2.88	4.98	—		
Leakage current	I_{LEAK}	Output transistor, Nch, V_{DS}=10.0 V, V_{DD}=10.0 V		—	—	0.1	μA	
Delay time	t_D	C_D=4.7 nF	V_{DD}=2.0 V S-80913 to 14	2.7	3.6	4.5	ms	4
			V_{DD}=3.5 V S-80915 to 26	20	27	34		
			V_{DD}=4.5 V S-80927 to 39					
			V_{DD}=6.0 V S-80940 to 54					
			V_{DD}=7.5 V S-80955 to 60					
Detection voltage temperature coefficient*2	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta=−40°C to +85°C		—	±100	±350	ppm/°C	1

***1.** $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Specified detection voltage (The center value of detection voltage range in **Table 1**.)

***2.** The temperature change ratio in the detection voltage [mV/°C] is calculated by using the following quation.

$$\frac{\Delta -V_{DET}}{\Delta Ta}\left[mV/°C\right]^{*1} = -V_{DET}(Typ.)\left[V\right]^{*2} \times \frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\left[ppm/°C\right]^{*3} \div 1000$$

***1.** Temperature change ratio of the detection voltage
***2.** Specified detection voltage
***3.** Detection voltage temperature coefficient

2. CMOS Output Products

Table 8

(Ta=25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage*1	$-V_{DET}$	—		$-V_{DET(S)}$ ×0.98	$-V_{DET(S)}$	$-V_{DET(S)}$ ×1.02	V	1
Hysteresis width	V_{HYS}	S-80913 to 14		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08		
		S-80915 to 60		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.07		
Current consumption	I_{SS}	V_{DD}=2.0 V	S-80913 to 14	—	1.0	2.5	μA	2
		V_{DD}=3.5 V	S-80915 to 26	—	1.1	2.8		
		V_{DD}=4.5 V	S-80927 to 39	—	1.2	3.0		
		V_{DD}=6.0 V	S-80940 to 54	—	1.3	3.3		
		V_{DD}=7.5 V	S-80955 to 60	—	1.4	3.5		
Operating voltage	V_{DD}	—		0.7	—	10.0	V	1
Output current	I_{OUT}	Output transistor, Nch, V_{DS}=0.5 V	V_{DD}=0.95 V S-80913 to 14	0.23	0.64	—	mA	3
			V_{DD}=1.2 V S-80915 to 60	0.59	1.36	—		
			V_{DD}=2.4 V S-80927 to 60	2.88	4.98	—		
		Output transistor, Pch, V_{DS}=0.5 V	V_{DD}=4.8 V S-80913 to 39	1.43	2.39	—		5
			V_{DD}=6.0 V S-80940 to 54	1.68	2.78	—		
			V_{DD}=8.4 V S-80955 to 60	2.08	3.42	—		
Delay time	t_D	C_D=4.7 nF	V_{DD}=2.0 V S-80913 to 14	2.7	3.6	4.5	ms	4
			V_{DD}=3.5 V S-80915 to 26	18	24	30		
			V_{DD}=4.5 V S-80927 to 39					
			V_{DD}=6.0 V S-80940 to 54					
			V_{DD}=7.5 V S-80955 to 60					
Detection voltage temperature coefficient *2	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta=−40°C to +85°C		—	±100	±350	ppm/°C	1

***1.** $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Specified detection voltage (The center value of detection voltage range in **Table 2**.)

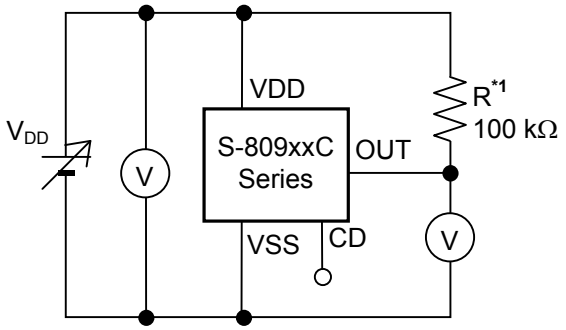
***2.** The temperature change ratio in the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta -V_{DET}}{\Delta Ta}\left[mV/°C\right]^{*1} = -V_{DET}(Typ.)\left[V\right]^{*2} \times \frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\left[ppm/°C\right]^{*3} \div 1000$$

***1.** Temperature change ratio of the detection voltage
***2.** Specified detection voltage
***3.** Detection voltage temperature coefficient

■ Test Circuits

1.



***1.** R is unnecessary for CMOS output products.

Figure 7

2.

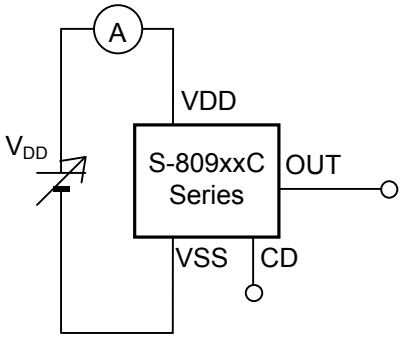


Figure 8

3.

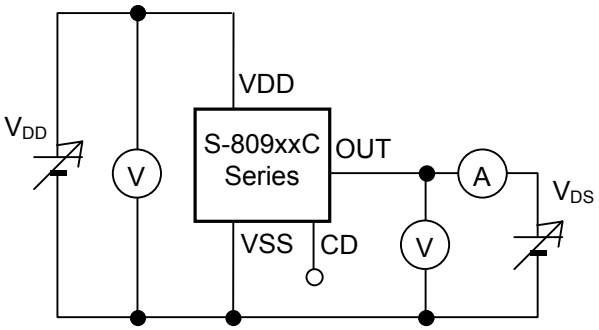
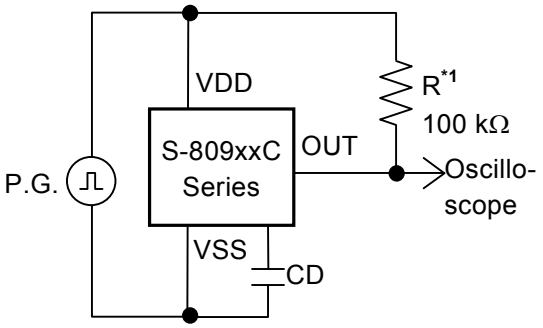


Figure 9

4.



***1.** R is unnecessary for CMOS output products.

Figure 10

5.

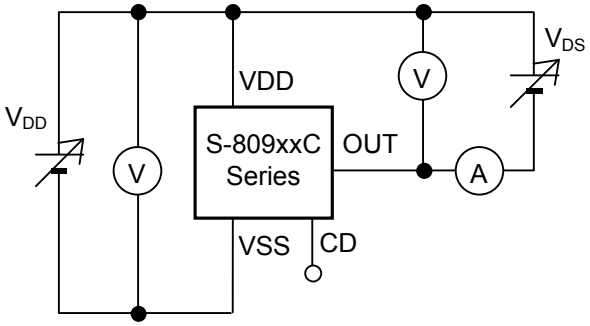


Figure 11

■ Timing Chart

1. Nch Open-drain Output Products

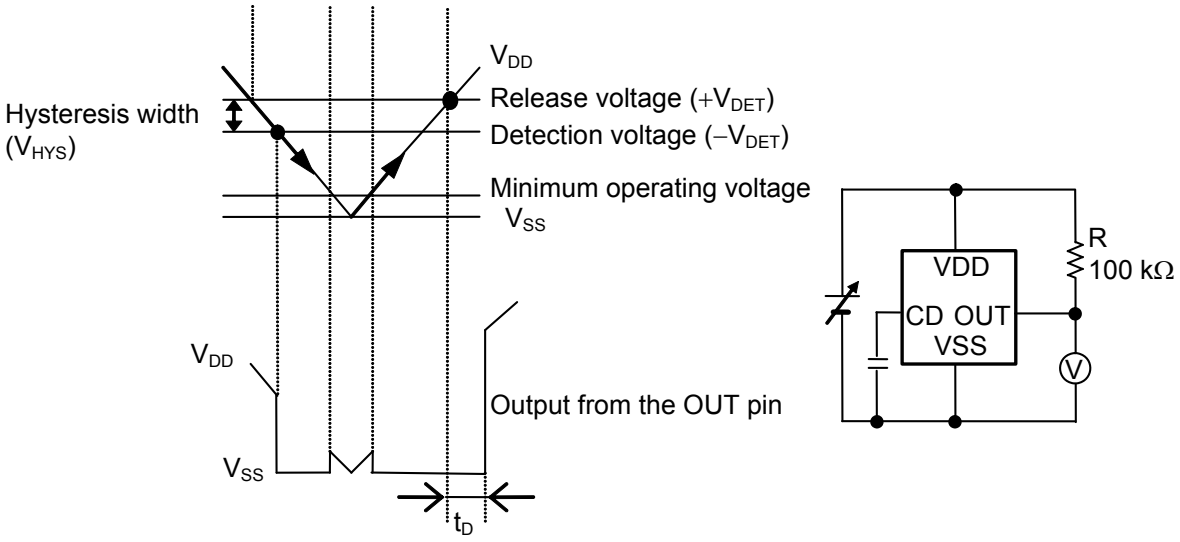
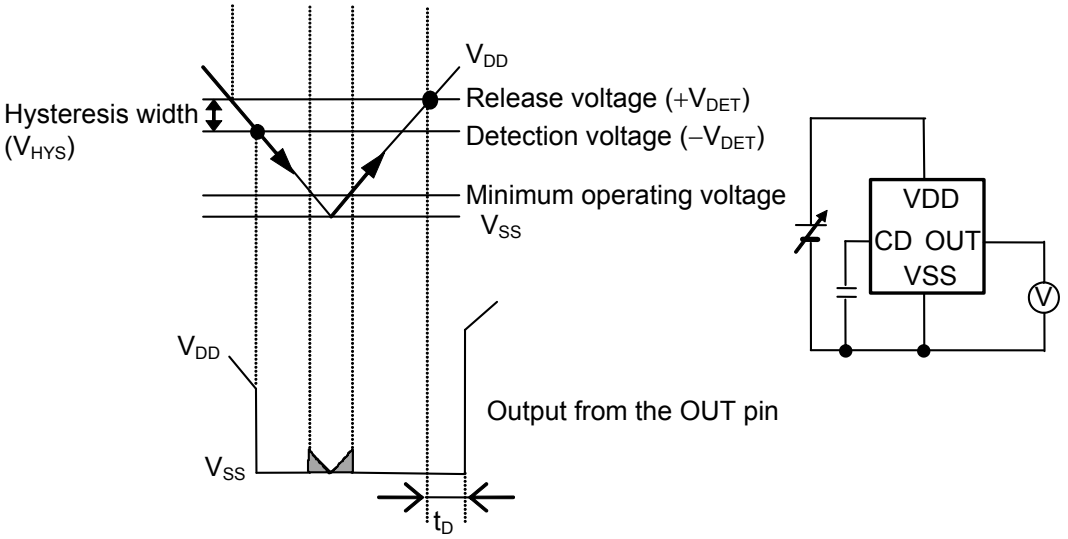


Figure 12

2. CMOS Output Products



Remark For values of V_{DD} less than minimum operating voltage, values of OUT pin output is free of the shaded region.

Figure 13

■ Operation

1. Basic Operation: CMOS Output (Active Low)

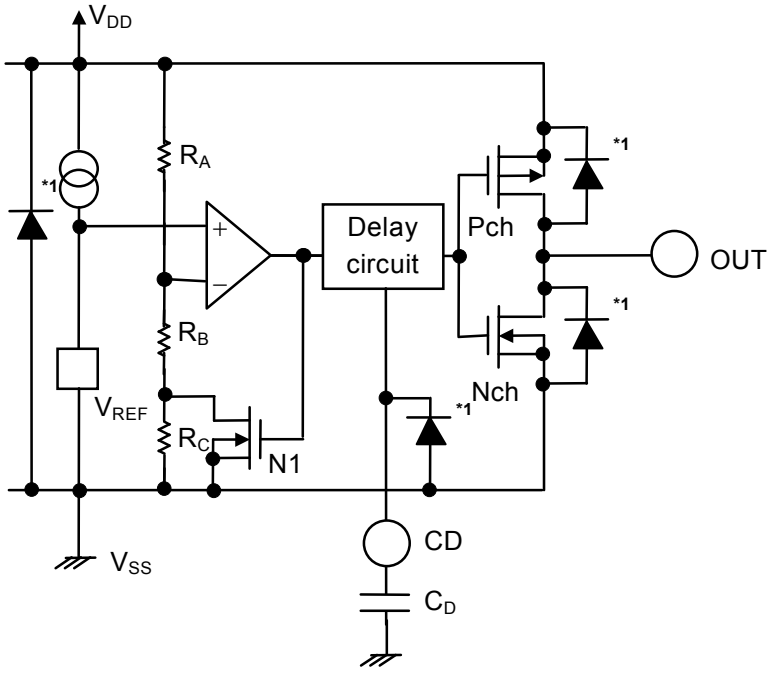
1-1. When the power supply voltage (V_{DD}) is higher than the release voltage ($+V_{DET}$), the Nch transistor is OFF and the Pch transistor is ON to provide V_{DD} (high) at the output. Since the Nch transistor N1 in **Figure 14** is OFF, the comparator input voltage is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

1-2. When the V_{DD} goes below $+V_{DET}$, the output provides the V_{DD} level, as long as the V_{DD} remains above the detection voltage $-V_{DET}$. When the V_{DD} falls below $-V_{DET}$ (point A in **Figure 15**), the Nch transistor becomes ON, the Pch transistor becomes OFF, and the V_{SS} level appears at the output. At this time the Nch transistor N1 in **Figure 14** becomes ON, the comparator input voltage is changed to $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

1-3. When the V_{DD} falls below the minimum operating voltage, the output becomes undefined, or goes to the V_{DD} when the output is pulled up to the V_{DD}.

1-4. The V_{SS} level appears when the V_{DD} rises above the minimum operating voltage. The V_{SS} level still appears even when the V_{DD} surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

1-5. When V_{DD} rises above $+V_{DET}$ (point B in **Figure 15**), the Nch transistor becomes OFF, and the Pch transistor becomes ON, and V_{DD} appears at the output after the delay time (t_D) counted by the delay circuit.



***1.** Parasitic diode

Figure 14 Operation 1

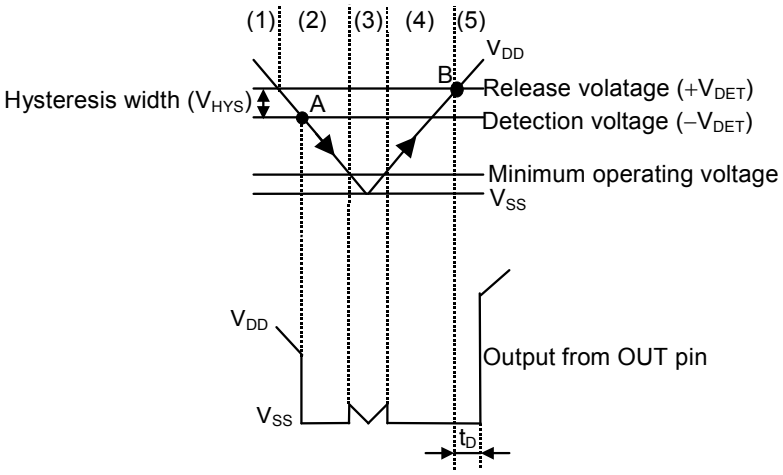


Figure 15 Operation 2

2. Delay Circuit

The delay circuit delays the output signal from the time at which the power voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$) when V_{DD} is turned on. The output signal is not delayed when the V_{DD} goes below the detection voltage ($-V_{DET}$) (Refer to **Figure 15)**. The delay time (t_D) is determined by the time constant of the built-in constant current (approx. 100 nA) and the attached external capacitor (C_D), and calculated from the following equation.

t_D (ms)=Delay coefficient×C_D (nF)

Delay coefficient: (25°C)

Detection voltage $-V_{DET} \leq 1.4$ V	Min. 0.57,	Typ. 0.77,	Max. 0.96
Detection voltage $-V_{DET} \geq 1.5$ V			
Nch open-drain output products:	Min. 4.3,	Typ. 5.7,	Max. 7.2
CMOS output products:	Min. 3.8,	Typ. 5.1,	Max. 6.4

Caution 1. When the CD pin is open, a double pulse shown in Figure 16 may appear at release. To avoid the double pulse, attach 20 pF or larger capacitor to the CD pin. Do not apply voltage to the CD pin.

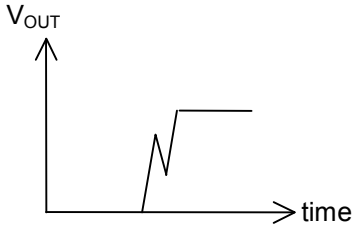


Figure 16

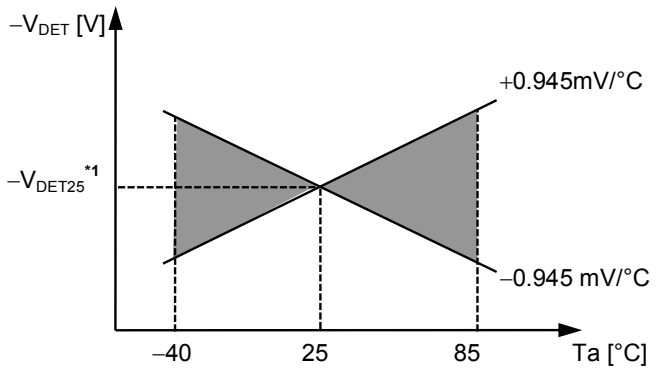
2. Print circuit board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.

3. There is no limit for the capacitance of the external capacitor (C_D) as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no release takes place.

3. Other characteristics

3-1. Temperature Characteristic of Detection Voltage

The shaded area in **Figure 17** shows the temperature characteristics of the detection voltage.



***1.** $-V_{DET25}$ is an actual detection voltage value at 25 °C.

Figure 17 Temperature Characteristic of Detection Voltage (Example forS-80927C)

3-2. Temperature Characteristics of Release Voltage

The temperature coefficient $\frac{\Delta + V_{DET}}{\Delta Ta}$ for the release voltage is calculated by the temperature coefficient of the detection voltage $\frac{\Delta - V_{DET}}{\Delta Ta}$ as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

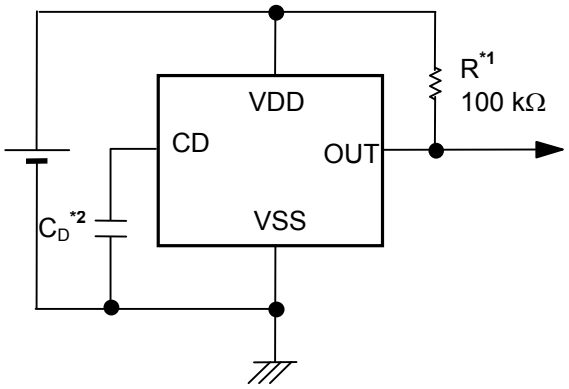
The temperature coefficients for the release voltage and the detection voltage have the same sign consequently.

3-3. Temperature Characteristics of Hysteresis Voltage

The temperature characteristics for the hysteresis voltage is expressed as $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

■ Standard Circuit



***1.** R is unnecessary for CMOS output products.
***2.** The delay capacitor (C_D) should be connected directly to the CD pin and to the VSS pin.

Figure 18

Caution The above connection diagram and constant will not guarantees successful operation. Perform through evaluation using the actual application to set the constant.

■ Technical Terms

1. Detection Voltage ($-V_{DET}$), Release Voltage ($+V_{DET}$)

The detection voltage ($-V_{DET}$) is a voltage at which the output turns to low. This detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$) Min. and maximum ($-V_{DET}$) Max. is called the detection voltage range (Refer to **Figure 19**).

Example: For the S-80927CN, detection voltage lies in the range of $2.646 \leq (-V_{DET}) \leq 2.754$.
This means that some S-80927CNs have 2.646 V for $-V_{DET}$ and some have 2.754 V.

The release voltage ($+V_{DET}$) is a voltage at which the output turns to high. This release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$) Min. and maximum ($+V_{DET}$) Max. is called the release voltage range (Refer to **Figure 20**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product and is expressed by $-V_{DET} \times 1.03 \leq +V_{DET} \leq -V_{DET} \times 1.08$ for S-80913 to S-80914, and by $-V_{DET} \times 1.03 \leq +V_{DET} \leq -V_{DET} \times 1.07$ for S-80915 to S-80960.

Example: For the S-80927CN, the release voltage lies in the range of $2.725 \leq (+V_{DET}) \leq 2.947$.
This means that some S-80927CNs have 2.725 V for $+V_{DET}$ and some have 2.947 V.

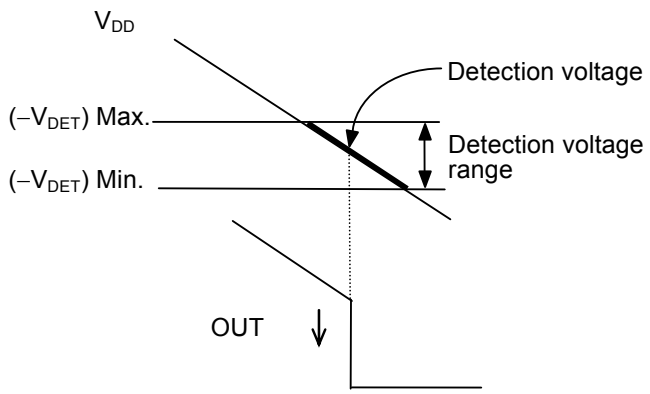


Figure 19 Detection Voltage (CMOS output products)

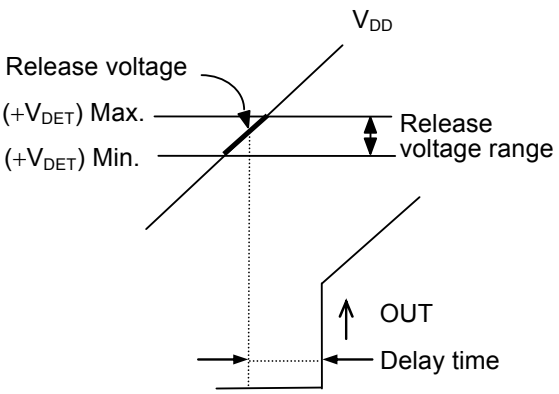


Figure 20 Release Voltage (CMOS output products)

Remark Although the detection voltage and release voltage overlap in the range of 2.725 V to 2.754 V, $+V_{DET}$ is always larger than $-V_{DET}$.

2. Hysteresis Width (V_{HYS})

Hysteresis width is the voltage difference between the detection voltage and the release voltage (The voltage at point B−The voltage at point A=V_{HYS} in **Figure 15**). The existence of the hysteresis width avoids malfunction caused by noise on input signal.

3. Delay Time (t_D)

Delay time is a time internally measured from the instant at which input voltage to the VDD pin exceeds the release voltage ($+V_{DET}$) to the point at which the output of the OUT pin inverts. The delay time changes according to the external capacitor (C_D).

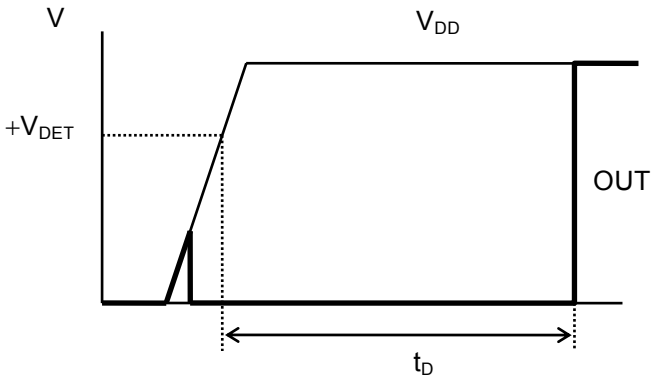


Figure 21

4. Through-type Current

The through-type current refers to the current that flows instantaneously at the time of detection and release of a voltage detector. The through-type current is large in CMOS output products, and small in Nch open-drain output products.

5. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 22**), taking a CMOS active low product for example, the through-type current, which is generated when the output goes from low to high (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the through-type current stops and its resultant voltage drop disappears, and the output goes from low to high. The through-type current again generated, a voltage drop appears, and repeatiing the process finally induces oscillation.

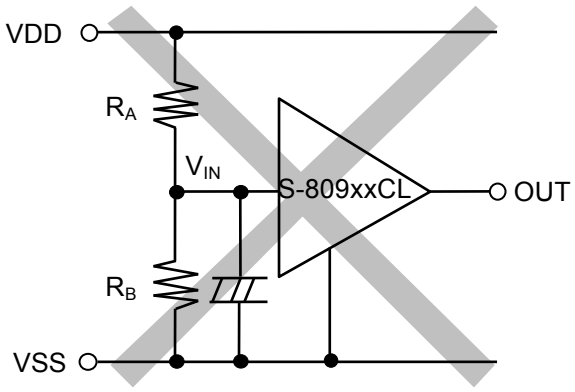


Figure 22 Example for Bad Implementation of Input Voltage Divider (CMOS Output Products)

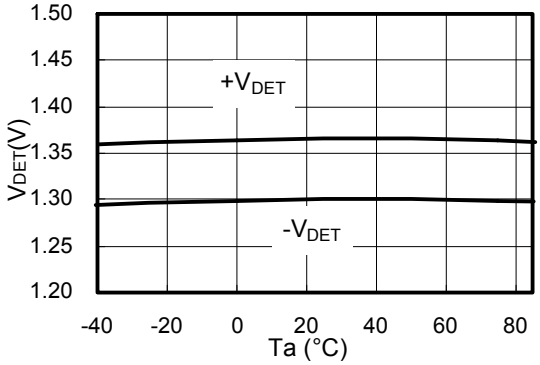
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output products of the S-809xxC series, the through-type current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the through-type current during releasing.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for the patents on the circuits described herein.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

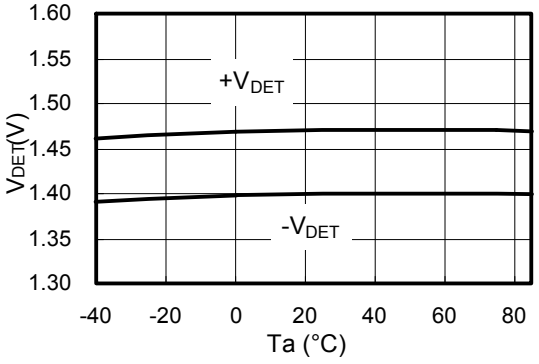
■ Characteristics (Typical Data)

1. Detection Voltage (V_{DET}) - Temperature (Ta)

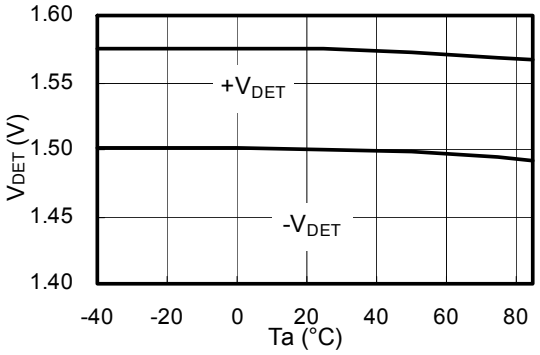
S-80913CN



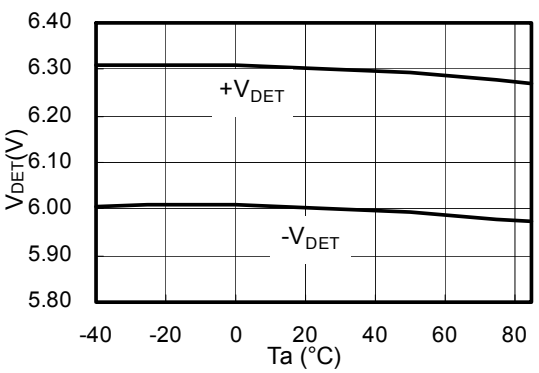
S-80914CN



S-80915CN

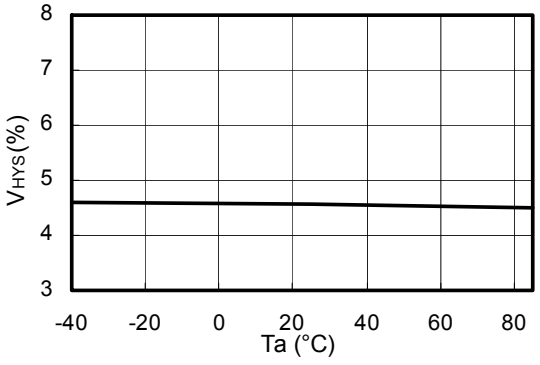


S-80960CN

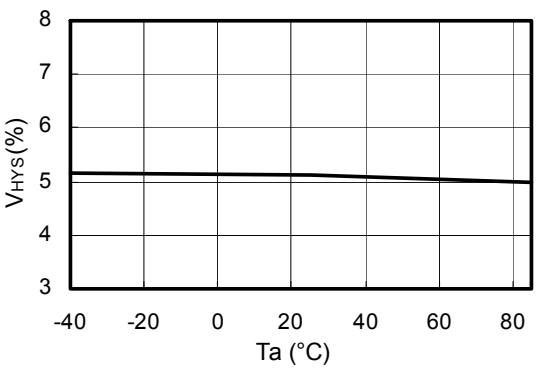


2. Hysteresis Voltage Width (V_{HYS}) - Temperature (Ta)

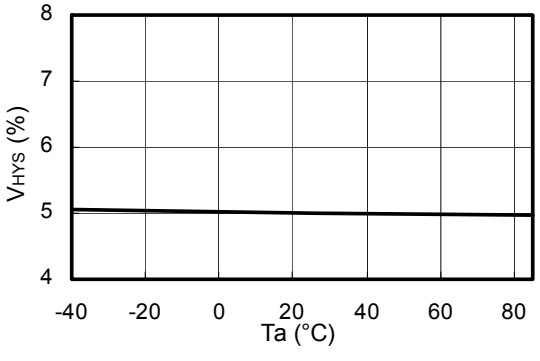
S-80913CN



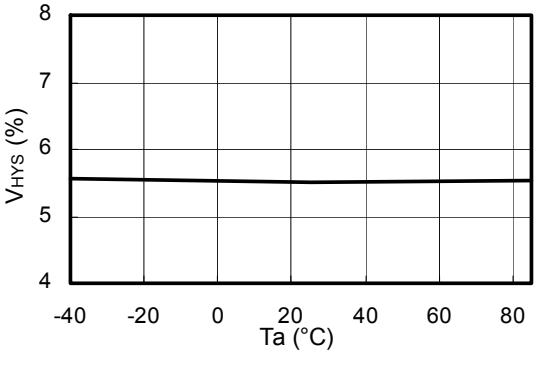
S-80914CN



S-80915CN

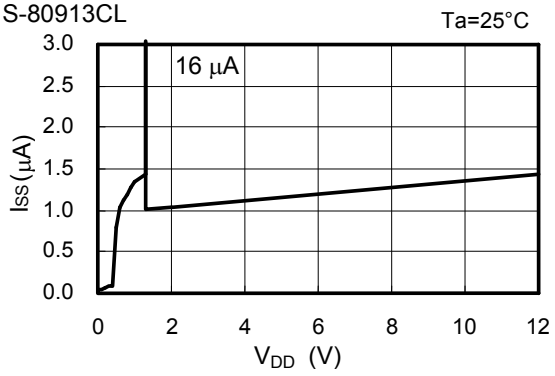


S-80960CN

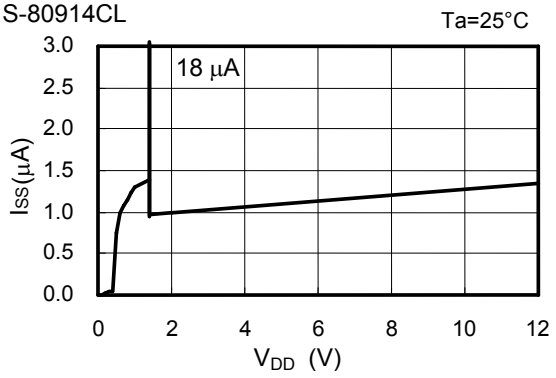


3. Current Consumption (I_{SS}) - Input Voltage (V_{DD})

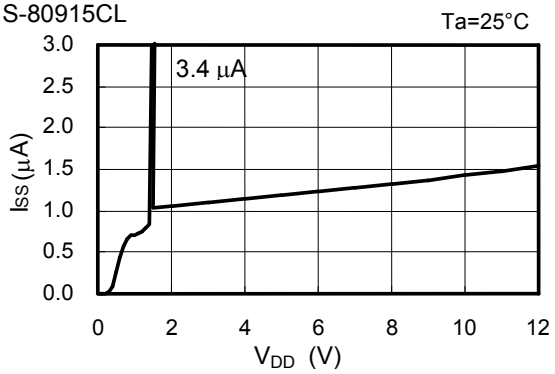
S-80913CL



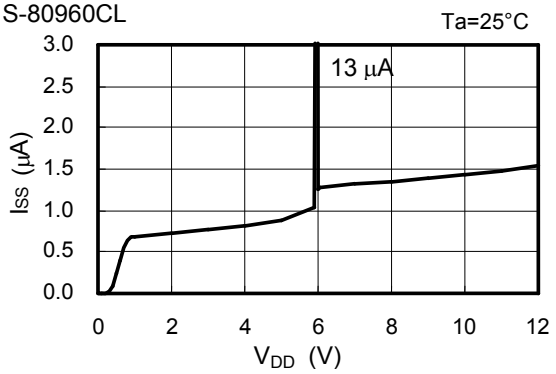
S-80914CL



S-80915CL

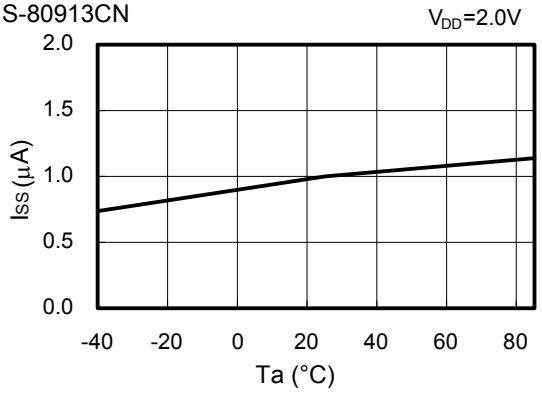


S-80960CL

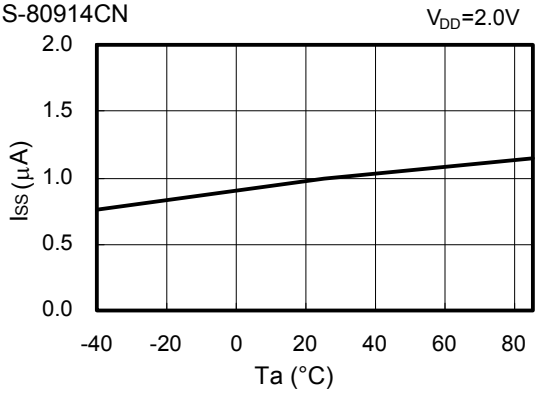


4. Current Consumption (I_{SS}) - Temperature (Ta)

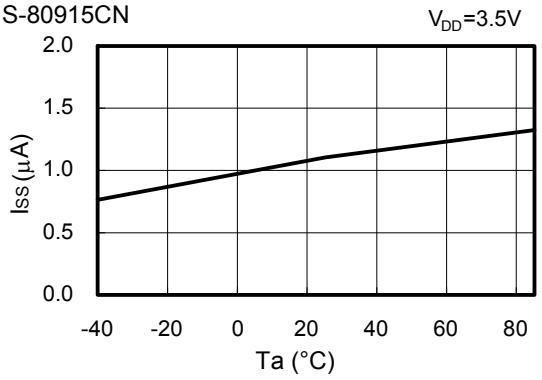
S-80913CN



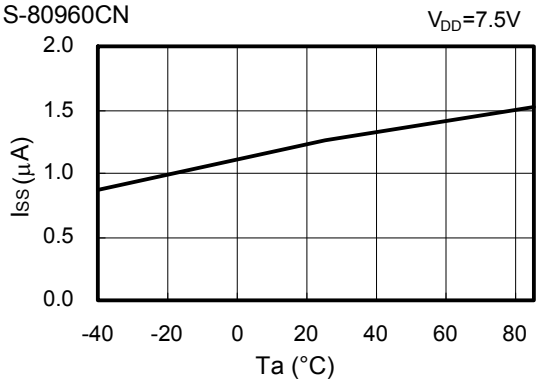
S-80914CN



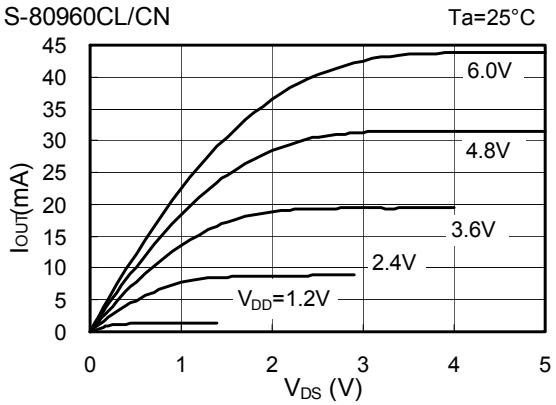
S-80915CN



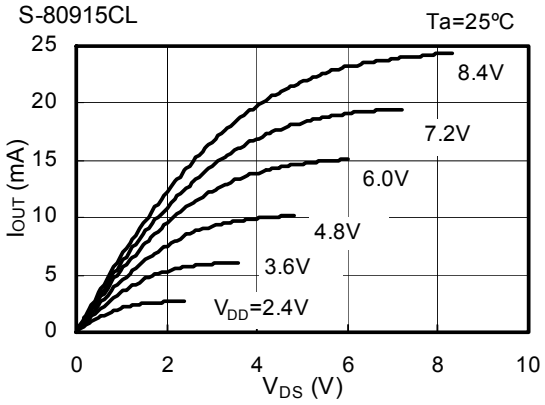
S-80960CN



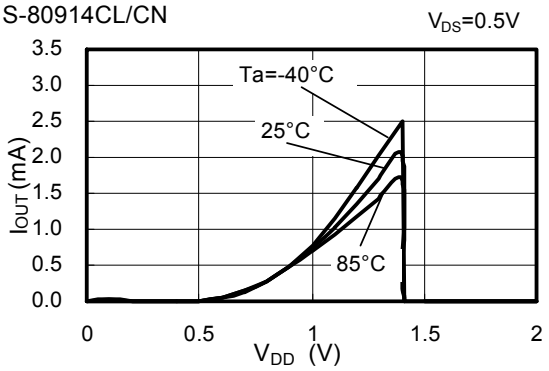
5. Nch Transistor Output Current (I_{OUT}) - V_{DS}

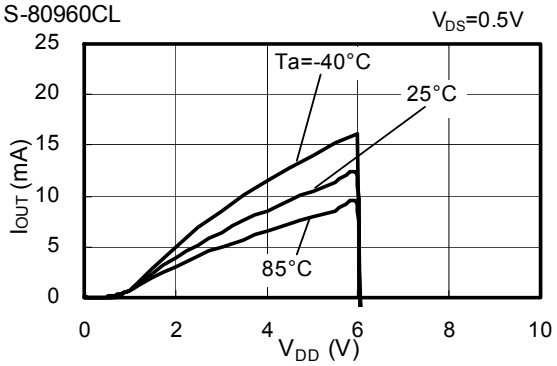


6. Pch Transistor Output Current (I_{OUT}) - V_{DS}

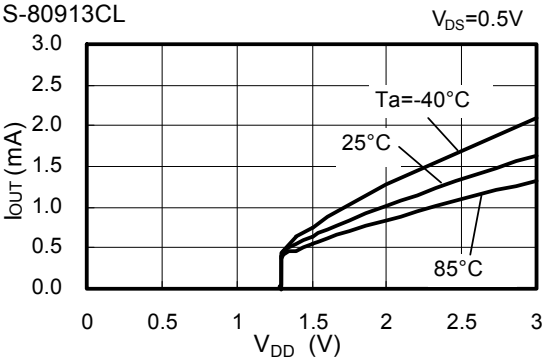


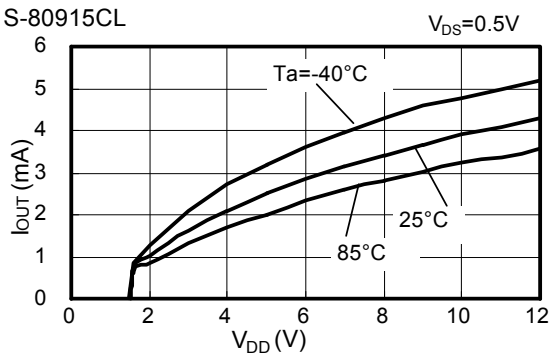
7. Nch Transistor Output Current (I_{OUT}) - Input Voltage(V_{DD})



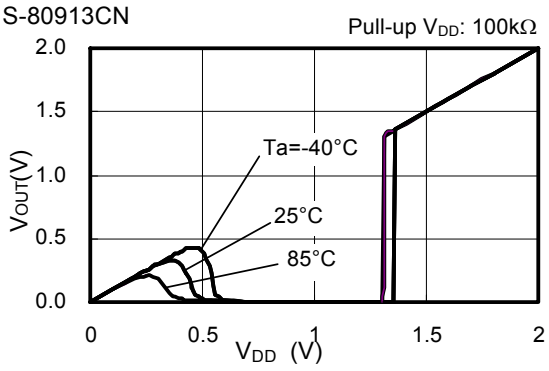


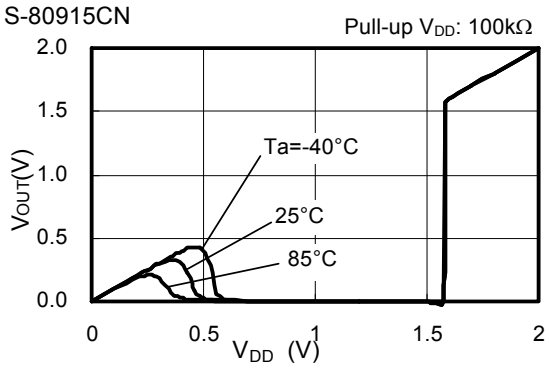
8. Pch Transistor Output Current (I_{OUT}) - Input Voltage(V_{DD})





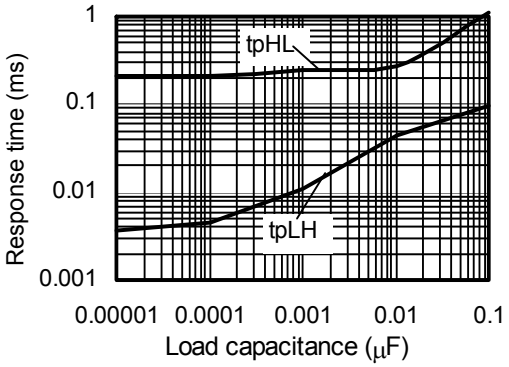
9. Minimum Operating Voltage - Input Voltage(V_{DD})



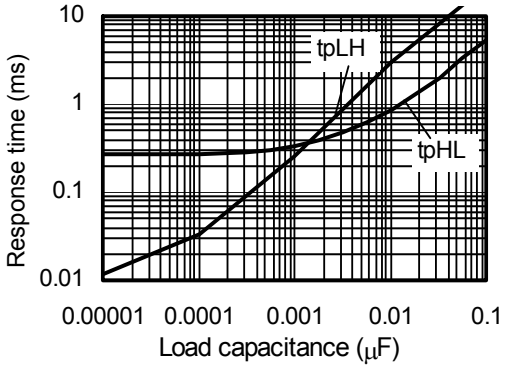


10. Dynamic Response - C_{OUT} (CD pin; open)

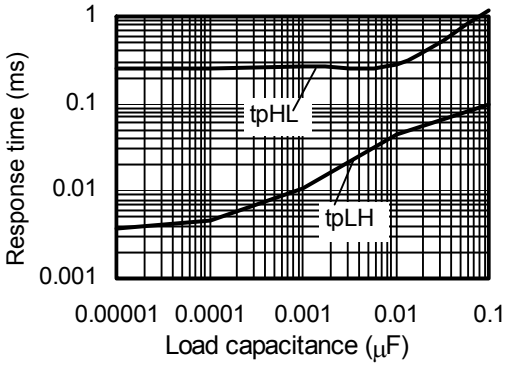
S-80913CL Ta=25°C



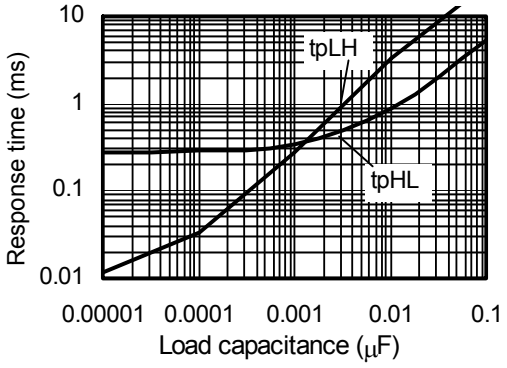
S-80913CN Ta=25°C



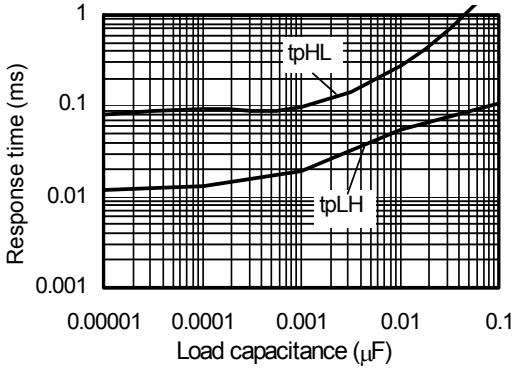
S-80914CL Ta=25°C



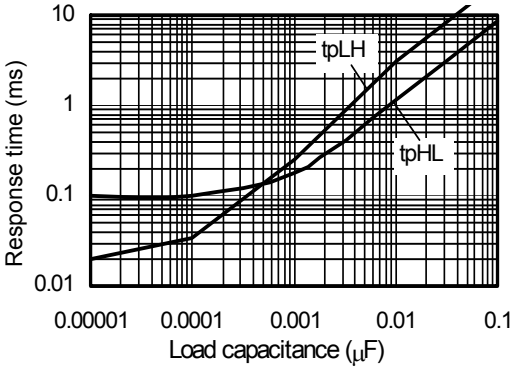
S-80914CN Ta=25°C



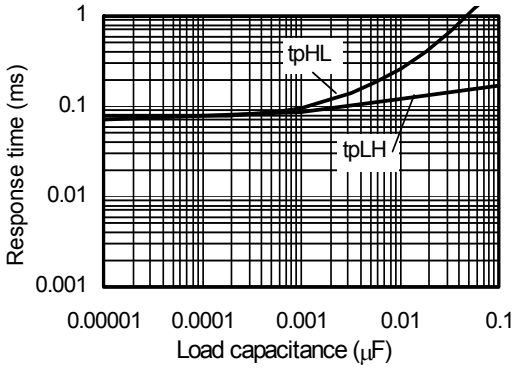
S-80915CL Ta=25°C



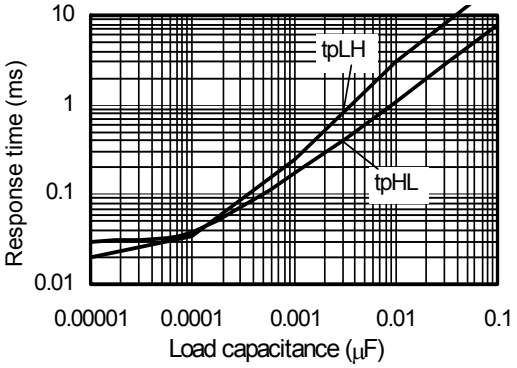
S-80915CN Ta=25°C

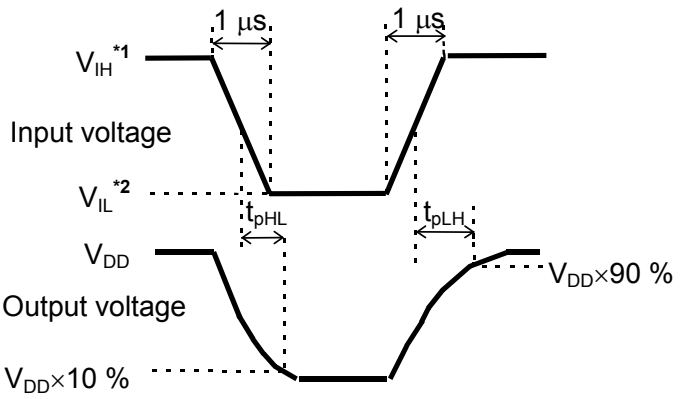


S-80960CL Ta=25°C



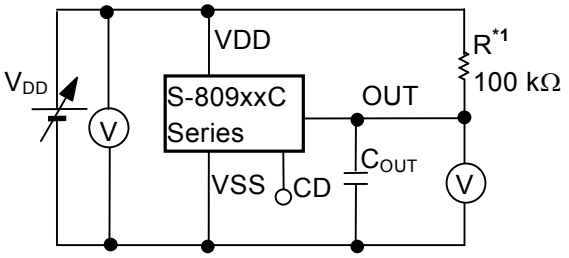
S-80960CN Ta=25°C





***1.** V_{IH}=10 V
***2.** V_{IL}=0.7 V

Figure 23 Measurement Condition for Response Time

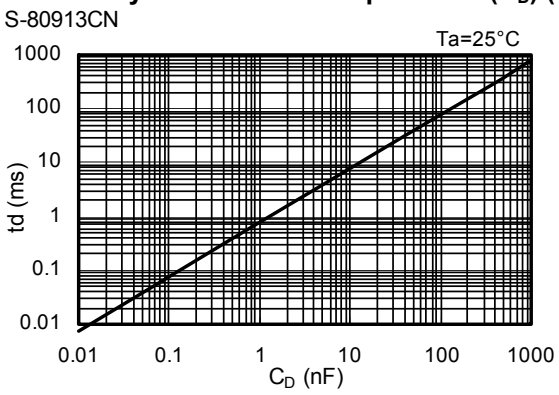


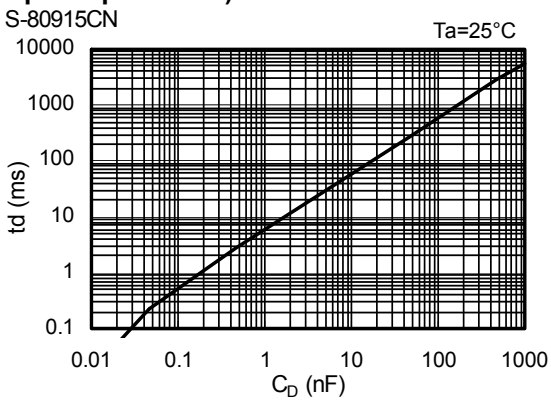
***1.** R is unnecessary for CMOS output products.

Figure 24 Measurement Circuit for Response Time

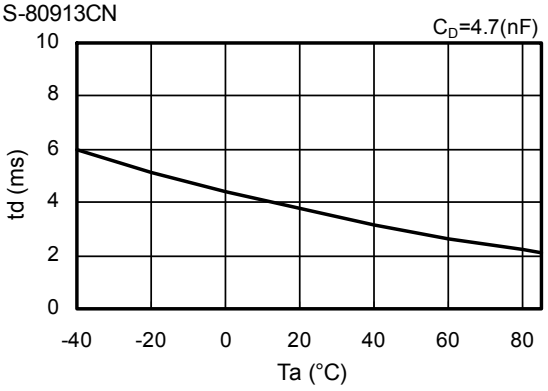
Caution The above connection diagram and constant will not guarantees successful operation. Perform through evaluation using the actual application to set the constant.

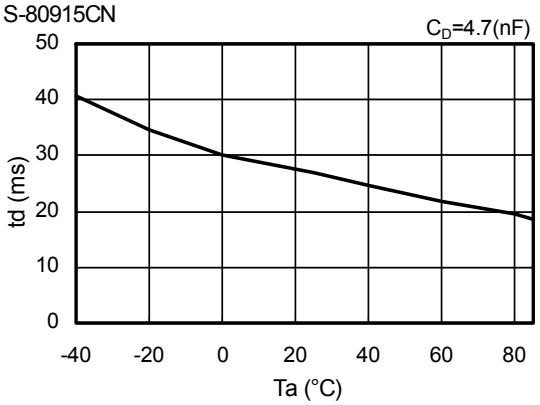
11. Delay Time - CD Pin Capacitance(C_D) (No output pin capacitance)

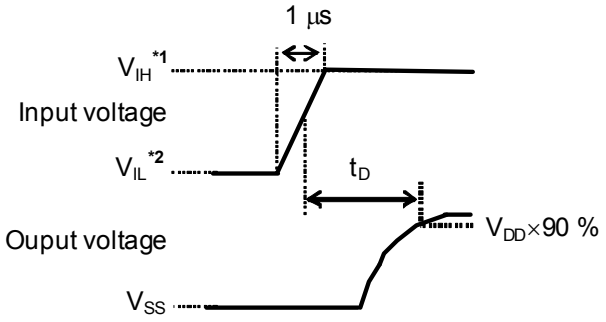




12. Delay Time - Temperature(Ta)







***1.** V_{IH}=10V
***2.** V_{IL}=0.7V

Figure 25 Measuring Conditions of Delay Time

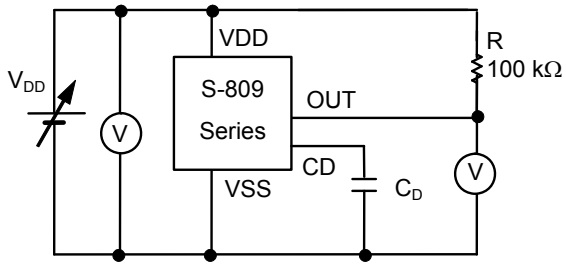


Figure 26 Measurement Circuit for Delay Time

Caution The above connection diagram and constant will not guarantees successful operation. Perform through evaluation using the actual application to set the constant.

■ Application Circuit Examples

1. Microcomputer Reset Circuits

If the power supply voltage to a microcomputer falls below the specified level, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to normal, the microcomputer needs to be initialized before normal operations can be done. Reset circuits protect microcomputers in the event of current being momentarily switched off or lowered. Reset circuits shown in **Figures 27 to 28** can be easily constructed with the help of the S-809xxC Series that has a low operating voltage, a high-precision detection voltage, hysteresis and the reset circuits.

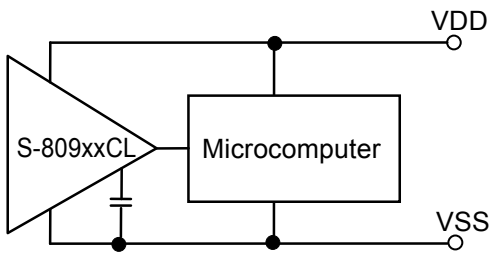
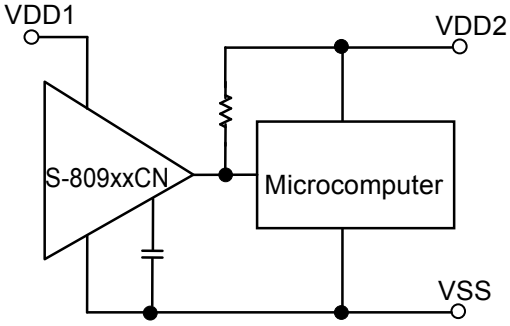


Figure 27 Example for Reset Circuits(S-809xxCL)



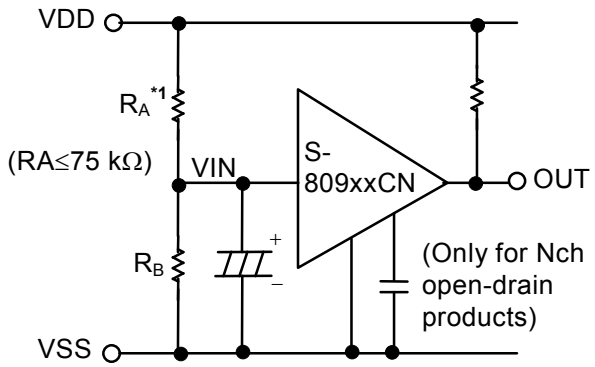
Only for Nch open-drain products.

Figure 28 Example for Reset Circuits(S-809xxCN)

Caution The above connection diagram and constant will not guarantees successful operation. Perform through evaluation using the actual application to set the constant.

2. Change of Detection Voltage

In Nch open-drain output products of the S-809xxC Series, detection voltage can be changed using resistance dividers or diodes as shown in **Figures 29** to **30**. In **Figure 29**, hysteresis width also changes.



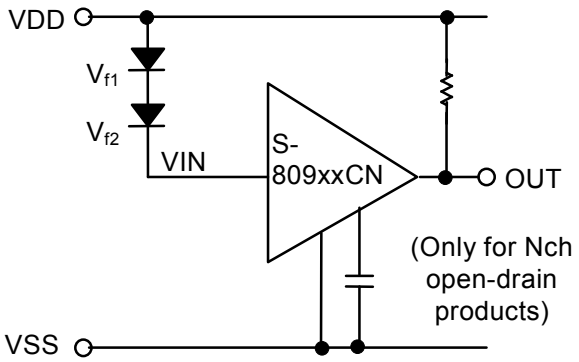
$$\text{Detection voltage} = \frac{R_A + R_B}{R_B} \bullet -V_{DET}$$

$$\text{Hysteresis width} = \frac{R_A + R_B}{R_B} \bullet V_{HYS}$$

***1.** R_A should be 75 kΩ or less tp prevent oscillation.

Caution If R_A and R_B are large, the hysteresis width may also be larger than the value given by the above equation due to through- type current (which flows slightly in an Nch open-drain products).

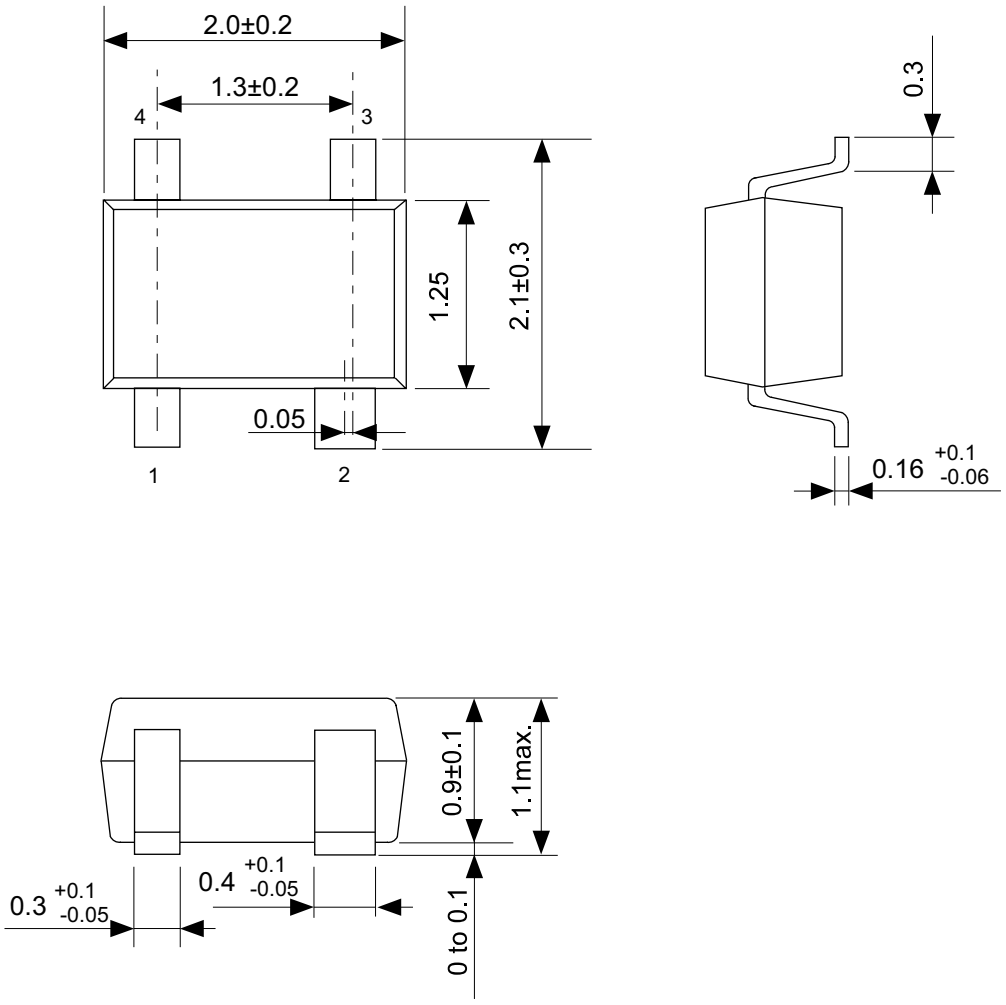
Figure 29



Detection voltage=$V_{f1}+V_{f2}+(-V_{DET})$

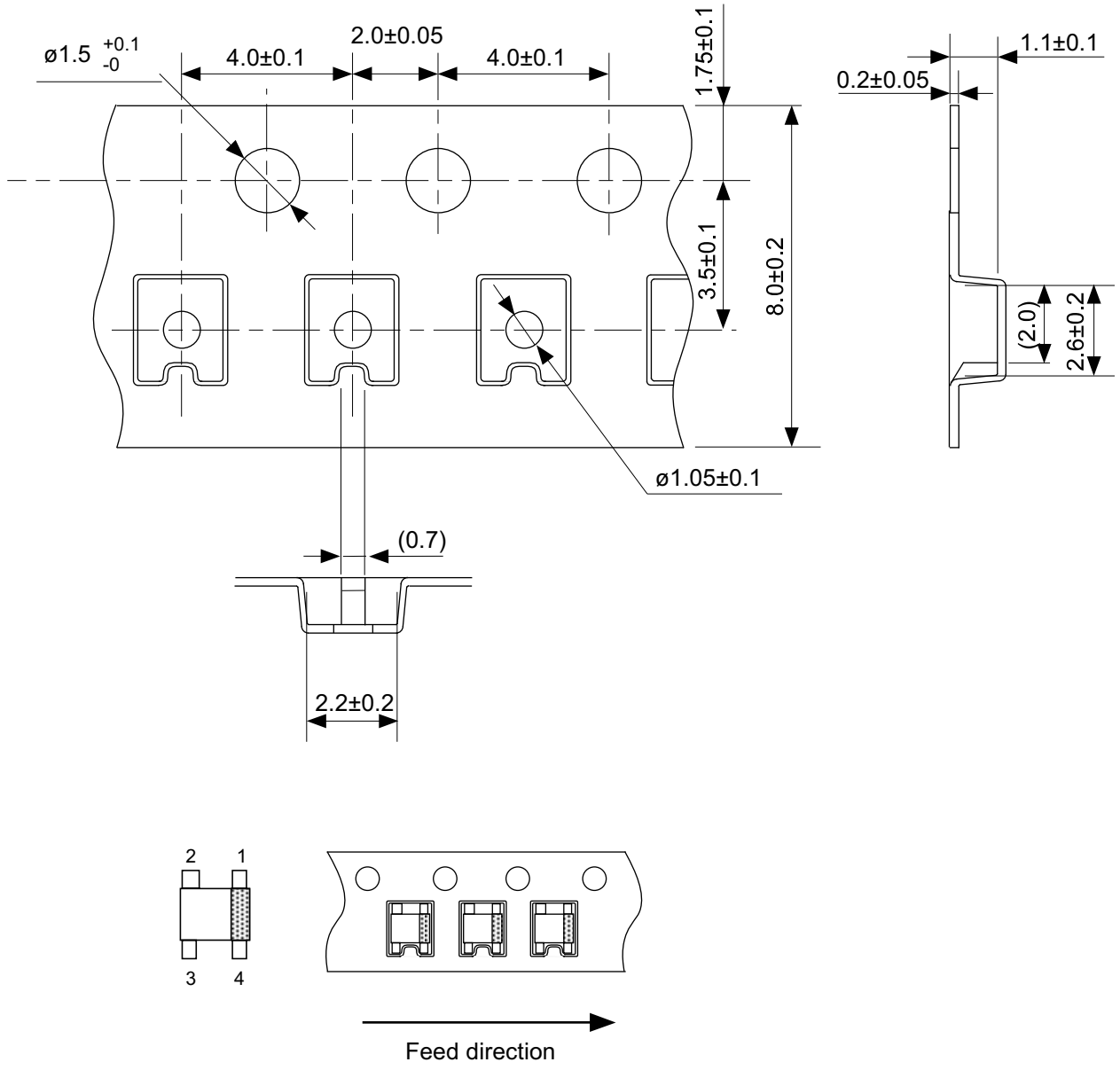
Figure 30

Caution The above connection diagram and constant will not guarantees successful operation. Perform through evaluation using the actual application to set the constant.



No. NP004-A-P-SD-2.0

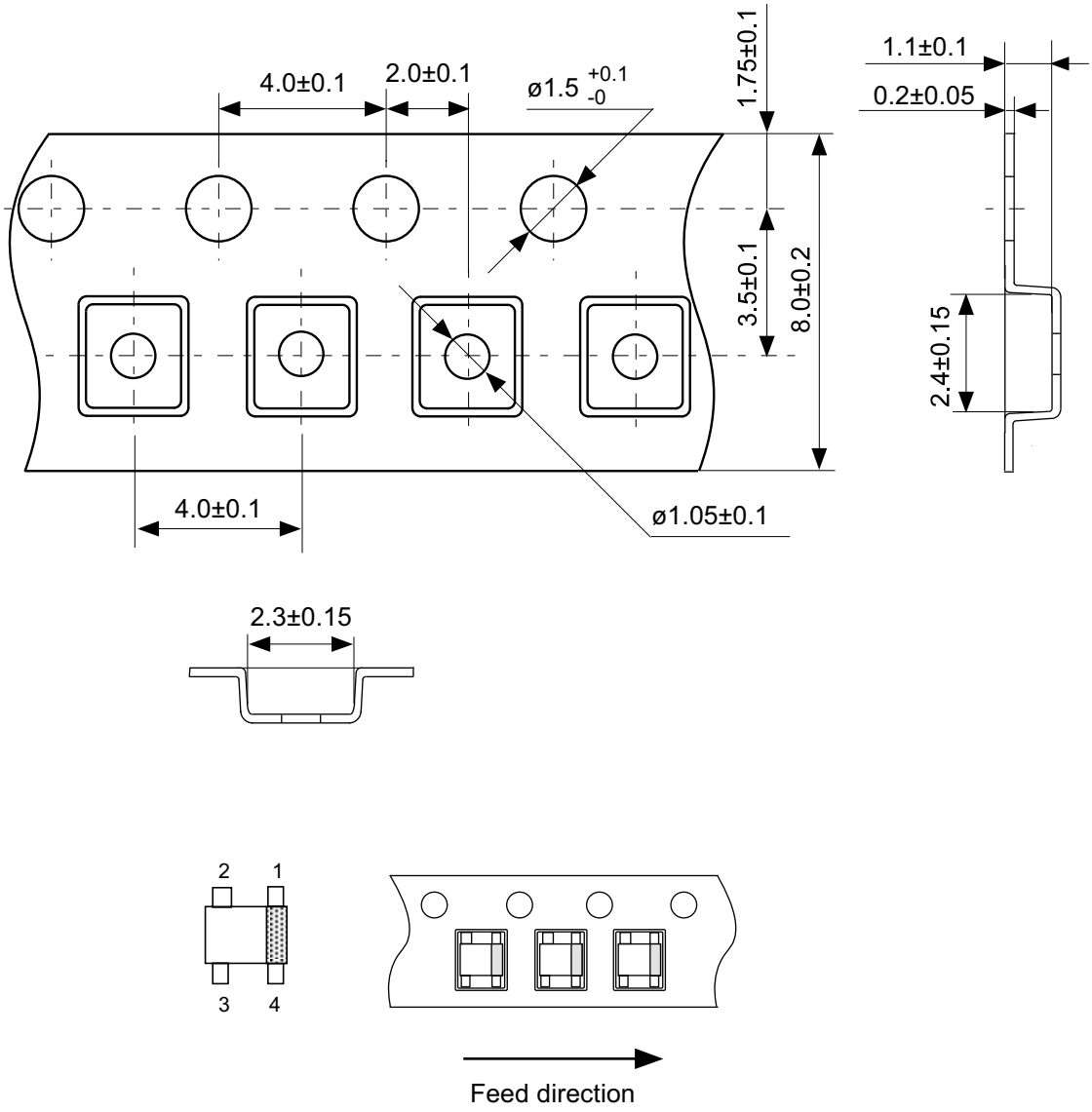
TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.



Feed direction

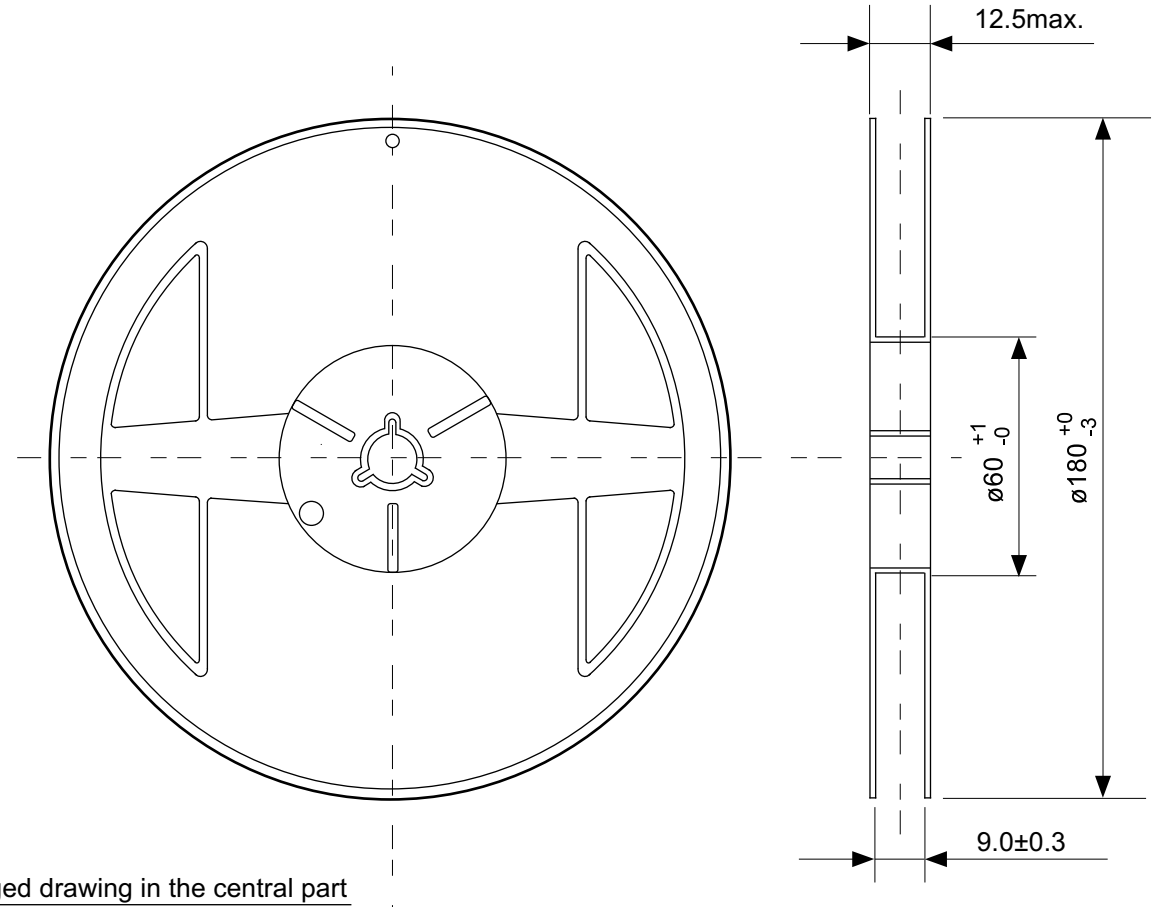
No. NP004-A-C-SD-3.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-SD-3.0
ANGLE	
UNIT	mm
	ABLIC Inc.

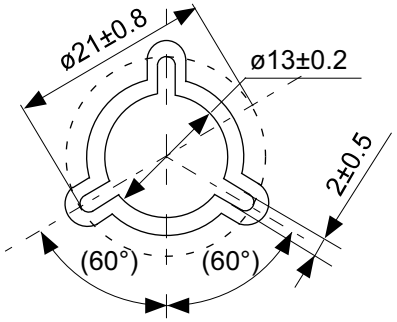


No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.

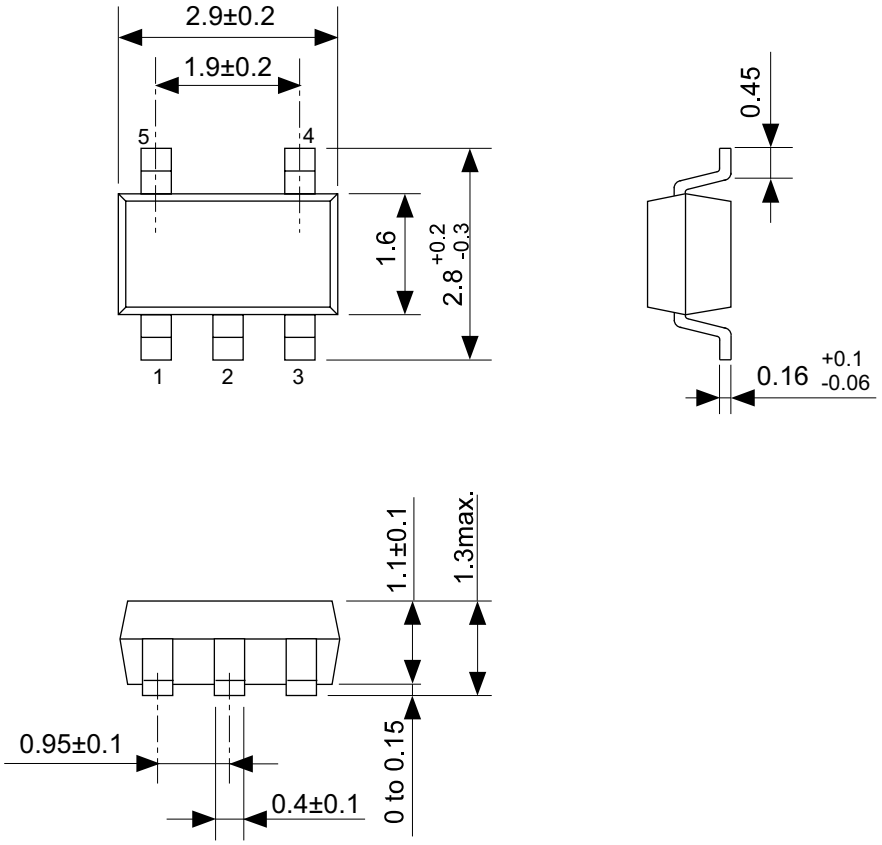


Enlarged drawing in the central part



No. NP004-A-R-SD-1.1

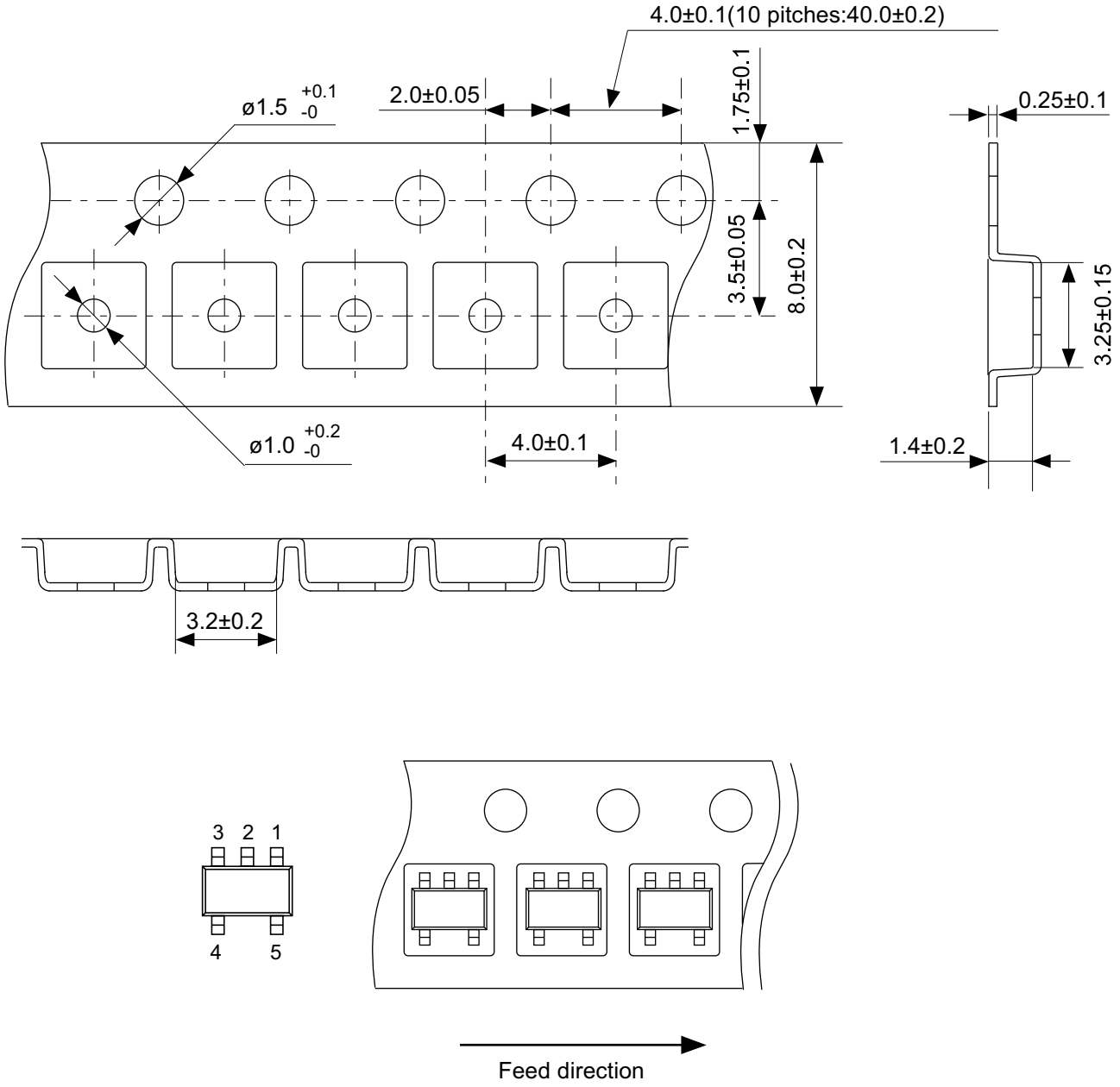
TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
	ABLIC Inc.		



No. MP005-A-P-SD-1.3

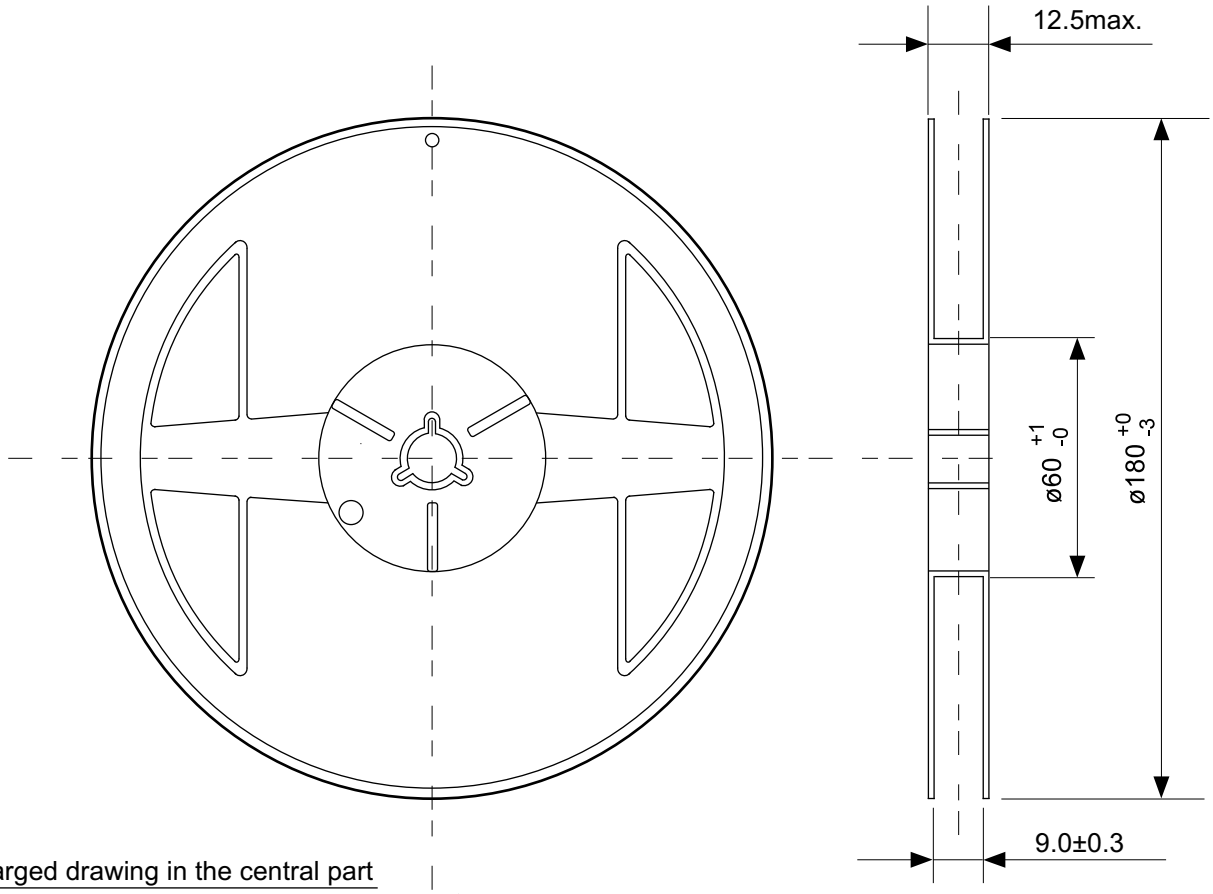
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

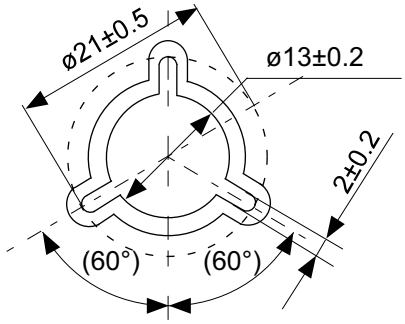


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

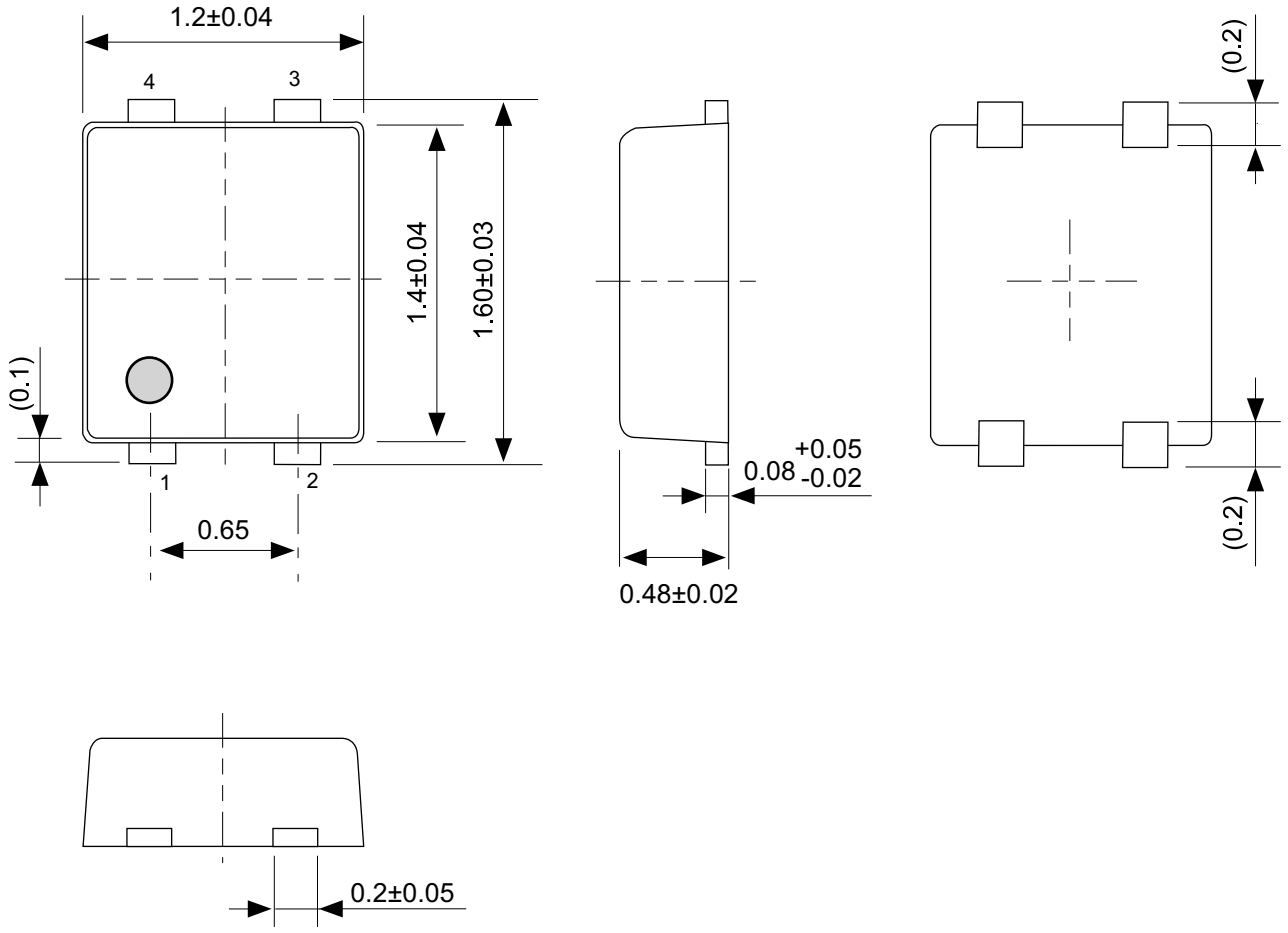


Enlarged drawing in the central part



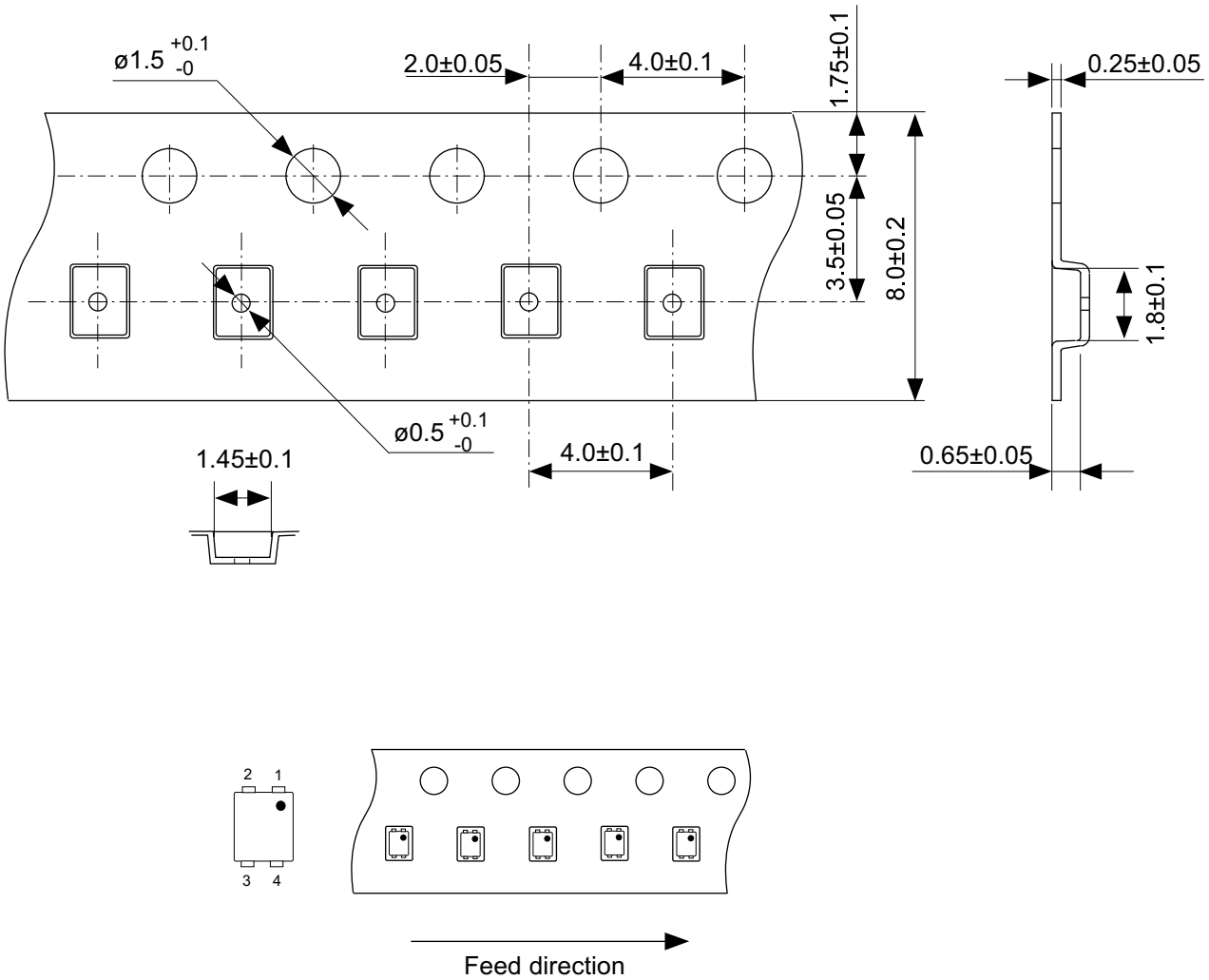
No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



No. PF004-A-P-SD-6.0

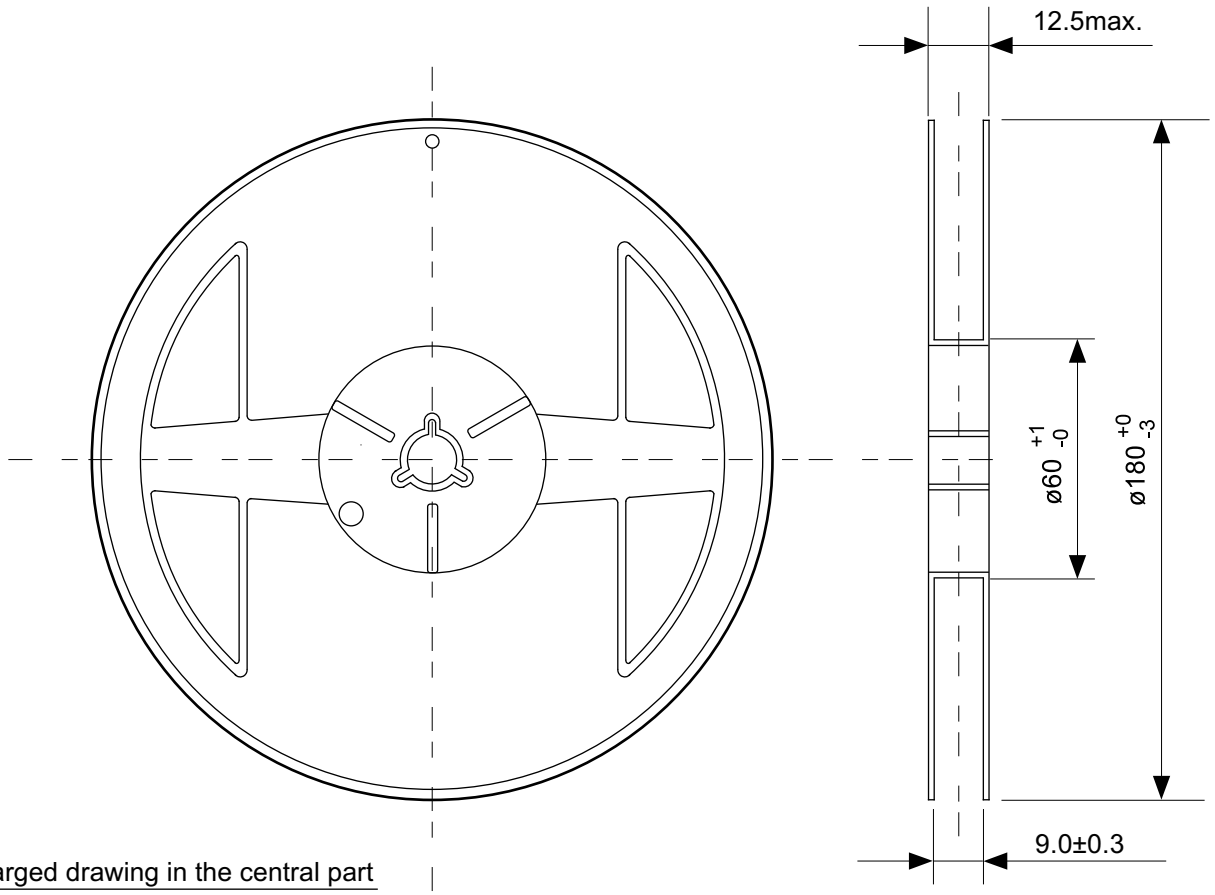
TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
ABLIC Inc.	



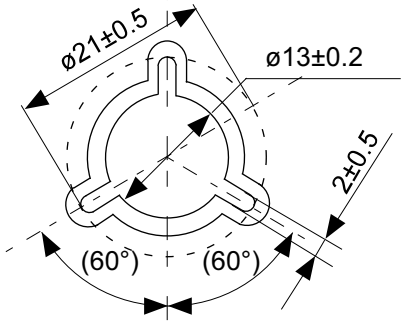
No. PF004-A-C-SD-2.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



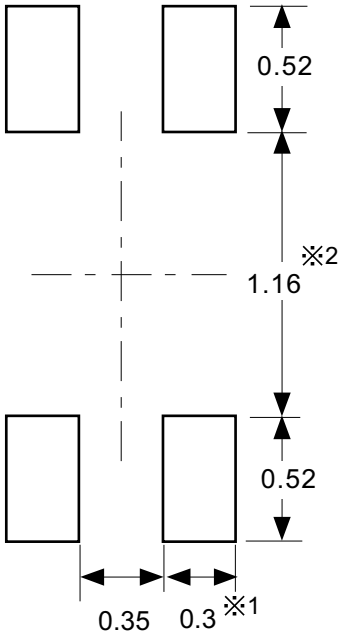
Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は ″SNTパッケージ活用の手引き″ を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm

ABLIC Inc.

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2.4-2019.07