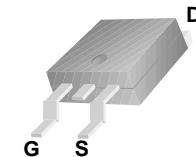
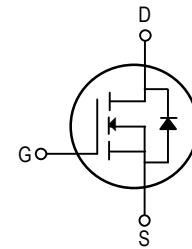


Features

- $R_{DS(on)}$ (Typical 5.5mΩ)@ $V_{GS}=10V$
- Improved dv/dt Capability, High Ruggedness
- 100% Avalanche Tested
- Maximum Junction Temperature Range (150°C)



TO-252

Absolute Maximum Ratings

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Symbol	Parameter	Rating	Unit	
Common Ratings ($T_J=25^{\circ}C$ Unless Otherwise Noted)				
V_{GS}	Gate-Source Voltage	± 20	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	40	V	
T_J	Maximum Junction Temperature	-50 to 175	°C	
T_{STG}	Storage Temperature Range	-50 to 175	°C	
I_S	Diode Continuous Forward Current	60	A	
Mounted on Large Heat Sink ($T_J=25^{\circ}C$ Unless Otherwise Noted)				
I_{DM}	Pulse Drain Current Tested (Silicon Limit) ^(Note1)	240	A	
I_D	Continuous Drain current@ $V_{GS}=10V$	$T_c=25^{\circ}C$	60	A
P_D	Maximum Power Dissipation	$T_c=25^{\circ}C$	47	W
E_{AS}	Sing Pulsed Avalanche Energy ^(Note2)	81	mJ	
$R_{\theta JC}$	Thermal Resistance Junction-to-Case	3.2	°C/W	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$ $I_{\text{D}}=250\mu\text{A}$	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain current($T_c=25^\circ\text{C}$)	$V_{\text{DS}}=40\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	--	--	± 100	nA
$V_{\text{GS}(\text{TH})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1	--	2.5	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance ^(Note3)	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	--	5.5	7	$\text{m}\Omega$
$R_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance ^(Note3)	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=20\text{A}$	--	9	12.5	$\text{m}\Omega$
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
C_{iss}	Input Capacitance	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	--	2400	--	pF
C_{oss}	Output Capacitance		--	192	--	pF
C_{rss}	Reverse Transfer Capacitance		--	165	--	pF
Q_g	Total Gate Charge	$V_{\text{DS}}=20\text{V}, I_{\text{D}}=30\text{A}$ $V_{\text{GS}}=10\text{V}$	--	37	--	nC
Q_{gs}	Gate-Source Charge		--	6	--	nC
Q_{gd}	Gate-Drain Charge		--	7	--	nC
Switching Characteristics note B						
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}}=20\text{V}$ $I_{\text{D}}=30\text{A}$, $R_{\text{GEN}}=3\Omega$, $R_{\text{L}}=1\Omega$, $V_{\text{GS}}=10\text{V}$	--	12	--	nS
t_r	Turn-on Rise Time		--	12	--	nS
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	38	--	nS
t_f	Turn-Off Fall Time		--	9	--	nS
Source- Drain Diode Characteristics@ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
V_{SD}	Forward on voltage	$I_{\text{S}}=20\text{A}, V_{\text{GS}}=0\text{V}$	--	--	1.2	V

Note :

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J=25^\circ\text{C}$, $V_{\text{DD}}=20\text{V}$, $V_{\text{G}}=10\text{V}$, $R_{\text{G}}=25\Omega$ $L=0.5\text{mH}$, $I_{\text{AS}}=18\text{A}$
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical characteristic curve:

Figure 1: Output Characteristics

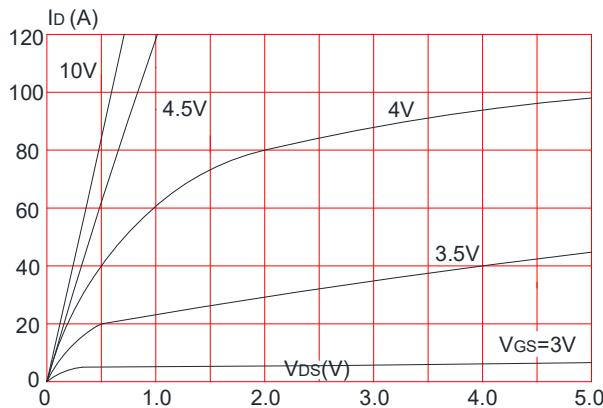


Figure 2: Typical Transfer Characteristics

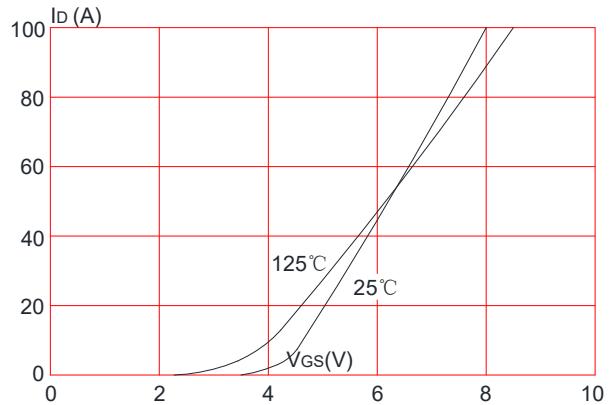


Figure 3: On-resistance vs. Drain Current

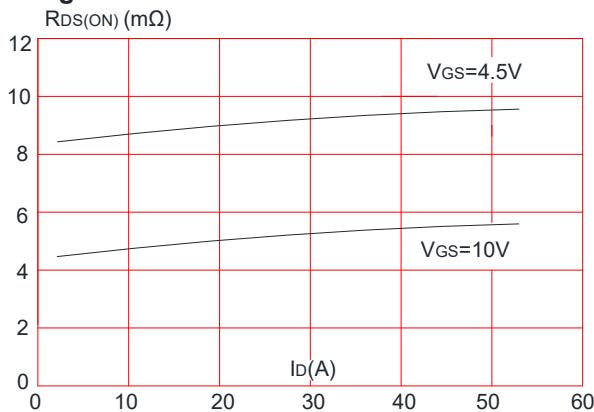


Figure 5: Gate Charge Characteristics

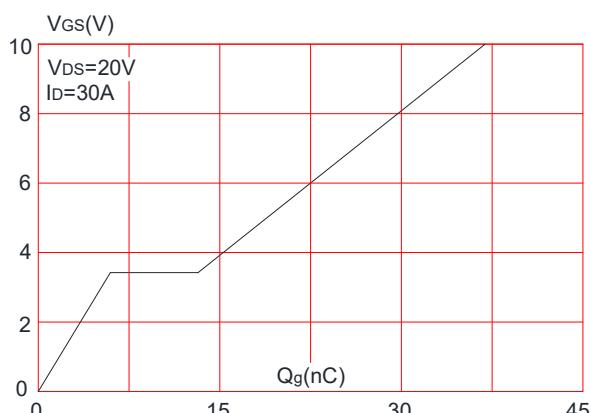


Figure 4: Body Diode Characteristics

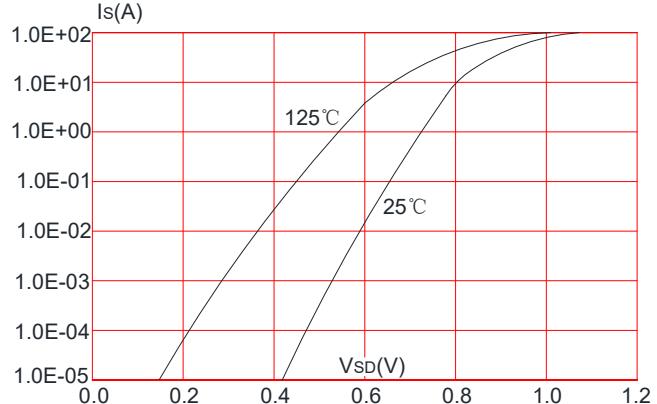


Figure 6: Capacitance Characteristics

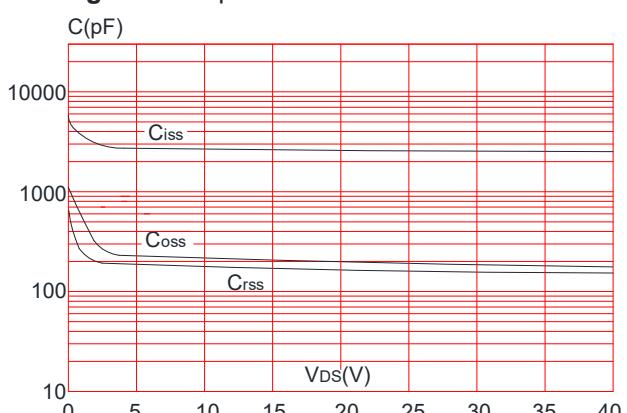
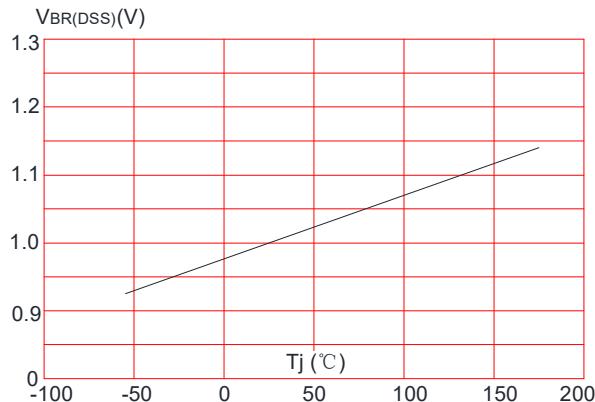
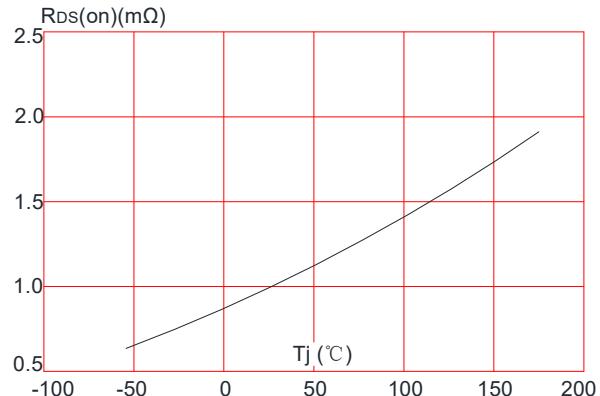
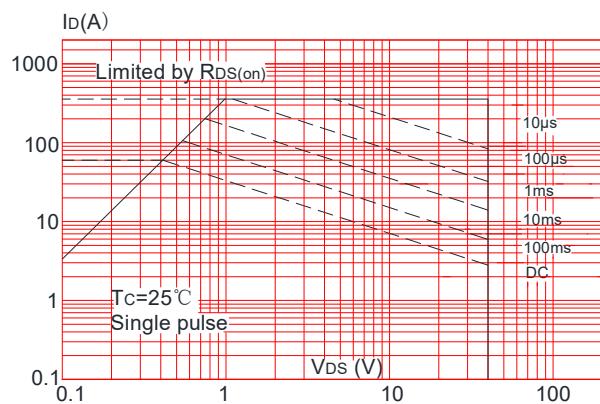
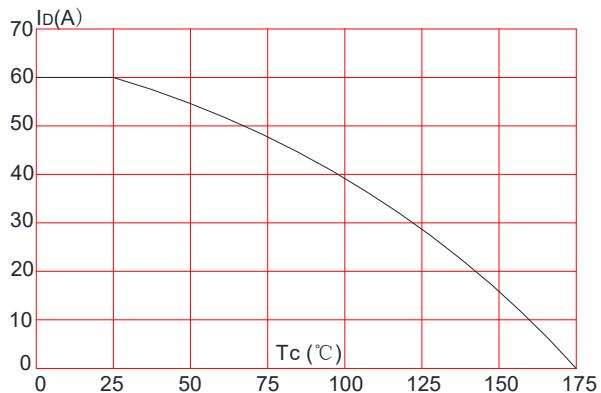
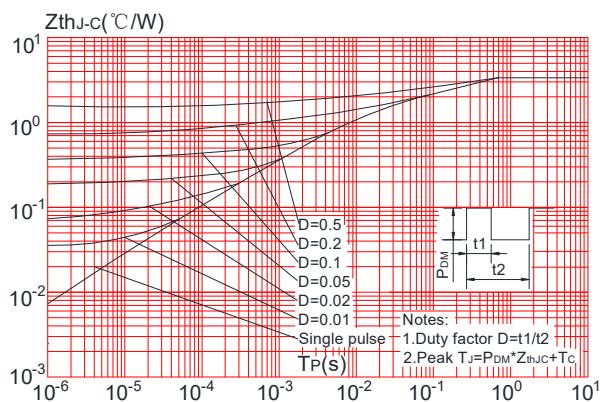


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**Figure 8:** Normalized on Resistance vs. Junction Temperature**Figure 9:** Maximum Safe Operating Area**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test Circuit and Waveform

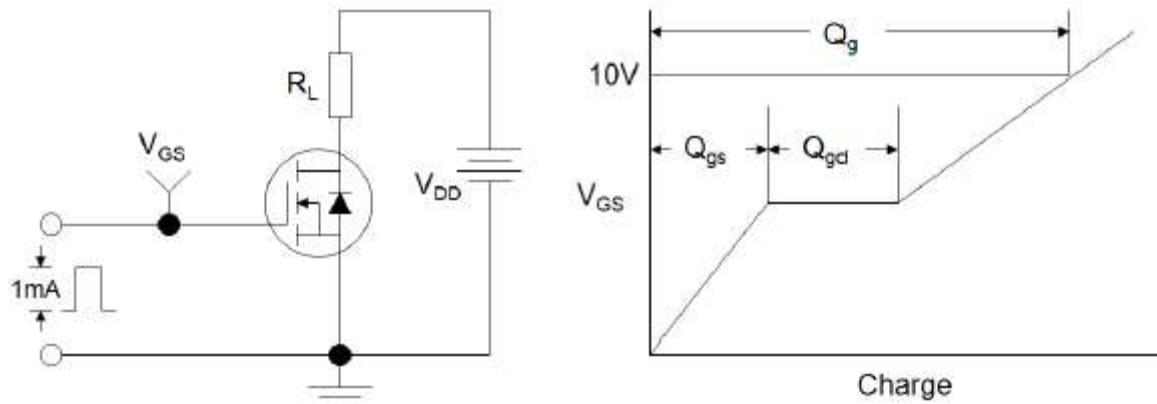


Figure 1: Gate Charge Test Circuit & Waveform

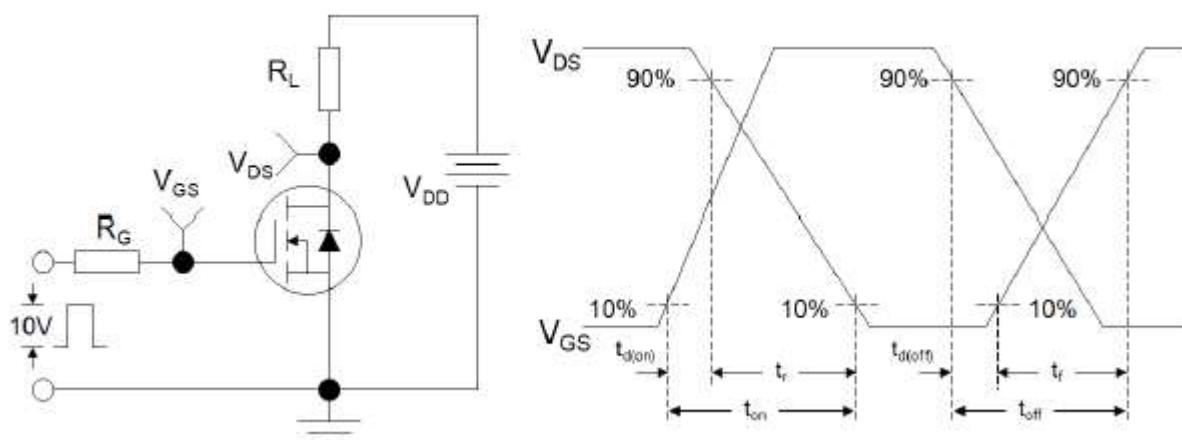


Figure 2: Resistive Switching Test Circuit & Waveforms

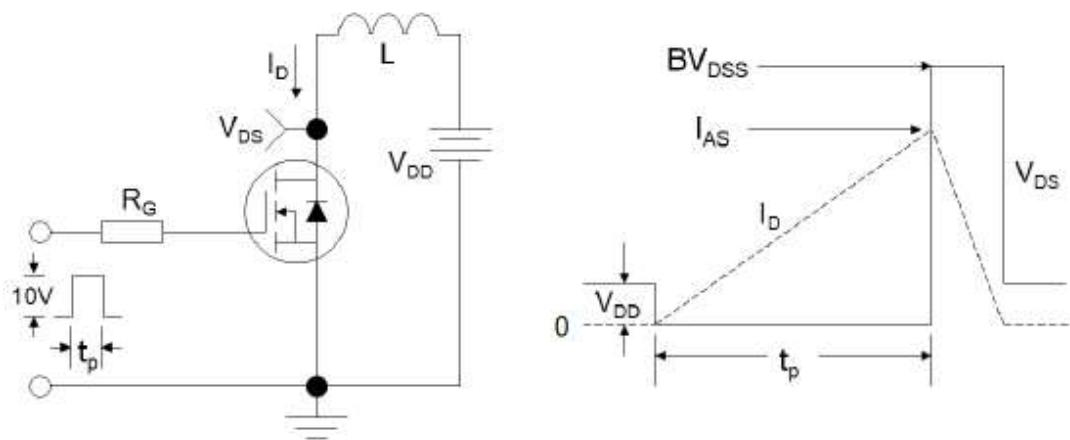


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms