LV8282PV

CD/DVD-ROM/RW 4.5ch Driver

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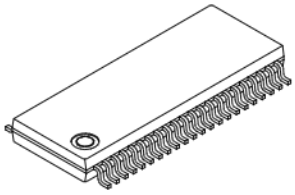


SSOP44K
CASE 940AF

Overview

LV8282PV is a system driver IC which incorporates driver circuits for CD/DVD player system on a single chip with 4 BTL type channels. It adopts 4 output and 5 control input method to use 4ch BTL for SLED and LOADING. When switched to LOADING mode, you can select a control reference voltage between IC internal voltage mode and external voltage (VREF input) mode. During LOADING operation, even if control reference voltage is not supplied, you can still operate the IC without any need for another supply voltage.

LV8282PV incorporates a pin to switch the operation of variable REG circuit independently. Therefore, this IC is suitable to use as regulator.

The dynamic range of this IC is wide with linear MOS technology.

Function

- Incorporated POWER AMP 4ch (BTL Method 4ch)
- I_O MAX: 1 A
- Incorporated Level Shift Circuit
  (BTL Method, Incorporated in the Entire 4ch)
- When BTL Circuit of the 4th ch is in LOADING Mode, you can Select a Control Reference Voltage between Internal Reference Voltage Mode and VREF (External Voltage) Mode
- Incorporated Variable Regulator Control Circuit (which Uses an External NPN-transistor. Voltage is Set by an External Resistor)
- Incorporated ON/OFF Switch Function Controllable Independently by Variable Regulator
- Internal 5 V Regulator Output Pin
- Incorporated Thermal Shutdown Protection Circuit (TSD)
  (Thermal Shutdown Protection Signal Output Pin Included)
- Incorporated Charge Pump

MARKING DIAGRAM

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

Device	Package	Shipping†
LV8282PV	SSOP44K (Pb-Free)	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Paramter	Conditions	Ratings	Unit
V_{CC} max	Supply Voltage		15.0	V
VM max	Output Block Supply Voltage		15.0	V
VG max	Pre-drive Voltage (Gate Voltage)	VG < VM + 8.0 V	21.0	V
I_O max1	Output Current	1ch to 4ch	1.0	A
P_d max1	Allowable Power Dissipation 1	Independent IC	0.55	W
P_d max2	Allowable Power Dissipation 2	Mounted on a specified board (Note 1)	1.65	W
T_{opr}	Operating Temperature Range		−40 to +85	°C
T_{stg}	Storage Temperature		−55 to +150	°C
T_j max	Junction Temperature		+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Mounted on a board:76.1 mm × 114.3 mm × 1.6 mm, glass epoxy board.

RECOMMENDED OPERATING CONDITIONS (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply Voltage 1		5.5 to 13	V
VM1,2	Output Block Supply Voltage 2		5.5 to 13	V
I_O max2	Output Current		0.8	A

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit Blocks shared in the system, T_A = 25°C, V_{CC} = VM1 = VM2 = 8.0 V, VREF = 2.5 V)

Symbol	Parameter	Condtions	Min	Typ	Max	Unit
$I_{CC}1$	Quiescent Current 1	Total voltage of V_{CC} + VM1 + VM2	–	6.5	9.0	mA
$I_{CC}2$	Quiescent Current 2	EN1, EN2 = L, SWREG = H Total current of V_{CC} + VSM1 + VM2	–	2.0	3.0	mA
$I_{CC}3$	Quiescent Current 3	EN1, EN2 = L, SWREG = L Total current of V_{CC} + VSM1 + VM2	0	–	10	μA
VG PIN						
VG1	Output Voltage 1	VM1 = VM2 = 8 V	VM + 5.5	VM + 8	VM + 8.5	V
OVERHEAT PROTECTION CIRCUIT						
TSD	Thermal Shutdown Temperature	Design target value	150	–	180	°C
ΔTSD	Hysteresis Width	Design target value	–	25	–	°C
TSDO	Signal Output Pin Voltage	Design target value: I_O = 0.5 mA	–	0.2	–	V
EN 1,2						
V_{ENH}	H Level Input Voltage Range		2.0	–	V_{CC}	V
V_{ENL}	L Level Input Voltage Range		0	–	0.6	V
IEN	Input Current	3.3 V input	30	65	80	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

BTL BLOCK at (1 to 4ch) (T_A = 25°C, V_{CC} = VM1 = VM2 = 8.0 V, VREF = 2.5 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DRIVE (BTL AMP)						
VREFIN	Reference Voltage Input Range		1	–	3	V
V_{IN}						
V_{IN}	Control Input Voltage Range		0	–	5	V
OUTPUT (V_O1,2,3,4±)						
VSAT	Output Saturation Voltage	Total of saturation voltages of upper and lower output transistors at I_O = 0.2 A (2.5 Ω assumed for upper and lower transistors)	–	0.5	0.9	V
VOFF	Offset Voltage between Outputs	At load of 8 Ω	−50	–	50	mV
VGAIN	Input-output Voltage Gain	At load of 8 Ω	24.0	24.4	25.2	dB
SR	Slew Rate	Design target value	–	1	–	V/μS
LVREF	LOADING Internal Reference Voltage	LOADING mode (only 4ch)	1.55	1.65	1.75	V

POWER SUPPLY BLOCK (T_A = 25°C, V_{CC} = VM1 = VM2 = 8.0 V, VREF = 2.5 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5 V REGULATOR BLOCK (REG5)						
REG5	Output Voltage	I_O = 0 mA	4.8	5.0	5.3	V
IREGO	Output Current		–	–	20	mA
LVSOFF	Voltage to Cancel the Reduced-Voltage Protection Voltage		3.95	4.15	4.7	V
LVSON	Voltage to Enable the Reduced-Voltage Protection	All outputs OFF	3.4	3.6	3.85	V
EXTERNAL VARIABLE REGULATOR CONTROL (REGO, FR)						
SWREG PIN						
V_{SWH}	H Level Input Voltage Range	Variable REG block ON	2.0	–	V_{CC}	V
V_{SWL}	L Level Input Voltage Range	Variable REG block OFF	0	–	0.6	V
REGO						
IREGO	Control Output Current	SOUCE current	1.0	1.3	1.5	mA
CHARGE PUMP (CP, CPC, VG)						
fcp	Switching Frequency 1	CPSW: 0 to 0.9 V	85	120	165	kHz
fcp	Switching Frequency 2	CPSW: 1.2 to 2.4 V	110	145	190	kHz
fcp	Switching Frequency 3	CPSW: 2.7 to 3.9 V	65	90	140	kHz
CPSW						
VCPSW	CPSW Input Voltage Range		0	–	REG5	V
CPSTOP	Charge Pump Stop Voltage		4.3	–	REG5	V
VG VOLTAGE LIMIT						
VGLIM1	VG Voltage Limit 1	Normal voltage step-up limit	V_{CC} + 7.0	V_{CC} + 8	V_{CC} + 8.5	V
VGLIM2	VG Voltage Limit 2	VG step-up maximum voltage limit	–	–	21	V

LV8282PV CONTROL TRUTH VALUE TABLE

InpUT			Drive Channel				Remarks
EN1	EN2	SWREG	1,2ch	3ch	4ch	VREF (5VREG)	
H	H	*	ACTIVE	MUTE	ACTIVE	ACTIVE	4chBTL: Controlled w/IN5 (LD) External control reference (VREF) input
H	L	*	ACTIVE	ACTIVE	ACTIVE	ACTIVE	4chBTL: Controlled w/IN4 (SL) External control reference (VREF) input
L	H	*	MUTE	MUTE	ACTIVE	ACTIVE	4chBTL: Controlled w/IN5 (LD) Switches to internal control reference voltage (typ = 1.65 V)
L	L	H	MUTE	MUTE	MUTE	ACTIVE	
L	L	L	MUTE	MUTE	MUTE	MUTE	Standby Mode

SWREG	Variable REG
H	ACTIVE
H	MUTE

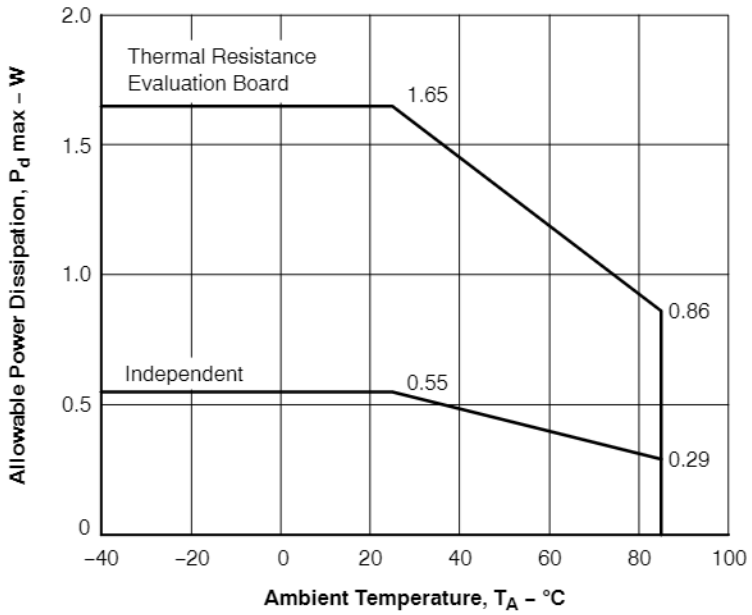


Figure 1. P_d max – T_A

BLOCK DIAGRAM

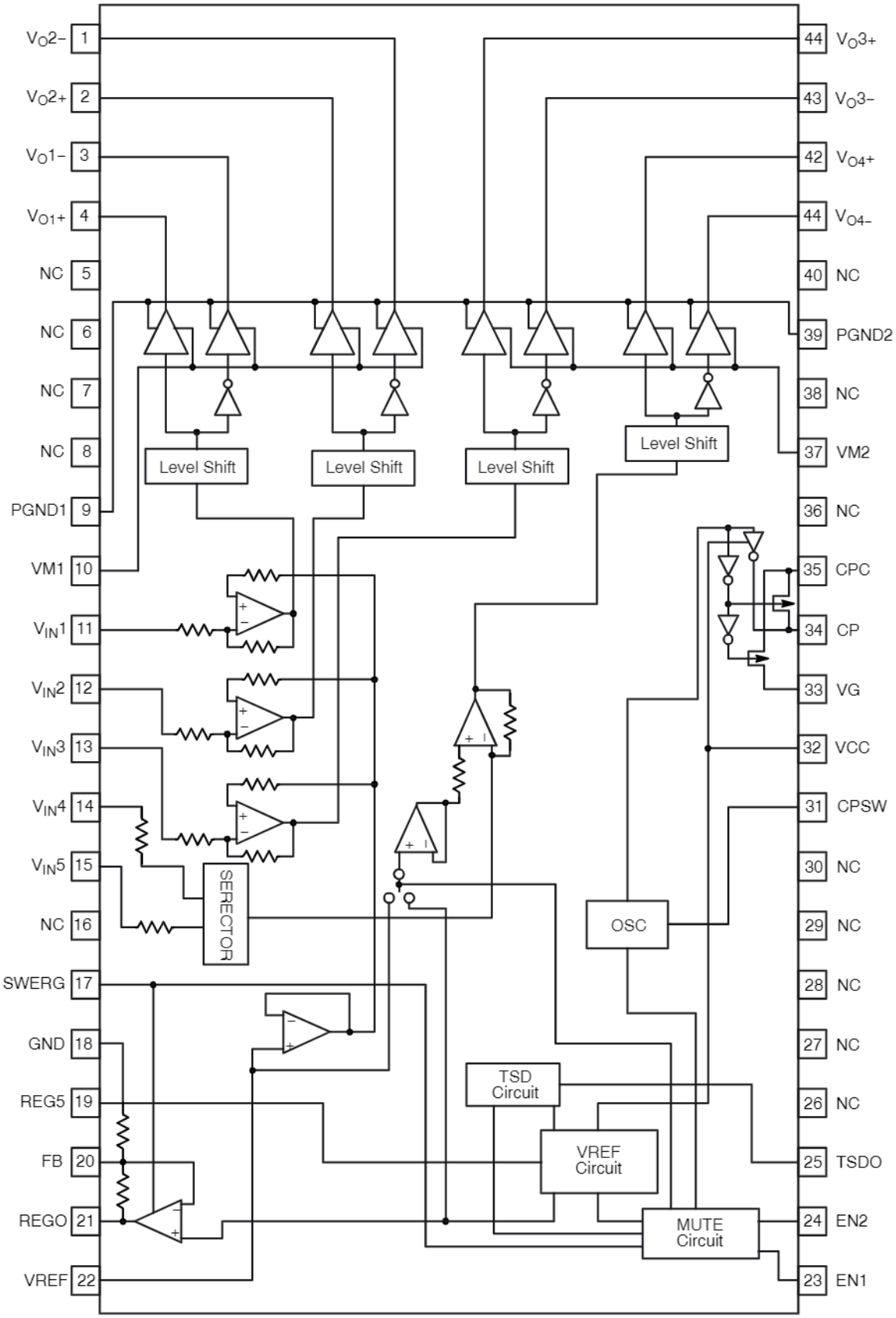
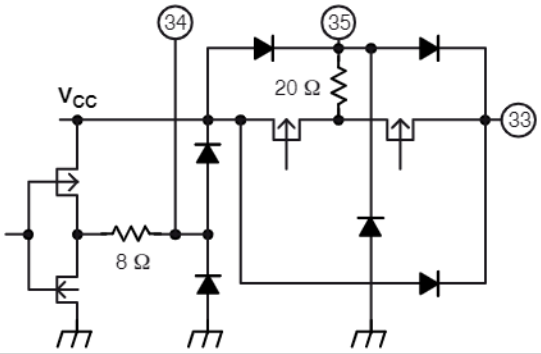
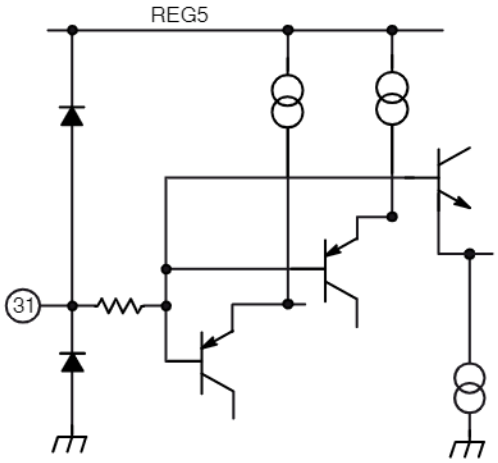
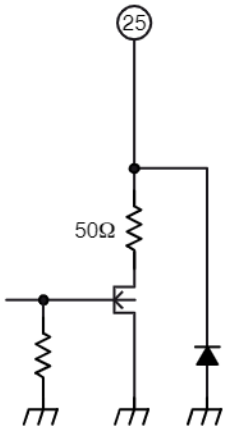
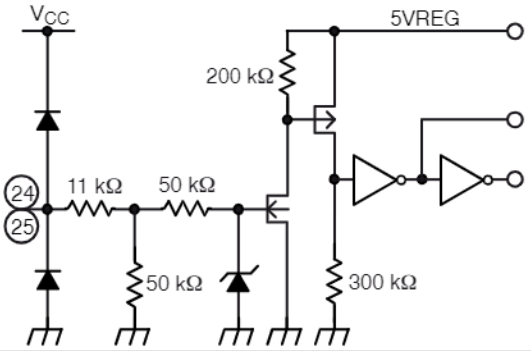
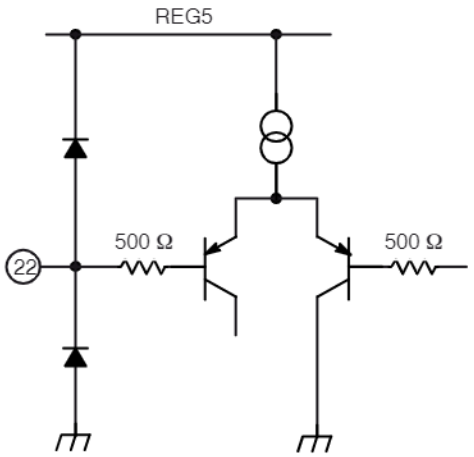
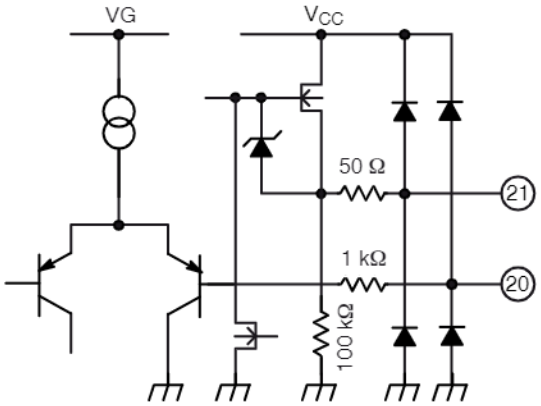
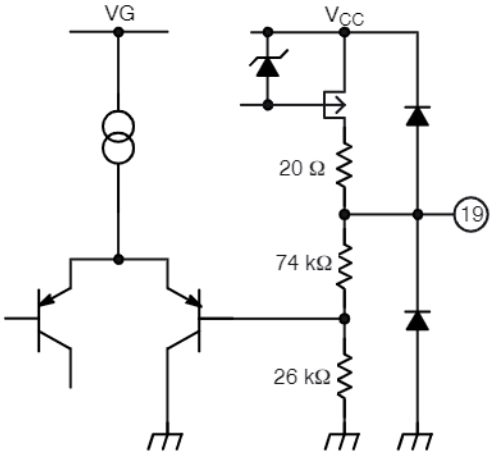


Figure 2. Block Diagram (Pin Assignment Top View)

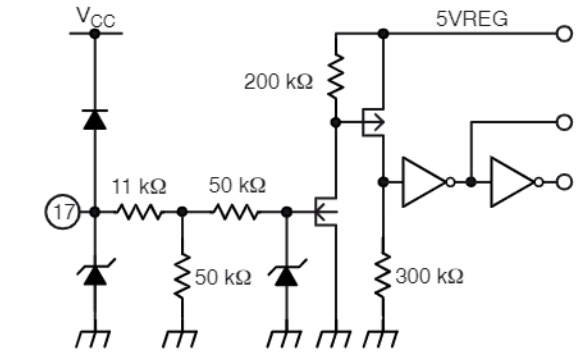
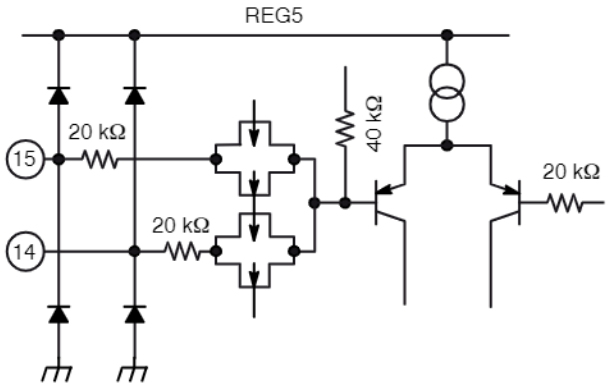
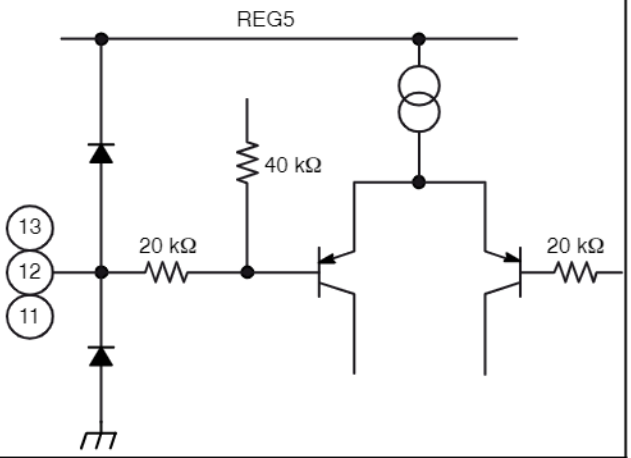
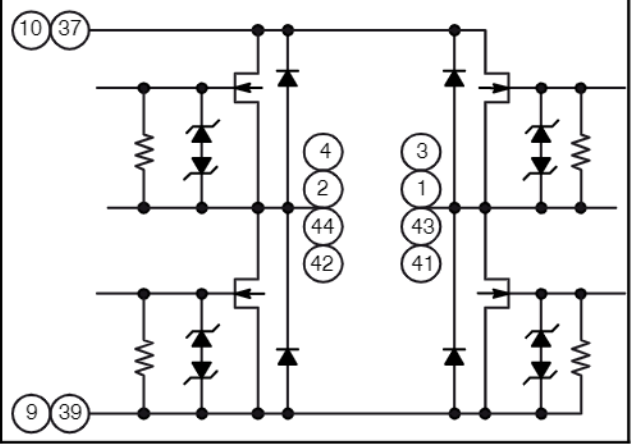
PIN FUNCTION

Pin No.	Pin Name	Function	Equivalent Circuit
35	CPC	Charge pump step−up pin. Make sure to connect a capacitor between CPC and CP (PIN11)	
34	CP	Charge pump step-up pin. Make sure to connect a capacitor between CP and CPC (PIN10)	
33	VG	Charge pump step-up output pin. Connect a capacitor between this pin and GND	
32	V_{CC}	Small signal block power pin	
31	CPSW	Switching frequency switching pin for charge pump	
25	TSDO	Thermal Shutdown circuit operation output pin	
24 23	EN2 EN1	Control signal input pin	

PIN FUNCTION (continued)

Pin No.	Pin Name	Function	Equivalent Circuit
22	VREF	VREF reference voltage input pin	
21 20	REGO FB	Regulator error amplifier output. Make sure to connect this pin to the base of the external NPN−transistor. Regulator error amplifier input	
19	REG5	Internal regulator output pin	
18	GND	Small signal system circuit GND pin	

PIN FUNCTION (continued)

Pin No.	Pin Name	Function	Equivalent Circuit
17	SWREG	Regulator ON−OFF control pin	
15 14	$V_{IN}5$ $V_{IN}4$	− CH5 control signal input pin − CH4 control signal input pin	
13 12 11	$V_{IN}3$ $V_{IN}2$ $V_{IN}1$	− CH3 control signal input pin − CH2 control signal input pin − CH1 control signal input pin	
37 10	VM2 VM1	CH3,CH4 motor power supply pin CH1,CH2 motor power supply pin Make sure to connect a capacitor between GND and this pin.	
3, 4	$V_O1\pm$	CH1 inverted/non-inverted output pin	
1, 2	$V_O2\pm$	CH2 inverted/non-inverted output pin	
43, 44	$V_O3\pm$	CH3 inverted/non-inverted output pin	
41, 42	$V_O4\pm$	CH4 inverted/non-inverted output pin	
39 9	PGND2 PGND1	CH1, CH2, CH3, CH4 POWER GND pin	

LV8282 CAUTION FOR USE

1. Supply voltage of VM1 and VM2:
   This IC is intended to be used under the following condition: VM1 = VM2 = V_{CC}. However, if you wish to use this IC with a different voltage, cautions are required.
   Make sure that power supply of VM2 (3ch, 4ch motor power supply) is the same as that of V_{CC}.
   If you supply different voltage to VM1 (1ch, 2ch motor power supply), the voltage should be as follows: VM2 = V_{CC} = VM1
   Supply power to V_{CC} = VM2 first.
   Do not supply power to VM1 alone.
2. Variable Regulator:
   Variable Regulator ON−OFF control pin: SWREG is a gate input pin of Nch MOS. If this pin is open, the operation of variable regulator may be unstable. If by any possibility SWREG pin is set to open, countermeasure is required such as use of a pull-down resistor.

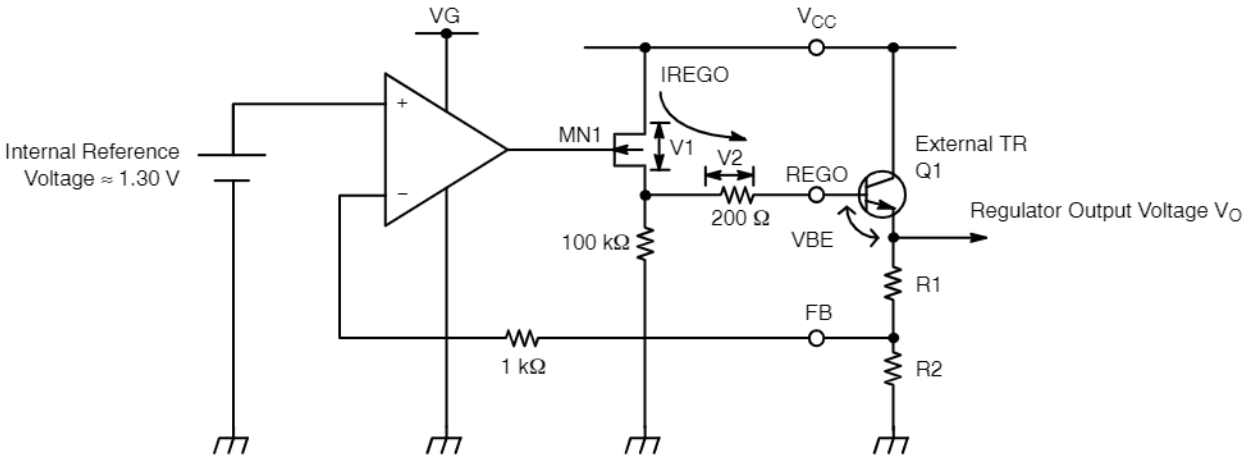


Figure 3. Variable Regulator Block

The maximum setting voltage of the regulator output voltage VO is expressed as
VO max = VCC − (VBE + V1 + V2) as shown in the figure above. (Approximately, this is VBE + V1 + V2 ≈ 1 V. Since VBE varies depending on the output load and the external Q1 to be used, check it by means of an actual application.)

3. Timing of Control Signal Input to EN1, EN2, and SWREG pins:
   When supplying voltage (V_{CC}, VM) to LV8282, make sure to adjust the timing so that power is supplied to EN1, EN2 and SWREG after the voltage levels are set to "L" level.
   After power supply, make sure to perform control when the voltage is stabilized. (The time varies depending on V_{CC} of LV8282 and capacitor between VM and GND.)
4. Relationship of Input and Output and Internal Gain Setting for LV8282 1, 2, 3 and 4ch.

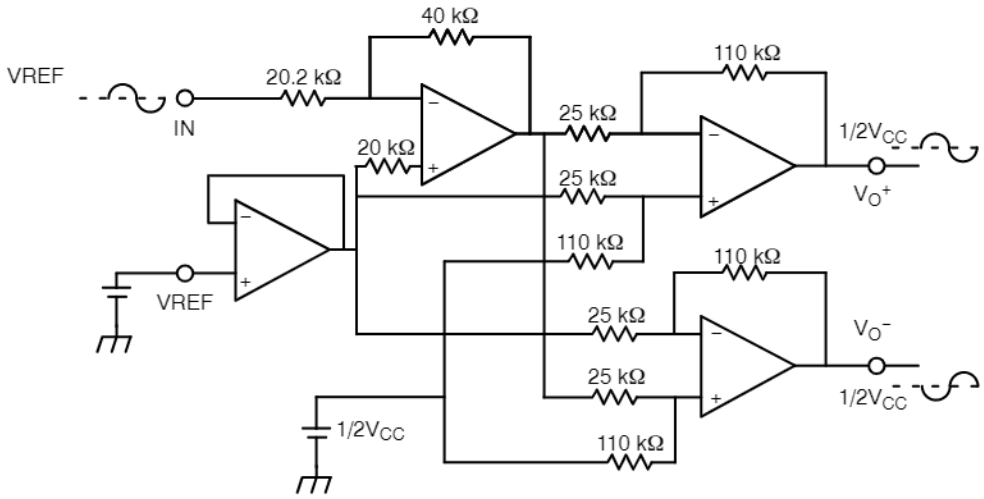


Figure 4.

The signal phases of IN input and VO+ output are the same.

5. Charge Pump Operation, and the VG Voltage Limit.

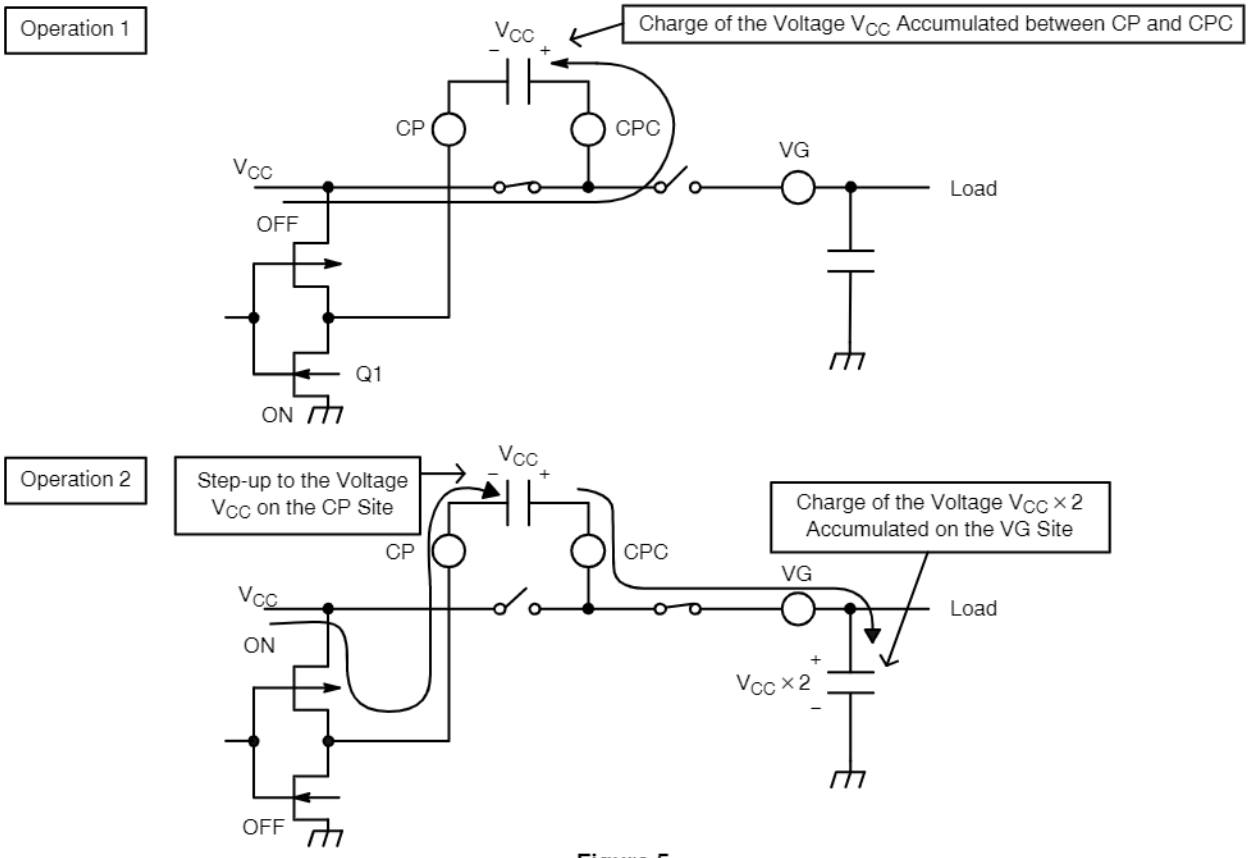


Figure 5.

When the VG pin voltage reaches the set voltage, the operation 1 controls (reduces) ON−DUTY of transistor Q1, limiting the charge level of the capacitor. (When the VG pin voltage exceeds the set voltage, the step−up operation is stopped. This is called VG limit voltage.)

In principle, V_{CC} voltage can be doubled and output to VG. However in general, the voltage

becomes lower than the theoretical value depending on the load conditions. This is because of the loss due to the transistor ON resistance and the resistance of charge transfer switch.
ON/OFF of Q1
(switching frequency fcp: 120 kHz: CPSW = 0V)

The relationship between the V_{CC} = VM voltage and the VG pin set voltage (VG limit voltage) is as follows.

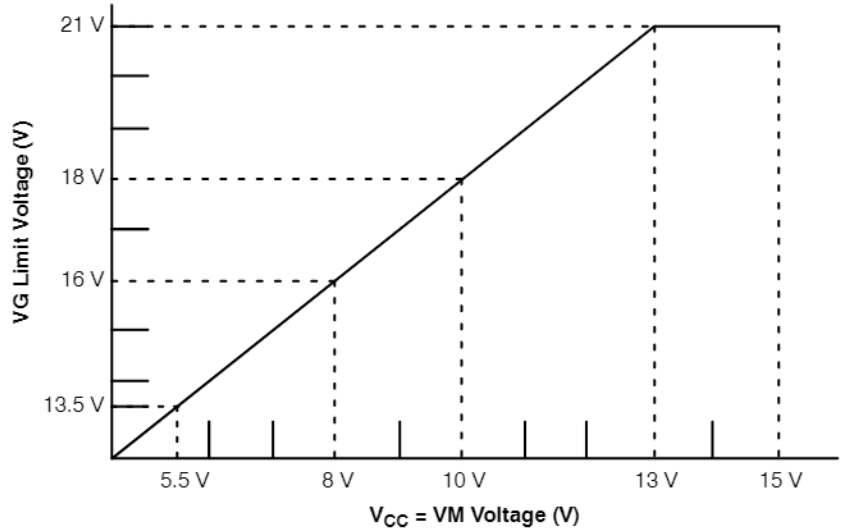


Figure 6. Correlation Diagram between V_{CC} = VM and VG Limit Voltage

6. Reduced-voltage Protection Function (LVS):
When the voltage of internal regulator (REG5) is monitored and if the voltage is 3.6 V (TYP) or lower, BTL output (VO1, 2, 3, 4±) and the external regulator (REGO) are turned off. When REG5 is 4.15 V (typ) or higher, control is performed according to truth value table (p3).

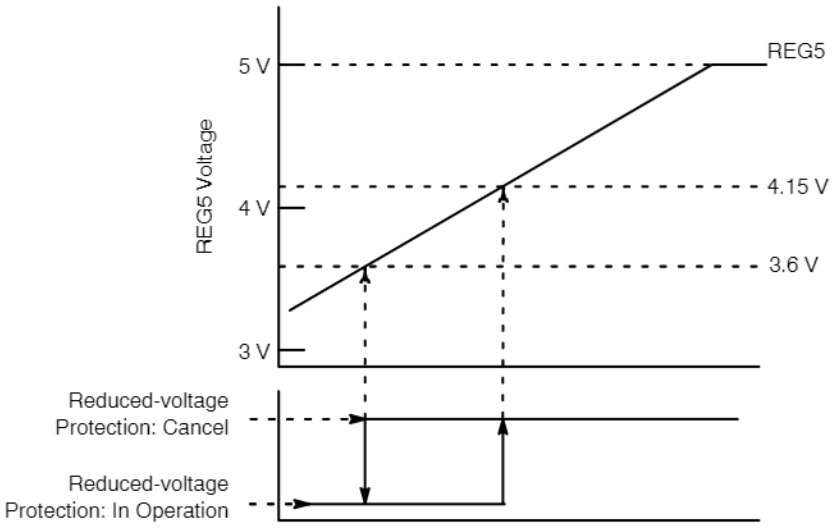


Figure 7. Correlation Diagram between Reduced-voltage Protection Operation and Internal 5 V Regulator Voltage (REG5)

7. TSD:
When TSDO is used with pull-up resistor, during operation of thermal shutdown circuit, the voltage level is set to “L”. In this case, VO1, 2, 3, 4± output of CH1, 2, 3, 4 are turned off.
(REGO: external regulator control circuit is not turned off.)

APPLICATION CIRCUIT EXAMPLE

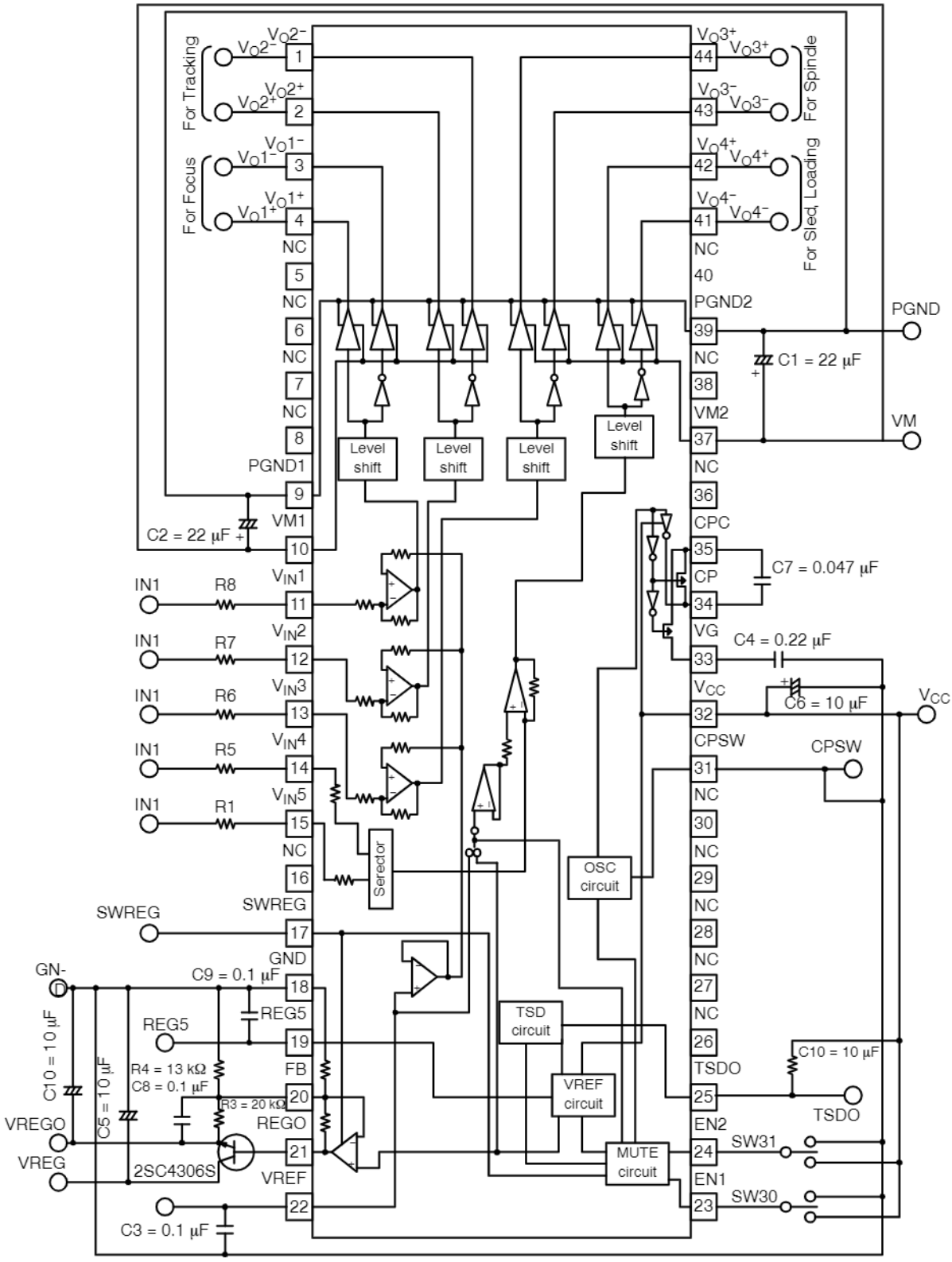
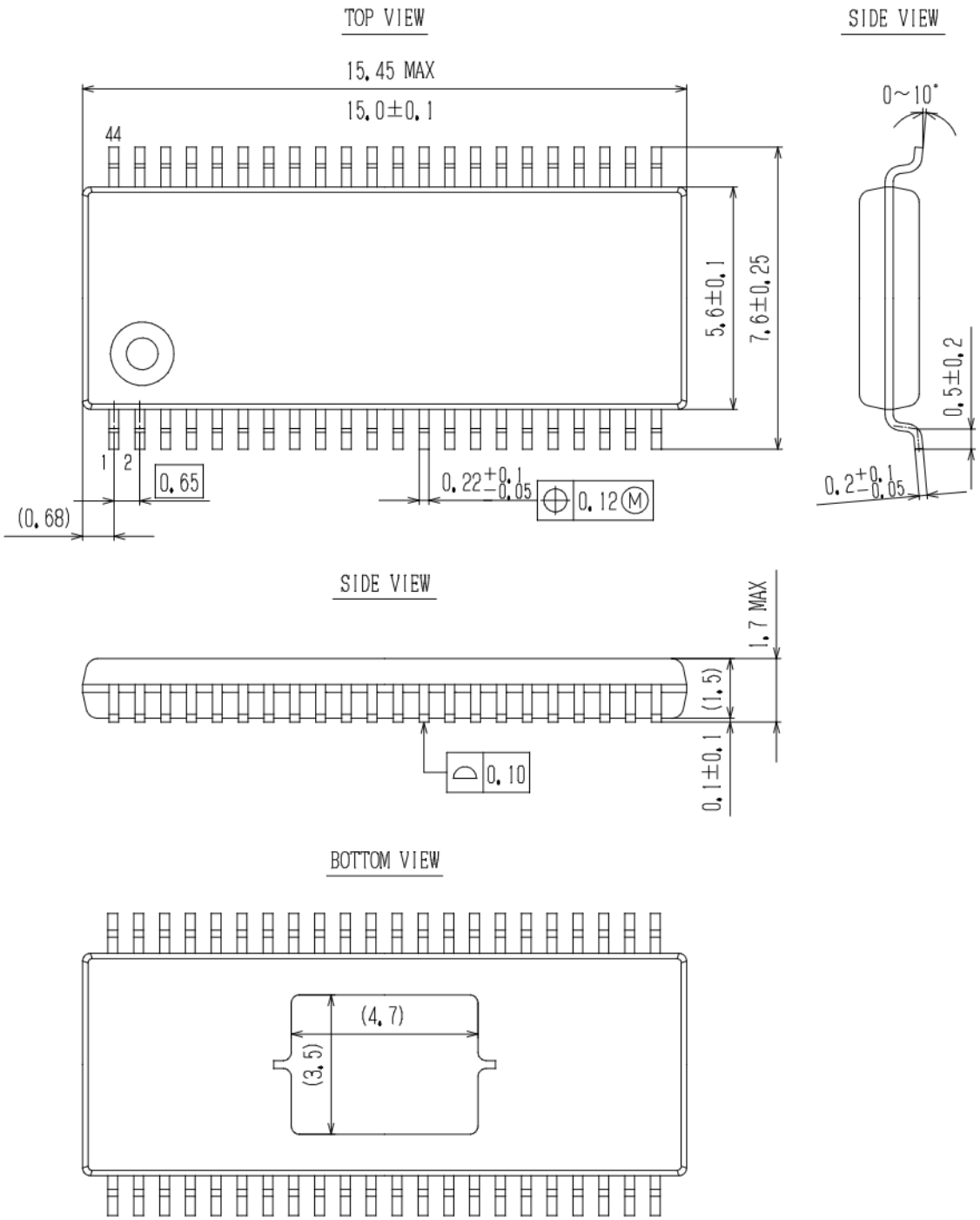


Figure 8. Application Circuit Example

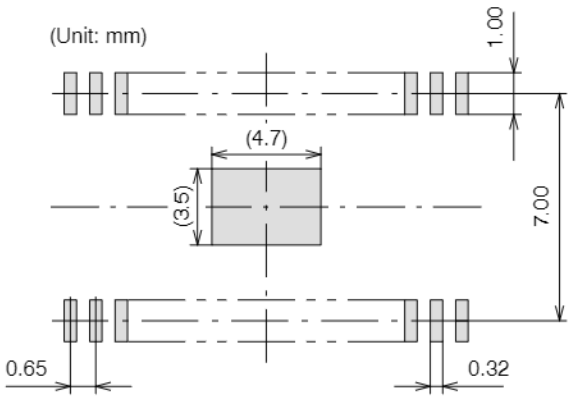
Regarding C4, C7 as shown in the example of application circuit, VG max voltage (21 V) may be supplied due to V_{CC} (= VM1, 2). Hence, caution is required on withstanding voltage of the part for use.

PACKAGE DIMENSIONS

SSOP44K (275mil) Exposed Pad
CASE 940AF
ISSUE A



SOLDERING FOOTPRINT*



NOTES:

1. The measurements are for reference only, and unable to guarantee.
2. Please take appropriate action to design the actual Exposed Die Pad and Fin portion.
3. After setting, verification on the product must be done.
   (Although there are no recommended design for Exposed Die Pad and Fin portion Metal mask and shape for Through−Hole pitch (Pitch & Via etc), checking the soldered joint condition and reliability verification of soldered joint will be needed. Void ▪ gradient ▪ insufficient thickness of soldered joint or bond degradation could lead IC destruction because thermal conduction to substrate becomes poor.)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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