MAX31911 Industrial, Octal, Digital Input Translator/Serializer

General Description

The MAX31911 industrial interface serializer translates, conditions, and serializes the 24V digital output of sensors and switches used in industrial, process, and building automation to 5V CMOS-compatible signals required by microcontrollers. It provides the front-end interface circuit of a programmable logic controller (PLC) digital input module.

The device features integrated current limiting, low-pass filtering, and channel serialization. Input current limiting allows a significant reduction in power consumed from the field voltage supply as compared to traditional discrete resistor-divider implementations. Selectable on-chip lowpass filters allow flexible debouncing and filtering of sensor outputs based on the application.

On-chip serialization allows a drastic reduction in the number of optocouplers used for isolation. The device serializer is stackable so that any number of input channels can be serialized and output through only one SPI-compatible port. This reduces the number of optocouplers needed to only three, regardless of the number of input channels.

For enhanced robustness with respect to high-frequency noise and fast electrical transients, a multibit CRC code is generated and transmitted through the SPI port for each 8 bits of data. The on-chip 5V voltage regulator can be used to power external optocouplers, digital isolators, or other external 5V circuitry.

For ultra-low-power applications, Maxim Integrated offers a pin-compatible version of this device, the MAX31910. The MAX31910 uses patent-pending circuit techniques to achieve further reduction of power beyond what is possible by input current limiting alone.

The MAX31912 and MAX31913 versions include energy-less LED drivers while maintaining pin compatibility.

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Very Low Power and Heat Dissipation
  - Low Quiescent Current (1.4mA typ)
  - Highly Accurate and Stable Input Current Limiters, Adjustable from 0.5mA to 6mA
- High Integration Reduces BOM Count, Board Size, and System Cost
  - Eight High-Voltage Input Channels (36V max)
  - On-Chip 8-1 Serialization with SPI Interface
  - On-Chip 5V Regulator
  - On-Chip Overtemperature Indicator
  - On-Chip Field Supply Voltage Monitor
  - Integrated Debounce Filters, Selectable from 0 to 3ms
- Robust Features and Performance for Industrial Environments
  - Multibit CRC Code Generation and Transmission for Error Detection and More Reliable Data Transmission
  - High ESD Immunity on All Field Input Pins
- Accepts Industry Standard Input Types
  - Configurable for IEC 61131-2 Input Types 1, 2, and 3
- Flexible Power Supply Capability Enables Usage in 5V, 12V, 24V, and Higher Voltage Systems
  - Wide Operating Field Supply Range of 7V to 36V
  - Can Be Powered from the Logic-Side Using a 5V Supply

Applications

- Digital Input Modules for PLCs
- Industrial, Building, and Process Automation
- Motor Control

19-6441; Rev 7; 8/17

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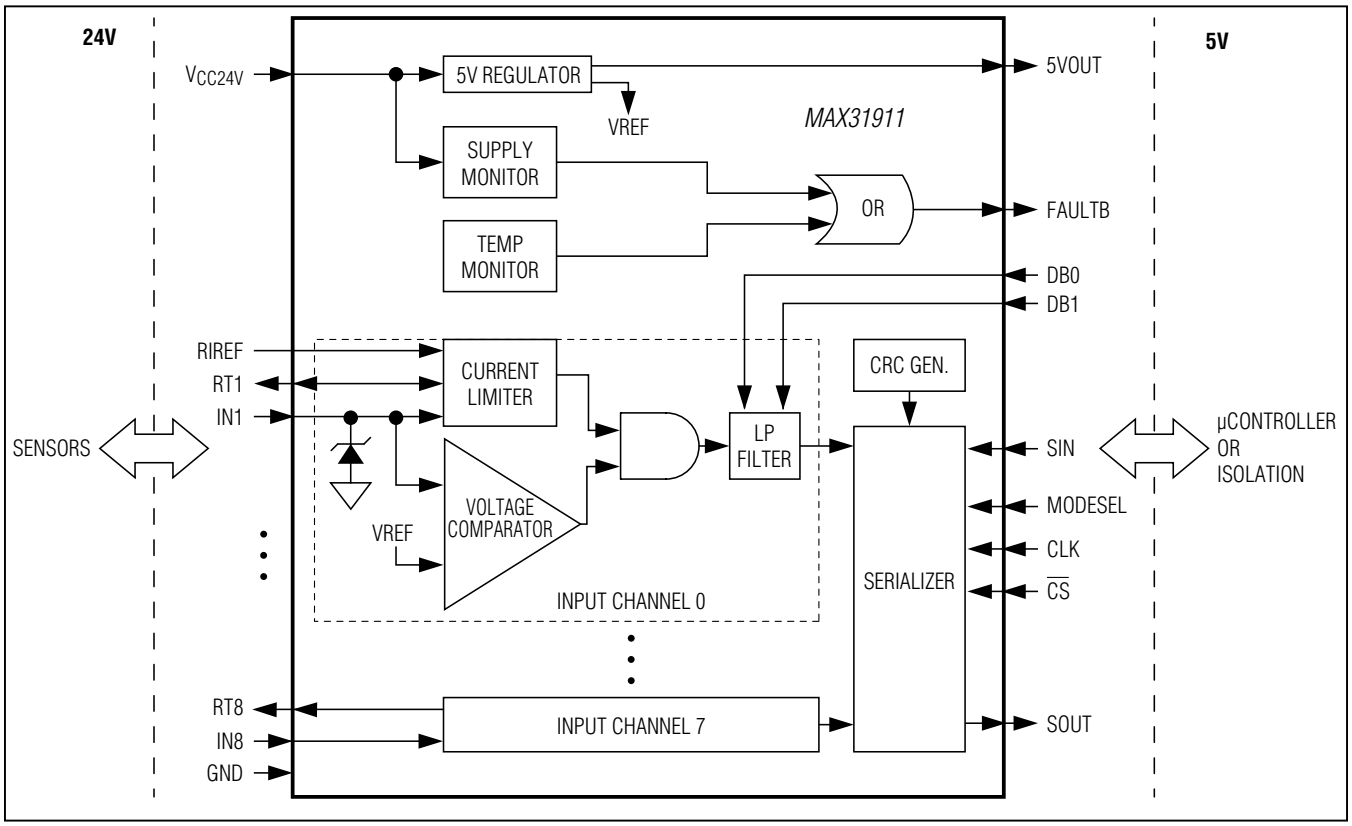
Block Diagram



Absolute Maximum Ratings

(Voltages relative to GND.)
Voltage Range on V_{CC24V} ..... -0.3V to +45V
Voltage Range on IN1–IN8 ..... -0.3V to +45V
Voltage Range on IN1–IN8
(through 2.2kΩ resistors)..... -45V to +45V
Voltage Range on DB0/DB1, CLK, SIN,
$\overline{CS}$, MODESEL ..... -0.3V to (V_{5VOUT} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 27mW/°C above +70°C)..... 2162.2mW

Operating Temperature Range
Ambient Temperature.....-40°C to +125°C
Junction Temperature.....-40°C to +150°C
Storage Temperature Range.....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....37°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Field Supply Voltage	V_{CC24V}		7		36	V
Field Inputs Voltage	V_{INn}	(Note 3)	-0.3		36	V
Logic Inputs Voltage	V_{LOGIC}		0		5.5	V
Current-Limit Setting Resistor	R_{REF}			15		kΩ
Field Input Data Rate	f_{IN}	(Note 4)		200		kHz

DC Electrical Characteristics

(V_{CC24V} = 7V to 36V, T_J = -40°C to +150°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Field-Supply Current	I_{CC24V}	IN1–IN8 = 24V, 5VOUT = open, RT1–RT8 = GND, all logic inputs open		1.4	2.0	mA
Field-Supply UVLO Off/On	V_{ONUVLO}			9	10	V
Field-Supply UVLO On/Off	$V_{OFFUVLO}$		7	8		V
Field Input Threshold High-to-Low	$V_{IN-(INF)}$	2.2kΩ external series resistor	6	7.5		V
Field Input Threshold Low-to-High	$V_{IN+(INF)}$	2.2kΩ external series resistor		8.5	10	V
Field Input Hysteresis	$V_{HYS(INF)}$	2.2kΩ external series resistor		1		V
Input Threshold High-to-Low (at IC pin)	$V_{TH-(INP)}$		2	2.5		V
Input Threshold Low-to-High (at IC pin)	$V_{TH+(INP)}$			3.5	4	V
Input Threshold Hysteresis (at IC pin)	$V_{HYS(INP)}$			1		V
Field Input Pin Resistance	R_{INP}			0.8		kΩ
Field Input Current Limit	I_{INLIM}	R_{REF} = 15kΩ, V_{CC24V} = 18V to 30V (Note 5)	2.2	2.4	2.6	mA
Filter Time Constant	t_{FILTER}	DB1/DB0 = 0/0: no filtering		0		ms
		DB1/DB0 = 0/1	0.008	0.025	0.038	
		DB1/DB0 = 1/0	0.25	0.75	1.1	
		DB1/DB0 = 1/1	1.0	3	4.5	
Linear Regulator Output	V_{5VOUT}	Max I_{LOAD} = 50mA	4.75	5.0	5.25	V
Regulator Line Regulation	$dVREG_{LINE}$	I_{LOAD} = 50mA		10	20	mV
Regulator Load Regulation	$dVREG_{LOAD}$	I_{LOAD} = 1mA to 50mA		20	50	mV
Logic-Low Output Voltage	V_{OL}	I_{OL} = 4mA		0.4	1.0	V
Logic-High Output Voltage	V_{OH}	I_{OH} = -4mA	4.0			V
Logic-Input Trip Point	V_{IH-IL}		0.3 x V_{5VOUT}	0.5 x V_{5VOUT}	0.7 x V_{5VOUT}	V
Logic-Input Leakage Current	I_{IL}		-50	-30	-15	µA
Overtemperature Alarm	T_{ALRM}			135		°C

AC Electrical Characteristics

(V_{CC24V} = 7V to 36V, T_J = -40°C to +150°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Field Input Pulse Width	t_{PW}	No external capacitors on pins IN1–IN8	1			µs
ESD		HBM, all pins except IN1-IN8		±2		kV
		HBM, IN1–IN8 with respect to GND		±15		

AC Electrical Characteristics: SPI Interface

(V_{CC24V} = 7V to 36V, T_J = -40°C to +150°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Pulse Duration	t_{CLKPW}	(Note 6)	20			ns
$\overline{CS}$ Pulse Duration	t_{CSPW}	(Note 7)	20			ns
SIN to CLK Setup Time	t_{SU1}	(Note 8)	5			ns
SIN to CLK Hold Time	t_{H1}	(Note 8)	8			ns
$\overline{CS}$ to CLK Setup Time	t_{SU2}	(Note 9)	8			ns
$\overline{CS}$ to CLK Recovery Time	t_{REC}	(Note 9)	12			ns
Clock Pulse Frequency	f_{CLK}	(Notes 6, 10)			25	MHz
Propagation Delay, CLK to SOUT	t_{P1}	(Note 6)			20	ns
Propagation Delay, $\overline{CS}$ to SOUT	t_{P2}	(Note 7)			20	ns
Rise/Fall Time SOUT/$\overline{FAULT}$	$t_{R/F}$	(Note 6)			40	ns

Note 2: Limits are 100% production tested at T_A = +25°C and/or T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 3: When using suggested external 2.2kΩ series resistors, limits of -3V to +36V apply.

Note 4: f_{IN} refers to the maximum pulse frequency ($1/f_{IN}$ = shortest pulse width) that can be detected from the field sensors and switches.

Note 5: External resistor R_{REF} can be adjusted to set any desired current limit between 0.5mA and 6mA.

Note 6: See Figure 9.

Note 7: See Figure 6.

Note 8: See Figure 8.

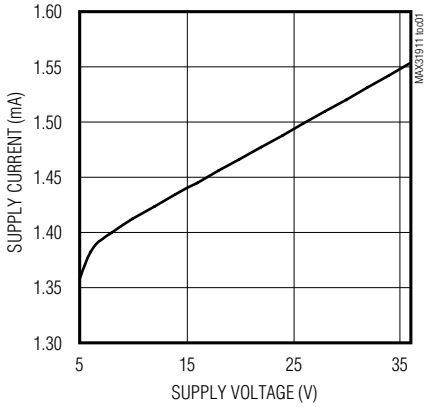
Note 9: See Figure 7.

Note 10: This is the maximum bit transfer rate through the serializer interface.

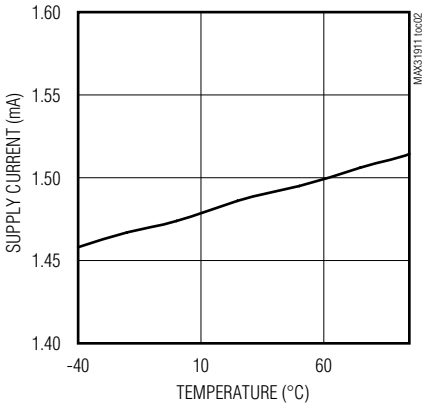
Typical Operating Characteristics

(T_A = +25°C, R_{REF} = 15kΩ, unless otherwise noted.)

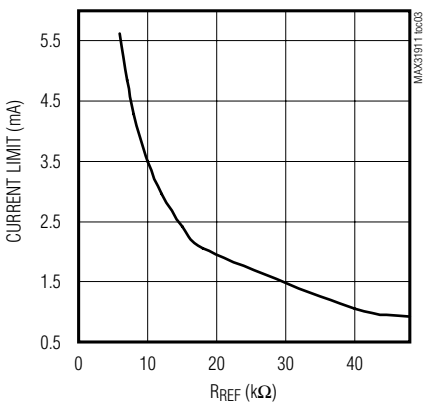
POWER-SUPPLY CURRENT vs. V_{CC24V} FIELD SUPPLY



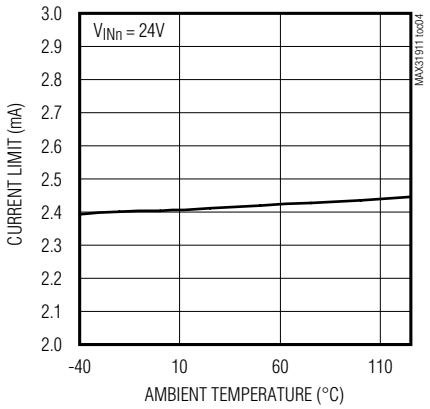
SUPPLY CURRENT vs. TEMPERATURE



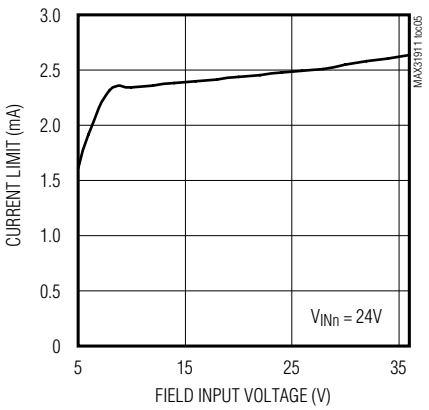
CURRENT LIMIT vs. R_{REF}



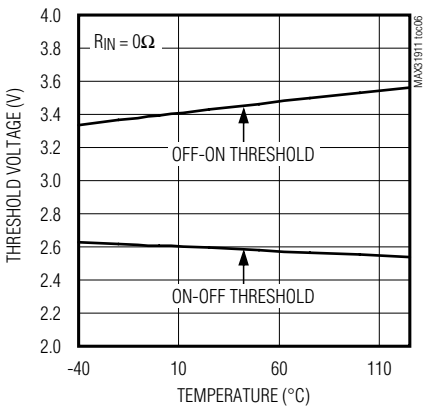
INPUT CURRENT LIMIT vs. TEMPERATURE



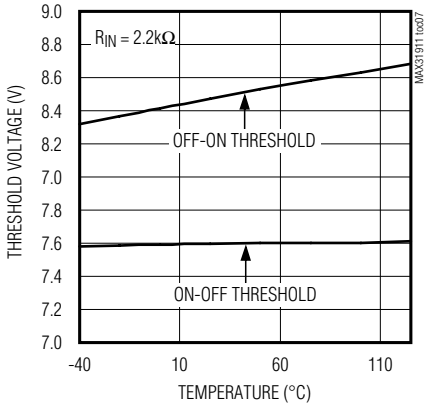
INPUT CURRENT LIMIT vs. FIELD INPUT VOLTAGE



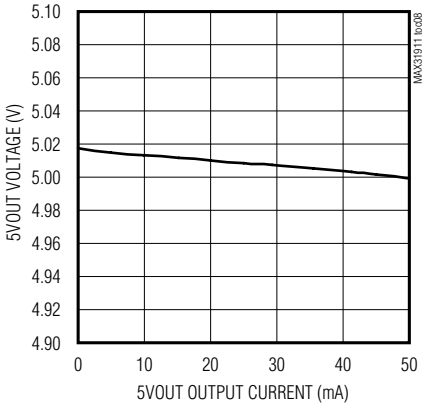
INPUT VOLTAGE HYSTERESIS vs. TEMPERATURE



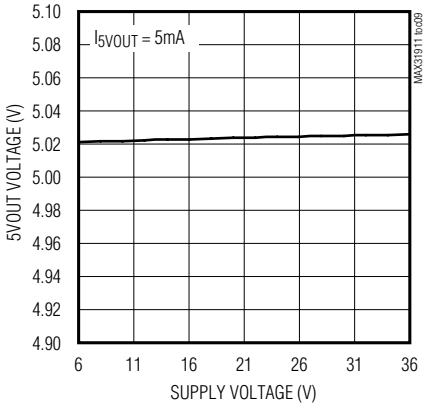
INPUT VOLTAGE HYSTERESIS vs. TEMPERATURE



LDO LOAD REGULATION



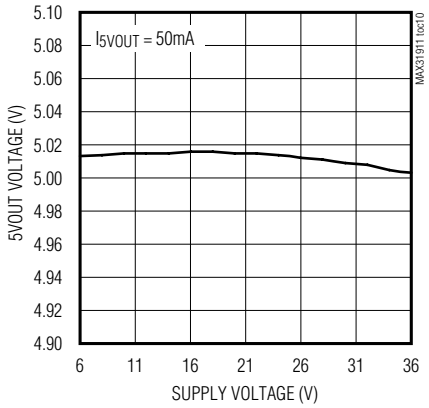
LDO LINE REGULATION



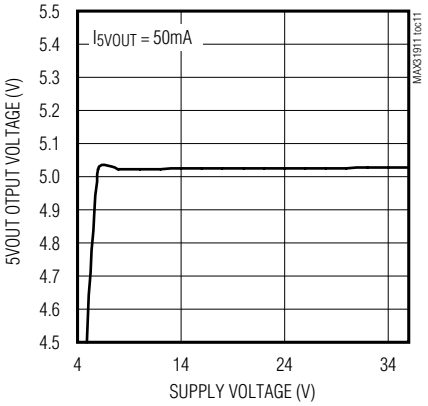
Typical Operating Characteristics (continued)

(T_A = +25°C, R_{REF} = 15kΩ, unless otherwise noted.)

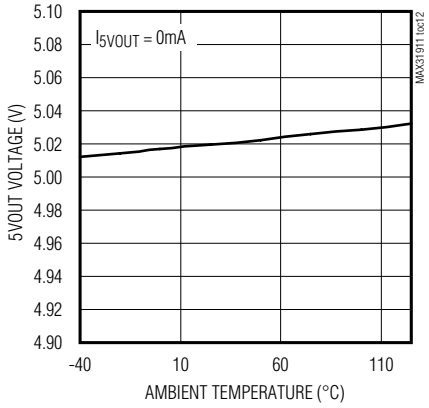
LDO LINE REGULATION



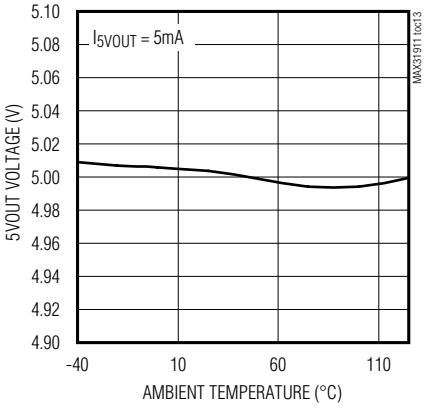
LDO OUTPUT vs. V_{CC24V} FIELD SUPPLY



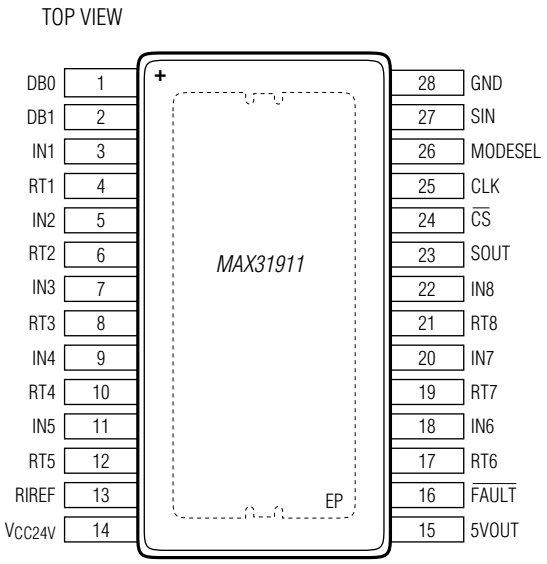
LDO OUTPUT VOLTAGE vs. TEMPERATURE



LDO OUTPUT VOLTAGE vs. TEMPERATURE



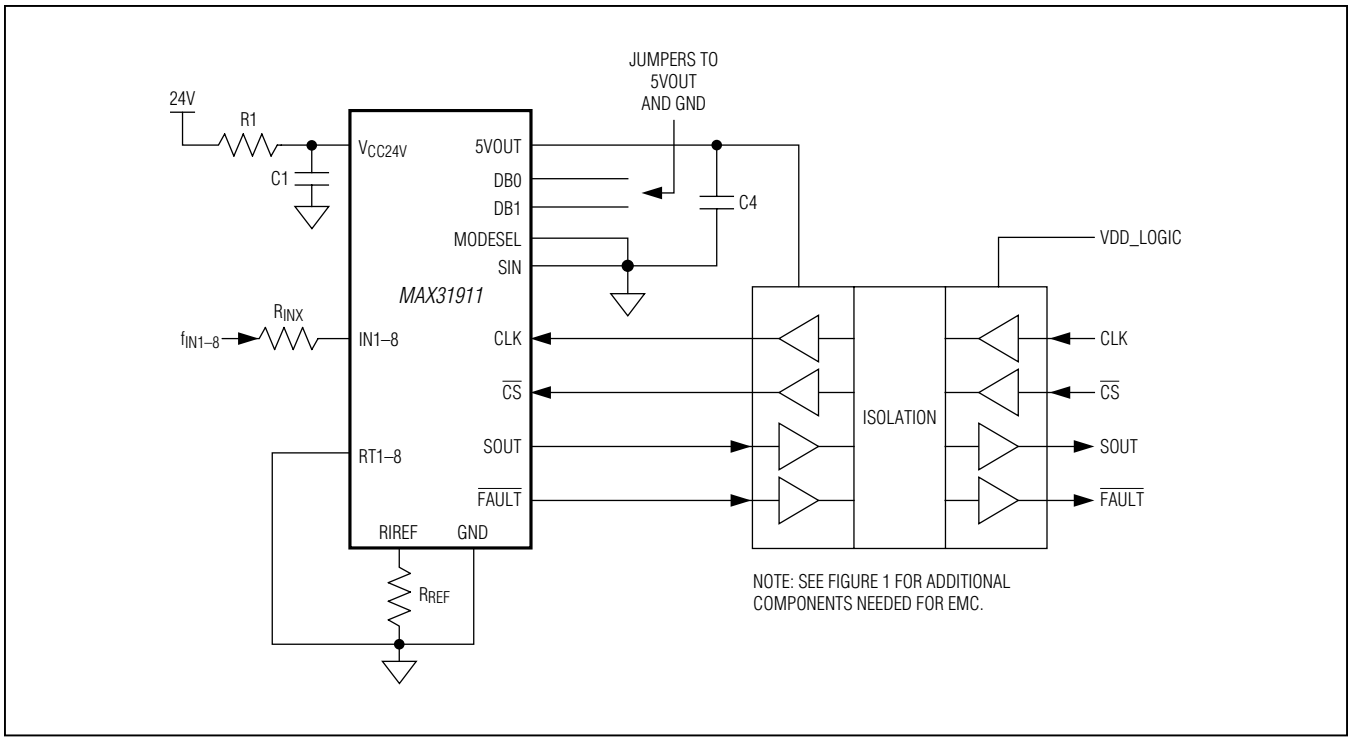
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 2	DB0, DB1	Debounce (Filtering) Time Select Inputs
3, 5, 7, 9, 11, 18, 20, 22	IN1–IN8	Field Inputs
4, 6, 8, 10, 12, 17, 19, 21	RT1–RT8	Connect directly to GND. These pins are reserved for energy-less LED drives in future versions of the device.
13	RIREF	Current-Limiter Reference Resistor
14	V_{CC24V}	Field-Supply Voltage
15	5VOUT	5V Regulator Output
16	$\overline{FAULT}$	Open-Drain Output. Active-low for overtemperature/undervoltage conditions.
23	SOUT	Serial-Data Out
24	$\overline{CS}$	Active-Low Chip-Select Input
25	CLK	Serial-Clock Input
26	MODESEL	Mode-Select Input MODESEL = 1: Selects 8-bit shift register MODESEL = 0: Selects 16-bit shift register
27	SIN	Serial-Data Input
28	GND	Field Ground
—	EP	Exposed Pad. Must be connected to the PCB ground plane.

Basic Application Circuit



Detailed Description

Input Current Clamp

The MAX31911 industrial interface serializer inputs (IN1–IN8) sense the state (on vs. off) of field sensors by monitoring both voltage and current flowing through the sensor output. The current sinking through these input pins rises linearly with input voltage until the limit set by the current clamp is reached. Any voltage increase beyond this point does not increase the input current any further.

The value of the current clamp is adjustable through an external resistor connected between the RIREF pin and GND. Pins RT1–RT8 must be connected directly to GND to provide a return path for the input current. The voltage and current at the IN1–IN8 input pins are compared against internally set references to determine whether the sensor is on (logic 1) or off (logic 0). The trip points determining the on/off status of the sensor satisfy the requirements of IEC 61131-2 Type 1 and 3 switches. The device can also be configured to work as a Type 2 switch.

Glitch Filter

A digital glitch filter provides debouncing and filtering of noisy sensor signals. The time constant of this filter is programmable from 0 to 3ms through the DB0 and DB1 pins. See Table 1 for debounce settings.

To provide the digital glitch filter, the device checks that an input is stable for at least three clock cycles. The duration of a clock cycle is 1/3 of the selected debounce time. If the input is not stable for at least three clock cycles, the input change is not sent to the internal shift register.

Reading Serial Data

The filtered outputs of the input comparators are latched into a shift register at the falling-edge of $\overline{CS}$. Clocking the CLK pin, while $\overline{CS}$ is held low, shifts the latched data out of SOUT 1 bit at a time.

The internal data serializer comprises a 16-bit shift register, containing 8 bits of data corresponding to the eight field inputs, as well as an 8-bit status byte containing supplementary status and CRC information. The status byte contains 1 bit representing the status of the field-supply voltage (UV), 1 bit representing the status of the internal temperature monitor (OT), a 5-bit CRC code internally calculated and generated, and a trailing 1 as a STOP bit.

The undervoltage (UV) bit is normally 0. If the supply voltage falls below $V_{OFFUVLO}$, the UV becomes a 1. The UV bit returns to 0 once the supply voltage has returned above V_{ONUVLO}.

The overtemperature (OT) bit is also normally 0. If the junction temperature increases to above T_{ALRM}, the OT bit becomes a 1. The bit returns to 0 once the junction temperature has returned below T_{ALRM}.

The CRC code can be used to check data integrity during transfer from the device to an external microcontroller. In applications where the integrity of data transferred is not of concern, the CRC bits can be ignored. The CRC uses the following polynomial:

$$P(x) = x^5 + x^4 + x^2 + x^0$$

The number of bits in the internal serializer can be selected between 8 bits or 16 bits. The MODESEL pin is used to configure the serializer as an 8-bit (disabling the status byte) or 16-bit shift register. In 8-bit mode, only the eight field input states are transferred through the SPI port and the status byte is ignored. Therefore, in multiple IC applications (input channels greater than 8), if desired, only a single status byte can be generated and transmitted for any number of input channels.

The shift register contents are read only (no write capability exists) through the SPI-compatible interface.

For higher input counts than 8, multiple devices can be cascaded. In this case, the SOUT pin of one device should be connected to the SIN pin of the next device, effectively cascading the internal shift registers. The CLK and $\overline{CS}$ pins of all the devices should be connected together in this configuration. See the *Serial-Port Operation* section for more detailed information on operating the SPI interface.

Temperature Monitoring

The internal junction temperature of the device is constantly monitored. An alarm is raised, by asserting the $\overline{FAULT}$ pin, if the temperature rises above T_{ALRM}. In addition to asserting $\overline{FAULT}$, the device sets the OT bit to a 1.

Supply Voltage Monitoring

A supply voltage monitor circuit constantly monitors the field-supply voltage. If this voltage falls below a threshold ($V_{OFFUVLO}$), an alarm is raised by asserting the $\overline{FAULT}$ pin, indicating that the part is experiencing a fault condition and the data in the serializer is not to be trusted. In addition, the device sets the UV bit to a 1. Once the field-supply voltage has recovered and goes above V_{ONUVLO}, the $\overline{FAULT}$ pin is released, indicating normal operation of the part.

Table 1. Debounce Settings

DB1	DB0	BINARY VALUE	DEBOUNCE TIME
0	0	0	0
0	1	1	25µs
1	0	2	0.75ms
1	1	3	3ms

Powering the Device through the 5VOUT pin

The device can alternatively be powered using a 5V supply connected to the 5VOUT pin. In this case a 24V supply is no longer needed and the VCC24V supply must be kept unconnected. (See Figure 1)

In this configuration, the device will always indicate a UVFAULT and the $\overline{FAULT}$ pin will always be active (pulled low). Faults due to the Supply Voltage monitoring will not be available. Faults due to the Temperature monitor can only be read through the SPI interface.

This configuration has lower power consumption and heat dissipation since the on-chip 5V voltage regulator is disabled.

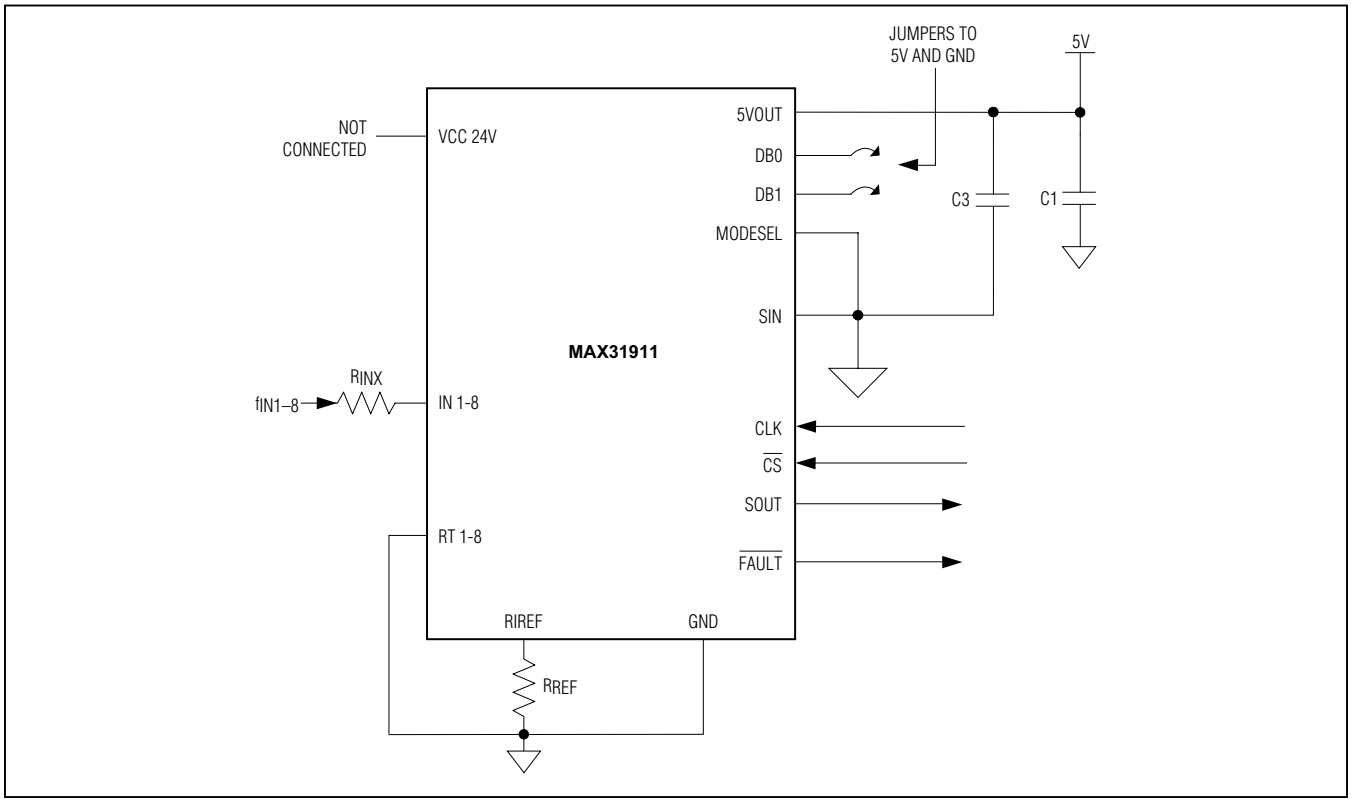


Figure 1. Basic Application Powered Through 5VOUT

Applications Information

EMC Standards Compliance

The external components shown in Figure 2 allow the device to operate in harsh industrial environments. Components were chosen to assist in suppression of voltage burst and surge transients, allowing the system to meet or exceed international EMC requirements. Table 2 lists an example device for each component in Figure 2. The system shown in Figure 2, using the components shown in Table 2, is designed to be robust against IEC Fast Transient Burst, surge, conducted RFI specifications, and ESD specifications (IEC 61000-4-4, -5, -6, and -2).

Table 2. Recommended Components

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED/OPTIONAL
C0	4.7nF, 2kV polypropylene capacitor	Recommended
C1	10µF, 60V ceramic capacitor	Required
C3	100nF, 10V ceramic capacitor	Recommended
C4	4.7µF, 10V low ESR ceramic capacitor	Required
C_{INX}	1nF, 60V ceramic capacitor	Optional: For higher EMC performance
D0	36V fast zener diode (ZSMB36)	Recommended
D1	General-purpose rectifier (IN4007)	Optional: For reverse polarity protection
R1	150Ω, 1/3W MELF resistor	Recommended
R_{INX}	2.2kΩ, 1/4W MELF resistor	Required
R_{REF}	15kΩ, 1/8W resistor	Required

Note: *For higher EFT performance, a minimum 1nF, 1000V capacitor can be added from nodes $f_{IN1–IN8}$ to earth or field ground. For additional methods to improve EFT robustness, please check the Maxim website regularly for upcoming application notes currently being developed.*

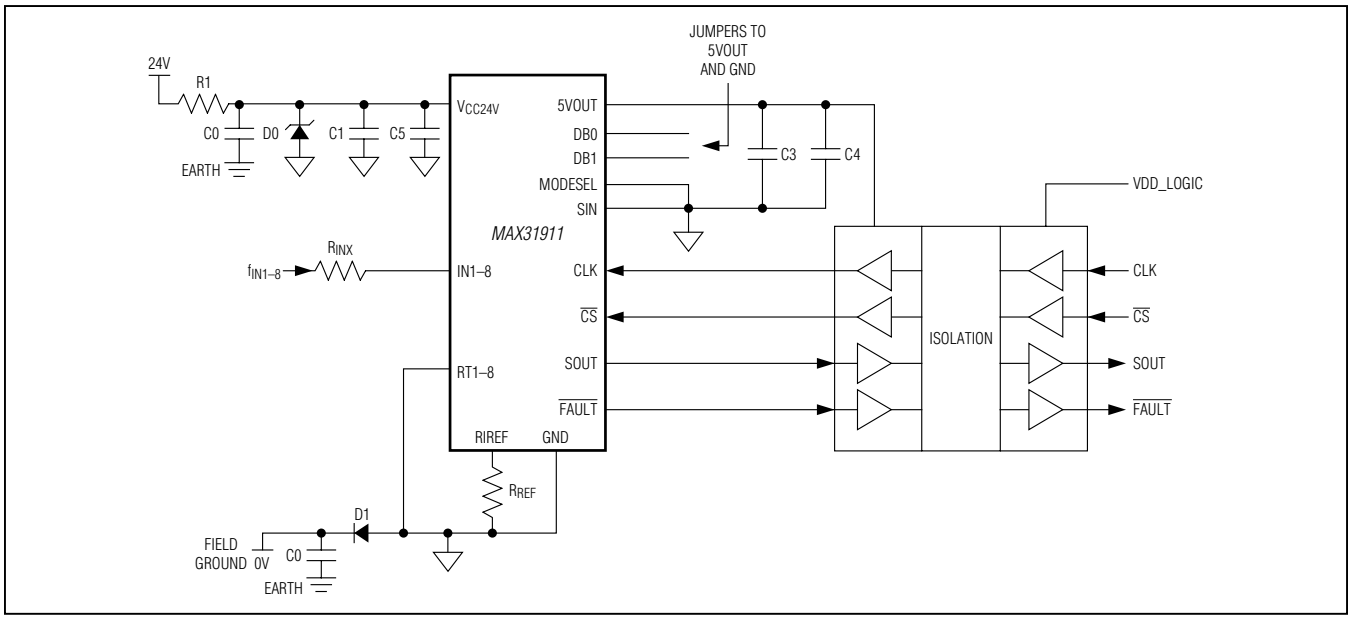


Figure 2. Typical EMC Protection Circuitry

Serial-Port Operation

Serial output of the device functions in one of two modes, depending on the MODESEL setting (Table 3). With MODESEL = 0, the device output includes a 5-bit CRC, an undervoltage alarm, and an overtemperature alarm. See the *Detailed Description* for CRC, undervoltage, and overtemperature functional descriptions. With MODESEL = 1, the device outputs only the state of the IN1–IN8 inputs and omits the CRC, undervoltage alarm, and overtemperature alarm.

Daisy-Chain Operation

For systems with more than eight sensor inputs, multiple devices can be daisy-chained to allow access to all data inputs through a single serial port. When using a daisy-chain configuration, connect SOUT of one of the devices to the SIN input of another upstream device. $\overline{CS}$ and SCK of all devices in the chain should be connected together in parallel (see Figure 3). In a daisy-chain configuration, external components used to enhance EMC robustness do not need to be duplicated for each device of a circuit board. Figure 4 illustrates a 16-input application.

SPI Waveforms

The serial output of the device adheres to the SPI protocol, running with CPHA = 0 and CPOL = 0. Input states on IN1–IN8 are latched in on the falling edge of $\overline{CS}$. The transfer of data out of the slave output, SOUT, starts immediately when $\overline{CS}$ is asserted (i.e., MSB is output onto SOUT independent of CLK). The remaining data bits are shifted out on the falling edge of CLK. The data bits are written to the output SOUT with MSB first. When $\overline{CS}$ is high, SOUT is high impedance. The resultant timing is shown in Figure 5. Note that all bits after IN1 are invalid if 8-bit operation mode is selected with the MODESEL input. Figure 6, Figure 7, Figure 8, and Figure 9 illustrate SPI timing specifications.

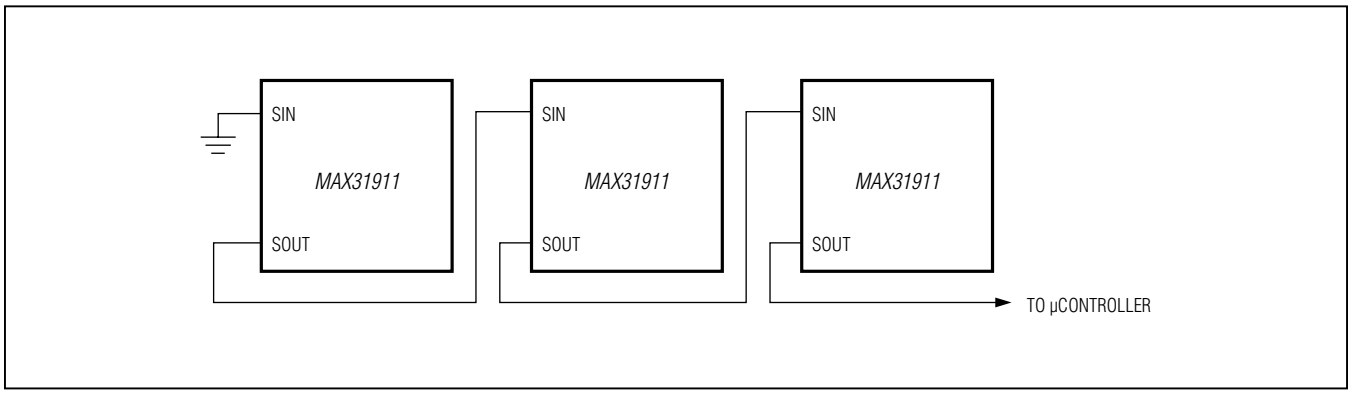


Figure 3. Daisy-Chain Operation

Table 3. MODESEL Settings

MODESEL SETTING	FUNCTIONALITY
0	16-bit output; [IN8–IN1][CRC (5 bit)][UV][OT][0]
1	8-bit output; [IN8–IN1]

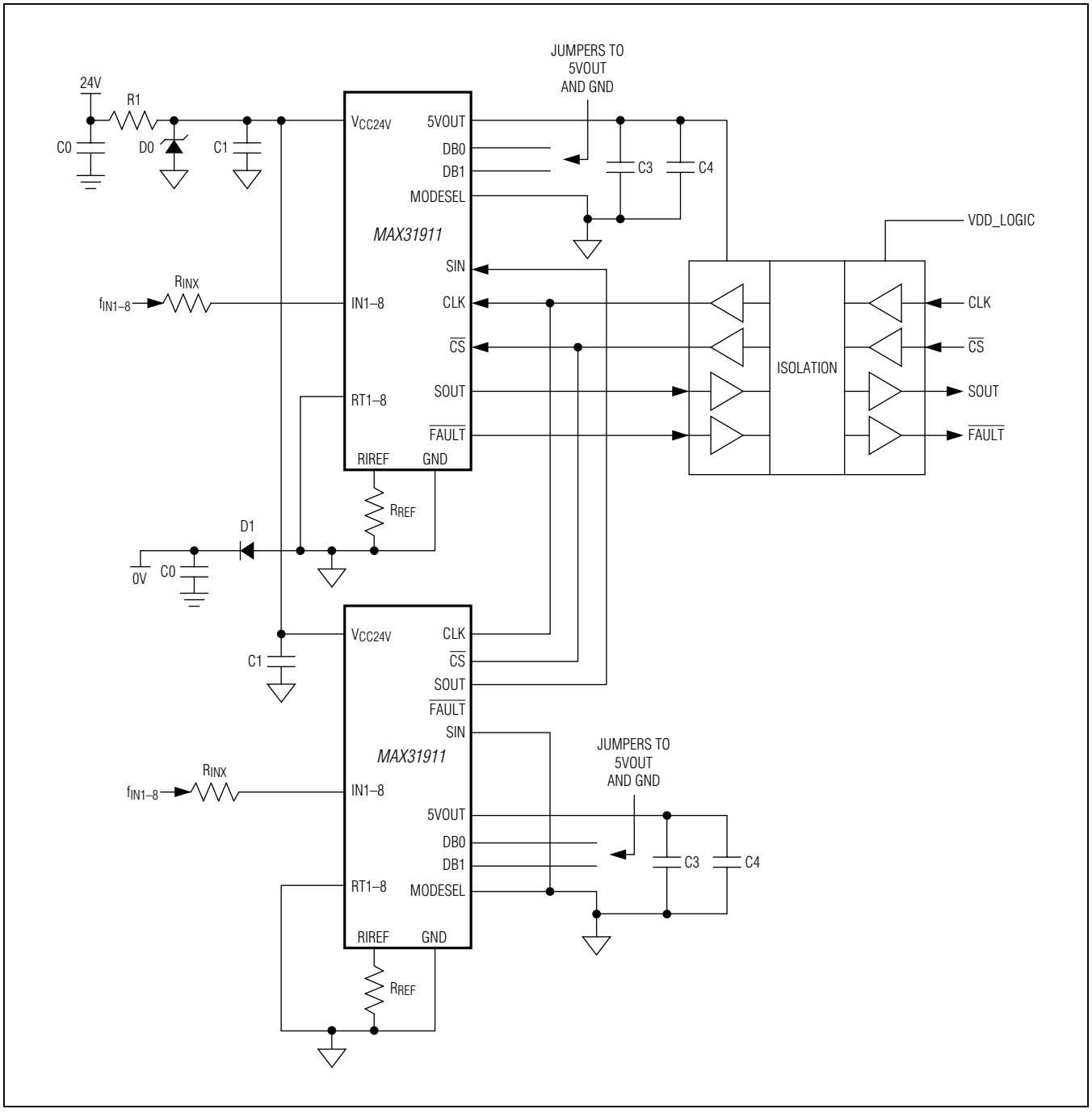


Figure 4. 16-Input Application Circuit

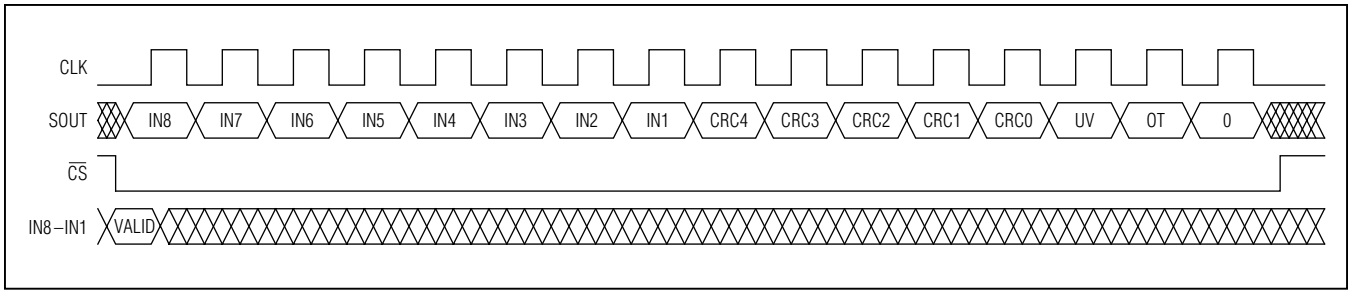


Figure 5. SPI Communication Example

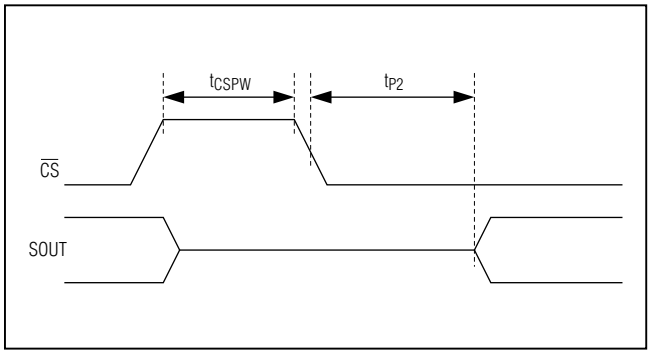


Figure 6. SPI Timing Diagram 1

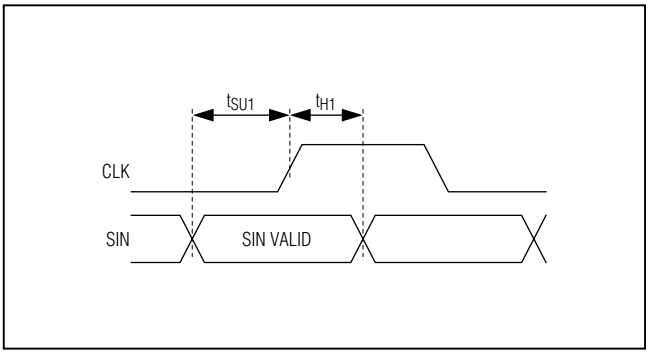


Figure 8. SPI Timing Diagram 3

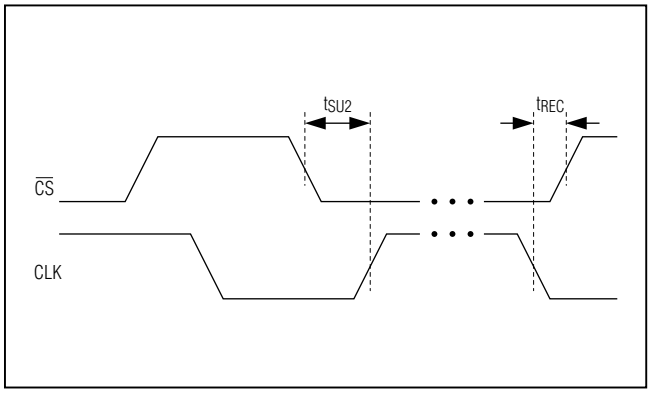


Figure 7. SPI Timing Diagram 2

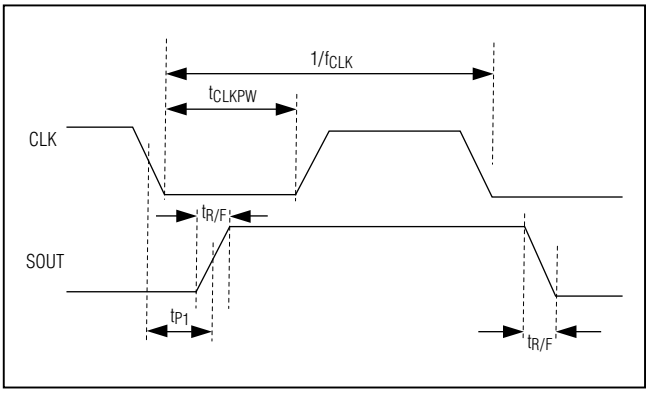


Figure 9. SPI Timing Diagram 4

Chip Information

PROCESS: S45JRS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	CARRIER
MAX31911AUI+	-40°C to +125°C	28 TSSOP	Bulk
MAX31911AUI+T	-40°C to +125°C	28 TSSOP	Tape and Reel

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TSSOP-EP	U28E+4		

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/12	Initial release	—
1	9/12	Changed the supply voltage minimum from 10V to 7V; changed the current limits in the EC table Note 5; added the CRC polynomial to the *Reading Serial Data* section	1–4, 9
2	10/13	Updated *Block Diagram*, TOCs 4, 5, 8, 9, 10, *Basic Application Circuit*, *Input Current Clamp* section, *EMC Standards Compliance* section, Table 2, Figure 1, Figure 3, and Figure 4	1, 5, 6, 8, 10, 12, 13
3	7/14	Deleted portion of Table 2 note	10
4	2/15	Updated page 1 content	1
5	3/15	Updated *Absolute Maximum Ratings*, *AC Electrical Characteristics*, and added *Powering the Device Through the 5VOUT Pin* section	1, 3, 5, 10-12, 14
6	4/15	Updated IEC diagram	13
7	8/17	Updated *Electrical Characteristics* and *Pin Description* tables, *Typical Operating Characteristics* section, and Table 3	5, 6, 8, 13, 15

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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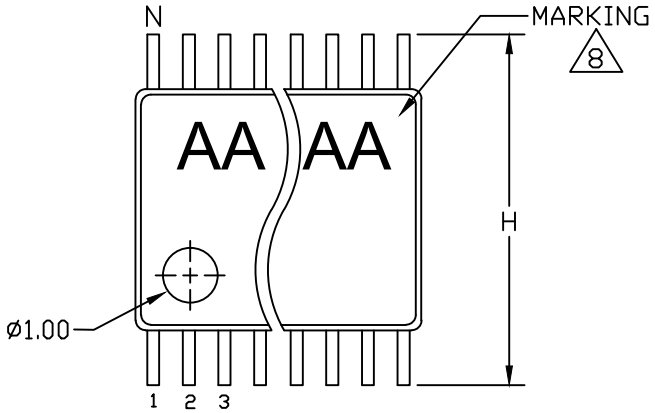
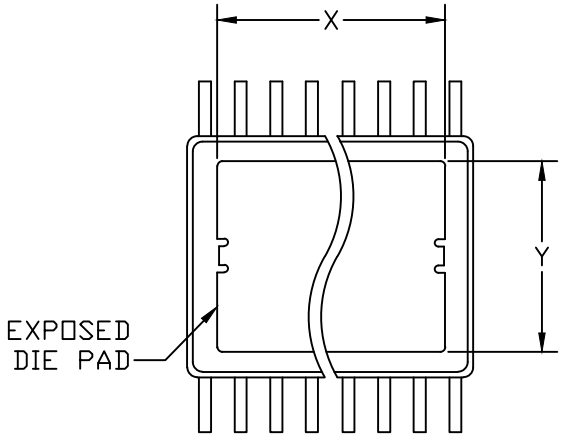
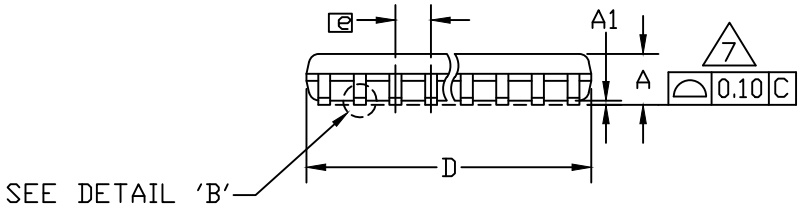


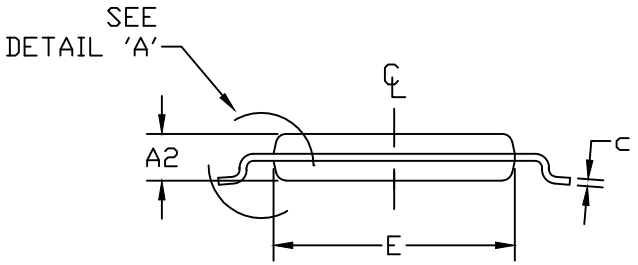
TOP VIEW



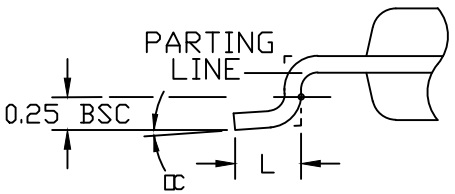
BOTTOM VIEW



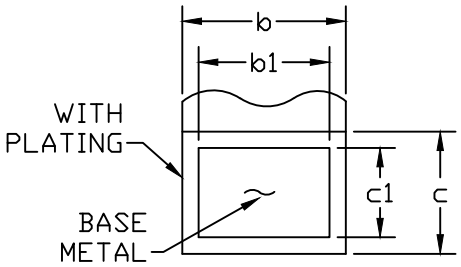
SIDE VIEW



END VIEW



DETAIL A



LEAD TIP DETAIL
DETAIL B

-DRAWING NOT TO SCALE-

maxim integrated™

TITLE:
PACKAGE OUTLINE,
TSSOP 4.4mm BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
KAI LIU	21-0108	Z	1/3

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.05	0.15	0.002	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
E	4.30	4.50	0.169	0.177
H	6.25	6.50	0.246	0.256
e	0.65 BSC		0.026 BSC	
α	0°	8°	0°	8°

JEDEC MO-153	N	Pkg.Code	VARIATIONS, MM							
			D		X		Y		L	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
ABT-1	14	U14E-3, U14E-3C	4.90	5.10	2.80	3.10	2.60	3.10	0.50	0.70
ABT	14	U14E-4, U14E-4C	4.90	5.10	2.59	2.95	2.49	2.84	0.45	0.75
ABT	16	U16E-3	4.90	5.10	2.60	3.10	2.60	3.10	0.50	0.70
ABT	16	U16E-3C	4.90	5.10	2.60	3.43	2.60	3.10	0.45	0.75
ABT	16	U16E-4	4.90	5.10	1.85	2.21	2.06	2.41	0.50	0.70
ABT	16	U16EN-7	4.90	5.10	2.59	2.79	2.11	2.31	0.50	0.70
ACT	20	U20E-1	6.40	6.60	3.80	4.20	2.60	3.10	0.50	0.70
ACT	20	U20E-4	6.40	6.60	4.50	4.90	2.60	3.10	0.50	0.70
ACT	20	U20E-6	6.40	6.60	3.68	4.20	2.49	3.10	0.50	0.70
ADT	24	U24E-1	7.70	7.90	4.44	4.64	2.64	2.84	0.50	0.70
AET	28	U28E-4	9.60	9.80	5.20	5.60	2.60	3.10	0.50	0.70
AET	28	U28E-5, U28E-5C, U28E-6C	9.60	9.80	6.50	6.90	2.60	3.10	0.50	0.70
AET	28	U28ME-1	9.60	9.80	6.50	6.90	2.60	3.10	0.50	0.70

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TITLE:
PACKAGE OUTLINE,
TSSOP 4.4mm BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
KAI LIU	21-0108	Z	2/3

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

maxim integrated™

TITLE:
PACKAGE OUTLINE,
TSSOP 4.4mm BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
KAI LIU	21-0108	Z	3/3