MOSFET – Dual N-Channel, POWERTRENCH®, SyncFET™

FDS6900AS

ON Semiconductor®

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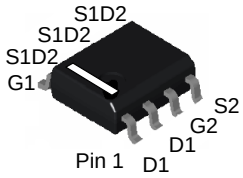


SOIC8
CASE 751EB

General Description

The FDS6900AS is designed to replace two single SO−8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6900AS contains two unique 30 V, N−channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency.

The high−side switch (Q1) is designed with specific emphasis on reducing switching losses while the lowside switch (Q2) is optimized to reduce conduction losses. Q2 also includes an integrated Schottky diode using ON Semiconductor's monolithic SyncFET technology.

Features

- **Q2**: Optimized to Minimize Conduction Losses Includes SyncFET Schottky Body Diode, 8.2 A, 30 V
  - $R_{DS(on)}$ = 22 mΩ at V_{GS} = 10 V
  - $R_{DS(on)}$ = 28 mΩ at V_{GS} = 4.5 V
- **Q1**: Optimized for Low Switching Losses Low Gate Charge (11 nC typical), 6.9 A, 30 V
  - $R_{DS(on)}$ = 27 mΩ at V_{GS} = 10 V
  - $R_{DS(on)}$ = 34 mΩ at V_{GS} = 4.5 V
- 100% R_G (Gate Resistance) Tested
- These Devices are Pb−Free and are RoHS Compliant

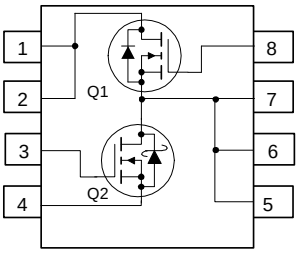
Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Q2	Q1	Units
V_{DSS}	Drain−Source Voltage	30	30	V
V_{GSS}	Gate−Source Voltage	±20	±20	V
I_D	Drain Current − Continuous (Note 1a) − Pulsed	 8.2 30	 6.9 20	A
P_D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	 1.6 1 0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150		°C

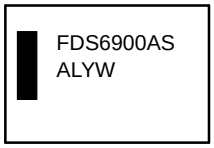
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CONNECTION



Dual N−Channel SyncFet

MARKING DIAGRAM



FDS6900AS = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
FDS6900AS	SOIC8 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	40	°C/W

Table 1. ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V I_D = 250 μA, V_{GS} = 0 V	Q2 Q1	30 30			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C I_D = 250 μA, referenced to 25°C	Q2 Q1		27 22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q2 Q1			500 1	μA
I_{GSS}	Gate−Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	Q2 Q1			±100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA V_{GS} = V_{DS}, I_D = 250 μA	Q2 Q1	1 1	1.9 1.9	3 3	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C I_D = 250 μA, referenced to 25°C	Q2 Q1		−3.2 −4.2		mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 8.2 A V_{GS} = 10 V, I_D = 8.2 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 7.6 A	Q2		17 23 21	22 36 28	mΩ
		V_{GS} = 10 V, I_D = 6.9 A V_{GS} = 10 V, I_D = 6.9 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 6.2 A	Q1		22 30 27	27 38 34	
$I_{D(on)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 8.2 A V_{DS} = 5 V, I_D = 6.9 A	Q2 Q1		25 21		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Q2 Q1		570 600		pF
C_{oss}	Output Capacitance		Q2 Q1		180 150		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		70 70		pF
R_G	Gate Resistance		Q2 Q1		2.8 2.2	4.9 3.8	Ω
SWITCHING CHARACTERISTICS (Note 2)							
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	Q2 Q1		10 9	19 18	ns
t_r	Turn−On Rise Time		Q2 Q1		5 4	10 8	ns
$t_{d(off)}$	Turn−Off Delay Time		Q2 Q1		26 23	42 32	ns
t_f	Turn−Off Fall Time		Q2 Q1		3 3	6 6	ns

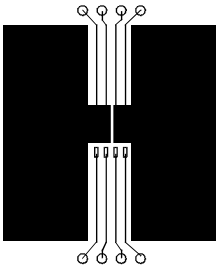
Table 1. ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	Q2 Q1		11 10	20 19	ns
t_r	Turn−On Rise Time		Q2 Q1		15 9	27 18	ns
$t_{d(off)}$	Turn−Off Delay Time		Q2 Q1		16 14	29 25	ns
t_f	Turn−Off Fall Time		Q2 Q1		6 4	12 8	ns
$Q_{g(TOT)}$	Total Gate Charge at V_{GS} = 10 V	Q2: V_{DS} = 15 V, I_D = 8.2 A Q1: V_{DS} = 15 V, I_D = 6.9 A	Q2 Q1		10 11	15 15	nC
Q_g	Total Gate Charge at V_{GS} = 5 V		Q2 Q1		5.8 6.1	8.2 8.5	nC
Q_{gs}	Gate−Source Charge		Q2 Q1		1.6 1.7		nC
Q_{gd}	Gate−Drain Charge		Q2 Q1		2.1 2.2		nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain−Source Diode Forward Current		Q2 Q1			2.3 1.3	A
T_{rr}	Reverse Recovery Time	I_F = 8.2 A, d_{iF}/d_t = 300 A/μs (Note 3)	Q2		15		ns
Q_{rr}	Reverse Recovery Charge				6		nC
T_{rr}	Reverse Recovery Time	I_F = 6.9 A, d_{iF}/d_t = 100 A/μs (Note 3)	Q1		19		ns
Q_{rr}	Reverse Recovery Charge				10		nC
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0V, I_S = 2.3 A (Note 2) V_{GS} = 0V, I_S = 5 A (Note 2) V_{GS} = 0V, I_S = 1.3 A (Note 2)	Q2 Q2 Q1		0.6 0.7 0.7	0.7 1.0 1.2	V

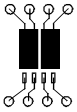
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

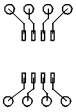
1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper.



b. 125°C/W when mounted on a 0.02 in^2 pad of 2 oz copper.



c. 135°C/W when mounted on a minimum pad

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. See "SyncFET Schottky body diode characteristics" below.

TYPICAL CHARACTERISTICS: Q2

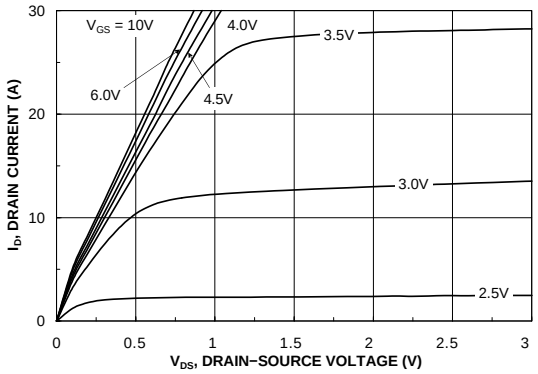


Figure 1. On−Region Characteristics

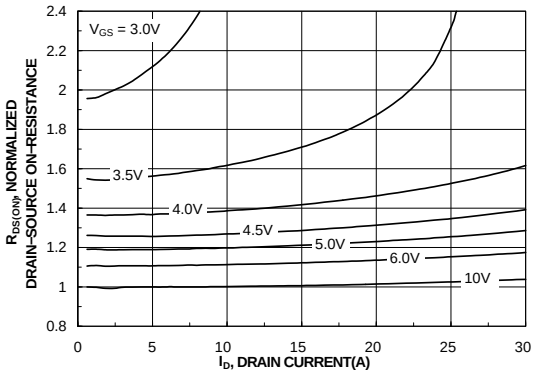


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

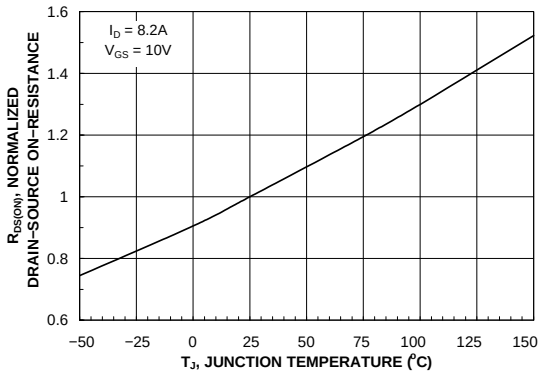


Figure 3. On−Resistance Variation with Temperature

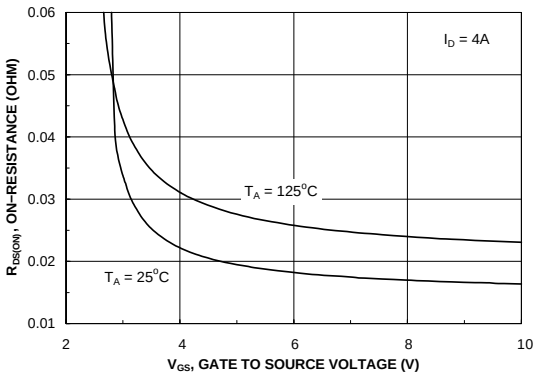


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

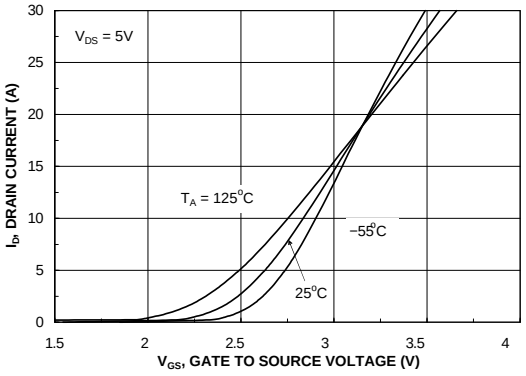


Figure 5. Transfer Characteristics

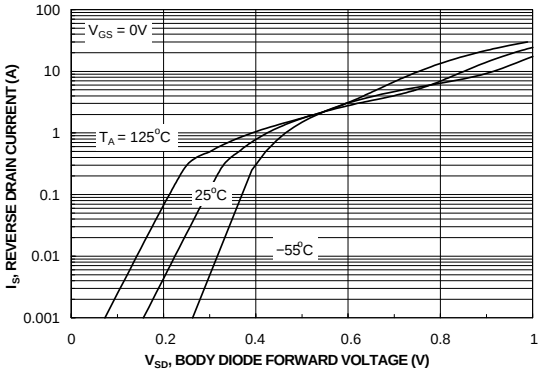


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: Q2 (Continued)

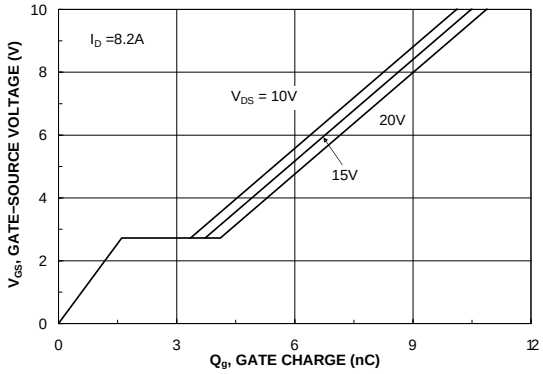


Figure 7. Gate Charge Characteristics

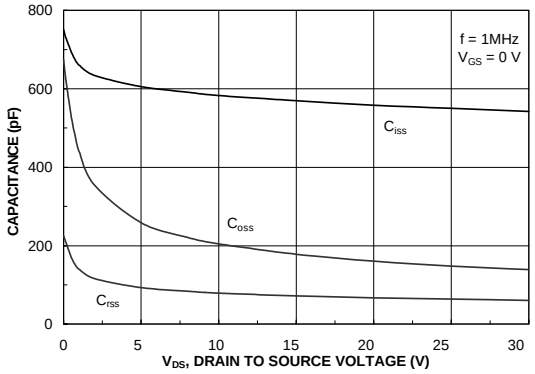


Figure 8. Capacitance Characteristics

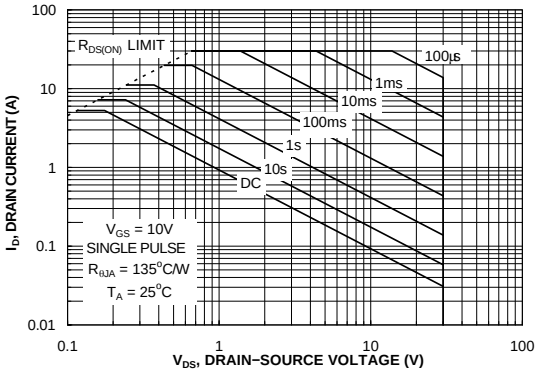


Figure 9. Maximum Safe Operating Area

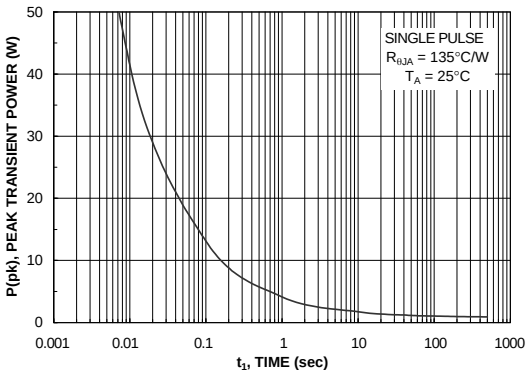


Figure 10. Single Pulse Maximum Power Dissipation

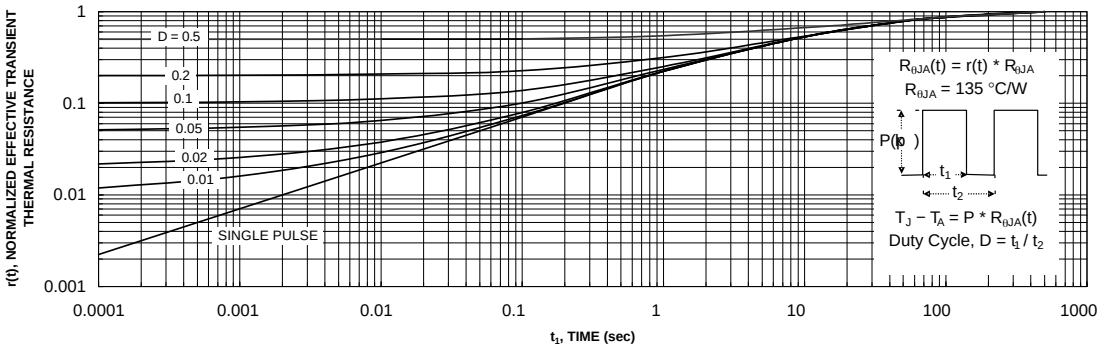


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

TYPICAL CHARACTERISTICS: Q1

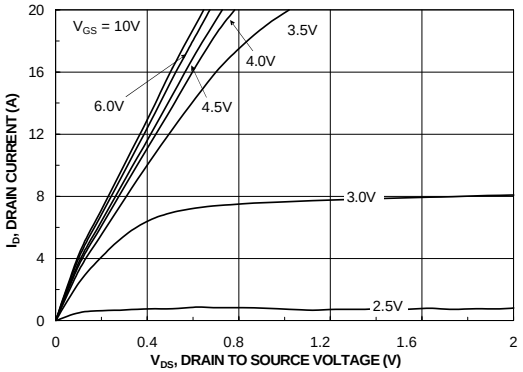


Figure 12. On−Region Characteristics

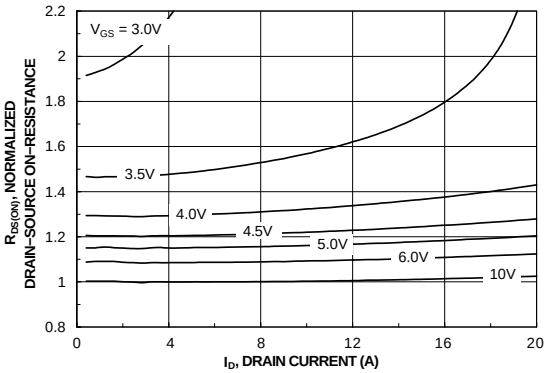


Figure 13. On−Resistance Variation with Drain Current and Gate Voltage

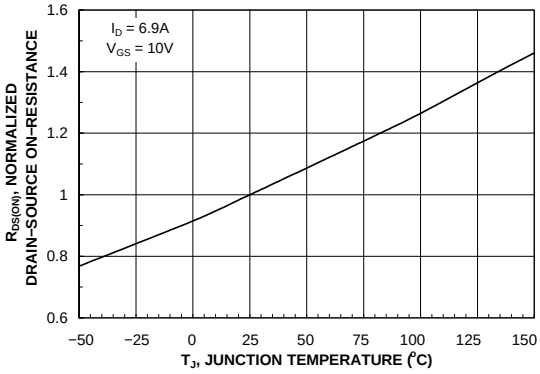


Figure 14. On−Resistance Variation with Temperature

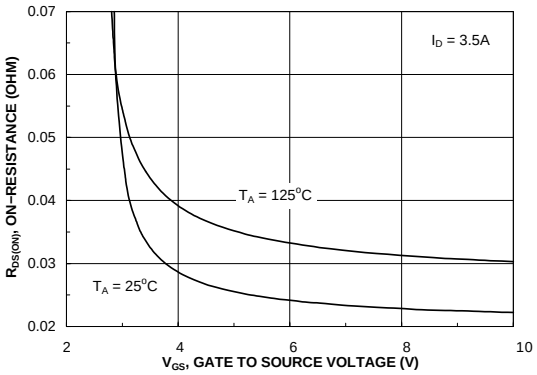


Figure 15. On−Resistance Variation with Gate−to−Source Voltage

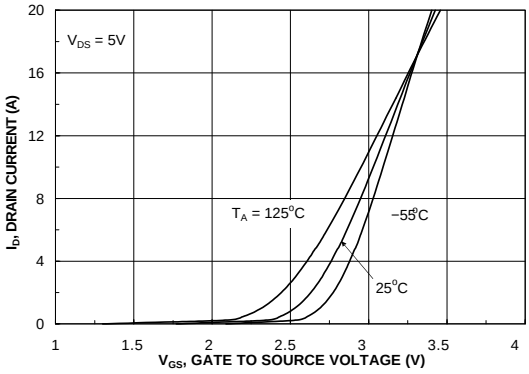


Figure 16. Transfer Characteristics

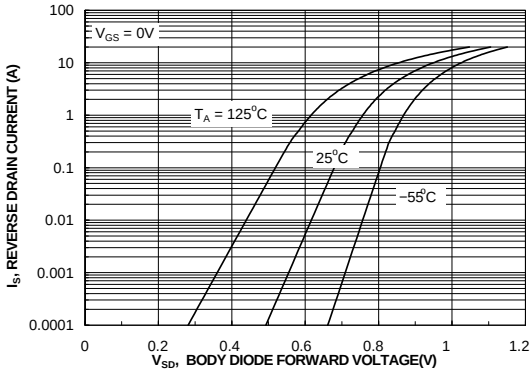


Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: Q1 (Continued)

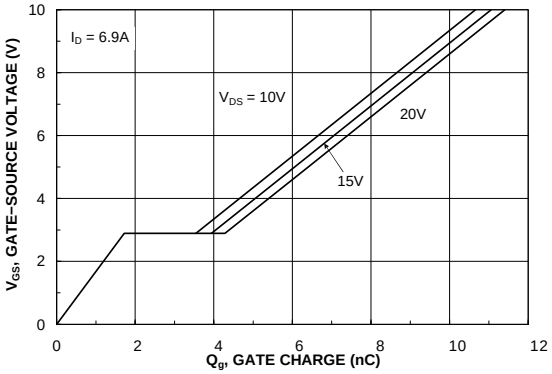


Figure 18. Gate Charge Characteristics

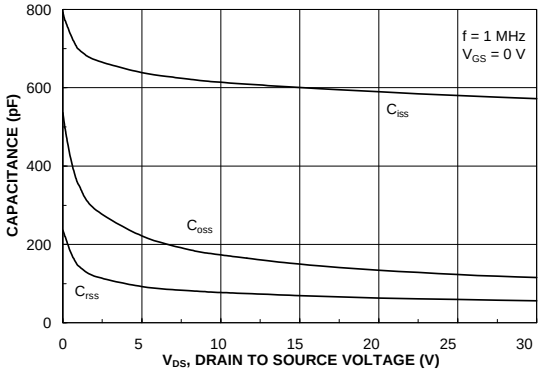


Figure 19. Capacitance Characteristics

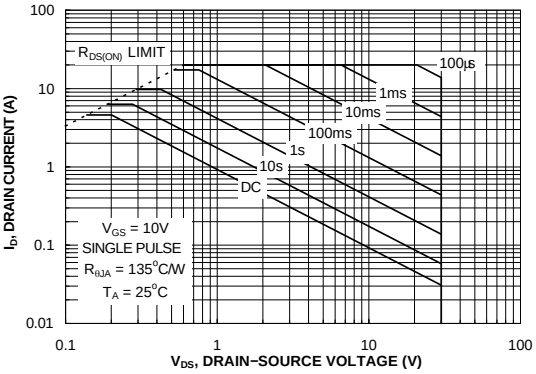


Figure 20. Maximum Safe Operating Area

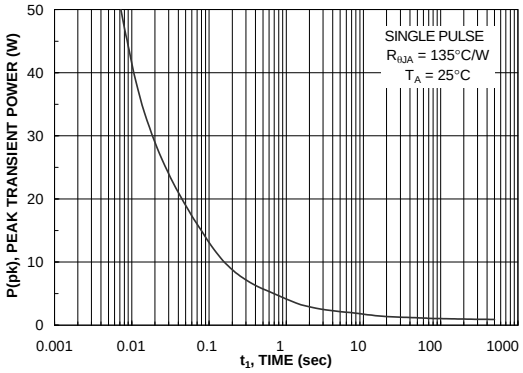


Figure 21. Single Pulse Maximum Power Dissipation

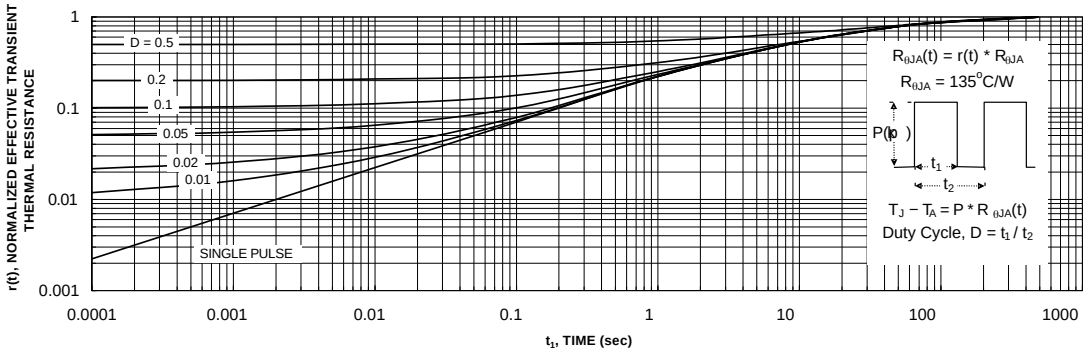


Figure 22. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

TYPICAL CHARACTERISTICS (Continued)

SyncFET Schottky Body Diode Characteristics

ON Semiconductor's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 23 shows the reverse recovery characteristic of the FDS6900AS.

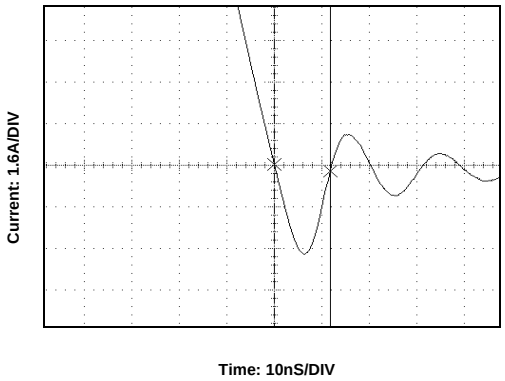


Figure 23. FDS6900AS SyncFET Body Diode Reverse Recovery Characteristics

For comparison purposes, Figure 24 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6690).

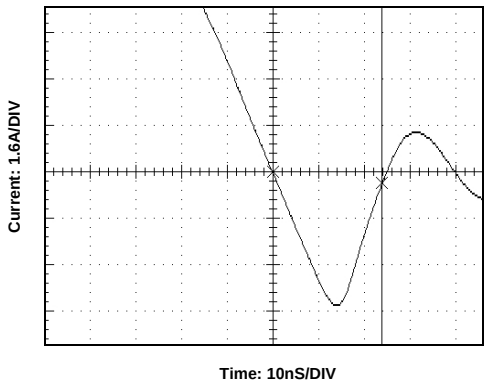


Figure 24. Non−SyncFET (FDS6690) Body Diode Reverse Recovery Characteristics

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

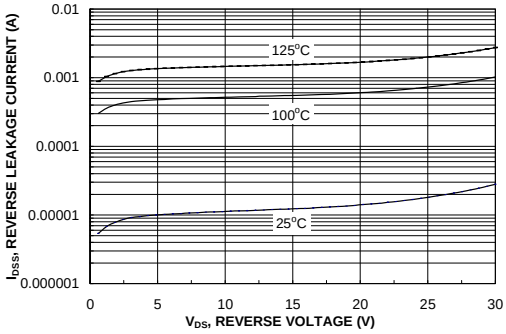


Figure 25. SyncFET Body Diode Reverse Leakage versus Drain−Source Voltage and Temperature

TYPICAL CHARACTERISTICS (Continued)

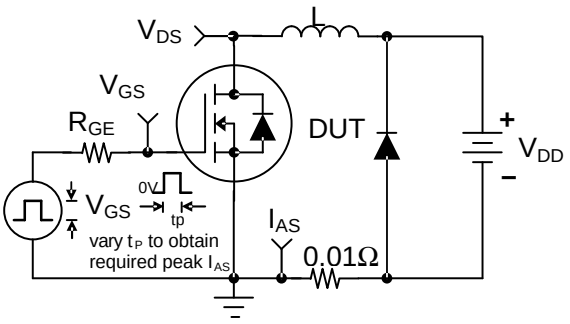


Figure 26. Unclamped Inductive Load Test Circuit

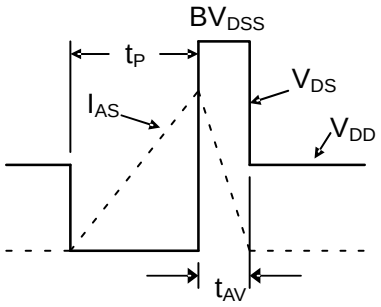


Figure 27. Unclamped Inductive Waveforms

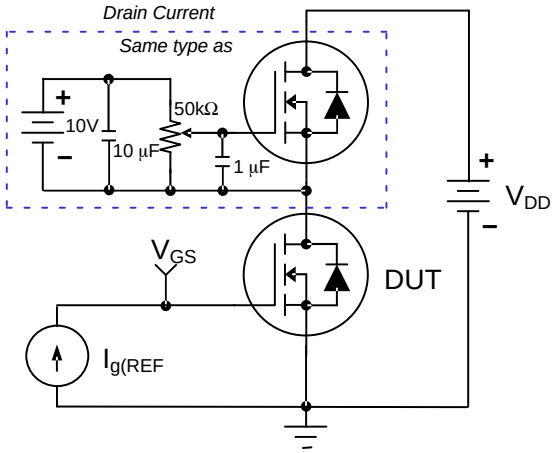


Figure 28. Gate Charge Test Circuit

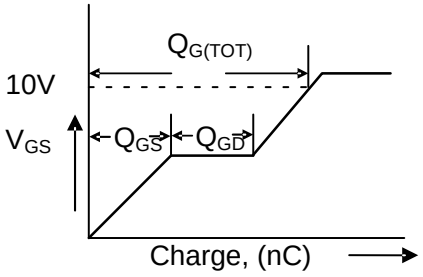


Figure 29. Gate Charge Waveform

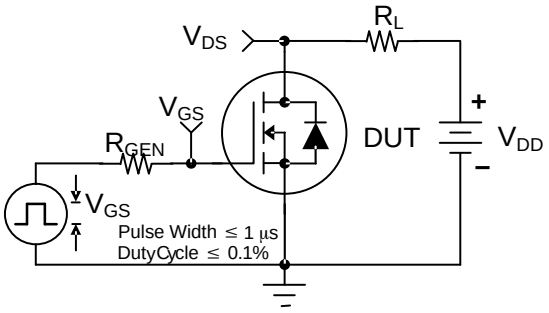


Figure 30. Switching Time Test Circuit

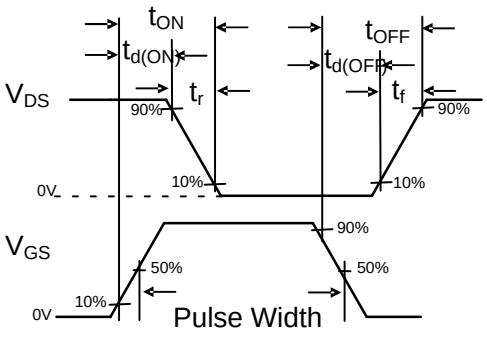


Figure 31. Switching Time Waveform

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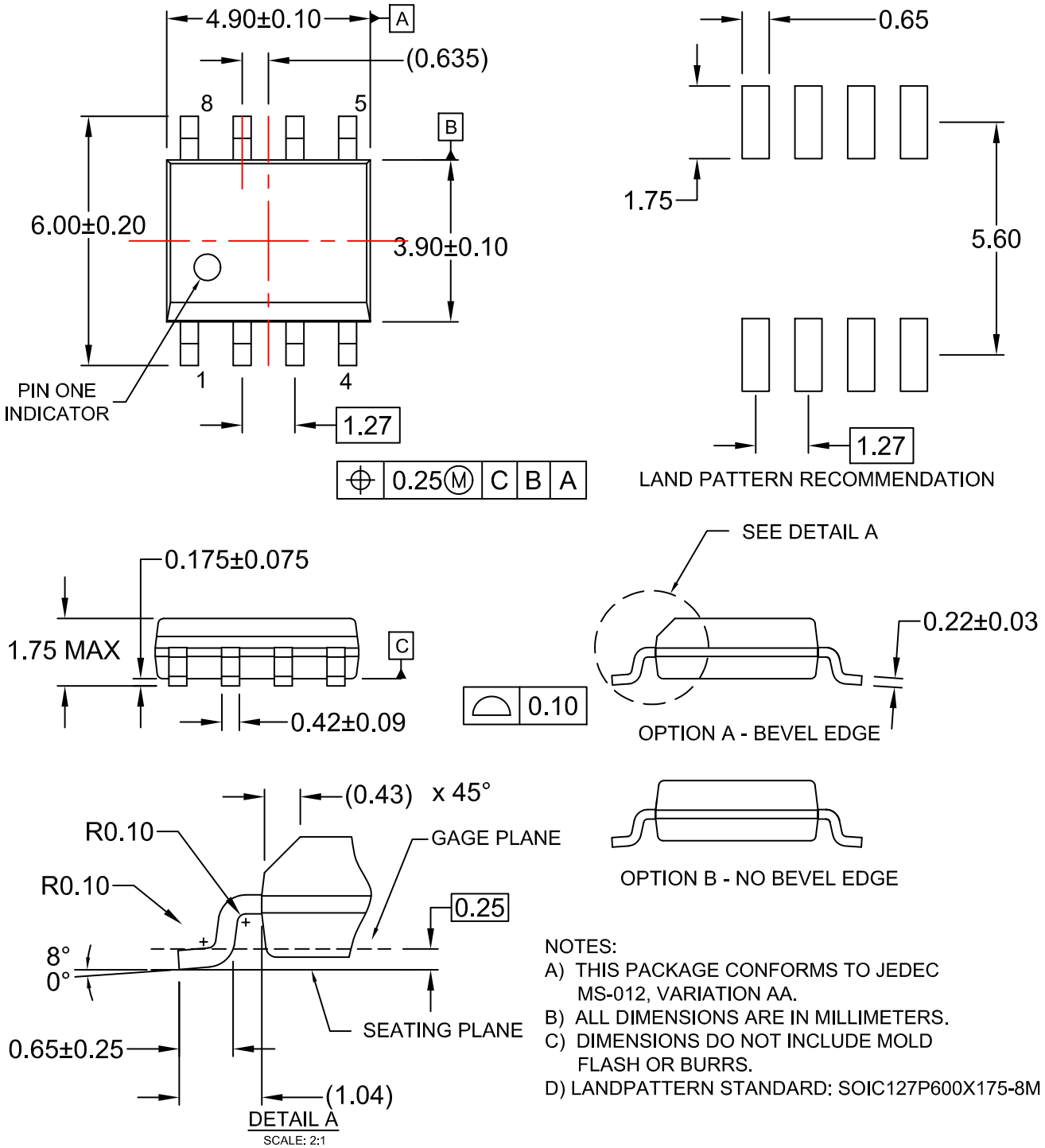

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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