

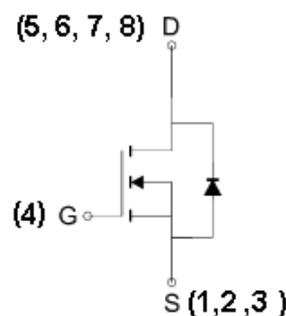
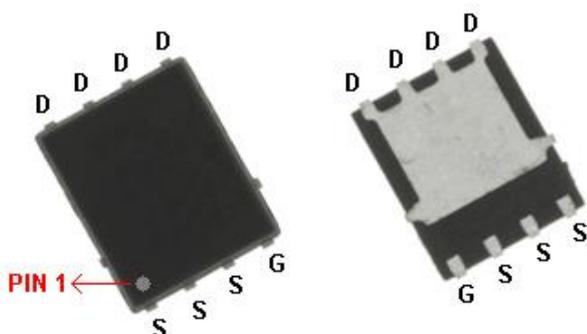
N-Channel 30V(D-S) Enhancement MOSFET

GENERAL DESCRIPTION

The ME7170-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

PowerDFN 5x6



N-Channel MOSFET

FEATURES

- $R_{DS(ON)} \leq 2.6m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 3.9m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- NB/MB Vcore Low side switching
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

Ordering Information: ME7170-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current*	T _A =25°C	I _D	110	A
	T _A =70°C		90	
Pulsed Drain Current		I _{DM}	450	A
Maximum Power Dissipation*	T _A =25°C	P _D	56	W
	T _A =70°C		36	
Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C
Thermal Resistance-Junction to Case*		R _{θJC}	2.2	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper



N-Channel 30V(D-S) Enhancement MOSFET
Electrical Characteristics ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1		2.2	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V$			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance ^a	$V_{GS}=10V, I_D=25A$		2.4	2.6	m Ω
		$V_{GS}=4.5V, I_D=19A$		3.3	3.9	
V_{SD}	Diode Forward Voltage	$I_S=25A, V_{GS}=0V$		0.8	1.2	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=15V, V_{GS}=10V, I_D=20A$		86		nC
Q_g	Total Gate Charge	$V_{DS}=15V, V_{GS}=4.5V, I_D=20A$		39		nC
Q_{gs}	Gate-Source Charge			19		
Q_{gd}	Gate-Drain Charge			12		
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, F=1MHz$		5406		pF
C_{oss}	Output Capacitance			487		
C_{rss}	Reverse Transfer Capacitance			418		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=15V, R_L=15\Omega$ $V_{GS}=10V, R_G=6\Omega$ $I_D=1A$		27		ns
t_r	Turn-On Rise Time			51		
$t_{d(off)}$	Turn-Off Delay Time			152		
t_f	Turn-Off Fall Time			54		

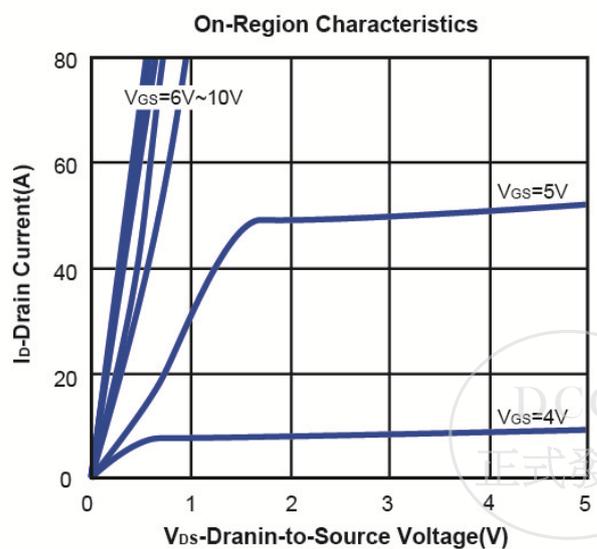
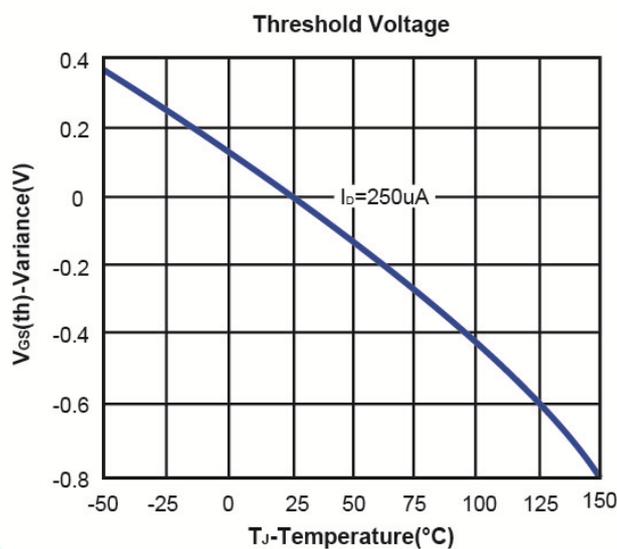
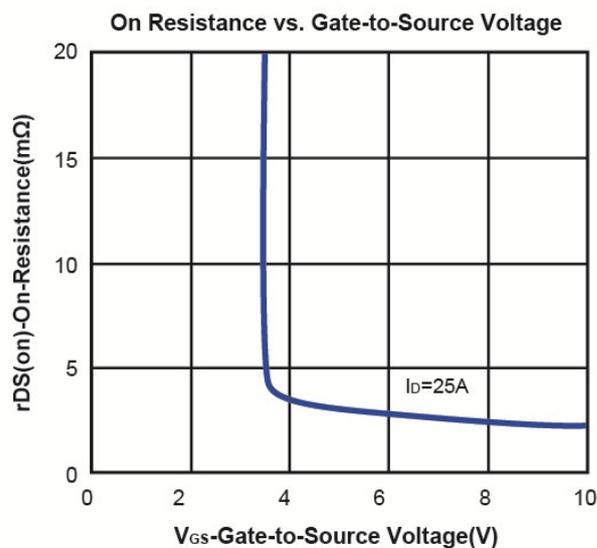
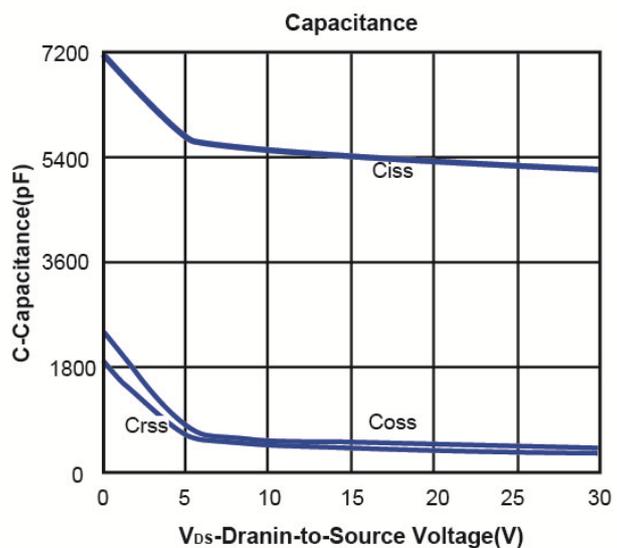
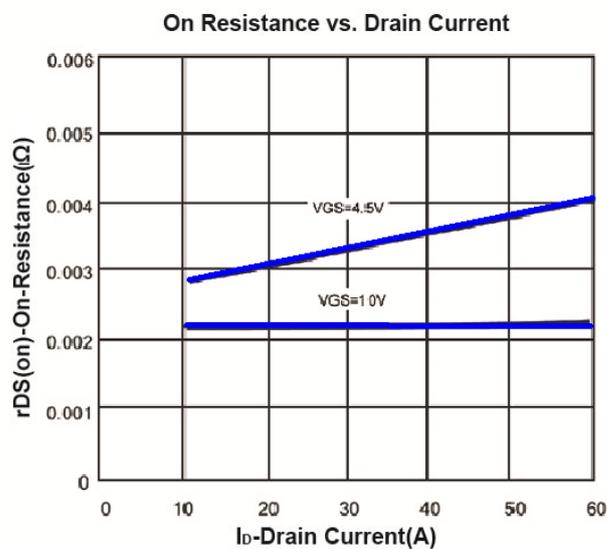
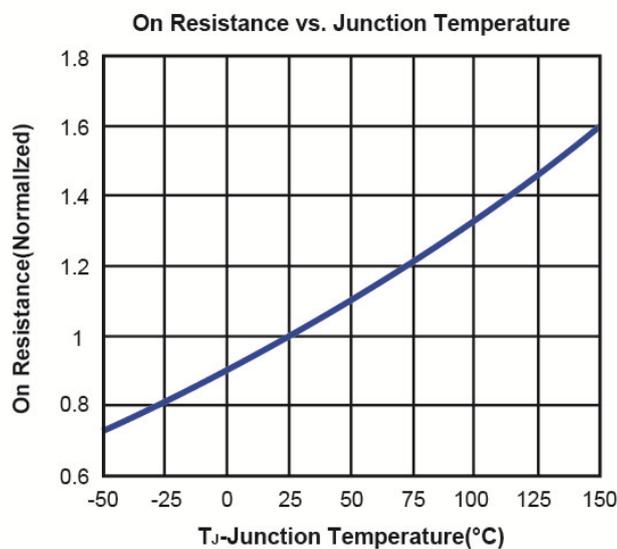
 Note: a. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



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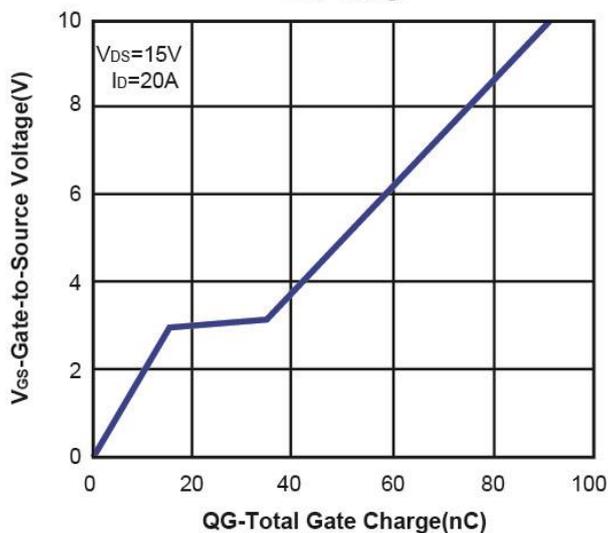
Typical Characteristics (T_J =25°C Noted)



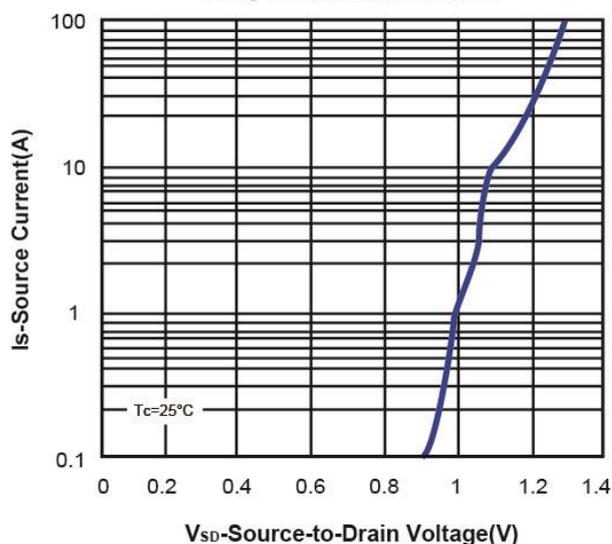
N-Channel 30V(D-S) Enhancement MOSFET

Typical Characteristics (T_J =25°C Noted)

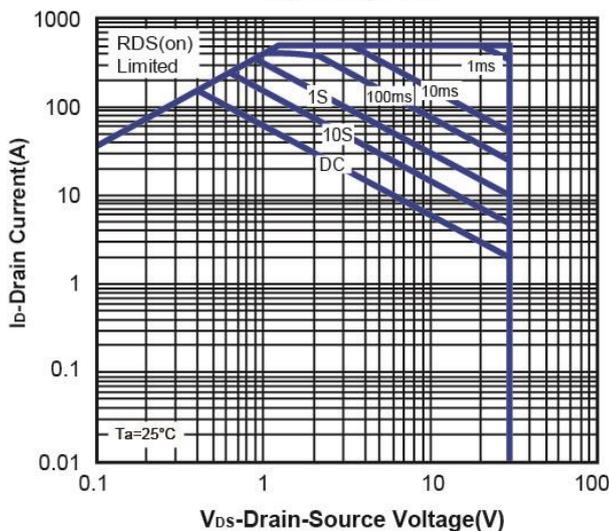
Gate Charge



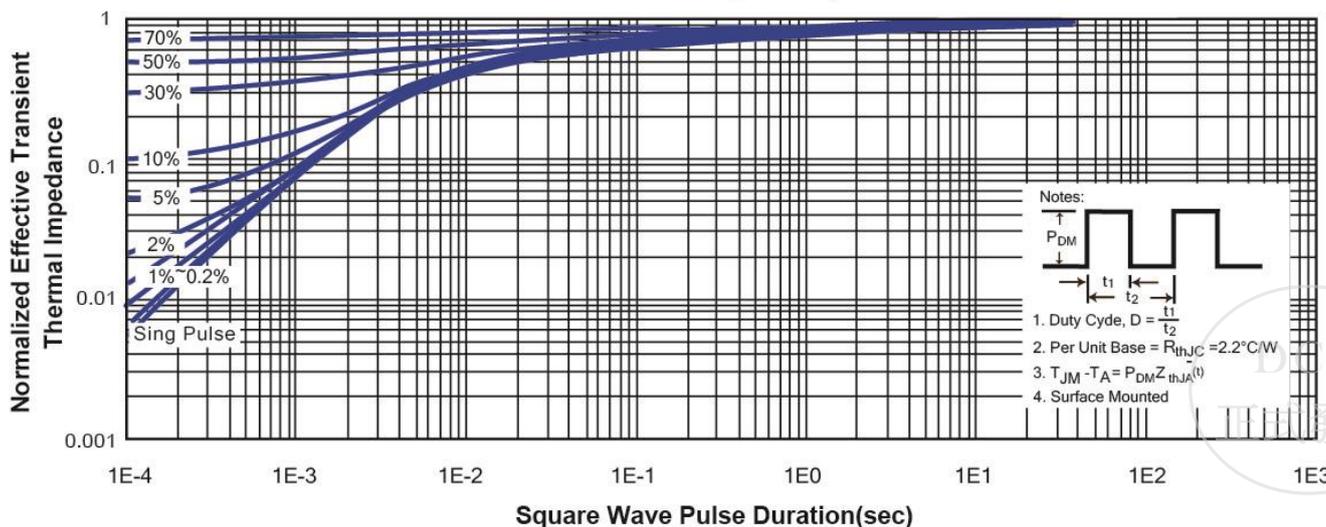
Body-diode characteristics



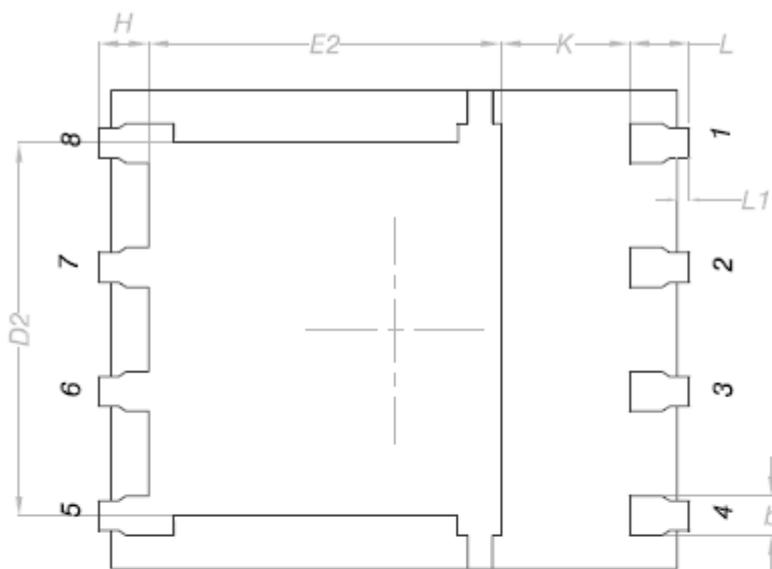
Maximum Forward Biased Safe Operating Area



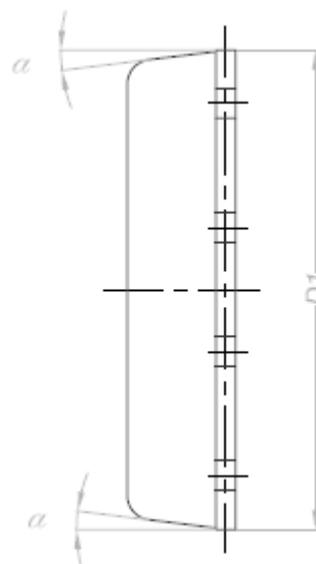
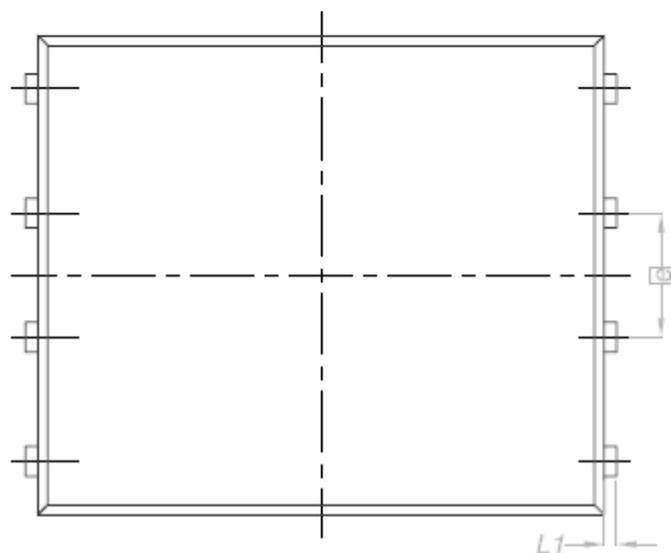
Normalized Thermal Transient Impedance, Junction-to-Ambient



PowerDFN 5x6 Package Outline



BACKSIDE VIEW



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°