

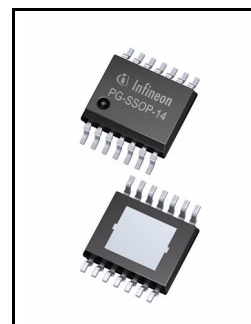
OPTIREG™ Linear TLS835D2ELVSE

Low Dropout Linear Voltage Regulator



Features

- Wide input voltage range from 3.0 V to 40 V
- Selectable output voltage 5 V or 3.3 V
- Output voltage precision $\leq \pm 2\%$
- Output current capability up to 350 mA
- Ultra low current consumption, typical 20 μA
- Very low dropout voltage, typical 100 mV, at output currents below 100 mA
- Stable with ceramic output capacitor of 1 μF
- Enable
- Reset
- Adjustable reset threshold down to 2 V
- Overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green Product (RoHS compliant)



Potential applications

- Automotive or other supply systems that are connected to the battery permanently
- Automotive supply systems that need to operate in cranking condition

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The OPTIREG™ Linear TLS835D2ELVSE is a linear voltage regulator with high performance, very low dropout linear voltage and very low quiescent current.

With an input voltage range of 3 V to 40 V and very low quiescent current of only 20 μA , this regulator is perfectly suitable for automotive or other supply systems permanently connected to the battery.

The new loop concept combines fast regulation and very high stability while requiring only one small ceramic capacitor of 1 μF at the output. At output currents below 100 mA the device has a very low dropout voltage of only 100 mV (for an output voltage of 5 V) and 120 mV (for an output voltage of 3.3 V). The operating range starts at an input voltage of only 3 V (extended operating range). This makes the TLS835D2ELVSE suitable for automotive systems that need to operate during cranking condition.

The device can be switched on and off by the enable feature.

The output voltage of the TLS835D2ELVSE can be selected between 5 V and 3.3 V by connecting the SEL pin to either V_Q or GND. When the SEL pin is connected to V_Q , the regulator's output is set to 5 V; when the SEL pin is connected to GND, the regulator's output is set to 3.3 V.

The output voltage is supervised by the reset feature, which includes an undervoltage reset, a delayed reset at power-on and an adjustable lower reset threshold.

Internal protection features such as output current limitation and overtemperature shutdown, protect the device from immediate damage caused by failures such as output shorted to GND, overcurrent or overtemperature conditions.

External components

An input capacitor C_I is recommended to compensate for line influences. The output capacitor C_O is necessary for the stability of the regulating circuit. The TLS835D2ELVSE is designed to be stable with low ESR ceramic capacitors.

Type	Package	Marking
TLS835D2ELVSE	PG-SSOP-14	835D2VSE

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Pin configuration

2 Pin configuration

2.1 Pin assignment TLS835D2ELVSE

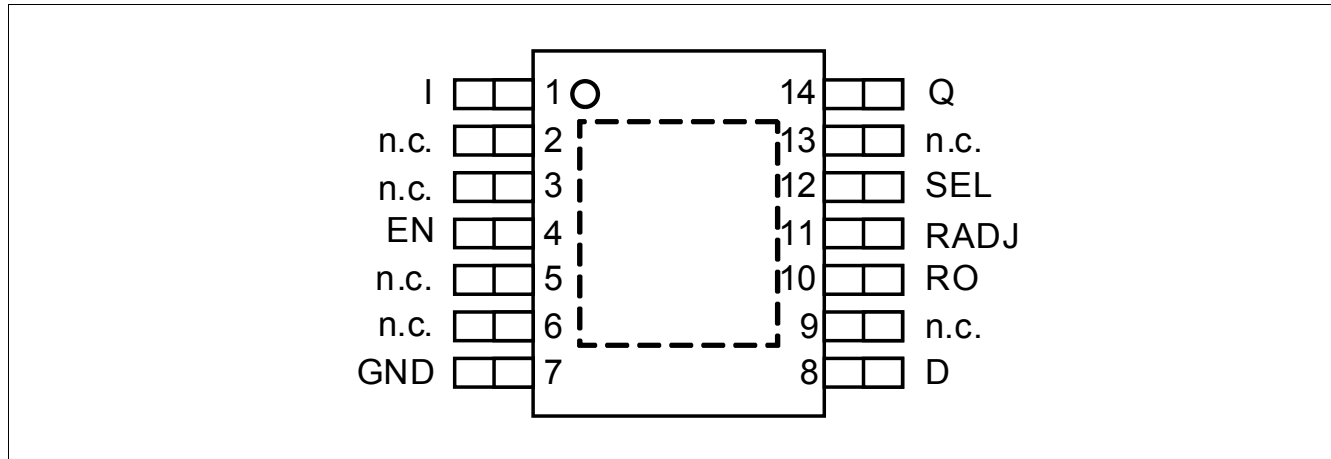


Figure 2 Pin configuration TLS835D2ELVSE

2.2 Pin definitions and functions TLS835D2ELVSE

Pin	Symbol	Function
1	I	Input It is recommended to place a small ceramic capacitor to GND, close to the pins, to compensate for line influences
2	n. c.	Not connected Leave open or connect to GND
3	n. c.	Not connected Leave open or connect to GND
4	EN	Enable (integrated pull-down resistor) Enable the IC with high level input signal Disable the IC with low level input signal
5	n. c.	Not connected Leave open or connect to GND
6	n. c.	Not connected Leave open or connect to GND
7	GND	Ground
8	D	Reset delay timing Connect a ceramic capacitor to GND for adjusting the reset delay time Leave open if the reset function is not needed
9	n. c.	Not connected Leave open or connect to GND
10	RO	Reset output (integrated pull-up resistor to Q) Open collector output Leave open if the reset function is not needed

Pin configuration

Pin	Symbol	Function
11	RADJ	Reset threshold adjustment Connect to GND to use standard value Connect an external voltage divider to adjust reset threshold
12	SEL	Output voltage selection Connect to Q to select 5 V output voltage Connect to GND to select 3.3 V output voltage
13	n. c.	Not connected Leave open or connect to GND
14	Q	Output voltage Connect output capacitor C_O to GND close to the pin, respecting the values specified for its capacitance and ESR in “Functional range” on Page 8
Pad	–	Exposed pad Connect to heatsink area; Connect to GND

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings¹⁾

$T_j = -40^{\circ}\text{C}$ to 150°C ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I, enable EN							
Voltage	V_I, V_{EN}	-0.3	–	45	V	–	P_4.1.1
Output Q, reset output RO							
Voltage	V_Q, V_{RO}	-0.3	–	7	V	–	P_4.1.2
Select SEL							
voltage	V_{SEL}	-0.3	–	7	V	–	P_4.1.3
Reset delay D, reset adjust RADJ							
Voltage	V_D, V_{RADJ}	-0.3	–	7	V	–	P_4.1.4
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.5
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.6
ESD absorption							
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	²⁾ HBM	P_4.1.7
ESD susceptibility to GND	V_{ESD}	-750	–	750	V	³⁾ CDM at all pins	P_4.1.8

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. Exceeding the absolute max ratings may cause permanent damage to the device and affects the device's reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as operation outside the normal operating range. Protection functions are not designed for continuous repetitive operation.

General product characteristics

3.2 Functional range

Table 2 Functional range

$T_j = -40^\circ\text{C}$ to 150°C ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	$V_{Q,nom} + V_{dr}$	–	40	V	¹⁾ –	P_4.2.1
Extended input voltage range	$V_{I,ext}$	3.0	–	40	V	²⁾ –	P_4.2.2
Enable voltage range	V_{EN}	0	–	40	V	–	P_4.2.3
Capacitance of output capacitor for stability	C_Q	1	–	–	μF	³⁾⁴⁾ –	P_4.2.4
Equivalent series resistance of output capacitor	$ESR(C_Q)$	–	–	50	Ω	³⁾ –	P_4.2.5
Junction temperature	T_j	-40	–	150	$^\circ\text{C}$	–	P_4.2.6

1) Output current is limited internally and depends on the input voltage, see electrical characteristics for more details.

2) If $V_{I,ext,min} \leq V_I \leq V_{Q,nom} + V_{dr}$, then $V_Q = V_I - V_{dr}$. If $V_I < V_{I,ext,min}$, then V_Q can drop to 0 V.

3) Not subject to production test, specified by design.

4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

General product characteristics

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 3 Thermal resistance of TLS835D2ELVSE in PG-SSOP-14 package

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	10	–	K/W	¹⁾ –	P_4.3.1
Junction to ambient	R_{thJA}	–	41	–	K/W	¹⁾²⁾ 2s2p board	P_4.3.2
Junction to ambient	R_{thJA}	–	125	–	K/W	¹⁾³⁾ 1s0p board, footprint only	P_4.3.3
Junction to ambient	R_{thJA}	–	59	–	K/W	¹⁾³⁾ 1s0p board, 300 mm ² heatsink area on PCB	P_4.3.4
Junction to ambient	R_{thJA}	–	51	–	K/W	¹⁾³⁾ 1s0p board, 600 mm ² heatsink area on PCB	P_4.3.5

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board. The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 μm Cu).

4 Block description and electrical characteristics

4.1 Voltage regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

The control loop stability depends on the following factors:

- output capacitor C_Q
- load current
- chip temperature
- internal circuit design

Output capacitor

To ensure stable operation, the capacitance of the output capacitor and its equivalent series resistor (ESR) requirements as specified in **“Functional range” on Page 8** must be maintained. The output capacitor must be sized according to the requirements of the application to be able to buffer load steps.

Input capacitors, reverse polarity protection diode

An input capacitor C_I is recommended to compensate for line influences.

In order to block influences such as pulses and high frequency distortion at the input, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

Smooth ramp-up

In order to prevent overshoots during startup, a smooth ramp-up function is implemented. This ensures almost no output voltage overshoots during startup, mostly independent from load and output capacitance.

Output current limitation

If the load current exceeds the specified limit, due to a short-circuit for example, then the output current is limited and the output voltage decreases.

Overtemperature shutdown

The overtemperature shutdown circuit prevents the IC from immediate destruction in case of a fault condition (for example a permanent short-circuit at the output) by switching off the power stage. After the IC has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the lifetime of the IC.

The diagram illustrates the internal architecture of a voltage regulator IC. Key components and connections include:

- Input Stage:** The input terminal **I** is connected to the **Supply** and has a bypass capacitor C_{I1} . The input current is I_I . A second bypass capacitor C_{I2} is connected to the input line before the IC pin.
- Internal Functional Blocks:**
 - Enable:** Controls the **EN** pin.
 - Current Limitation:** Monitors the input current.
 - Temperature Shutdown:** Monitors the junction temperature.
 - Bandgap Reference:** Provides a stable reference voltage.
 - Reset:** Controls the **SEL** and **RO** pins.
- Output Stage:** The output terminal **Q** provides the **Regulated Output Voltage** with current I_Q . It includes a sense resistor R_1 and a feedback resistor R_2 connected to the **RADJ** pin. The output is filtered by capacitor C_Q (with ESR) and drives a load R_{LOAD} . The output voltage is V_Q .
- Other Pins:** The **D** pin is connected to **GND**. The **SEL** and **RO** pins are connected to the **Reset** block.

Block description and electrical characteristics

Table 4 Electrical characteristics voltage regulator

$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5\text{ V}$, all voltages with respect to ground (unless otherwise specified)

Typical values are given at $T_j = 25^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
5 V output voltage							
Output voltage accuracy	V_Q	4.9	5.0	5.1	V	0.05 mA ≤ I_Q ≤ 350 mA 5.8 V ≤ V_I ≤ 28 V SEL connected to Q	P_5.1.1
Output voltage accuracy	V_Q	4.9	5.0	5.1	V	0.05 mA ≤ I_Q ≤ 175 mA 5.45 V ≤ V_I ≤ 40 V SEL connected to Q	P_5.1.2
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	250	500	mV	¹⁾ I_Q = 250 mA, SEL connected to Q	P_5.1.7
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	100	200	mV	¹⁾ I_Q = 100 mA, SEL connected to Q	P_5.1.9
Power supply ripple rejection	$PSRR$	–	60	–	dB	²⁾ f_{ripple} = 100 Hz V_{ripple} = 0.5 V_{pp} I_Q = 10 mA SEL connected to Q	P_5.1.10

3.3 V output voltage

Output voltage accuracy	V_Q	3.23	3.3	3.37	V	$0.05\text{ mA} \leq I_Q \leq 350\text{ mA}$ $4.21\text{ V} \leq V_I \leq 28\text{ V}$ SEL connected to GND	P_5.1.12
Output voltage accuracy	V_Q	3.23	3.3	3.37	V	$0.05\text{ mA} \leq I_Q \leq 175\text{ mA}$ $3.79\text{ V} \leq V_I \leq 40\text{ V}$ SEL connected to GND	P_5.1.13
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	300	600	mV	¹⁾ $I_Q = 250\text{ mA}$, SEL connected to GND	P_5.1.18
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	120	240	mV	¹⁾ $I_Q = 100\text{ mA}$, SEL connected to GND	P_5.1.20
Power supply ripple rejection	$PSRR$	–	63	–	dB	²⁾ $f_{\text{ripple}} = 100\text{ Hz}$ $V_{\text{ripple}} = 0.5 V_{pp}$ $I_Q = 10\text{ mA}$ SEL connected to GND	P_5.1.21

Other electrical characteristics

Output current limitation	$I_{Q,max}$	351	500	780	mA	$0\text{ V} < V_Q < V_{Q,nom} - 0.1\text{ V}$	P_5.1.24
Load regulation steady-state	$\Delta V_{Q,load}$	-15	-5	–	mV	$I_Q = 0.05\text{ mA}$ to 350 mA $V_I = 6.5\text{ V}$	P_5.1.29
Line regulation steady-state	$\Delta V_{Q,line}$	–	1	10	mV	$V_I = 8\text{ V}$ to 32 V $I_Q = 5\text{ mA}$	P_5.1.30

Block description and electrical characteristics

Table 4 Electrical characteristics voltage regulator (cont'd)

$T_j = -40^{\circ}\text{C}$ to 150°C , $V_I = 13.5\text{ V}$, all voltages with respect to ground (unless otherwise specified)
 Typical values are given at $T_j = 25^{\circ}\text{C}$

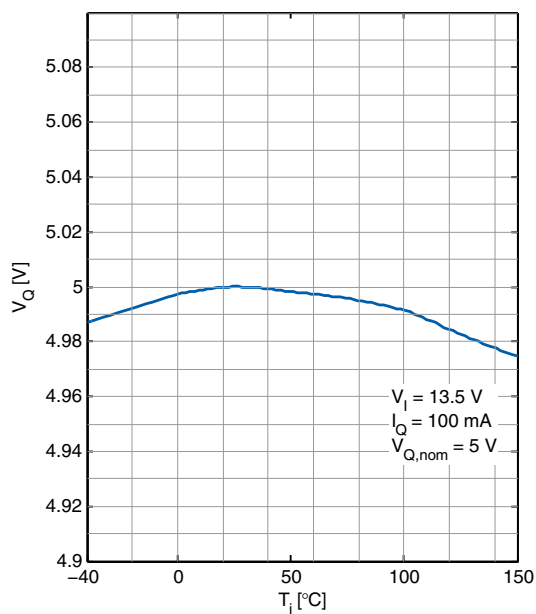
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overtemperature shutdown threshold	$T_{j,sd}$	151	175	200	$^{\circ}\text{C}$	²⁾ T_j increasing	P_5.1.31
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	²⁾ T_j decreasing	P_5.1.32

1) Measured when the output voltage V_O has dropped by 100 mV while input voltage was gradually decreased.

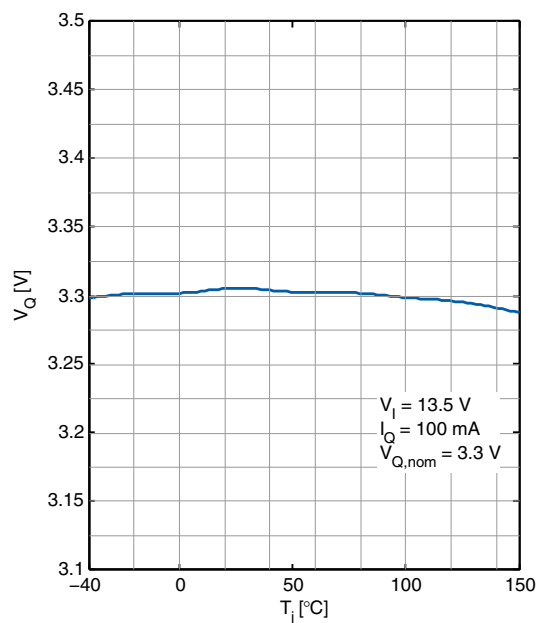
2) Not subject to production test, specified by design

4.2 Typical performance characteristics voltage regulator

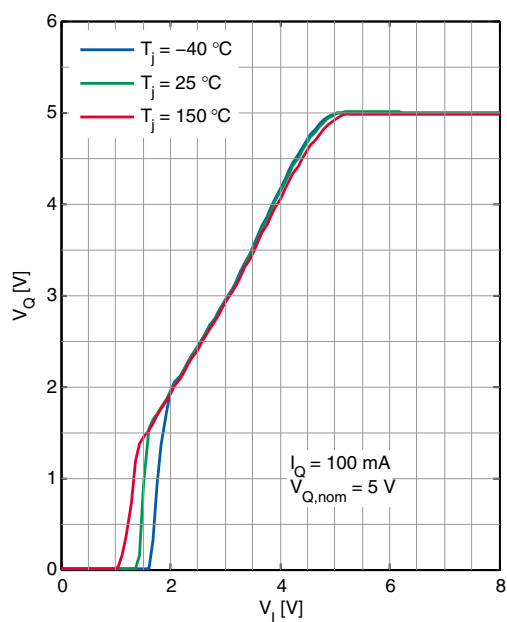
**Output voltage V_Q versus
junction temperature T_j**



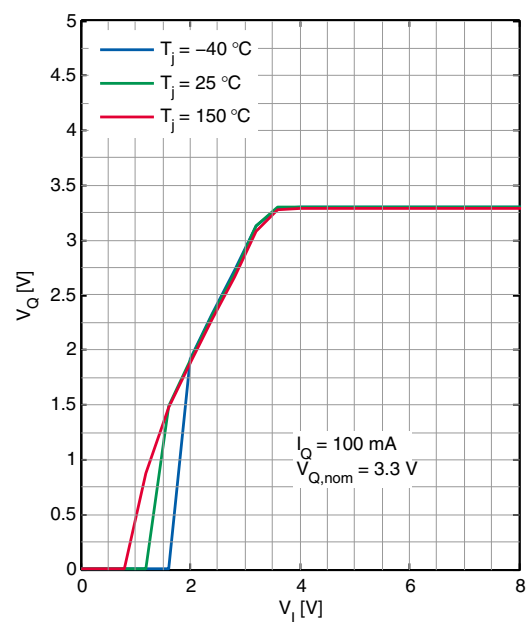
**Output voltage V_Q versus
junction temperature T_j**



**Output voltage V_Q versus
input voltage V_I**

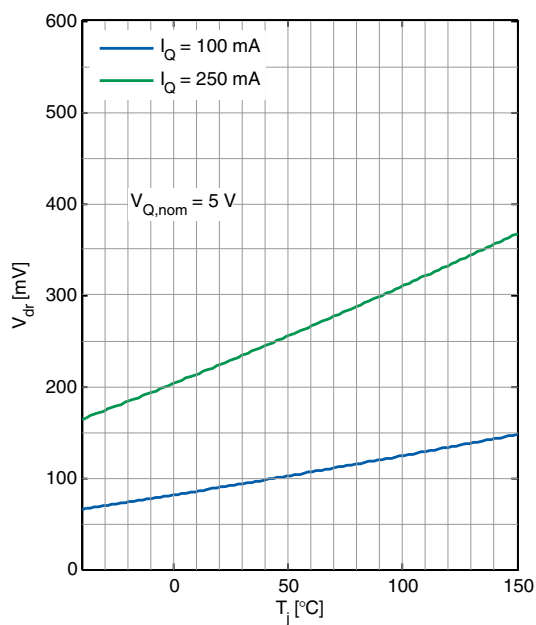


**Output voltage V_Q versus
input voltage V_I**

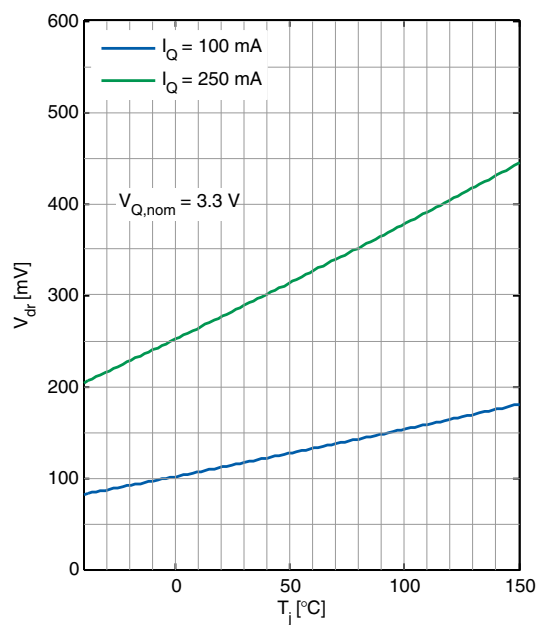


Block description and electrical characteristics

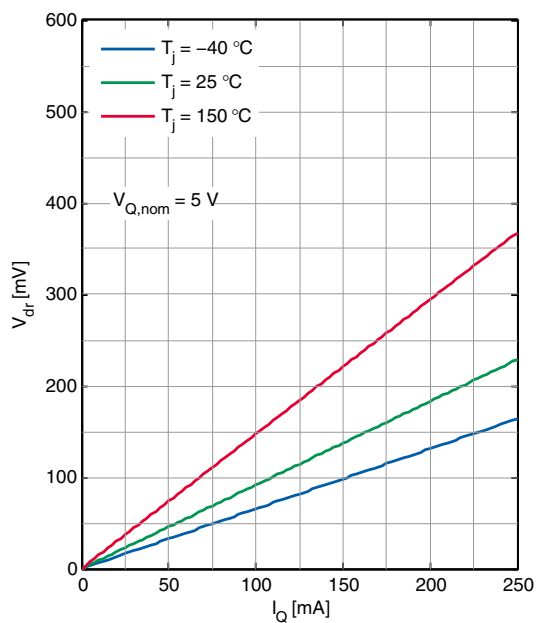
**Dropout voltage V_{dr} versus
junction temperature T_j**



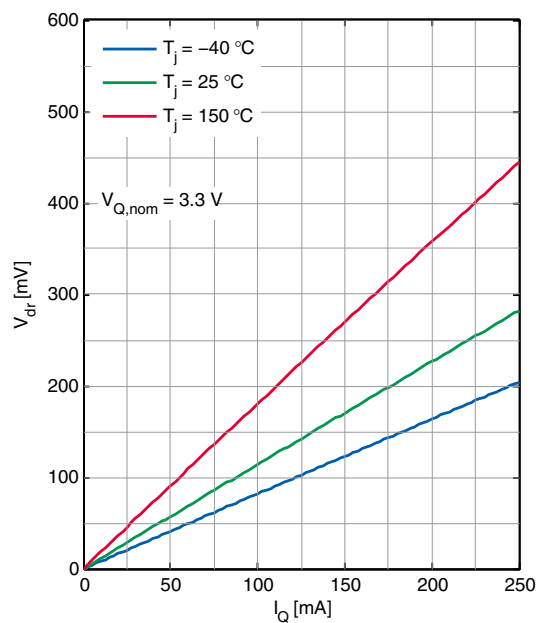
**Dropout voltage V_{dr} versus
junction temperature T_j**



**Dropout voltage V_{dr} versus
output current I_Q**

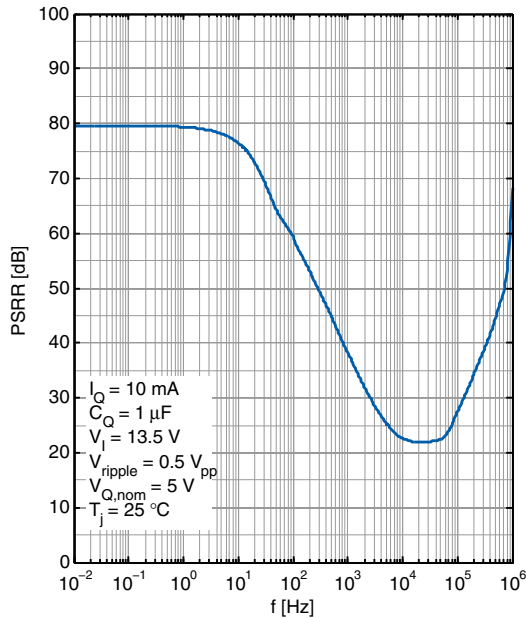


**Dropout voltage V_{dr} versus
output current I_Q**

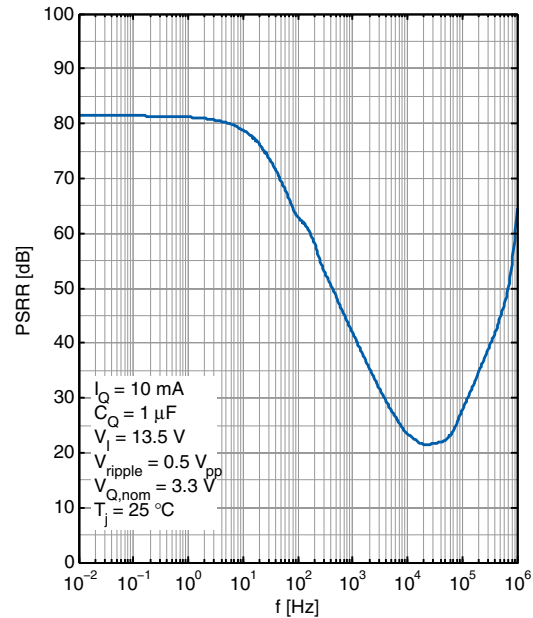


Block description and electrical characteristics

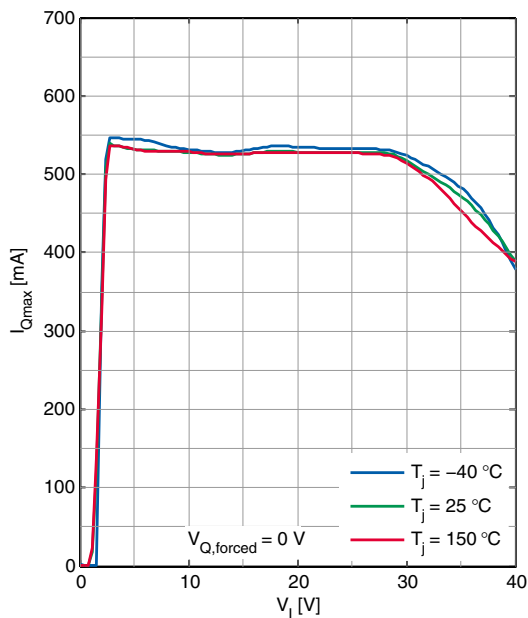
Power supply ripple rejection $PSRR$ versus ripple frequency f



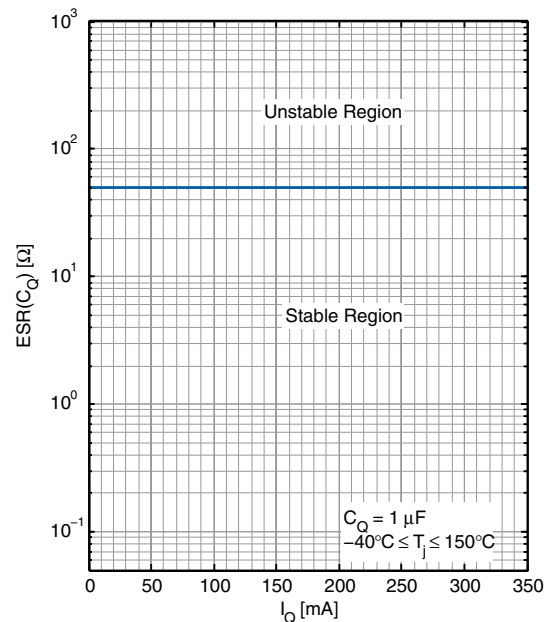
Power supply ripple rejection $PSRR$ versus ripple frequency f



Maximum output current I_Q versus input voltage V_I

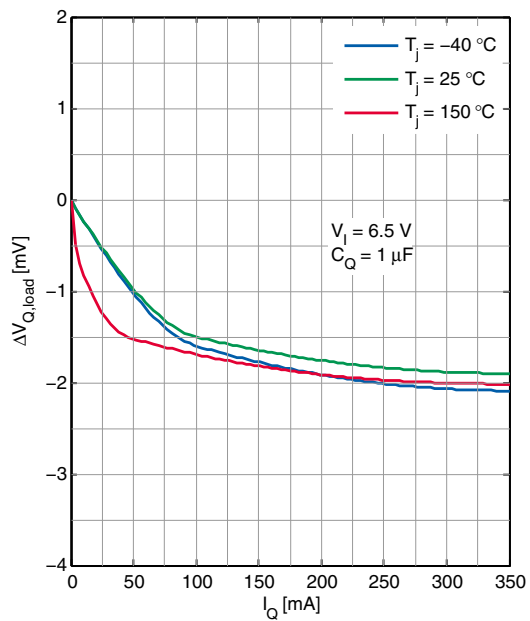


Equivalent series resistance of output capacitor $ESR(C_Q)$ versus output current I_Q

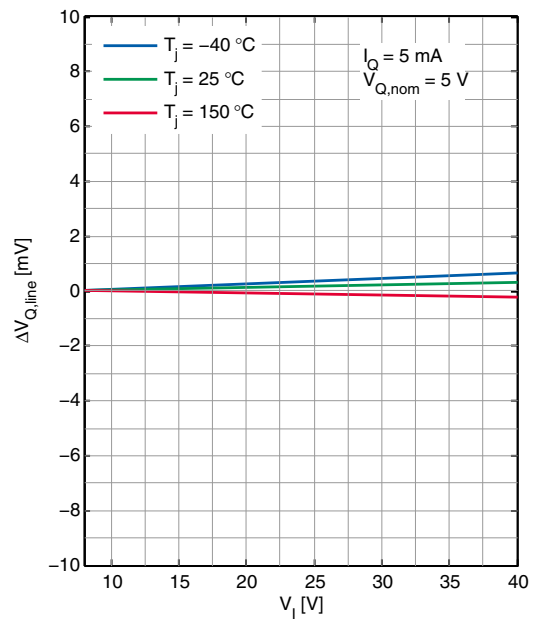


Block description and electrical characteristics

Load regulation $\Delta V_{Q,load}$ versus output current change I_Q



Line regulation $\Delta V_{Q,line}$ versus input voltage V_I



Block description and electrical characteristics

4.3 Current consumption

Table 5 Electrical characteristics current consumption

$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5\text{ V}$ (unless otherwise specified)

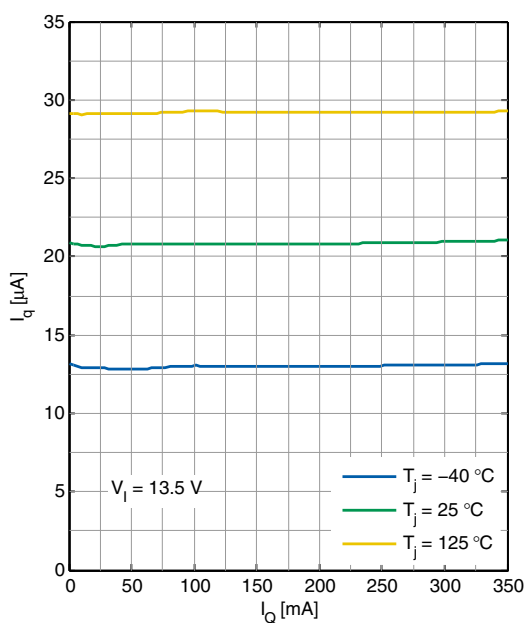
Typical values are given at $T_j = 25^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	1	μA	$V_{EN} = 0\text{ V}; T_j < 105^\circ\text{C}$	P_5.3.8
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	2	μA	$V_{EN} = 0.4\text{ V}; T_j < 125^\circ\text{C}$	P_5.3.10
Current consumption $I_q = I_I - I_Q$	I_q	–	20	30	μA	$I_Q = 0.05\text{ mA}$ $T_j = 25^\circ\text{C}$	P_5.3.11
Current consumption $I_q = I_I - I_Q$	I_q	–	23	36	μA	$I_Q = 0.05\text{ mA}$ $T_j < 125^\circ\text{C}$	P_5.3.12
Current consumption $I_q = I_I - I_Q$	I_q	–	25	42	μA	¹⁾ $I_Q = 350\text{ mA}$ $T_j < 125^\circ\text{C}$	P_5.3.13

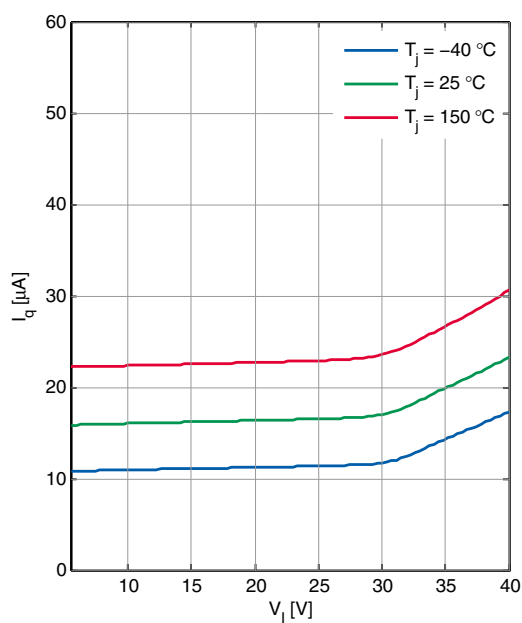
1) Not subject to production test, specified by design

4.4 Typical performance characteristics current consumption

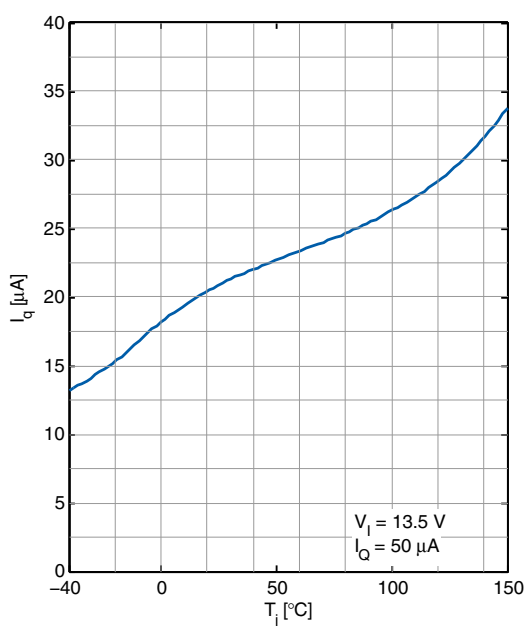
Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I



Current consumption I_q versus junction temperature T_j



Block description and electrical characteristics

4.5 Enable

The TLS835D2ELVSE can be switched on and off by the enable feature. Applying a “high” level as specified below with $V_{EN} \geq 2 \text{ V}$ to the EN pin enables the device. Applying a “low” level as specified below with $V_{EN} \leq 0.8 \text{ V}$ shuts down the device. The enable feature has a built-in hysteresis to avoid toggling between the ON/OFF state, when a signal with slow slope is applied to the EN pin.

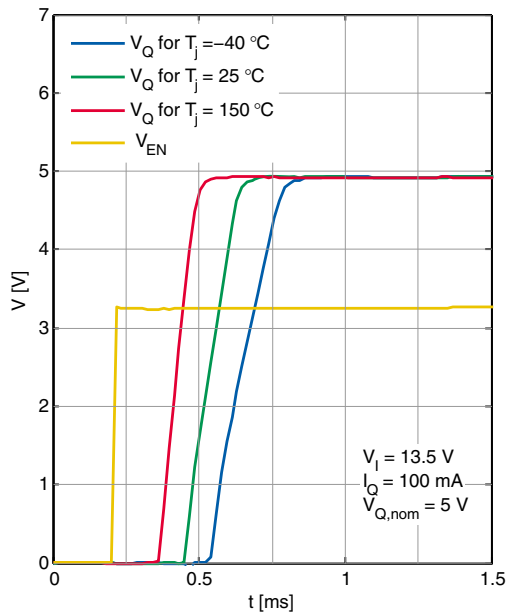
Table 6 Electrical characteristics enable

$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5 \text{ V}$, all voltages with respect to ground (unless otherwise specified)
 Typical values are given at $T_j = 25^\circ\text{C}$

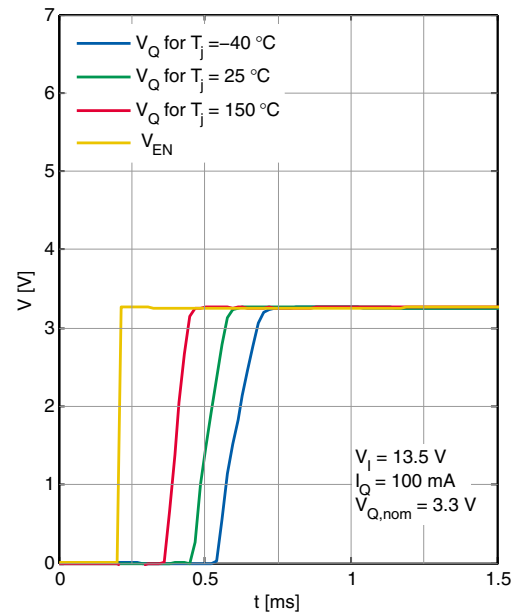
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable “high” input voltage	$V_{EN,H}$	2	–	–	V	–	P_5.5.1
Enable “low” input voltage	$V_{EN,L}$	–	–	0.8	V	–	P_5.5.2
Enable threshold hysteresis	$V_{EN,HY}$	90	–	–	mV	–	P_5.5.3
Enable “high” input current	$I_{EN,H}$	–	–	1	μA	$V_{EN} = 5 \text{ V}$	P_5.5.4
Enable “high” input current	$I_{EN,H}$	–	–	6	μA	$V_{EN} \leq 18 \text{ V}$	P_5.5.5
Enable internal pull-down resistor	R_{EN}	2.8	10	20	$\text{M}\Omega$	–	P_5.5.6

4.6 Typical performance characteristics enable

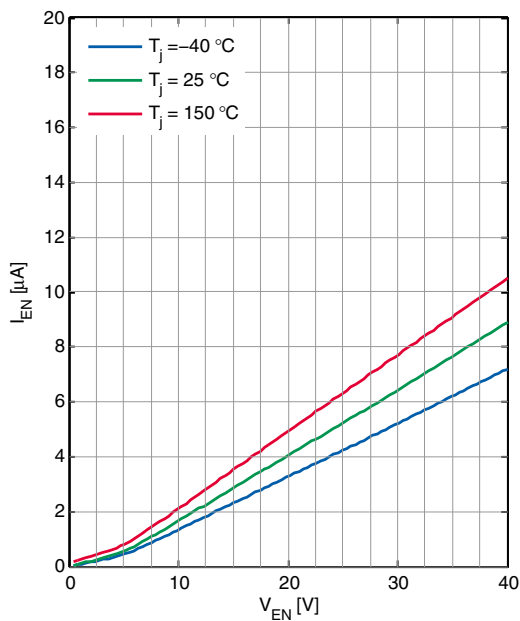
Output voltage V_Q versus time t (EN switched on)



Output voltage V_Q versus time t (EN switched on)



Enable input current I_{EN} versus enable input voltage V_{EN}



Block description and electrical characteristics

4.7 Output voltage selection

The output voltage V_Q of TLS835D2ELVSE can be selected by the SEL pin as follows:

SEL pin connected to Q: $V_Q = 5\text{ V}$;

SEL pin connected to GND: $V_Q = 3.3\text{ V}$.

4.8 Reset function

The reset function monitors the output voltage V_Q and indicates a potential imminent loss of power. This then allows enough time for the system to shut down or do the transition into a safe state. To meet the requirements of the application, some reset parameters can be adjusted by measures described in the following subsections.

Output undervoltage reset

The reset output RO is an open collector stage. It is internally pulled up to V_Q via a resistor **Reset output internal pull-up resistor** (Table 7). In the case of an undervoltage event at V_Q , RO is pulled to “low”. This signal can then be used to reset a microcontroller during low supply voltage.

Optional output undervoltage reset pull-up resistor $R_{RO,ext}$

Although the reset output RO is an open collector output with an integrated pull-up resistor, an additional, external pull-up resistor can be added to the output Q, if needed. A minimum value for the external resistor $R_{RO,ext}$ is specified in Table 7 in case this option is used.

Power-on reset delay time

The power-on reset delay time t_{rd} allows a microcontroller and oscillator to start up. This delay time is the time interval from exceeding the reset switching threshold $V_{RT,high}$ until the reset is released by switching the reset output RO from “low” to “high”. The power-on reset delay time t_{rd} is defined by an external delay capacitor C_D connected to pin D. C_D is charged by the delay capacitor charge current $I_{D,ch}$ starting from $V_D = 0\text{ V}$.

If the application requires a power-on reset delay time t_{rd} that differs from the default value specified in Table 7, the required value of the delay capacitor can be derived from the specified value and the desired power-on delay time as follows:

$$C_D = \frac{t_{rd}}{t_{rd,100\text{ nF}}} \cdot C_{D,100\text{ nF}} \quad (4.1)$$

where

- C_D : required capacitance of the delay capacitor
- t_{rd} : desired power-on reset delay time
- $t_{rd,100\text{ nF}}$: **Power-on reset delay time** (Table 7) for $C_D = 100\text{ nF}$ as specified in this data sheet

For a precise calculation, the tolerance of the delay capacitor also has to be taken into consideration.

Reset reaction time

The reset reaction time ensures that short undervoltage spikes do not trigger an unwanted reset “low” signal. The reset reaction time $t_{rr,total}$ comprises of the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor C_D . Therefore, the total reset reaction time becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d} \quad (4.2)$$

where

- $t_{rr,total}$: **Reset reaction time**

Block description and electrical characteristics

- $t_{rr,int}$: **Internal reset reaction time**
- $t_{rr,d}$: **Delay capacitor discharge time**

Reset adjust function

For selecting the default switching threshold as specified in **Table 7** under $V_{RT,low}$, connect the RADJ pin to GND.

To adjust the undervoltage reset lower switching threshold according to the requirements of the application, an external voltage divider (R_{ADJ1} , R_{ADJ2}) is required at pin RADJ. In this case, it should be noted that an additional current is dissipated by the resistors of the voltage divider.

With a voltage divider connected, the adjusted undervoltage reset lower switching threshold $V_{RT,low,new}$ is calculated according to the following equation:

$$V_{RT,low,new} = V_{RADJ,th} \left(\frac{R_{ADJ1}}{R_{ADJ2}} + 1 \right) \quad (4.3)$$

where

- $V_{RT,low,new}$: the desired new undervoltage reset switching lower threshold
- R_{ADJ1} , R_{ADJ2} : resistors of the external voltage divider
- $V_{RADJ,th}$: reset adjustment switching threshold given in **Table 7**

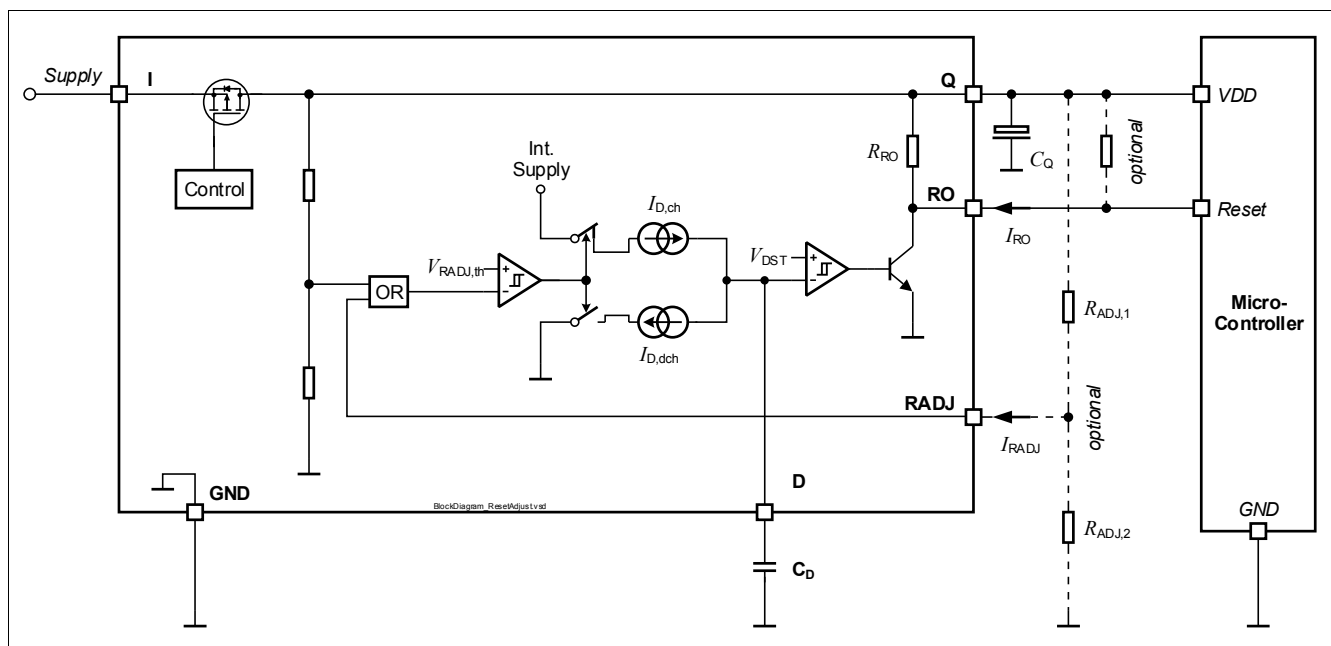


Figure 5 Block diagram reset function

Block description and electrical characteristics

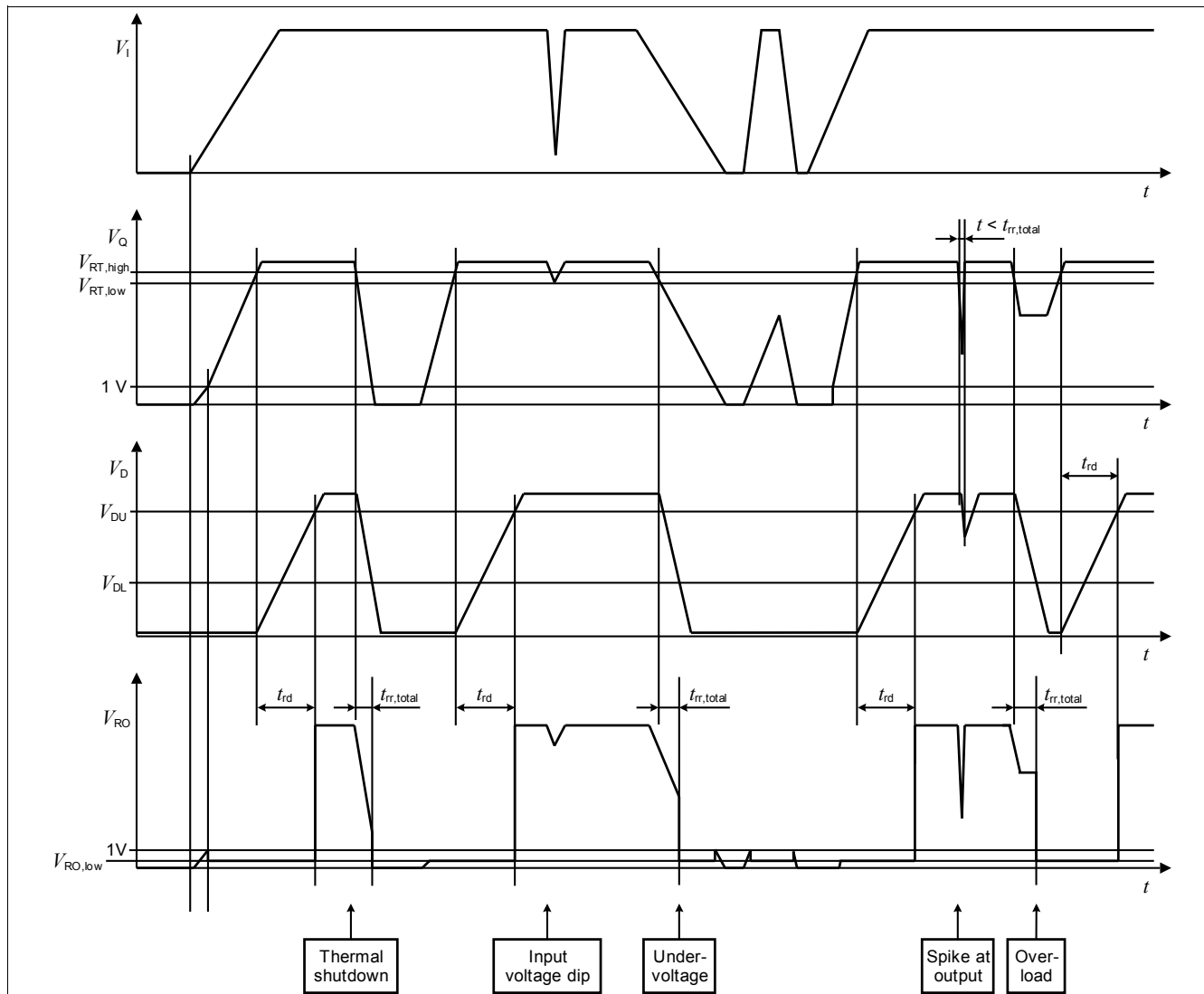


Figure 6 Timing diagram reset

Table 7 Electrical characteristics reset

$T_j = -40^{\circ}\text{C}$ to 150°C , $V_i = 13.5\text{ V}$, all voltages with respect to ground (unless otherwise specified).
 Typical values are given at $T_j = 25^{\circ}\text{C}$, $V_i = 13.5\text{ V}$.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output undervoltage reset (5 V output voltage)							
Output undervoltage reset upper switching threshold	$V_{RT,high}$	4.6	4.7	4.8	V	V_Q increasing, $V_{EN} \geq 2.0\text{ V}$, RADJ connected to GND, SEL connected to Q	P_5.8.1
Output undervoltage reset lower switching threshold	$V_{RT,low}$	4.5	4.6	4.7	V	V_Q decreasing, $V_{EN} \geq 2.0\text{ V}$, RADJ connected to GND, SEL connected to Q	P_5.8.2

Block description and electrical characteristics

Table 7 Electrical characteristics reset (cont'd)

$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5\text{ V}$, all voltages with respect to ground (unless otherwise specified).
 Typical values are given at $T_j = 25^\circ\text{C}$, $V_I = 13.5\text{ V}$.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset adjustment switching threshold	$V_{\text{RADJ,th}}$	0.86	0.9	0.94	V	SEL connected to Q	P_5.8.4
Reset threshold adjustment range	$V_{\text{RT,range}}$	2	–	4.2	V	SEL connected to Q	P_5.8.5

Output undervoltage reset (3.3 V output voltage)

Output undervoltage reset upper switching threshold	$V_{\text{RT,high}}$	3.03	3.10	3.17	V	V_Q increasing, $V_{\text{EN}} \geq 2.0\text{ V}$, RADJ connected to GND, SEL connected to GND	P_5.8.6
Output undervoltage reset lower switching threshold	$V_{\text{RT,low}}$	2.97	3.03	3.10	V	V_Q decreasing, $V_{\text{EN}} \geq 2.0\text{ V}$, RADJ connected to GND, SEL connected to GND	P_5.8.7
Reset adjustment switching threshold	$V_{\text{RADJ,th}}$	0.86	0.9	0.94	V	SEL connected to GND	P_5.8.9
Reset threshold adjustment range	$V_{\text{RT,range}}$	2	–	2.75	V	SEL connected to GND	P_5.8.10

Reset output RO

Reset output “low” voltage	$V_{\text{RO,low}}$	–	0.2	0.4	V	$1\text{ V} \leq V_Q \leq V_{\text{RT}}$; $R_{\text{RO}} > 4.7\text{ k}\Omega$	P_5.8.11
Reset output internal pull-up resistor	$R_{\text{RO,int}}$	13	20	36	k Ω	internally connected to Q	P_5.8.12
Reset output external pull-up resistor to V_Q	$R_{\text{RO,ext}}$	4.7	–	–	k Ω	$1\text{ V} \leq V_Q \leq V_{\text{RT}}$; $V_{\text{RO}} \leq 0.4\text{ V}$	P_5.8.13

Reset delay timing

Power-on reset delay time	t_{rd}	17	25	37	ms	$C_D = 100\text{ nF}$ Calculated value	P_5.8.15
Upper delay switching threshold	V_{DU}	–	0.9	–	V	–	P_5.8.16
Lower delay switching threshold	V_{DL}	–	0.6	–	V	–	P_5.8.17
Delay capacitor charge current	$I_{\text{D,ch}}$	–	3.6	–	μA	$V_D = 1\text{ V}$	P_5.8.18
Delay capacitor discharge current	$I_{\text{D,dch}}$	–	210	–	mA	$V_D = 1\text{ V}$	P_5.8.19
Delay capacitor discharge time	$t_{\text{rr,d}}$	–	2	4	μs	$C_D = 100\text{ nF}$ Calculated value	P_5.8.20

Block description and electrical characteristics

Table 7 Electrical characteristics reset (cont'd)

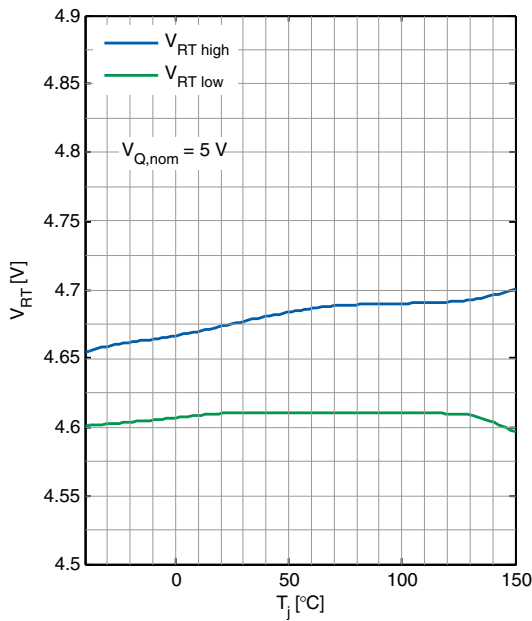
$T_j = -40^\circ\text{C}$ to 150°C , $V_I = 13.5\text{ V}$, all voltages with respect to ground (unless otherwise specified).
 Typical values are given at $T_j = 25^\circ\text{C}$, $V_I = 13.5\text{ V}$.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Internal reset reaction time ¹⁾	$t_{rr,int}$	–	8	14	μs	$C_D = 0\text{ nF}$	P_5.8.21
Reset reaction time	$t_{rr,total}$	–	10	18	μs	$C_D = 100\text{ nF}$ Calculated value	P_5.8.22

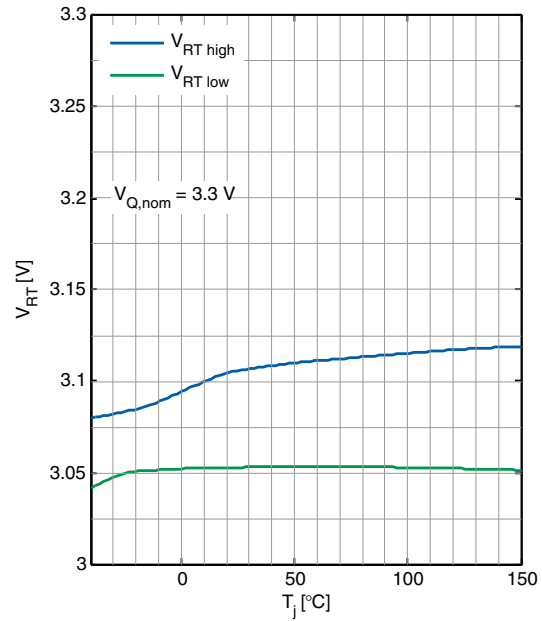
1) Parameter not subject to production test; specified by design.

4.9 Typical performance characteristics Reset

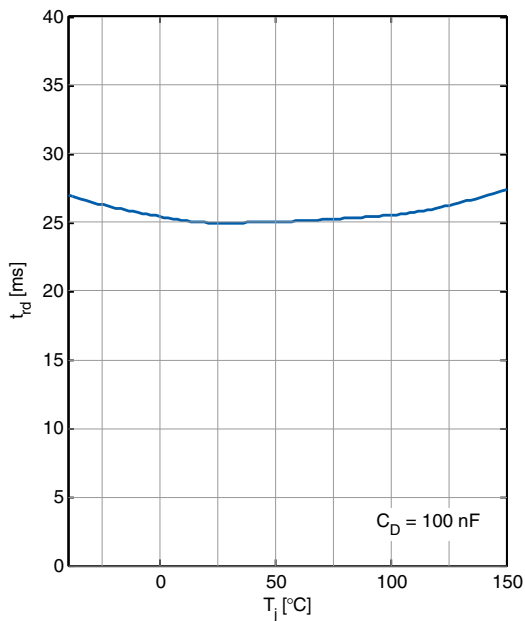
Undervoltage reset threshold V_{RT} versus junction temperature T_j



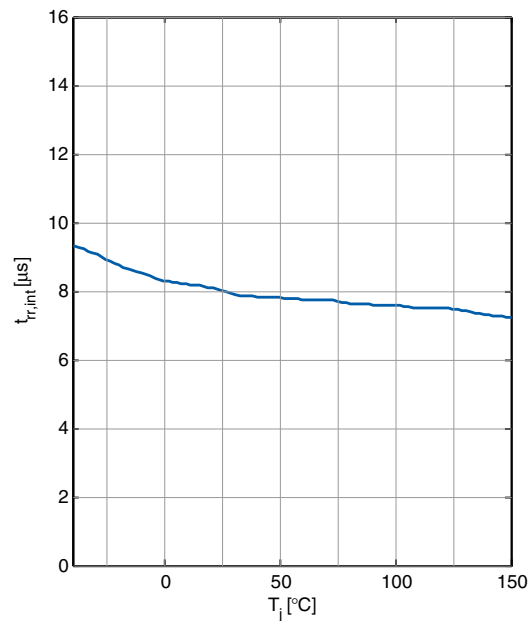
Undervoltage reset threshold V_{RT} versus junction temperature T_j



Power-on reset delay time t_{rd} versus junction temperature T_j



Reset reaction time t_{rr} versus junction temperature T_j



Application information

TLS835D2ELVSE is designed to also be stable with low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the voltage regulator's output pin and GND pin and on the same side of the PCB as the regulator itself.

In case of input voltage or load current transients, the capacitance should be dimensioned accordingly. The configuration has to be verified in the real application to ensure that the output stability requirements are fulfilled.

5.3 Thermal considerations

From the known input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated as follows:

$$P_D = (V_I - V_Q)I_Q + V_I I_q \quad (5.1)$$

with

- P_D : continuous power dissipation
- V_I : input voltage
- V_Q : output voltage
- I_Q : output current
- I_q : quiescent current

The maximum acceptable thermal resistance R_{thJA} is given by:

$$R_{thJA} = \frac{T_{j,max} - T_a}{P_D} \quad (5.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined by referencing the specification for **“Thermal resistance” on Page 9**.

5.4 Reverse polarity protection

TLS835D2ELVSE is not protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is necessary. The absolute maximum ratings of the device as specified in **“Absolute maximum ratings” on Page 7** must be maintained.

5.5 Further application information

For further information you may contact <https://www.infineon.com/>

Package information

6 Package information

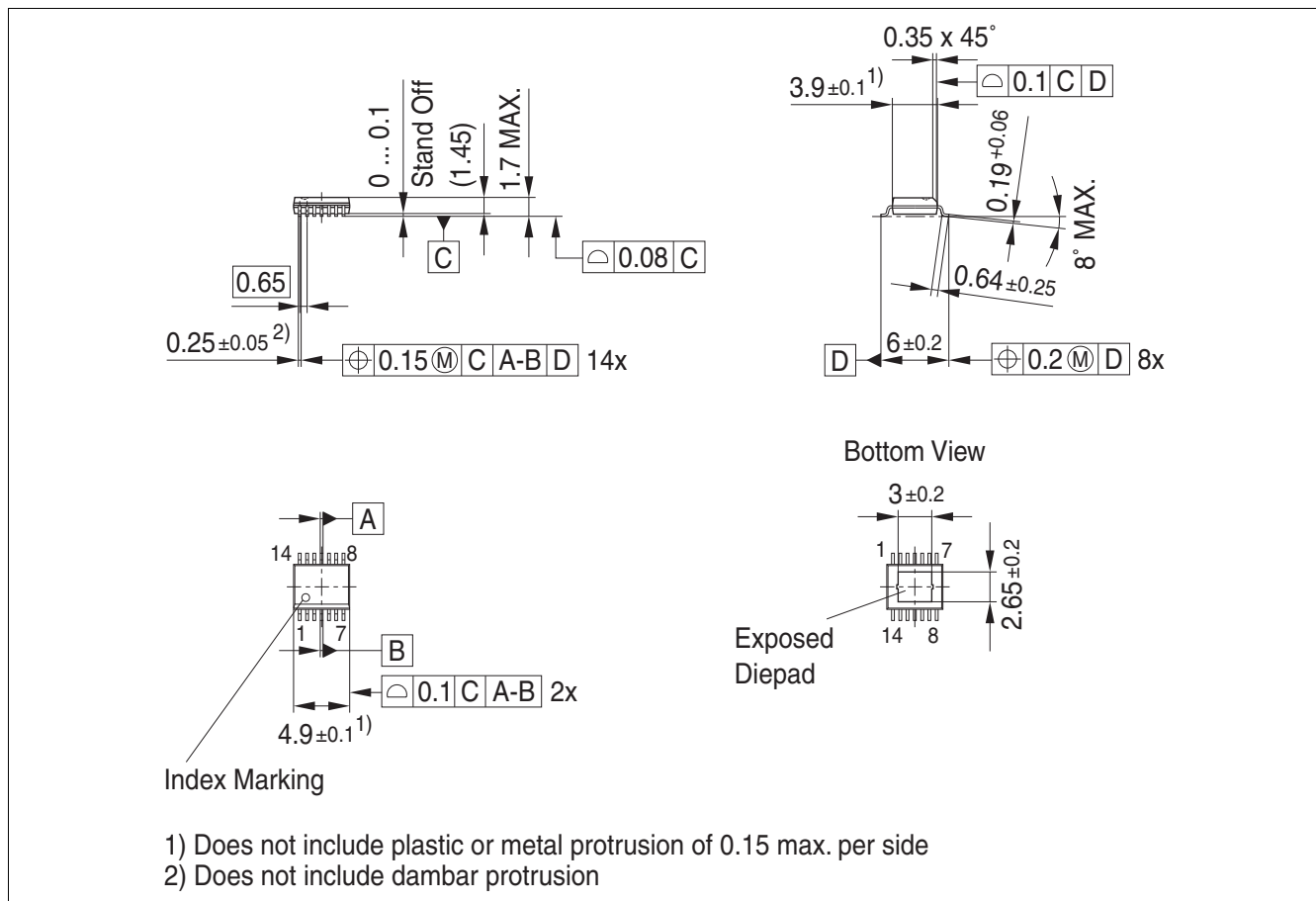


Figure 8 PG-SSOP-14¹⁾

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

Revision history

7 Revision history

Revision	Date	Changes
1.1	2018-09-17	Editorial changes Updated T to T_J in graph of “Equivalent series resistance of output capacitor $ESR(C_Q)$ versus output current I_Q ” Reworked reset description, updated timing diagram reset
1.01	2018-03-12	Editorial Changes
1.0	2018-02-19	Initial Version

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Edition 2018-09-17

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

Z8F61372421

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