

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C7

650V CoolMOS™ C7 Power Transistor
IPB65R045C7

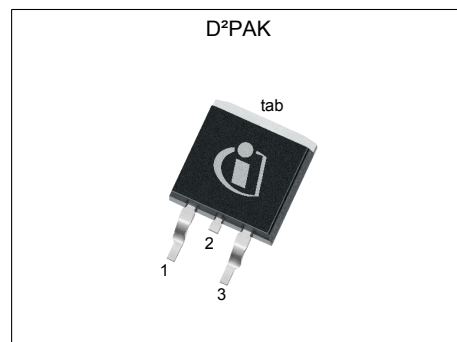
Data Sheet

Rev. 2.1
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.



Features

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- Best in class $R_{DS(on)}$ /package
- Easy to use/drive
- Pb-free plating, halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Enabling higher system efficiency
- Enabling higher frequency / increased power density solutions
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures

Applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

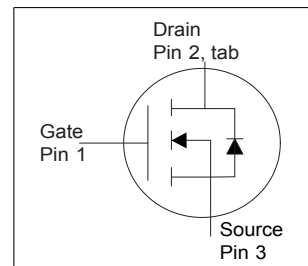


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	45	mΩ
$Q_{g,typ}$	93	nC
$I_{D,pulse}$	212	A
$E_{oss@400V}$	11.7	μJ
Body diode di/dt	60	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPB65R045C7	PG-TO 263	65C7045	see Appendix A

Table of Contents

Description	2
Maximum ratings	4
Thermal characteristics	5
Electrical characteristics	6
Electrical characteristics diagrams	8
Test Circuits	12
Package Outlines	13
Appendix A	14
Revision History	15
Disclaimer	15

2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	46 29	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	212	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	249	mJ	$I_D=12\text{A}$; $V_{DD}=50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	1.25	mJ	$I_D=12\text{A}$; $V_{DD}=50\text{V}$
Avalanche current, single pulse	I_{AS}	-	-	12.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	227	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	I_S	-	-	46	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	212	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1.5	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$
Maximum diode commutation speed	di/dt	-	-	60	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_G .

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.55	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=1.25mA$
Zero gate voltage drain current	I_{DSS}	-	-	2	μA	$V_{DS}=650$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=650$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.040 0.096	0.045 -	Ω	$V_{GS}=10V$, $I_D=24.9A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=24.9A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.85	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4340	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	70	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	146	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	1630	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=24.9A$, $R_G=3.3\Omega$
Rise time	t_r	-	14	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=24.9A$, $R_G=3.3\Omega$
Turn-off delay time	$t_{d(off)}$	-	82	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=24.9A$, $R_G=3.3\Omega$
Fall time	t_f	-	7	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=24.9A$, $R_G=3.3\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	23	-	nC	$V_{DD}=400V$, $I_D=24.9A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	30	-	nC	$V_{DD}=400V$, $I_D=24.9A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	93	-	nC	$V_{DD}=400V$, $I_D=24.9A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=400V$, $I_D=24.9A$, $V_{GS}=0$ to $10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=24.9A$, $T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	725	-	ns	$V_R=400V$, $I_F=46A$, $di_F/dt=60A/\mu s$
Reverse recovery charge	Q_{rr}	-	13	-	μC	$V_R=400V$, $I_F=46A$, $di_F/dt=60A/\mu s$
Peak reverse recovery current	I_{rrm}	-	36	-	A	$V_R=400V$, $I_F=46A$, $di_F/dt=60A/\mu s$

5 Electrical characteristics diagrams

Table 8

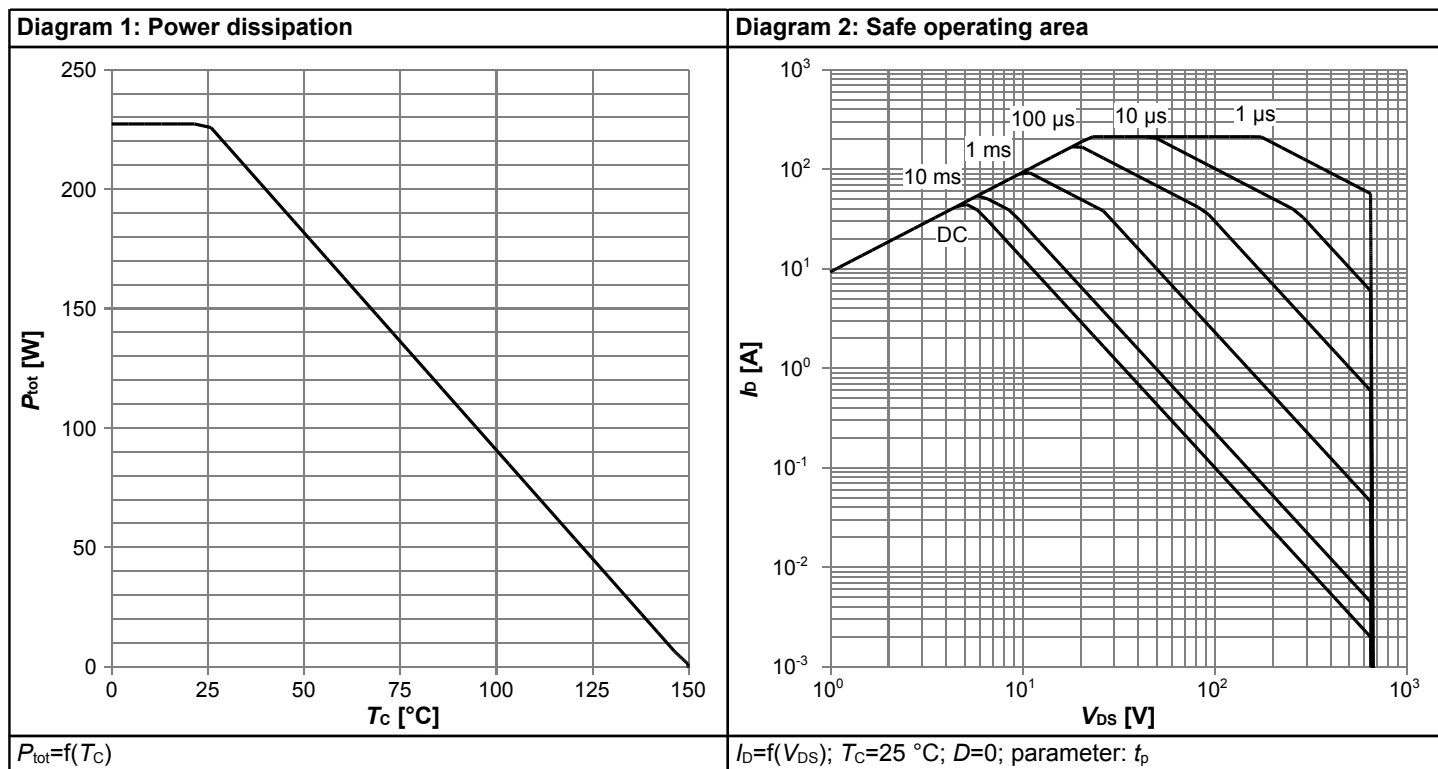


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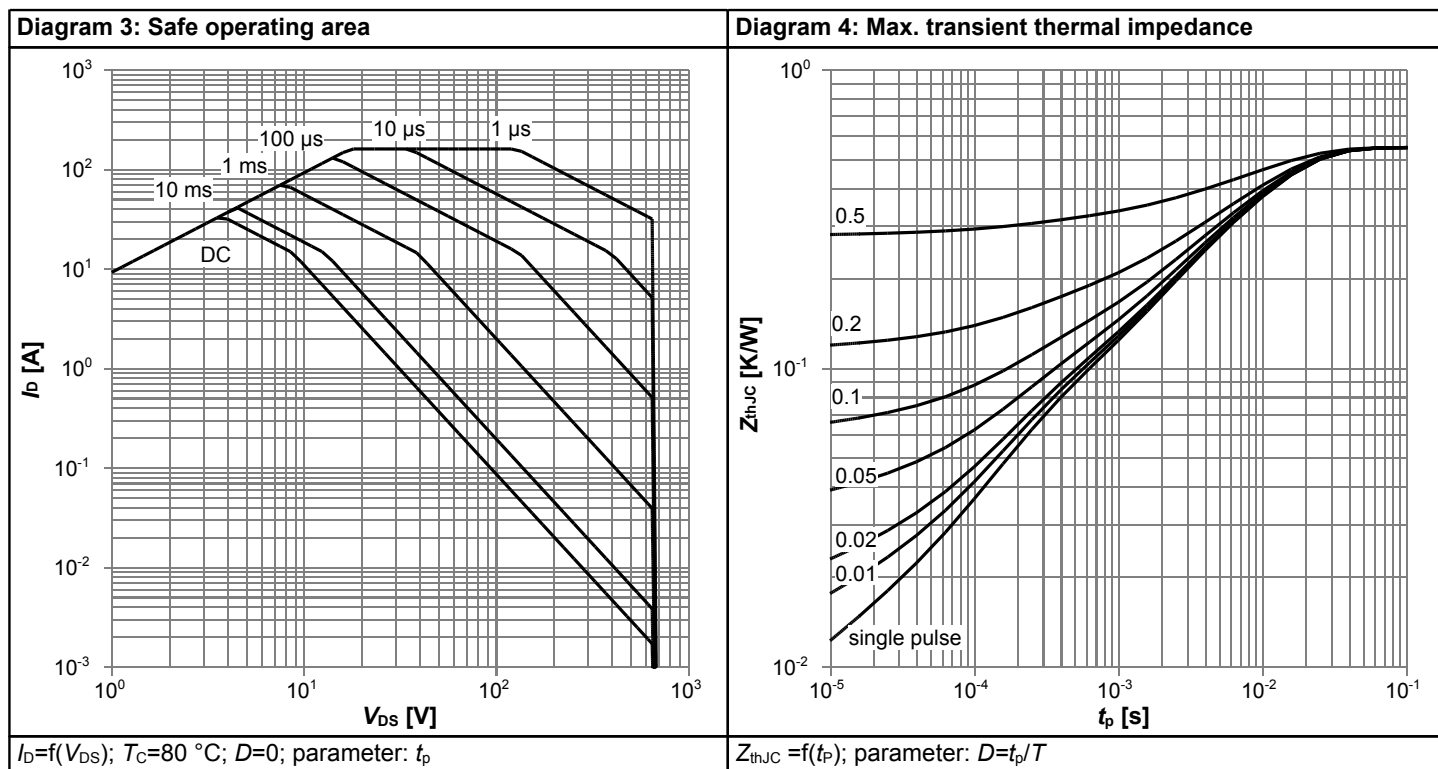


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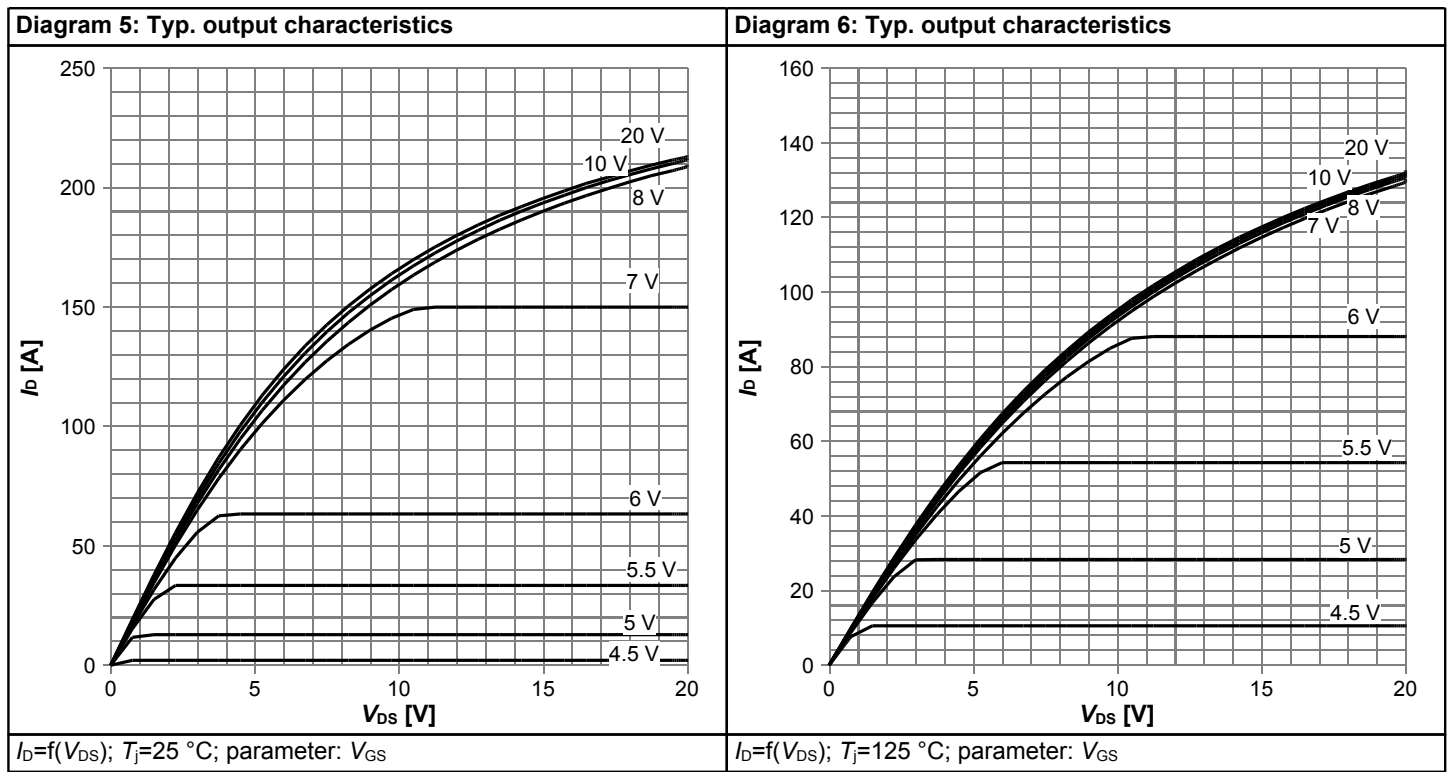


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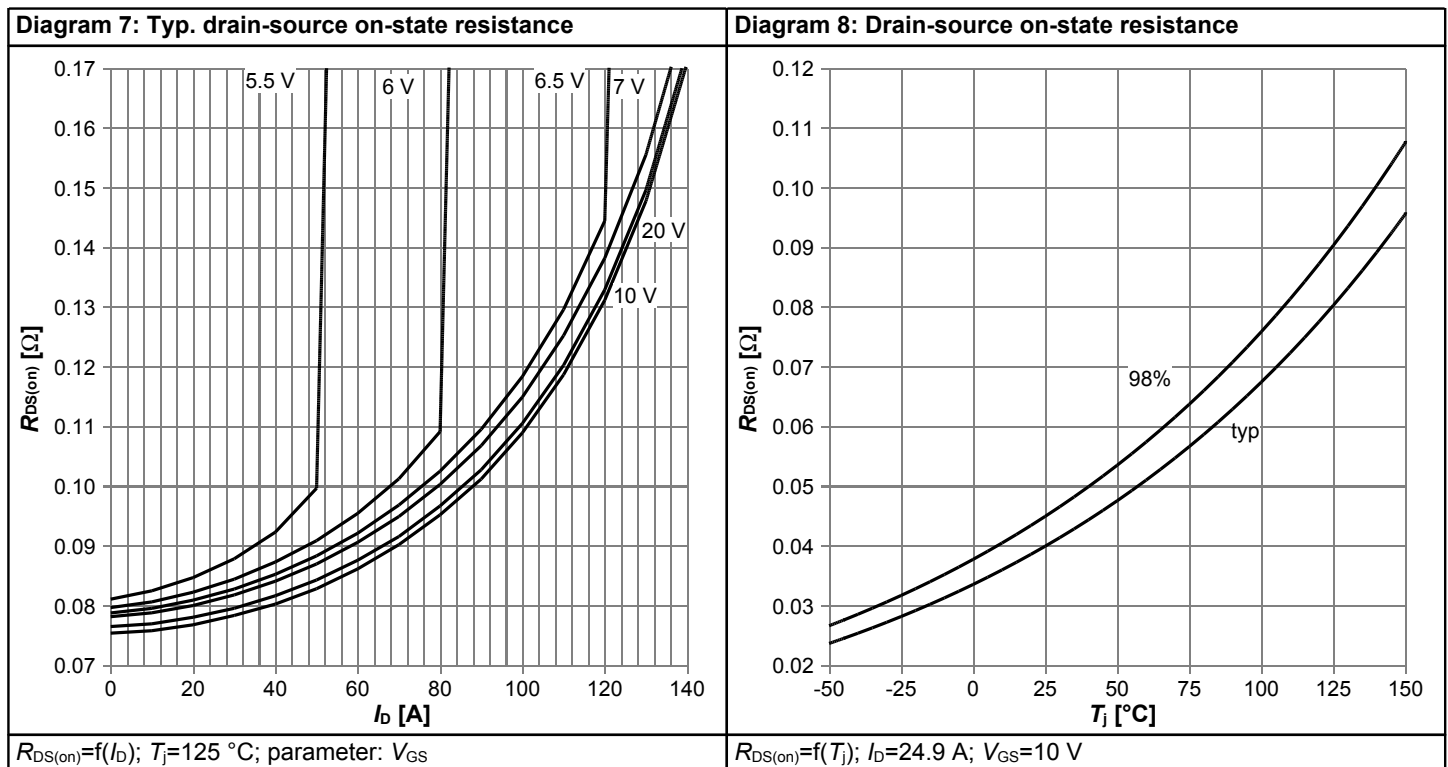


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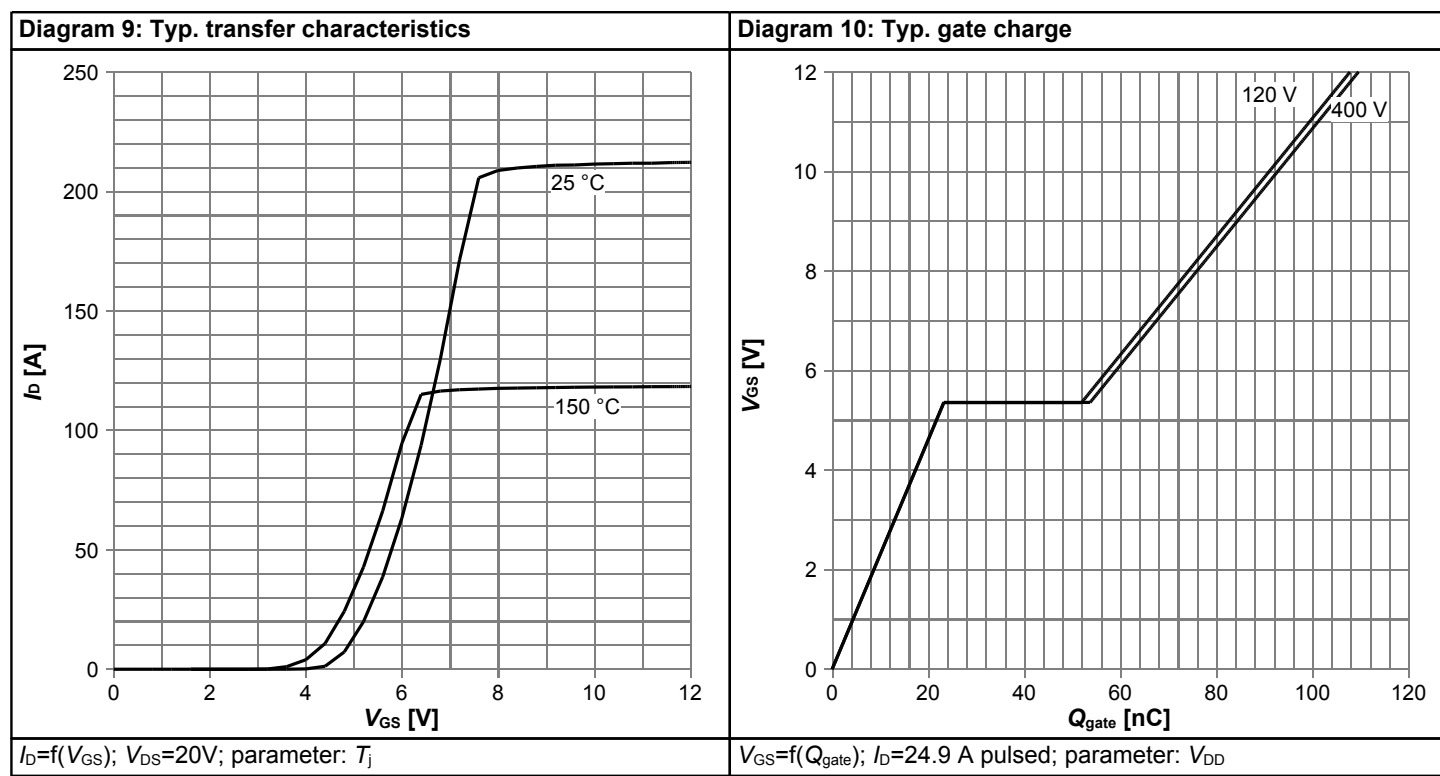


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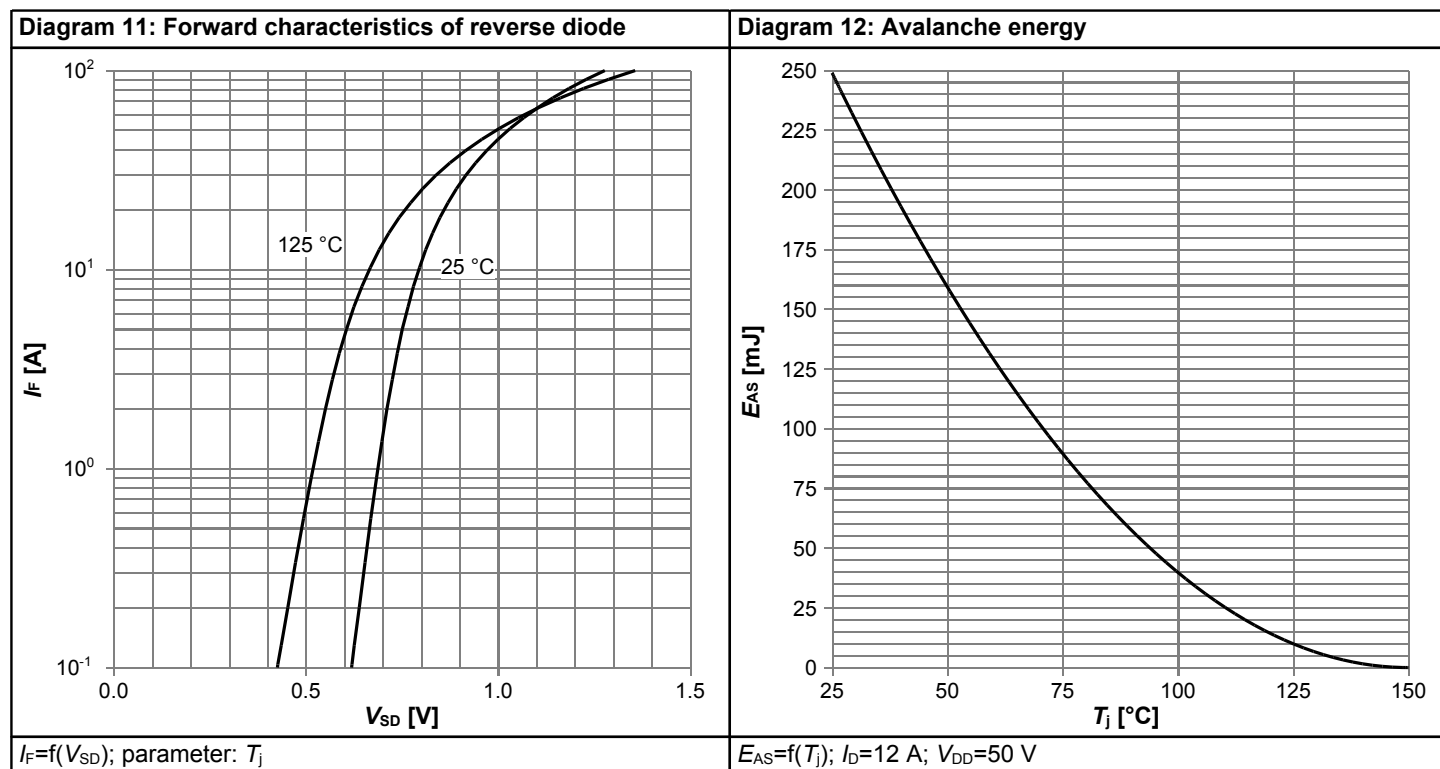


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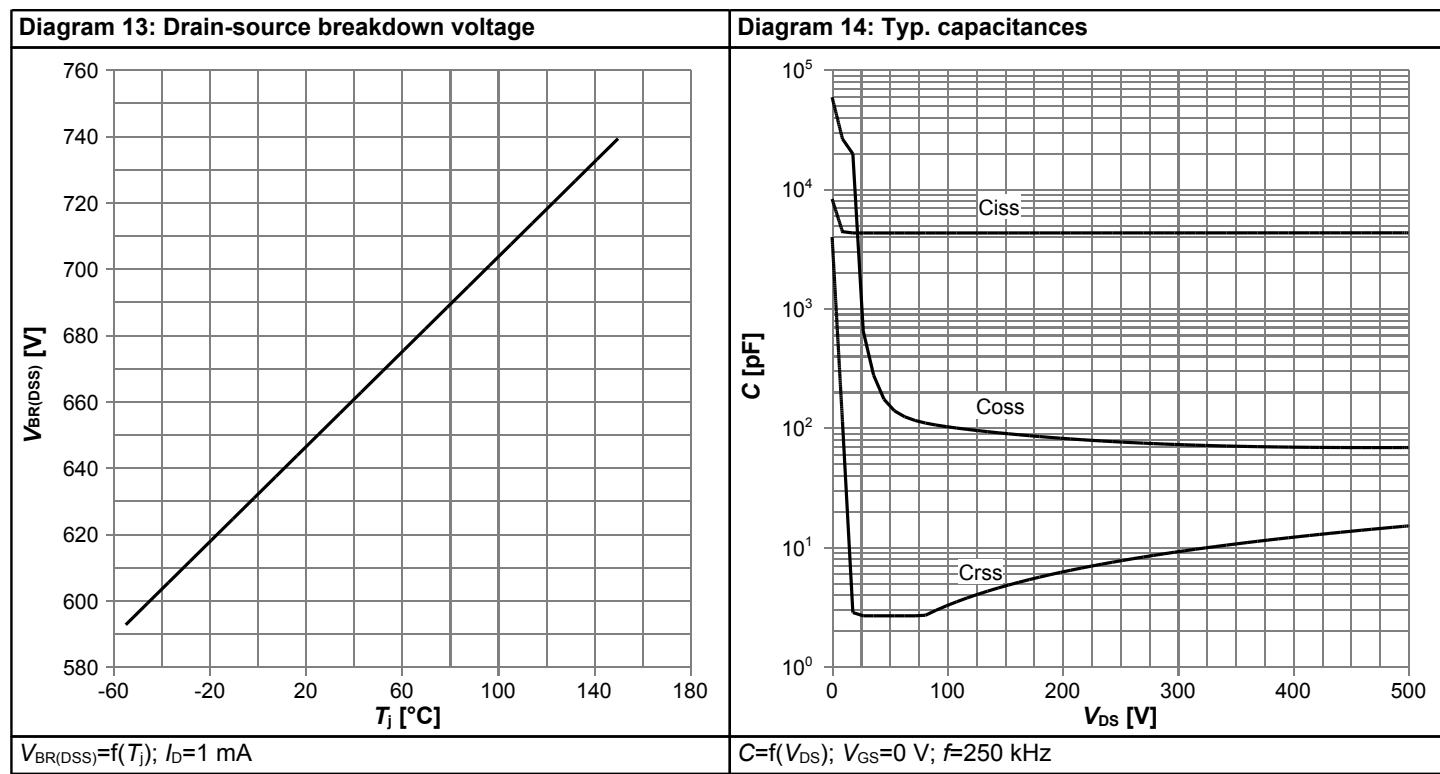
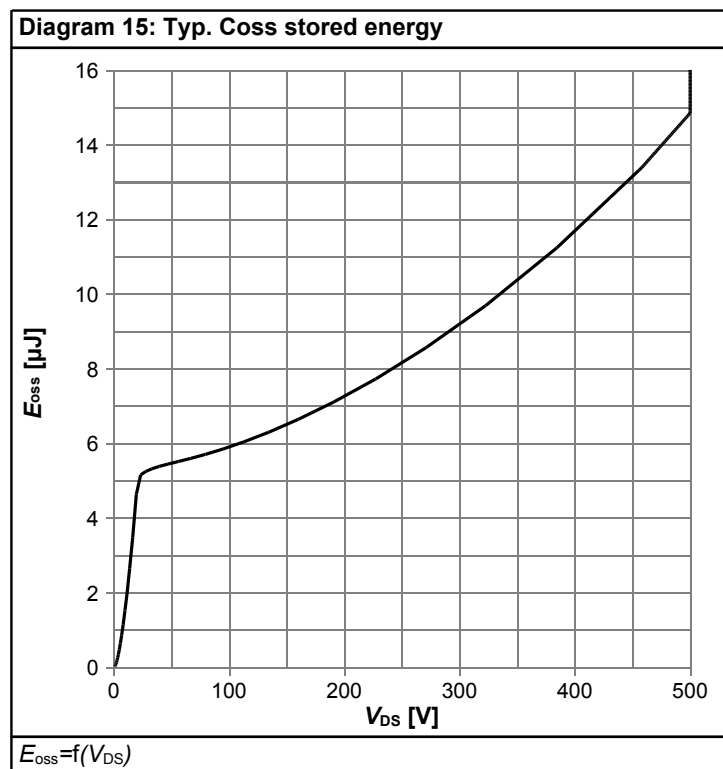


Table 15



6 Test Circuits

Table 16 Diode characteristics

Figure 1 consists of two parts. The left part is a schematic diagram of a test circuit for diode characteristics. It shows two diodes connected in series, each with a gate resistor R_{g1} and R_{g2} . The diodes are connected to a common load inductor. The forward current I_F is measured through the inductor. The reverse voltage V_{DS} is measured across the diodes. The gate resistors are equal, $R_{g1} = R_{g2}$. The right part is a graph of the diode recovery waveform. The vertical axis represents voltage V and current I . The horizontal axis represents time t . The forward current I_F is shown as a solid line, and the reverse current I_{rm} is shown as a dashed line. The forward voltage V_{DS} is shown as a solid line, and the reverse voltage $V_{DS(peak)}$ is shown as a dashed line. The forward recovery time t_F is the time from the start of the reverse current to the point where the reverse current is 10% of the forward current. The reverse recovery time t_{rr} is the time from the start of the reverse current to the point where the reverse current is 10% of the forward current. The storage time t_s is the time from the point where the reverse current is 10% of the forward current to the end of the reverse current. The forward charge Q_F is the area under the forward current curve, and the reverse charge Q_s is the area under the reverse current curve. The total reverse charge Q_{rr} is the sum of Q_F and Q_s .

Table 17 Switching times

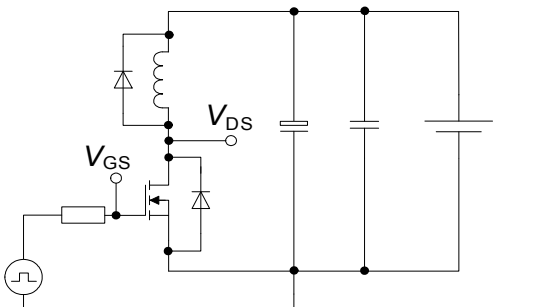
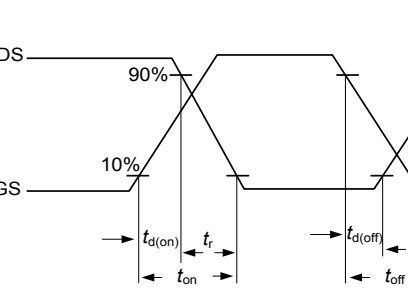
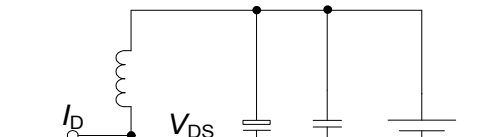
Switching times test circuit for inductive load	Switching times waveform
 The diagram illustrates a switching test circuit for an inductive load. A MOSFET is connected in a common-source configuration. The drain is connected to a DC supply through an inductor, with an anti-parallel diode. The gate is driven by a pulse generator through a resistor. The drain voltage V_{DS} and gate voltage V_{GS} are the signals of interest.	 The waveform shows the relationship between drain-source voltage V_{DS} and gate-source voltage V_{GS} during switching. Key time intervals are defined as follows: $t_{d(on)}$: Delay time from 10% V_{GS} to 90% V_{DS}. t_r: Rise time of V_{DS} from 90% to 100%. t_{on}: Total turn-on time from 10% V_{GS} to 100% V_{DS}. $t_{d(off)}$: Delay time from 90% V_{DS} to 10% V_{GS}. t_f: Fall time of V_{DS} from 90% to 10%. t_{off}: Total turn-off time from 90% V_{DS} to 10% V_{GS}.

Table 18 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines

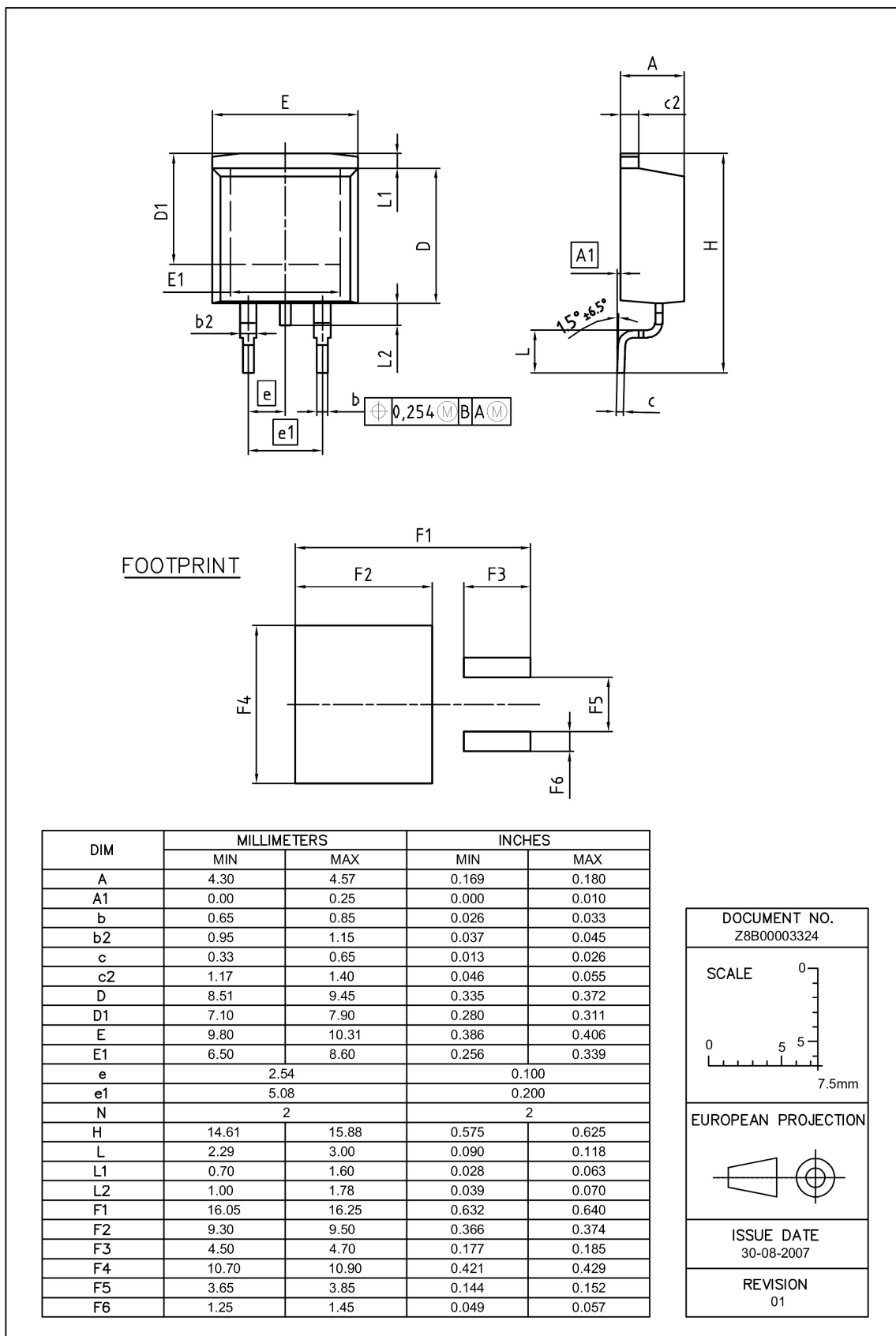


Figure 1 Outline PG-TO 263, dimensions in mm/inches

8 Appendix A

Table 19 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPB65R045C7

Revision: 2013-04-30, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-04-18	Release of final version
2.1	2013-04-30	Body diode di/dt update

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