

Application Note: SY6924

High Efficiency, 2.5A, Multi-Cell Li-Ion Battery Charger

General Description

SY6924 is a 4-14V input, 2.5A multi-cell Li-Ion battery step-down charger. The charge current up to 2.5A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timeout and adaptive input power limit for safety battery charge operation. It consists of 16V rating reverse blocking FET and power switching FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY6924 along with small QFN3×3 footprint provides small PCB area application.

Ordering Information



Features

- Integrated Synchronous Buck and Reverse Blocking FET with 16V Rating
- Adaptive Input Power Limit for 4-14V Wide Input Voltage
- Maximum 2.5A Programmable Charge Current
- 4.2V and 4.35V Constant Voltage Selectable
- +/-0.5% Cell Voltage Accuracy
- Support Single-cell or Two-cell Battery Pack
- External Shutdown Function
- Input Voltage UVLO and OVP
- Thermal Fold-back Protection
- Over Temperature Protection
- Battery Short Protection
- Programmable Charge Timeout
- Charge Status Indication
- Low Profile QFN3×3 Package for Portable Applications

Applications

- Power Bank
- Cellular Telephones, PDA, MP3 Players, MP4 Players
- PSP Game Players, NDS Game Players
- Notebook



Figure1. Schematic Diagram

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Pinout (top view)



Top Mark: **Ynxyz**, (Device code: Yn, *x=year code*, *y=week code*, *z= lot number code*)

Pin Name	Pin Number	Description
RS	1	Charge current sense resistor positive pin. The sensed voltage drop between RS and BAT is used for charge current regulation and charge termination detection.
CELL	2	Battery voltage selection pin. Floating for two cells battery and grounding for single cell battery. CELL pin can't be pulled high to any bias voltage higher than 3.3V.
TIM	3	Charge time-out programming pin. Connect this pin with a capacitor to ground to program the time-out protection threshold. Internal current source charge the capacitor for TC mode and fast charge (CC&CV) mode's charge time limit. TC charge time limit is about 1/9 of fast charge time.
NTC	4	Battery thermal sense pin. The voltage on the NTC pin is sensed for battery thermal protection. UTP threshold is typical 75% of V_{IN} and OTP threshold is typical 45% of V_{IN} . NTC pin also can be used for the adaptive input power limit reference refresh. The adaptive input power limit threshold will be refreshed when NTC is pulled low for more than 100ms. SY6924 sets the charge current to the trickle value; the IC will refresh the adaptive input power limit threshold according the input voltage. For higher than 6V input, the IC will clamp the input voltage at V_{IN} -0.6V by regulating the duty cycle of Buck converter. For lower than 6V input, the clamped input voltage is set by VSEN pin.
CV	5	Battery CV voltage selection pin.
VSEN	6	Input voltage sense pin for adaptive input power limit. If the voltage drops to internal 1.19V reference voltage, the V_{IN} will be clamped to setting value and input current will be limited.
EN	7	Enable control pin. High logic for enable on and low logic for enable off.
SGND	8	Signal ground pin.



STAT	9	Charge status indication pin. Open drain pin. Pull high to IN thru a LED to indicate the charge in process. When the charge is done, LED is off.
BD	10, 13	Connect to the drain of internal blocking FET. Bypass at least a 10μ F ceramic cap to GND.
BST	11	Boot-strap pin. Supply main FET's gate driver. Decouple this pin to LX with a 0.1μ F ceramic cap.
IN	12	DC power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.
LX	14	Switch node pin. Connect to external inductor.
PGND	15	Power ground pin.
BAT	16	Battery voltage sense pin.

Absolute Maximum Ratings (Note 1)

IN, BAT, LX, NTC, STAT, BD, EN, CV, VSEN	18V
TIM, CELL	4V
BST-LX Voltage	4V
RS	BAT-0.3~BAT+0.3V
LX Pin Current Continuous	5A
Power Dissipation, PD @ TA = 25°C, QFN3×3	2.1W
Package Thermal Resistance (Note 2)	
θ_{JA}	48 °C/W
θ _{IC}	4 °C/W
Junction Temperature Range	40°C to 125°C
Lead Temperature (Soldering, 10 sec.)	
Storage Temperature Range	65°C to 150°C

Recommended Operating Conditions (Note 3)

IN	4V to 14V
BAT, LX, NTC, STAT, BD, EN, CV, VSEN	0V to16V
TIM, CELL	0V to 3.3V
BST-LX Voltage	0V to 3.3V
RS	
LX Pin Current Continuous	4.5A
Junction Temperature Range	40°C to 100°C
Ambient Temperature Range	40°C to 85°C



Electrical Characteristics

 $T_{A}\!=\!25^{\circ}C, \ V_{IN}\!=\!5V, \ GND\!=\!0V, \ C_{IN}\!=\!10\mu F, \ L\!=\!2.2\mu H, \ R_{S}\!=\!10m\Omega, \ C_{TIM}\!=\!330nF, \ unless \ otherwise \ specified.$

Symbol	Conditions	Min	Тур	Max	Unit
V		4		14	V
V IN		4		14	v
V	V _{IN} rising and measured			4	V
V UVLO	from IN to ground			4	v
A 17	Measured from IN to		0.2		V
Δ V UVLO	ground		0.2		v
V_{IN_OVP}	V _{IN} rising and measured from IN to ground	13.5			V
437	Measured from IN to		0.5		V
$\Delta \mathbf{v}_{OVP}$	ground		0.5		v
I _{BAT}	V _{IN} absent or EN=Low		5	10	μA
	Disable charge		0.8	1.1	mA
<u></u>	· · · · · · · · · · · · · · · · · · ·			•	
fsw			500		kHz
-3 W	1	1	200	1	
D			20		0
R _{NFET_M}			30		mΩ
R _{NFET_R}			55		mΩ
R _{NFET_B}			45		mΩ
		-			
V _{BAT_REG}	1-cell battery, V _{CV} <0.4V	4.179	4.2	4.221	
	1-cell battery, V _{CV} >1.5V	4.328	4.35	4.371	V
	2-cell battery, V _{CV} <0.4V	8.358	8.4	8.442	v
	2-cell battery, V _{CV} >1.5V	8.656	8.7	8.744	
437	1-cell battery	50	100	150	V
$\Delta \mathbf{v}_{\text{RCH}}$	2-cell battery	100	200	300	mV
	1-cell battery	2.7	2.8	2.9	17
V TRK	2-cell battery	5.4	5.6	5.8	V
Modify			•		
V _{NTC}	NTC falling edge	0.4			V
	Low gulas width		100		-
LDET	Low pulse width		100		ms
T	I = -25 m W/P	100/		100/	
ICC	$I_{CC} = 25 \text{ mV/K}_{S}$	-10%		10%	
T	L 25mV/D	500/		500/	
ITC	$I_{TC}=2.3IIIV/K_S$	-30%		30%	
I _{TERM}	$I_{\text{TERM}} = 2.5 \text{mV}/\text{R}_{\text{S}}$	-50%		50%	
V _{O_OVP}		105%	110%	115%	V_{BAT_REG}
eference					
		1 1 4	1 10	1.00	17
V _{SEN}		1.10	1.19	1.22	V
ΔV_{AICL}	NTC pull low than 100ms		600		mV
	V_{IN} V_{UVLO} ΔV_{UVLO} ΔV_{IN_OVP} ΔV_{OVP} I_{BAT} I_{IN} f_{SW} R_{NFET_A} R_{NFET_A} R_{NFET_B} V_{BAT_REG} ΔV_{RCH} V_{TRK} V_{TRK} $Modify$ V_{NTC} I_{DET} I_{CC} I_{TC} I_{TERM}	VIN VIN V_{UVLO} V_{IN} rising and measured from IN to ground ΔV_{UVLO} Measured from IN to ground ΔV_{IN_OVP} V_{IN} rising and measured from IN to ground ΔV_{OVP} Measured from IN to ground ΔV_{OVP} Measured from IN to ground ΔV_{OVP} Measured from IN to ground I_{BAT} V_{IN} absent or EN=Low I_{IN} Disable charge f_{SW} Image: State in the imag	$\begin{array}{c c c c c c c } V_{IN} & & & & & & & & & & & & & & & & & & &$	$\begin{tabular}{ c c c c c } \hline V_{\rm IN} & & & & & & & & & & & & & & & & & & &$	$\begin{array}{c c c c c c c c c c c c c c c c c c c $

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Timer						
Trickle Current Charge	4		0.26	0.5	0.64	1
Timeout	t _{TC}		0.36	0.5	0.64	hour
Constant Current Charge	t		3.5	4.5	5.5	hour
Timeout	t _{CC}		5.5	4.5	5.5	noui
Charge Mode Change Delay	t			30		ms
Time	t _{MC}			50		1115
Termination Delay Time	t _{TERM}			30		ms
Recharge Time Delay	t _{RCHG}			30		ms
Short Circuit Protection					-	
Output Short Protection	V _{SHORT}		1.7	2.00	2.3	v
Threshold, Falling Edge	* SHORT		1.7	2.00	2.5	v
Auto Shut Down					-	
Auto Shutdown Voltage	V _{ASD}	V_{IN} fall, measured from IN to	40	110	180	
Threshold	• ASD	BAT	40	110		mV
Auto Shutdown Voltage	ΔV_{ASD}	V_{IN} rise, measured from IN to		65		111 V
Threshold Hysteresis	A V ASD	BAT		05		
Logical Control	•					
High Level Logic for Enable	V _{ENH}		1.5			v
Control	▼ ENH		1.5			•
Low Level Logic for Enable	V _{ENL}				0.4	v
Control					0.1	•
High Level Logic for CV	V _{CVH}		1.5			V
Low Level Logic for CV	V _{CVL}				0.4	V
Battery Thermal Protection N	TC	1	1	1		
Under Temperature Protection	V _{NTC_UTP}		74%	75%	76%	
Under Temperature Protection	V	C UTP HYS Falling edge		5%		
Hysteresis	V _{NTC_UTP_HYS}	Failing edge		5%		V _{IN}
Over Temperature Protection	V _{NTC_OTP}		44%	45%	46%	V IN
Over Temperature Protection	17	D' 1		1.50/		
Hysteresis	V _{NTC_OTP_HYS}	Rising edge		1.5%		
Thermal Fold-back and Therm	al Shutdown					
Thermal Fold-back Threshold	T _{Fold}			120		°C
Thermal Fold-back Hysteresis				20		°C
Falling Edge	T _{FoldHYS}			20		÷C
Thermal Fold-back Ratio	I _{Fold}			0.25		I _{CC}
Thermal Shutdown		Rising threshold		160		°C
Temperature				160		Ē
Thermal Shutdown	т			30		°C
Temperature Hysteresis	T _{SDHYS}			50		C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}C$ on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.



Typical Performance Characteristics

 $(T_A=25^{\circ}C, V_{IN}=5V, V_{BAT}=3.6V \text{ for single-cell battery application. } V_{IN}=9V, V_{BAT}=7.6V \text{ for two-cell battery application. } R_s=10m\Omega, C_{TIM}=330nf, unless otherwise specified.)}$

















Time (100ms/div)







Adaptive Input Power Limit Reference Refresh (Input Adapter changes to 7V/1A V_{BAT}=3.6V) CH1: V_{IN} CH2:V_{NTC} CH3: V_{BAT} CH4:I_{BAT}





General Function Description

SY6924 is a 4V-14V input, 2.5A step-down multicell Li-Ion battery charger, which integrates reverse blocking FET, 500 kHz synchronous buck and full protection functions. The charge current up to 2.5A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timeout and adaptive input power limit for safety battery charge operation. It consists of 16V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

STAT is an open drain pin and a pull up resistor is needed for charging status indication. Connect a LED from IN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3Hz means Fault Mode.

- 1. Charge-In-Process Pull and keep STAT pin to Low;
- 2. Charge Done Pull and keep STAT pin to High;
- **3.** Fault Mode Output high and low voltage alternatively with 1.3Hz frequency. The faults include input OVP, BAT OVP, BAT short, BAT UTP, BAT OTP, time-out and thermal shutdown.

Switching Mode Buck Charger Basic Operation Description

Switching Mode Control Strategy

SY6924 utilizes quasi-fixed frequency control to simplify the internal close-loop compensation design. The quasi-fixed frequency settled at 500 kHz is easy for the size minimization of peripheral circuit design. During the light load operation, the OFF time of the main switch is going to be stretched to achieve frequency fold back.

Operation Principle

SY6924 works as a synchronous Buck mode battery charger when the adapter is present. It utilizes 500 kHz switching frequency to minimize the PCB design.

The charger will operate in battery short mode, trickle charge mode, constant current charge mode and constant voltage charge mode according to the battery voltage. The charge current in every mode is showed in following charge curve. In constant voltage mode, if charge current is lower than termination current, the charger will stop charging until battery voltage drops to recharge voltage.



Basic Adaptive Input Power Limit Principle

SY6924 can limit the input power adaptively and adjust this threshold according the input voltage. It will automatically decrease charge current when IN voltage drops to adaptive input power limit reference V_{REF} .

For typical 5V adapter, V_{REF} is set by VSEN pin, that is calculated as :

$$V_{\text{REF}} = 1.19 \times \frac{R_{\text{UP}} + R_{\text{DN}}}{R_{\text{DN}}}$$

If IN voltage is higher than 6V, V_{REF} is calculated as:

$$V_{REF} = V_{IN} - \Delta V_{AICL}$$

Where, ΔV_{AICL} is 0.6V typically.

 V_{IN} is the input voltage when adapter insert. V_{REF} can be modified after a more than 100ms low pulse on NTC pin if the adapter is always present.

When NTC is pulled low, the charge current is set to the trickle value; battery thermal protection and adaptive input power limit function are disabled.

Full Charger Protections Description

In charge mode, SY6924 has full protection to protect the IC and the battery.

Input Over Voltage Protection – SY6924 has IN over voltage protection. It will turn off switching charger when input OVP occurs. IC will auto recover normal operation when fault removes.

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<u>BAT Over Voltage Protection</u> – SY6924 will stop charging when BAT OVP occurs. The IC will auto recover normal operation when fault removes.

<u>**Timeout Protection**</u> – The charger can detect a bad battery. It will stop charge and latch off when the charger works over safety time which is set by C_{TIM} . Only recycling the input can release this fault.

Battery Thermal Protection – When NTC voltage is lower than OTP threshold and higher than 0.4V or higher than UTP threshold, the converter will stop switching. IC will auto recovery when fault removes.

Thermal Shutdown Protection – The IC will stop operation when the junction temperature is higher than 160°C. It will auto recover normal when fault removes.

Applications Information

Because of the high integration of SY6924, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{BD} , output capacitor C_{OUT} , inductor L, NTC resistors R1, R2, charging current sense resistor Rs and timer capacitor C_{TIM} need to be selected for the targeted applications specifications.

NTC Resistor:

SY6924 monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the ratio K (K= $V_{\rm NTC}/V_{\rm IN}$) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps are:

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- 1. Define K_{UT} , $K_{UT} = 74 \sim 76\%$
- 2. Define K_{OT} , $K_{OT} = 44 \sim 46\%$
- 3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
- 4. Calculate R2, $R2=\frac{Kot(1-Kut)Rut-Kut(1-Kot)Rot}{Kut-Kot}$ 5. Calculate R1

 $R1 = (1/K_{\text{OT}}-1)(R2+R_{\text{OT}})$

If choose the typical values $K_{\rm UT}$ =75% and $K_{\rm OT}{=}45\%,$ then

R2=0.375Rut-1.375Rot R1=1.222(R2+Rot)

SY6924 accepts flexible NTC divider circuits. For below method, R1 and R2 can be calculated by below equations.



$$R1 = \frac{R2 \times R_{UT} \times (1-K_{UT})}{K_{UT} \times (R2+R_{UT})}$$

If choose the typical values K_{UT} =75% and $K_{\text{OT}}\text{=}45\%,$ then

$$R2=\frac{0.3Rut \times Rot}{0.1125 \times Rut-0.4125 \times Rot}$$
$$R1=\frac{R2 \times Rut}{3(Rut+R2)}$$

Charging Current Sense Resistor Rs

The charging current sense resistor R_S is calculated as below:

$$R_s = \frac{25mV}{I_{cc}}$$
, Unit: m Ω

Where the I_{CC} is the battery constant charging current, unit: A.

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Timer Capacitor CTIM

The charger also provides a programmable charging timer. The charging time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

 $\begin{array}{ll} C_{\text{TIM}}{=}2{\times}10^{{\cdot}11}\,\text{S}{\times}\text{T}_{\text{CC}}, & \text{Unit: F} \\ T_{\text{CC}} \text{ is the permitted fast charging time, unit: s.} \end{array}$

Input Capacitor CBD

The ripple current through input capacitor is greater than

$$I_{C_{BD}-MIN} = I_{CC} \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X7R or a better grade ceramic capacitor really close to the BD and GND pins. Care should be taken to minimize the loop area formed by C_{BD} , and BD/GND pins.

Output Capacitor Cout

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor with 10μ F capacitance.

Output Inductor L

There are several considerations in choosing this inductor.

 Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average charge current. The inductance is calculated as:

$$L = \frac{V_{\text{OUT}} \times (1 - V_{\text{OUT}} / V_{\text{IN,MAX}})}{F_{\text{SW}} \times I_{\text{OUT,MAX}} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{\text{OUT},\text{MAX}}$ is the maximum load current.

SY6924 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

Isat,min>Iout,max+
$$\frac{V_{OUT} \times (1-V_{OUT}/V_{IN, MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to

achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<20m Ω to achieve a good overall efficiency. SY6924 is a high integrated charger and the internal compensation circuits also limit the inductor choice. Out of the range from 0.68 μ H to 3.3 μ H is not suggested. The 2.2 μ H inductor can almost cover the

Layout Design

normal applications.

The layout design of SY6924 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{BD} , L.

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) C_{BD} must be close to pins BD and GND. The loop area formed by C_{BD} and GND must be minimized. Following picture is the recommended layout design of C_{BD} .



- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The capacitor C_{TIM} and the trace connecting to the TIM pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 5) The current sense resistor should be adjacent to the junction of the inductor and output capacitor. The routes from the sense leads on the sense resistor to the IC pins should be close to each other to minimize loop area. Please don't route the sense leads through a high current path. Following picture is the recommended layout design.





Figure2. PCB Layout Suggestion















1. Taping orientation





2. Carrier Tape & Reel specification for packages



Package type	Tape width	Pocket	Reel size	Trailer	Leader length	Qty per
	(mm)	pitch(mm)	(Inch)	length(mm)	(mm)	reel
QFN3x3	12	8	13''	400	400	5000

3. Others: NA



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