BL702/704/706

Datasheet

Version：2.1

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Features

- **Wireless**
  - 2.4 GHz RF transceiver
  - Bluetooth® Specification v5.0
  - Bluetooth® Low Energy 1Mbps and 2Mbps
  - Bluetooth® Long Range Coded 500Kbps and 125Kbps
  - Zigbee 3.0, Base Device Behavior, Core Stack R21, Green Power
  - IEEE 802.15.4 MAC/PHY
  - Support BLE/zigbee coexistence
  - Integrated balun, PA/LNA
- **MCU Subsystem**
  - 32-bit RISC CPU with FPU
  - Level-1 cache
  - One RTC timer update to one year
  - Two 32-bit general purpose timers
  - Eight DMA channels
  - CPU frequency configurable from 1MHz to 144MHz
  - JTAG development support
  - XIP QSPI Flash/pSRAM with hardware encryption support
- **Memory**
  - 132KB RAM
  - 192KB ROM
  - 1Kb eFuse
  - Embedded Flash (optional)
  - Embedded pSRAM (BL704/BL706,optional)
- **Security**
  - Secure boot
  - Secure debug ports
  - QSPI Flash On-The-Fly AES Decryption (OTFAD) - AES-128, CTR+ mode
  - Support AES 128/192/256 bits
  - Support MD5, SHA-1/224/256/384/512
  - Support TRNG (True Random Number Generator)
  - Support PKA (Public Key Accelerator)
- **Peripheral**
  - USB2.0 FS (Full-Speed) device interface
  - IR remote control interface
  - One SPI master/slave
  - Two UARTs
    Support ISO 17987(Local Interconnect Network)
  - One I2C master
  - One I2S master/slave
  - Five PWM channels
  - Quadrature decoder
  - Key-Scan-Matrix interface
  - 12-bit general ADC
  - 10-bit general DAC
  - PIR (Passive Infra-Red) detection
  - Ethernet RMII interface(BL704/BL706)
  - Camera interface(BL706)

  - 15(BL702)/23(BL704)/31(BL706) Flexible GPIOs (flexible)

- **Power Management**
  - Active CPU
  - Idle
  - Power Down Sleep (flexible)
  - Hibernate
  - Off
  - Active Rx
  - Active Tx

- **Clock**
  - External main clock XTAL 32MHz
  - External low power consumption and the RTC clock XTAL 32/32.768kHz
  - Internal RC 32kHz oscillator
  - Internal RC 32MHz oscillator
  - Internal System PLL
  - Internal Audio PLL

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1 Overview

BL702/BL704/BL706 is highly integrated BLE and zigbee combo chipsets for IoT applications.

Wireless subsystem contains 2.4G radio, BLE+zigbee baseband and MAC designs. Microcontroller subsystem contains 32-bit RISC CPU, high-speed cache and memories. Power Management Unit controls ultra-low-power modes. Moreover, variety of security features are supported.

Peripheral interfaces include USB2.0, Ethernet(BL704/BL706), IR-remote, SPI, UART, ISO 17987, I2C, I2S, PWM, QDEC, KeyScan, ADC, DAC, PIR, Camera(BL706), and GPIOs.

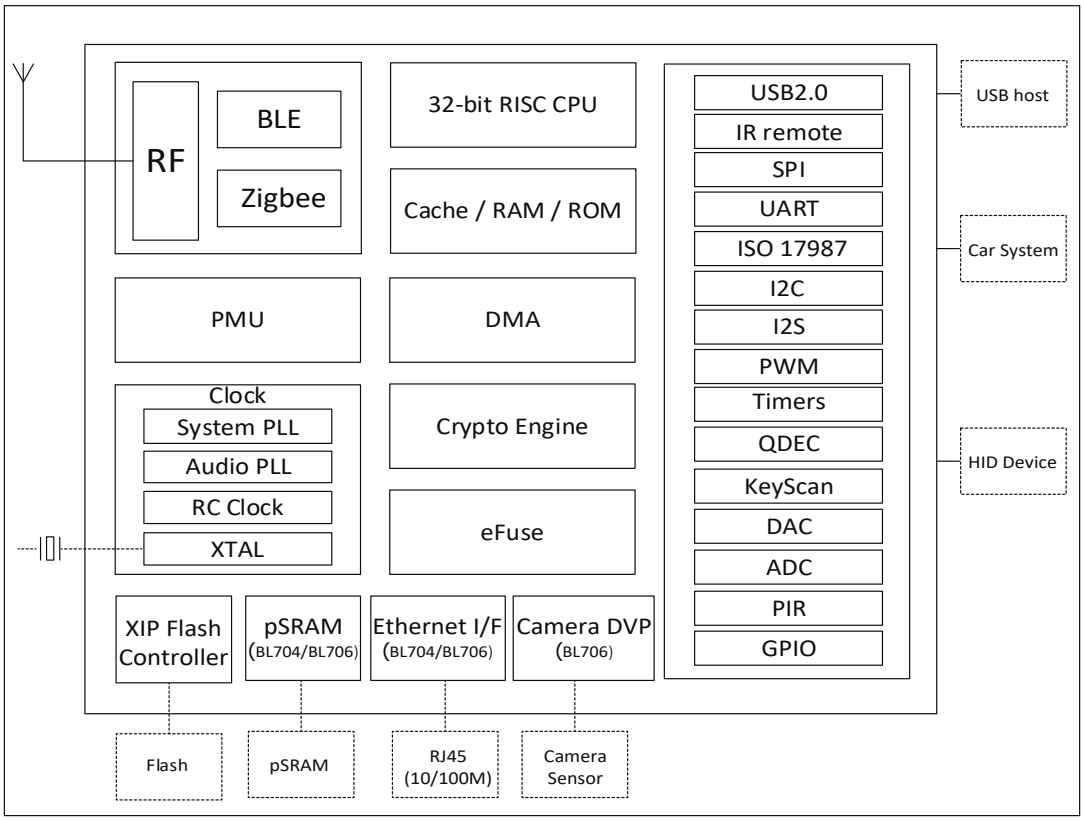

Fig. 1.1: Block Diagram

2 Functional Description

BL702/BL704/BL706 main functions described as follows：

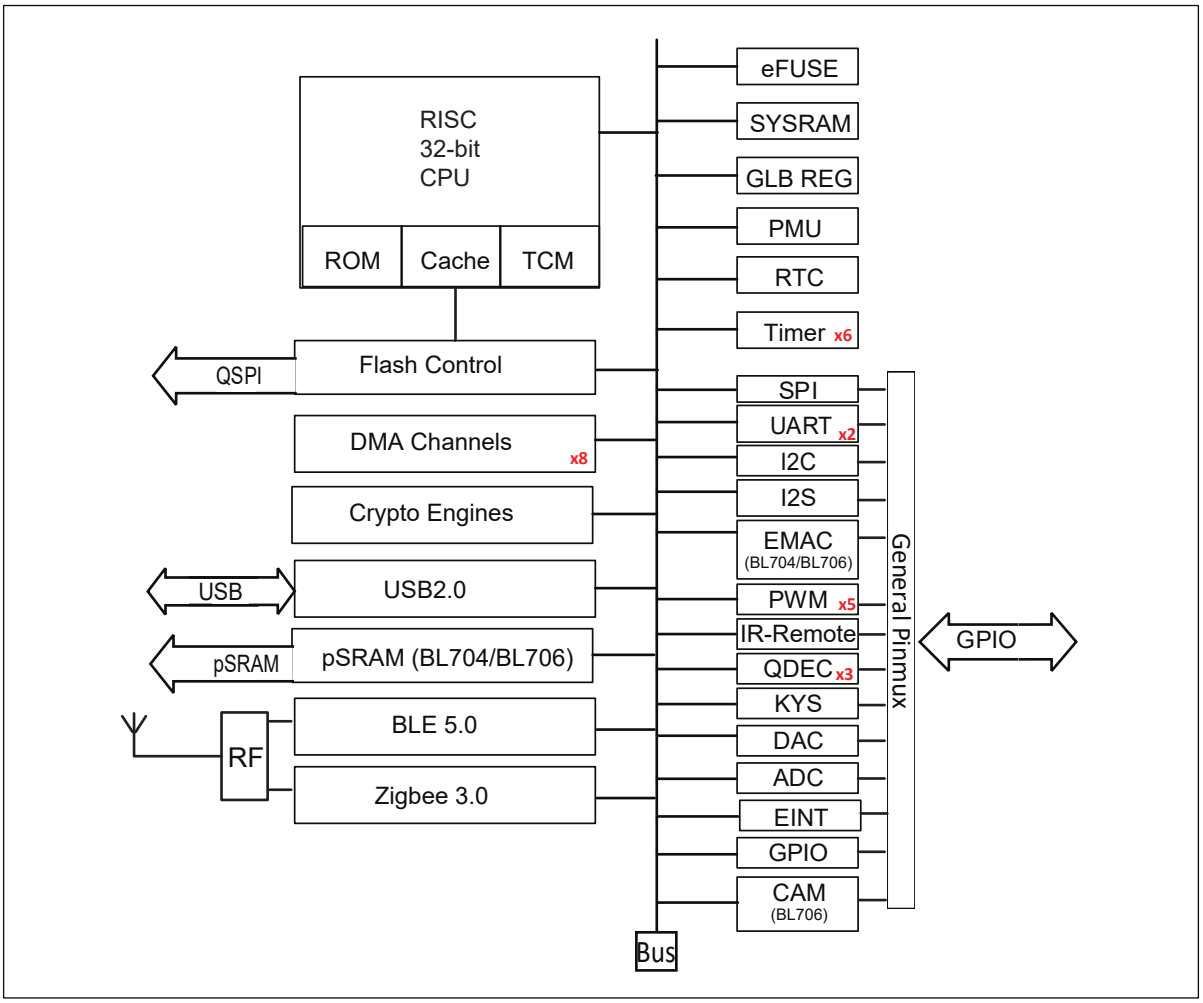

Fig. 2.1: System Architecture

2.1 CPU

BL702/BL704/BL706 32-bit RISC CPU contains FPU (floating-point unit) for 32-bit single-precision arithmetic, three-stage pipelined (IF, EXE, WB), compressed 16 and 32-bit instruction set, standard JTAG debugger port including 4 hardware-programmable breakpoints, interrupt controller including 64 interrupts and 16 interrupt levels/priorities for low latency interrupt processing. Up to 144MHz clock frequency, can be dynamically configured to change clock frequency, enter the power saving mode to achieve low power consumption.

Both zigBee/BLE stack and application run on single 32-bit RISC CPU for simple and ultra-low power applications. CPU performance ~1.46 DMIPS/MHz. ~3.1 CoreMark/MHz.

2.2 Cache

BL702/BL704/BL706 cache improves CPU performance to access external memory. Cache memories can be partially or fully configured as TCM (tightly coupled memory).

2.3 Memory

BL702/BL704/BL706 memories include: on-chip zero-delay SRAM memories, read-only memories, write-once memories, embedded flash memory (optional), embedded pSRAM (BL704/BL706,optional).

2.4 DMA

BL702/BL704/BL706 DMA (direct memory access) controller has eight dedicated channels that manage data transfer between peripherals and memories to improve cpu/bus efficiency.

There are four main types of transfers including memory to memory, memory to peripheral, peripheral to peripheral and peripheral to memory. DMA also supports LLI (link list item) that multiple transfers are pre-defined by a series of linked lists, then hardware automatically complete all transfers according to each LLI size and address. DMA supports peripheral USB, UART, I2C, I2S, SPI, ADC and DAC.

2.5 Bus

BL702/BL704/BL706 bus fabric connection and memory-map summarized as follows：

Table 2.1: Bus Connectiom

Slave/ Master	CPU	Ethernet	DMA	Crypto Engine	Debug
SRAM	V	V	V	V	V
Peripheral	V	-	V	-	V
BLE/zigbee	V	-	V	-	V

Table 2.2: Memory Map

Module	Base Address	Size	Description
RETRAM	0x40010000	4KB	Deep sleep memory (Retention RAM)
HBN	0x4000F000	4KB	Deep sleep control (Hibernate)
PDS	0x4000E000	4KB	Sleep control (Power Down Sleep)
USB	0x4000D800	1KB	USB control
EMAC	0x4000D000	2KB	Ethernet MAC control (BL704/BL706)
DMA	0x4000C000	4KB	DMA control
QSPI	0x4000B000	4KB	Flash/pSRAM QSPI control
CAM	0x4000AD00	256B	CAM control (BL706)
I2S	0x4000AA00	256B	I2S control
KYS	0x4000A900	256B	Key-Scan control
QDEC2	0x4000A880	64B	Quadrature decoder control
QDEC1	0x4000A840	64B	Quadrature decoder control
QDEC0	0x4000A800	64B	Quadrature decoder control
IRR	0x4000A600	256B	IR Remote control
TIMER	0x4000A500	256B	Timer control
PWM	0x4000A400	256B	Pulse Width Modulation *5 control
I2C	0x4000A300	256B	I2C control
SPI	0x4000A200	256B	SPI master/slave control
UART1	0x4000A100	256B	UART control (support ISO 17987)
UART0	0x4000A000	256B	UART control (support ISO 17987)
L1C	0x40009000	4KB	Cache control
eFuse	0x40007000	4KB	eFuse memory control
SEC	0x40004000	4KB	Security engine
GPIP	0x40002000	4KB	General purpose DAC/ADC/ACOMP interface control
MIX	0x40001000	4KB	Mixed signal register
GLB	0x40000000	4KB	Global control register
pSRAM	0x24000000	8MB	pSRAM memory
XIP	0x23000000	8MB	XIP Flash memory
OCRAM	0x22020000	64KB	On-chip memory
DTCM	0x22014000	48KB	Data cache memory
ITCM	0x22010000	16KB	Instruction cache memory

Table 2.2: Memory Map

Module	Base Address	Size	Description
ROM	0x21000000	192KB	Read-only memory

2.6 Interrupt

BL702/BL704/BL706 supports internal RTC wake-up and external GPIO interrupts wake-up.

The CPU interrupt controller supports a total of 64 maskable interrupt trigger sources including UART interrupt, I2C interrupt, SPI interrupt, timer interrupt, DMA interrupt, etc. All I/O pins can be configured as external interrupt input mode. The external interrupt supports four trigger types: high level trigger, low level trigger, rising edge trigger and falling edge trigger.

2.7 Boot

BL702/BL704/BL706 supports multiple boot options: UART, USB, and Flash.

2.8 Power

PMU (power management unit) manages the power of the entire chip and is divided into running, idle, sleep, hibernation and power off modes. The software can be configured to enter sleep mode and wake-up via RTC timer or EINT to achieve low-power sleep and accurate wake-up management.

Power down sleep modes are flexible for applications to configure as the lowest power consumption.

2.9 Clock

Clock control unit generates clocks to the core MCU and the peripheral SOC devices. The root clock source can be XTAL, PLL or RC oscillator. Dynamic power-saved by proper configurations such as sel, div, en, etc. PMU runs at 32KHz clock to keep system low-power in sleep mode.

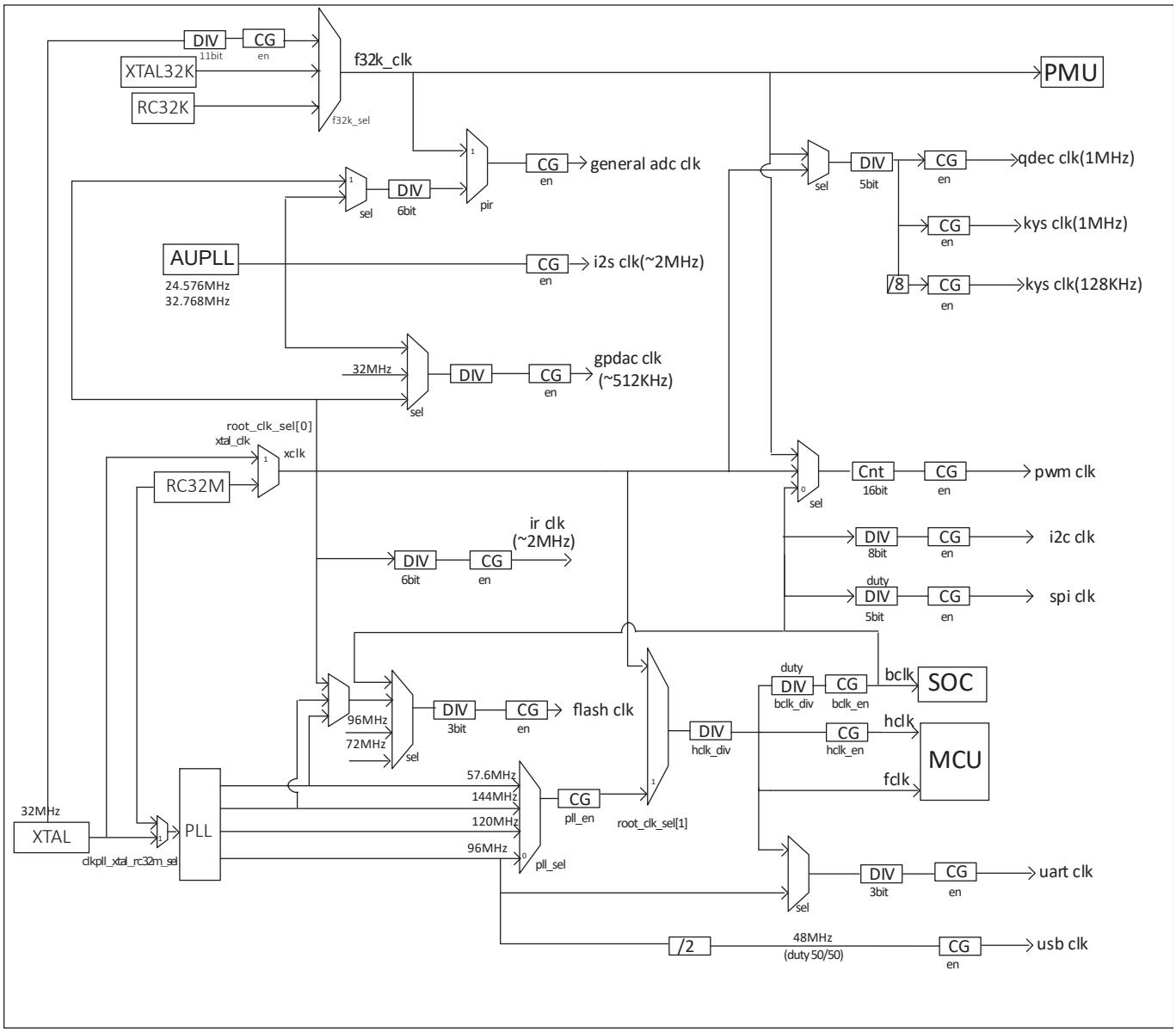

Fig. 2.2: Clock Architecture

2.10 Peripherals

Peripherals include USB2.0, Ethernet, IR-remote, SPI, UART, ISO 17987, I2C, I2S, PWM, QDEC, KeyScan, ADC, DAC, PIR, Camera. Each peripheral can be assigned to different groups of GPIOs through flexible configurations. Each GPIO can be used as a general-purpose input and output function.

2.10.1 GPIO

BL702 includes 15 GPIOs, BL704 includes 23 GPIOs, BL706 includes 31 GPIOs, and each GPIO can be used as a general-purpose input and output function. The pull-up/pull-down/floating can be configured by software. Each GPIO supports interrupt function, interrupt supports rising edge trigger, falling edge trigger, high level trigger and low level trigger.

Each GPIO can be set to a high impedance state for power saving in low power consumption mode.

2.10.2 UART

Built-in 2 UARTs (UART0 and UART1), and support LIN master/slave function. The working clock of the UART module can be selected as FCLK or 96M, and the maximum baud rate is 8M. Support hardware CTS and RTS signal management. TX and RX have independent FIFOs with a FIFO depth of 128 bytes and support DMA functions.

2.10.3 SPI

One SPI interface, which can be configured as master mode or slave mode, and the SPI module clock is BCLK. As a master, the maximum SPI Clock can reach 36MHz. As a slave, the maximum SPI Clcok of the master is 24MHz. The bit width of each frame can be configured as 8 bits/16 bits/24 bits/32 bits.

The transmission and reception of SPI has independent FIFO, and the FIFO depth is fixed to 4 frames (that is, if the bit width of the frame is 8 bits, the depth of the FIFO is 4 bytes), and the DMA function is supported.

2.10.4 I2C

One I2C interface, support host mode and 7 bit addressing, I2C module clock is BCLK, support standard and fast mode. With device address register, register address register, the length of the register address can be configured as 1 byte/2 bytes/3 bytes/4 bytes.

The I2C transceiver has an independent FIFO, the FIFO depth is 2 words, and it supports DMA function.

2.10.5 I2S

One I2S interface, support Left-justified/Right-justified/DSP and other data formats, support 8/16/24/32 bit data width, in addition to mono/dual-channel mode, support four-channel mode at the same time.

The I2S transceiver has an independent FIFO, and the FIFO depth is 16 frames. When the data width is 16 bits, the FIFO depth can be set to 32 frames. The I2S module has an independent Audio PLL, and supports two types of sampling rates of 48K (and its integer frequency division) and 44.1K (and its integer frequency division).

2.10.6 TIMER

The TIMER module contains two general-purpose timers and a watchdog timer. The clock source of the general-purpose timer can be FCLK/32K/1K/XTAL, and the clock source of the watchdog timer can be FCLK/32K/XTAL. Each The counter has an 8-bit frequency divider.

Each group of general-purpose timers contains three compare registers, supports compare interrupts, and count mode supports FreeRun mode and PreLoad mode.

The bit width of the watchdog timer counter is 16 bits, and it supports two watchdog overflow modes: interrupt and reset.

2.10.7 PWM

5-channel PWM interface, three kinds of clock sources BCLK/XCLK/32K can be selected, the bit width of the frequency divider register is 16 bits, and the bit width of the period register is 16 bits. Supports adjustable output polarity and dual threshold settings to increase the flexibility of pulse output. Support PWM cycle counting interrupt, used to count the number of output pulses, etc.

2.10.8 IR(IR-remote)

One infrared remote control, supports two modes of generating and receiving, supports receiving data with fixed protocols NEC and RC-5, and also supports receiving data in any format in pulse width counting mode.

The IR module clock source is XCLK, which has powerful infrared waveform editing capabilities and can send out waveforms that conform to various protocols. The transmit power is adjustable in 15 levels, and the receive FIFO depth can reach 64 bytes.

2.10.9 USB2.0(Full Speed)

Built-in a device controller compatible with full-speed USB, following the full-speed USB device standard, with 8 endpoints, each of which has a 64-byte deep FIFO, except for endpoint 0, all other endpoints support interrupt /batch /synchronous transmission . With standby /resume function. The 48MHz clock dedicated to USB is directly generated by the internal main PLL.

2.10.10 EMAC

EMAC is a 10/100Mbps Ethernet controller (Ethernet Media Access Controller) compatible with IEEE 802.3.

Compatible with the MAC layer functions defined by IEEE 802.3, support the PHY of the RMII interface defined by IEEE 802.3, interact with the PHY through MDIO, support 10Mbps and 100Mbps Ethernet, support half-duplex and full-duplex, data transmission and reception are realized through the Buffer Descriptor data structure .

EMAC control is embedded with AHB Master, which can read or write data directly from the memory. The Buffer Descriptor data structure is stored in the internal RAM of EMAC. The total number of Buffer Descriptors is up to 128. The user can flexibly configure the number of Buffer Descriptors for transmission and receiving according to the scene.

2.10.11 QDEC

The chip has built-in three sets of quadrature decoders, which are used to decode the two sets of pulses with a phase difference of 90 degrees generated by the dual-channel rotary encoder into the corresponding speed and rotation. Direction.

QDEC clock source can be 32K (f32k_clk) or 32M (xclk), with 16-bit pulse count range (-32768~32767 pulse/sample), with 12 configurable sample periods (32us~131ms per sample at 1MHz)), with a 16-bit settable report period (0~65535 ample/report).

2.10.12 ADC

The chip has a built-in 12bits successive approximation analog-to-digital converter (ADC) with a maximum working clock of 2MHz, supports 12 external analog inputs and several internal analog signal selections, and supports single-channel conversion and multi-channel scanning modes.

ADC can work in two modes of single conversion and multi-channel scanning. It supports 2.0V, 3.2V optional internal reference voltage, and the conversion result is 12/14/16bits (achieved by oversampling) left-justified mode.

The ADC has a FIFO with a depth of 32, supports a variety of interrupts, and supports DMA operations.

In addition to measuring common analog signals, ADC can also be used to measure power supply voltage. In addition, ADC can also be used for temperature detection by measuring internal/external diode voltage.

2.10.13 DAC

The chip has a built-in 10bits digital-to-analog converter (DAC) with a FIFO depth of 1 word and supports 2 DAC modulation outputs. Can be used for audio playback, conventional analog signal modulation, DAC input clock can be selected as 32M or Audio PLL, support DMA to transfer memory to the DAC modulation register, DAC output pin is fixed to ChannelA to GPIO11, ChannelB to GPIO17.

2.10.14 Debug interface

Support standard JTAG 4-wire debugging interface, and use debuggers such as Jlink/OpenOCD/CK Link for debugging.

3 Pin Definition

BL702 32-pin package includes 11 power pins, 6 analog pins, and 15 flexible GPIO pins.

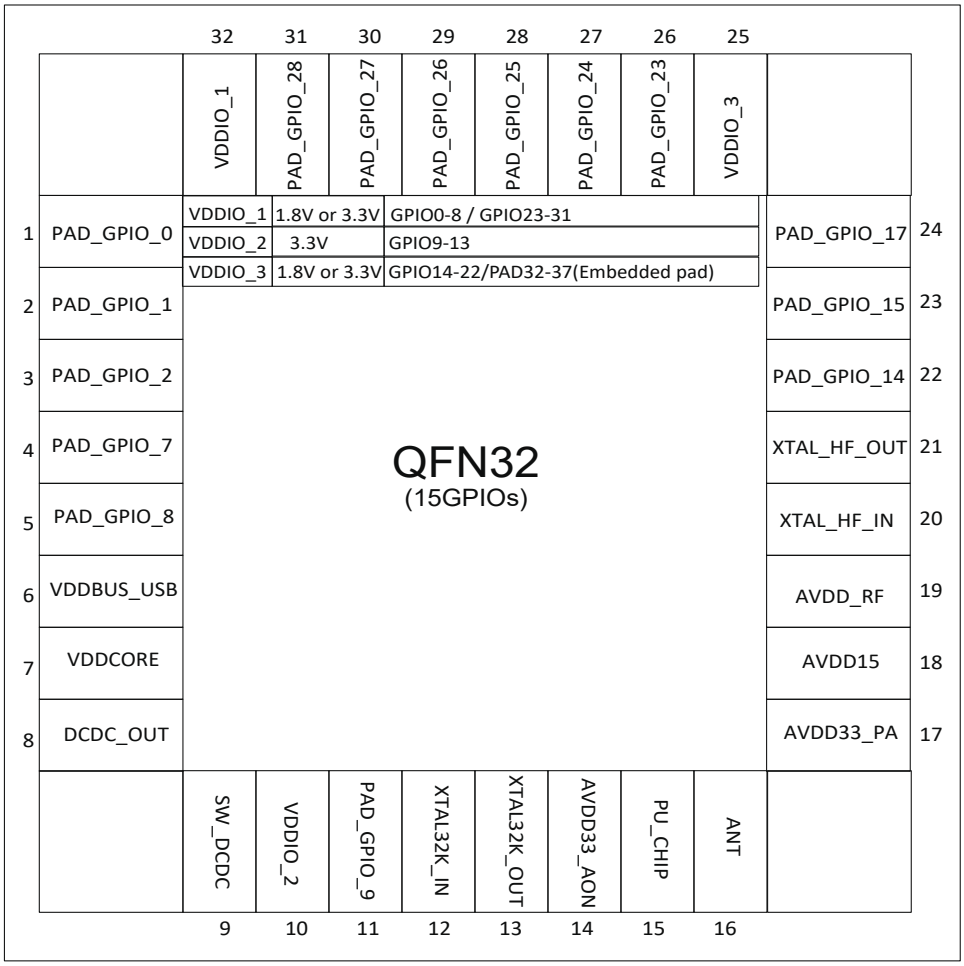

Fig. 3.1: Pin layout (QFN32)

BL704 40-pin package includes 11 power pins, 6 analog pins, and 23 flexible GPIO pins.

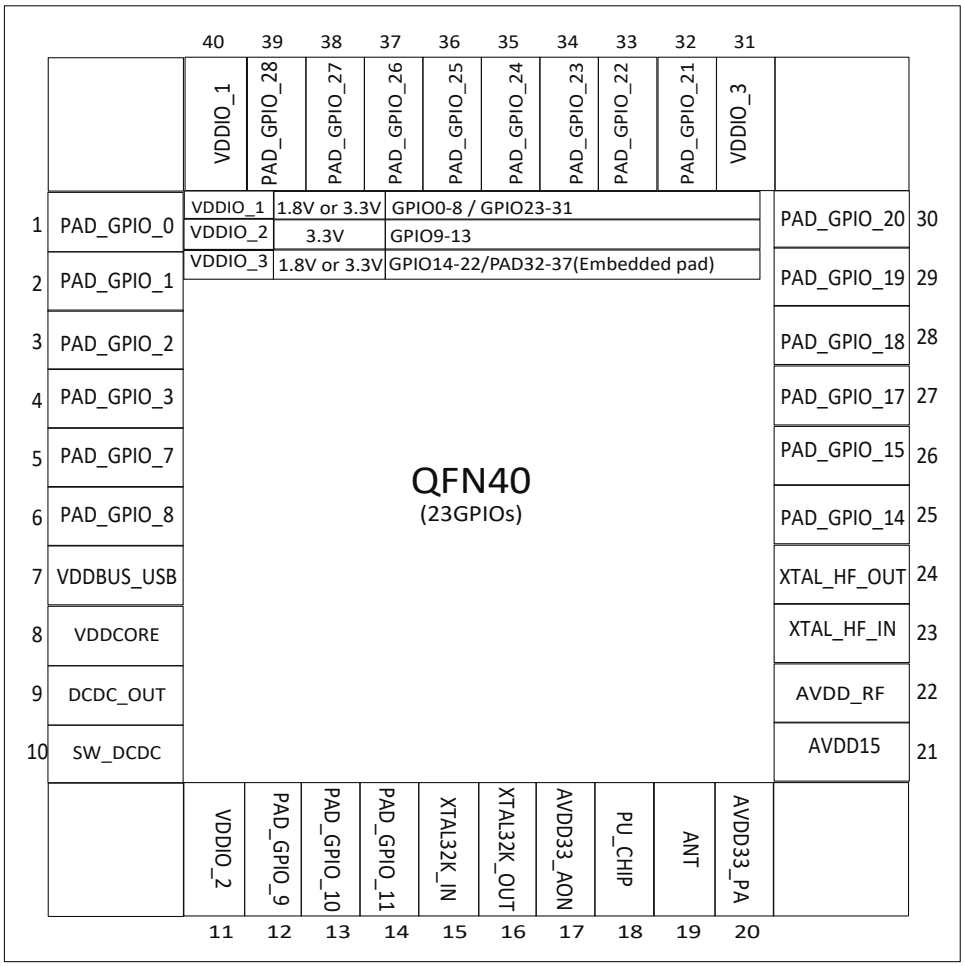

Fig. 3.2: Pin layout (QFN40)

BL706 48-pin package includes 11 power pins, 6 analog pins, and 31 flexible GPIO pins.

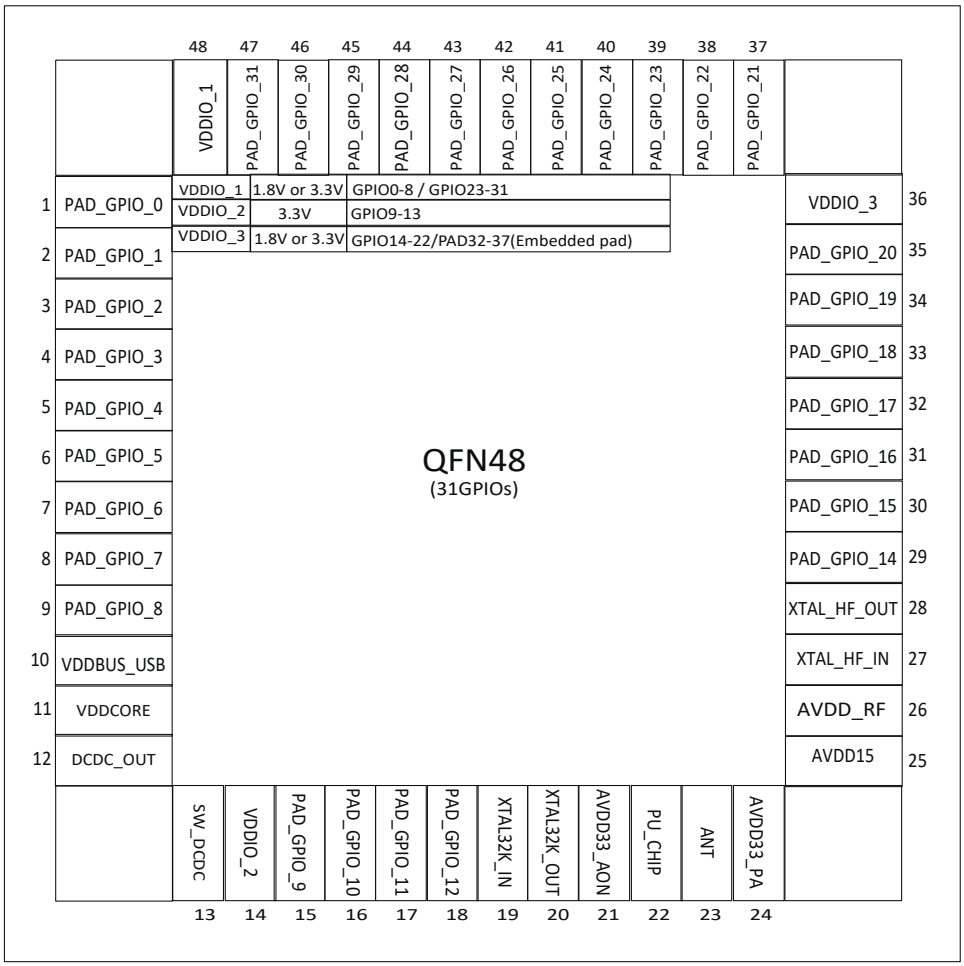

Fig. 3.3: Pin layout (QFN48)

Table 3.1: Pin description

No	Voltage Domain	BL702	BL704	BL706	I/O Type	Pin Name	Description
1	VDDIO_1	1	1	1	DI/DO	PAD_GPIO_0	-
2	VDDIO_1	2	2	2	DI/DO	PAD_GPIO_1	-
3	VDDIO_1	3	3	3	DI/DO	PAD_GPIO_2	-
4	VDDIO_1	-	4	4	DI/DO	PAD_GPIO_3	-
5	VDDIO_1	-	-	5	DI/DO	PAD_GPIO_4	-
6	VDDIO_1	-	-	6	DI/DO	PAD_GPIO_5	-
7	VDDIO_1	-	-	7	DI/DO	PAD_GPIO_6	-
8	VDDIO_1	4	5	8	DI/DO	PAD_GPIO_7	-
9	VDDIO_1	5	6	9	DI/DO	PAD_GPIO_8	-
10	VDDIO_2	11	12	15	DI/DO	PAD_GPIO_9	-
11	VDDIO_2	-	13	16	DI/DO	PAD_GPIO_10	-
12	VDDIO_2	-	14	17	DI/DO	PAD_GPIO_11	-
13	VDDIO_2	-	-	18	DI/DO	PAD_GPIO_12	-

Table 3.1: Pin description

No	Voltage Domain	BL702	BL704	BL706	I/O Type	Pin Name	Description
14	VDDIO_3	22	25	29	DI/DO	PAD_GPIO_14	-
15	VDDIO_3	23	26	30	DI/DO	PAD_GPIO_15	-
16	VDDIO_3	-	-	31	DI/DO	PAD_GPIO_16	-
17	VDDIO_3	24	27	32	DI/DO	PAD_GPIO_17	-
18	VDDIO_3	-	28	33	DI/DO	PAD_GPIO_18	-
19	VDDIO_3	-	29	34	DI/DO	PAD_GPIO_19	-
20	VDDIO_3	-	30	35	DI/DO	PAD_GPIO_20	-
21	VDDIO_3	-	32	37	DI/DO	PAD_GPIO_21	-
22	VDDIO_3	-	33	38	DI/DO	PAD_GPIO_22	-
23	VDDIO_1	26	34	39	DI/DO	PAD_GPIO_23	-
24	VDDIO_1	27	35	40	DI/DO	PAD_GPIO_24	-
25	VDDIO_1	28	36	41	DI/DO	PAD_GPIO_25	-
26	VDDIO_1	29	37	42	DI/DO	PAD_GPIO_26	-
27	VDDIO_1	30	38	43	DI/DO	PAD_GPIO_27	-
28	VDDIO_1	31	39	44	DI/DO	PAD_GPIO_28	-
29	VDDIO_1	-	-	45	DI/DO	PAD_GPIO_29	-
30	VDDIO_1	-	-	46	DI/DO	PAD_GPIO_30	-
31	VDDIO_1	-	-	47	DI/DO	PAD_GPIO_31	-
32	VDDIO_3	-	-	-	DI/DO	PAD_32	Embedded pad for embedded psram or flash
33	VDDIO_3	-	-	-	DI/DO	PAD_33	Embedded pad for embedded psram or flash
34	VDDIO_3	-	-	-	DI/DO	PAD_34	Embedded pad for embedded psram or flash
35	VDDIO_3	-	-	-	DI/DO	PAD_35	Embedded pad for embedded psram or flash
36	VDDIO_3	-	-	-	DI/DO	PAD_36	Embedded pad for embedded psram or flash
37	VDDIO_3	-	-	-	DI/DO	PAD_37	Embedded pad for embedded psram or flash
38	AVDD33_AON	12	15	19	Analog	XTAL32K_IN	Crystal oscillator 32.768kHz input
39	AVDD33_AON	13	16	20	Analog	XTAL32K_OUT	Crystal oscillator 32.768kHz output
40	AVDD33_AON	20	23	27	Analog	XTAL_HF_IN	External crystal input, 32MHz
41	AVDD33_AON	21	24	28	Analog	XTAL_HF_OUT	External crystal output, 32MHz
42	AVDD33_AON	15	18	22	Analog	PU_CHIP	Chip power-up
43	AVDD15	16	19	23	Analog	ANT	RF input and output (single pin)
44	-	32	40	48	Power	VDDIO_1	Externally powered 3.3V or 1.8V
45	-	10	11	14	Power	VDDIO_2	Externally powered 3.3V
46	-	25	31	36	Power	VDDIO_3	Externally powered 3.3V or 1.8V
47	-	14	17	21	Power	AVDD33_AON	Externally powered 3.3V
48	-	17	20	24	Power	AVDD33_PA	Externally powered 3.3V
49	-	19	22	26	Power	AVDD_RF	Externally powered 3.3/1.8/1.5V

Table 3.1: Pin description

No	Voltage Domain	BL702	BL704	BL706	I/O Type	Pin Name	Description
50	-	18	21	25	Power	AVDD15	Internal LDO output (for internal use only)
51	-	9	10	13	Power	SW_DCDC	DCDC power 1.8V
52	-	8	9	12	Power	DCDC_OUT	DCDC power 1.8V
53	-	6	7	10	Power	VDDBUS_USB	USB power
54	-	7	8	11	Power	VDDCORE	Internal LDO output (for internal use only)

Table 3.2: GPIO Muxed Pins

Pin Name	Flash[1]	I2S	SPI (Default /SWAP=1)	CAM	UART[2] (Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	Ether_Mac	QDEC	Key_Scan_In	Key_Scan_Drive	IR
PAD_GPIO_0	-	BCLK	MOSI /MISO	PIX_CLK	SIG0 /SIG4	SCL	PWM_CH0	-	FEM0	TMS/TCK	RMII_REF_-CLK	QDEC0_a	ROW0	COL0	-
PAD_GPIO_1	-	FS	MISO /MOSI	FRAME_VLD	SIG1 /SIG5	SDA	PWM_CH1	-	FEM1	TDI/TDO	RMII_TXD[0]	QDEC0_b	ROW1	COL1	-
PAD_GPIO_2	-	DIO/DO	SS	LINE_VLD	SIG2 /SIG6	SCL	PWM_CH2	-	FEM2	TCK/TMS	RMII_TXD[1]	QDEC0_led	ROW2	COL2	-
PAD_GPIO_3	-	RCLK_O /DI	SCLK	PIX_DAT0	SIG3 /SIG7	SDA	PWM_CH3	-	FEM3	TDO/TDI	-	QDEC1_a	ROW3	COL3	-
PAD_GPIO_4	-	BCLK	MOSI /MISO	PIX_DAT1	SIG4 /SIG0	SCL	PWM_CH4	-	FEM4	TMS/TCK	-	QDEC1_b	ROW4	COL4	-
PAD_GPIO_5	-	FS	MISO /MOSI	PIX_DAT2	SIG5 /SIG1	SDA	PWM_CH0	-	FEM0	TDI/TDO	-	QDEC1_led	ROW5	COL5	-
PAD_GPIO_6	-	DIO/DO	SS	PIX_DAT3	SIG6 /SIG2	SCL	PWM_CH1	-	FEM1	TCK/TMS	-	QDEC2_a	ROW6	COL6	-
PAD_GPIO_7	-	RCLK_O /DI	SCLK	-	SIG7 /SIG3	SDA	PWM_CH2	USB_-DP/ADC_-CH6	FEM2	TDO/TDI	RMII_RXD[0]	QDEC2_b	ROW7	COL7	-
PAD_GPIO_8	-	BCLK	MOSI /MISO	-	SIG0 /SIG4	SCL	PWM_CH3	USB_-DM/ADC_-CH0	FEM3	TMS/TCK	RMII_RXD[1]	QDEC2_led	ROW0	COL8	-
PAD_GPIO_9	-	FS	MISO /MOSI	-	SIG1 /SIG5	SDA	PWM_CH4	ADC_CH7	FEM4	TDI/TDO	-	QDEC0_a	ROW1	COL9	-
PAD_GPIO_10	-	DIO/DO	SS	-	SIG2 /SIG6	SCL	PWM_CH0	MICBIAS	FEM0	TCK/TMS	-	QDEC0_b	ROW2	COL10	-
PAD_GPIO_11	-	RCLK_O /DI	SCLK	-	SIG3 /SIG7	SDA	PWM_CH1	ADC_CH3	FEM1	TDO/TDI	-	QDEC0_led	ROW3	COL11	-
PAD_GPIO_12	-	BCLK	MOSI /MISO	PIX_DAT4	SIG4 /SIG0	SCL	PWM_CH2	ADC_CH4	FEM2	TMS/TCK	-	QDEC1_a	ROW4	COL12	-
PAD_GPIO_13	-	FS	MISO /MOSI	-	SIG5 /SIG1	SDA	PWM_CH3	-	FEM3	TDI/TDO	-	QDEC1_b	ROW5	COL13	-
PAD_GPIO_14	-	DIO/DO	SS	-	SIG6 /SIG2	SCL	PWM_CH4	ADC_CH5	FEM4	TCK/TMS	-	QDEC1_led	ROW6	COL14	-
PAD_GPIO_15	-	RCLK_O /DI	SCLK	-	SIG7 /SIG3	SDA	PWM_CH0	ADC_CH1	FEM0	TDO/TDI	-	QDEC2_a	ROW7	COL15	-
PAD_GPIO_16	-	BCLK	MOSI /MISO	-	SIG0 /SIG4	SCL	PWM_CH1	-	FEM1	TMS/TCK	-	QDEC2_b	ROW0	COL16	-
PAD_GPIO_17	SF1_IO0 /SF2_CS2	FS	MISO /MOSI	PIX_DAT4	SIG1 /SIG5	SDA	PWM_CH2	ADC_-CH2/psw_-irrcv	FEM2	TDI/TDO	-	QDEC2_led	ROW1	COL17	IRRX (ir_rx_gpio_sel=1)
PAD_GPIO_18	SF1_IO1	DIO/DO	SS	PIX_DAT5	SIG2 /SIG6	SCL	PWM_CH3	ADC_CH8	FEM3	TCK/TMS	RMII_MDC	QDEC0_a	ROW2	COL18	IRRX (ir_rx_gpio_sel=2)
PAD_GPIO_19	SF1_CS	RCLK_O /DI	SCLK	PIX_DAT6	SIG3 /SIG7	SDA	PWM_CH4	ADC_CH9	FEM4	TDO/TDI	RMII_MDIO	QDEC0_b	ROW3	COL19	IRRX (ir_rx_gpio_sel=3)
PAD_GPIO_20	SF1_IO3	BCLK	MOSI /MISO	PIX_DAT7	SIG4 /SIG0	SCL	PWM_CH0	ADC_CH10	FEM0	TMS/TCK	RMII_RXERR	QDEC0_led	ROW4	COL0	IRRX (ir_rx_gpio_sel=4)
PAD_GPIO_21	SF1_CLK	FS	MISO /MOSI	-	SIG5 /SIG1	SDA	PWM_CH1	ADC_CH11	FEM1	TDI/TDO	RMII_TX_EN	QDEC1_a	ROW5	COL1	IRRX (ir_rx_gpio_sel=5)

Table 3.2: GPIO Muxed Pins

Pin Name	Flash[1]	I2S	SPI (Default /SWAP=1)	CAM	UART[2] (Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	Ether_Mac	QDEC	Key_Scan_In	Key_Scan_Drive	IR
PAD_GPIO_22	SF1_IO2	DIO/DO	SS	-	SIG6 /SIG2	SCL	PWM_CH2	IRTX	FEM2	TCK/TMS	RMII_RX_DV	QDEC1_b	ROW6	COL2	IRRX (ir_rx_gpio_sel=6)
PAD_GPIO_23	SF2_IO2	RCLK_O /DI	SCLK	PIX_DAT4	SIG7 /SIG3	SDA	PWM_CH3	IRTX	FEM3	TDO/TDI	-	QDEC1_led	ROW7	COL3	IRRX (ir_rx_gpio_sel=7)
PAD_GPIO_24	SF2_IO1	BCLK	MOSI /MISO	PIX_DAT5	SIG0 /SIG4	SCL	PWM_CH4	-	FEM4	TMS/TCK	RMII_MDC	QDEC2_a	ROW0	COL4	IRRX (ir_rx_gpio_sel=8)
PAD_GPIO_25	SF2_CS	FS	MISO /MOSI	PIX_DAT6	SIG1 /SIG5	SDA	PWM_CH0	-	FEM0	TDI/TDO	RMII_MDIO	QDEC2_b	ROW1	COL5	IRRX (ir_rx_gpio_sel=9)
PAD_GPIO_26	SF2_IO3	DIO/DO	SS	PIX_DAT7	SIG2 /SIG6	SCL	PWM_CH1	-	FEM1	TCK/TMS	RMII_RXERR	QDEC2_led	ROW2	COL6	IRRX (ir_rx_gpio_sel=10)
PAD_GPIO_27	SF2_CLK	RCLK_O /DI	SCLK	-	SIG3 /SIG7	SDA	PWM_CH2	-	FEM2	TDO/TDI	RMII_TX_EN	QDEC0_a	ROW3	COL7	IRRX (ir_rx_gpio_sel=11)
PAD_GPIO_28	SF2_IO0	BCLK	MOSI /MISO	PIX_DAT4	SIG4 /SIG0	SCL	PWM_CH3	-	FEM3	TMS/TCK	RMII_RX_DV	QDEC0_b	ROW4	COL8	IRRX (ir_rx_gpio_sel=12)
PAD_GPIO_29	-	FS	MISO /MOSI	PIX_DAT5	SIG5 /SIG1	SDA	PWM_CH4	-	FEM4	TDI/TDO	-	QDEC0_led	ROW5	COL9	IRRX (ir_rx_gpio_sel=13)
PAD_GPIO_30	-	DIO/DO	SS	PIX_DAT6	SIG6 /SIG2	SCL	PWM_CH0	-	FEM0	TCK/TMS	-	QDEC1_a	ROW6	COL10	IRRX (ir_rx_gpio_sel=14)
PAD_GPIO_31	-	RCLK_O /DI	SCLK	PIX_DAT7	SIG7 /SIG3	SDA	PWM_CH1	-	FEM1	TDO/TDI	-	QDEC1_b	ROW7	COL11	IRRX (ir_rx_gpio_sel=15)

[1] There are 2 groups of Flash, and the smallest selection unit is group, which is configured according to group when used.
In Dual CS mode, PAD_GPIO_17 can be configured as SF2_CS2 function.

[2] The default UART signal mapping table is shown below.

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Table 3.3: UART Signal Mapping(Default)

UART Signal	uart_sig_x_sel	Mapping Signal
UART_SIG0	uart_sig_0_sel=0	UART0_RTS
UART_SIG1	uart_sig_1_sel=1	UART0_CTS
UART_SIG2	uart_sig_2_sel=2	UART0_TXD
UART_SIG3	uart_sig_3_sel=3	UART0_RXD
UART_SIG4	uart_sig_4_sel=4	UART1_RTS
UART_SIG5	uart_sig_5_sel=5	UART1_CTS
UART_SIG6	uart_sig_6_sel=6	UART1_TXD
UART_SIG7	uart_sig_7_sel=7	UART1_RXD

Note: UART_SIG0-UART_SIG7 can be configured as any of 8 Mapping Signals. For example: UART_SIG0 can also be configured as UART_RXD. The specific signal mapping example is shown in the table below.

Table 3.4: UART Signal Mapping(Example)

UART Signal	uart_sig_x_sel	Mapping Signal
UART_SIG0	uart_sig_0_sel=7	UART1_RXD
UART_SIG1	uart_sig_1_sel=6	UART1_TXD
UART_SIG2	uart_sig_2_sel=5	UART1_CTS
UART_SIG3	uart_sig_3_sel=4	UART1_RTS
UART_SIG4	uart_sig_4_sel=3	UART0_RXD
UART_SIG5	uart_sig_5_sel=2	UART0_TXD
UART_SIG6	uart_sig_6_sel=1	UART0_CTS
UART_SIG7	uart_sig_7_sel=0	UART0_RTS

4 Electrical Specifications

4.1 Absolute Maximum Rating

Table 4.1: Absolute Maximum Rating

Pin Name	Min.	Max.	Unit
VDDIO_1	-0.3	3.63	V
VDDIO_2	-0.3	3.63	V
VDDIO_3	-0.3	3.63	V
VSSBUS_USB	-0.3	5.5	V
AVDD33_AON	-0.3	3.63	V
AVDD33_PA	-0.3	3.63	V
AVDD33_RF	-0.3	3.63	V
ESD Protection (HBM)		2000	V
Storage Temperature	-40	125	°C

4.2 Operating Condition

4.2.1 Power characteristics

Table 4.2: Recommended Power Operating Range

Pin Name	Min.	Typ	Max.	Unit
VDDIO_1	1.62/1.8	1.8/3.3	1.92/3.63	V
VDDIO_2	1.8	3.3	3.63	V
VDDIO_3	1.8	3.3	3.63	V
VDDBUS_USB	4.5	5	5.5	V
AVDD33_AON	1.8	3.3	3.63	V
AVDD33_PA	1.4/2.97	1.5/3.3	1.6/3.63	V
AVDD33_RF	1.4/2.97	1.5/3.3	1.6/3.63	V

4.2.2 Temperature sensor characteristics

Table 4.3: Recommended Temperature Operating Range

Item		Min.	Max.	Unit
Temperature	Main Die	-40	105	°C
	Multi-Die SiP	-40	85	°C

4.2.3 General operating conditions

Table 4.4: General Operating Conditions

Item	Description	Min.	Typ	Max.	Unit
FCPU	CPU/TCM/Cache clock frequency	0	32	144	MHz
FSYS	System clock frequency	0	32	72	MHz

4.2.4 GPADC characteristics

Table 4.5: GPADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD33	Vbat supply voltage		2.3		3.6	V
T	Working tempreture		-40		125	°C
I_{vdd33}	Current consumption of ADC on VDD33	PGA1&2 off (2M clock)		150		μA
		PGA1&2 on(2M clock)		350		
Fclk	ADC input top clock frequency	Clock from SOC	1.5		32	MHz
Fsample	Sampling rate	2.048M(12bit mode) 32K-128K(14bit mode) 8K-16K(16bit mode)			2	MHz
Vin	Input conversion voltage range	Differential mode			6.4	V(vpp)
		Single-ended mode			3.2	
Rin	Total input channel resistance				2	KΩ
Tcal	Calibration time	Fsample=2M (16bit mode)			140	uS
Tpu	Power up time				1	uS
Tconv	Total conversion time	12bit mode			1	1/Fsample
		14bit mode [1]			16	
		14bit mode [2]			64	
		16bit mode [3]			128	
		16bit mode [4]			256	

1. 14-bit mode with 16 times average
2. 14-bit mode with 64 times average
3. 16-bit mode with 128 times average
4. 16-bit mode with 256 times average

Note: Unless otherwise specified, the parameters given in Table 1 are derived from test under -40 to 125oC, supply AVDD=3.3V, DVDD=1.1V.

Table 4.6: ADC electrical characteristic

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DNL [1]	Differential linearity error				+/-1	LSB
INL [1]	Integral linearity error				+/-2	LSB
Offset	Input offset				+/-2	LSB
Ge [1&2]	Gain error				+/-1	%
ENOB	Effective number of bits	12bit mode(201KHz input)	9.7	10.5		bit
		14bit mode(2.5KHz input)	10.8	11.4		
		16bit mode(1KHz input)	11.5	12.3		
SNDR	Signal-to-noise-distortion (PGA on)	12bit mode(201KHz input)	59	65		dB
		14bit mode(2.5KHz input)	66	72.4		
		16bit mode(1KHz input)	71	76.8		
SNDR	Signal-to-noise-distortion (PGA gain=4)	12bit mode(201KHz input)	58	64		dB
		14bit mode(2.5KHz input)	64	69.5		
		16bit mode(1KHz input)	70	74		

1. more test needed

2. after calibration

5 Product use

5.1 Moisture Sensitivity Level(MSL)

The moisture sensitivity level of the chip is: MSL3. After the vacuum package is opened, it needs to be used up within 168 hours (7 days) at ≤30°C/60%RH, otherwise it needs to be baked and put online.

For baking temperature and time, please refer to IPC/JEDECJ-STD-033B01.

Table 5.1: Reference Conditions for Drying Mounted or Unmounted SMD Packages
(User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤5% RH		Bake @ 40°C ≤5% RH	
		Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h
Thickness ≤1.4 mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

5.2 Electro-Static discharge（ESD）

- Human Body Model(HBM): 2000V
- Charged-Device Model(CDM): 500V

5.3 Reflow Profile

For details, please refer to IPC/JEDEC J-STD-020E.

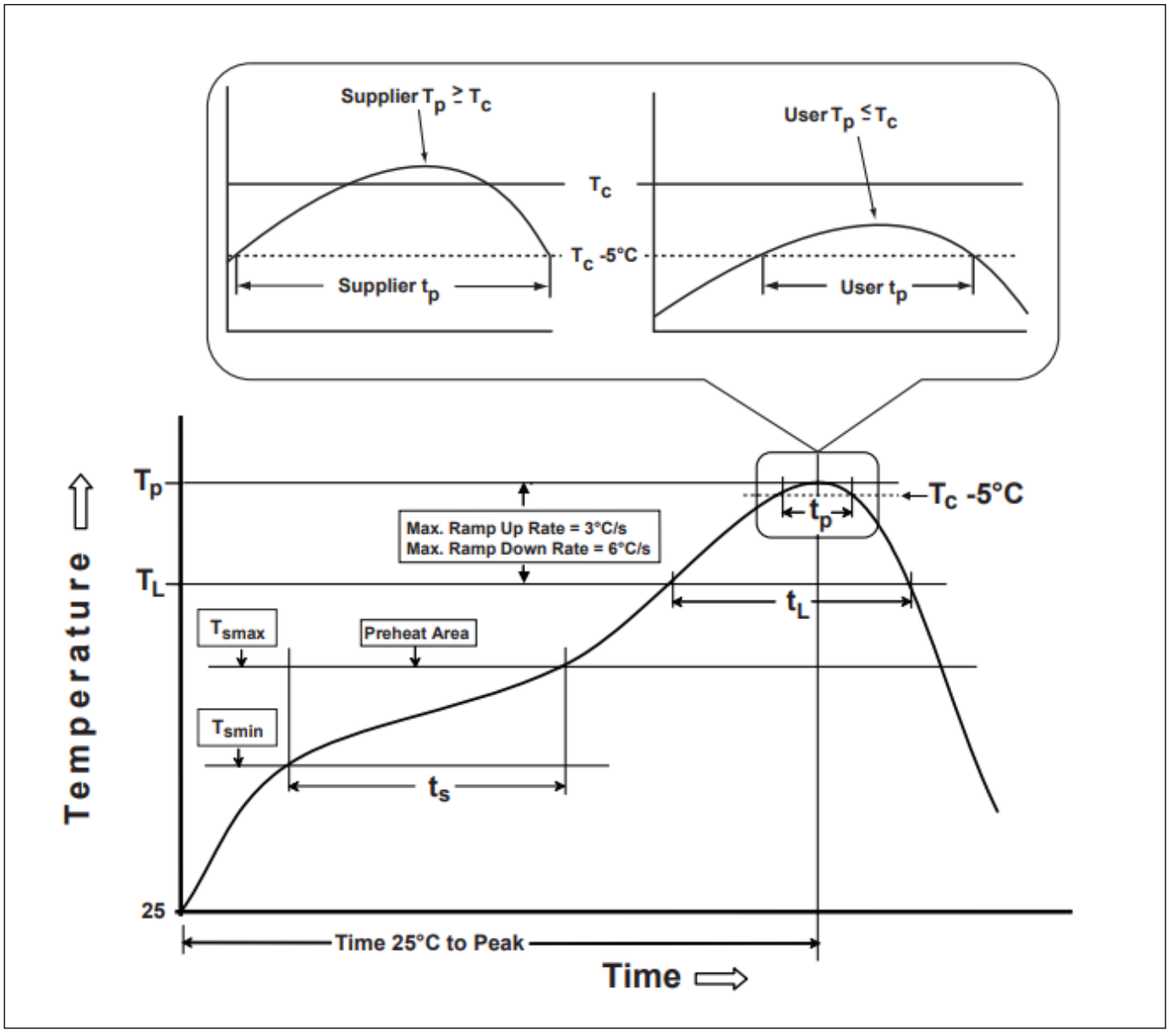

Fig. 5.1: Classification Profile (Not to scale)

Table 5.2: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min (T_{smin})	100 °C	150 °C
Temperature Max (T_{smax})	150 °C	200 °C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time (t_L) maintained above T_L	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)	240 °C+0/-5 °C	250 °C+0/-5 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max
- Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

6 Reference Design

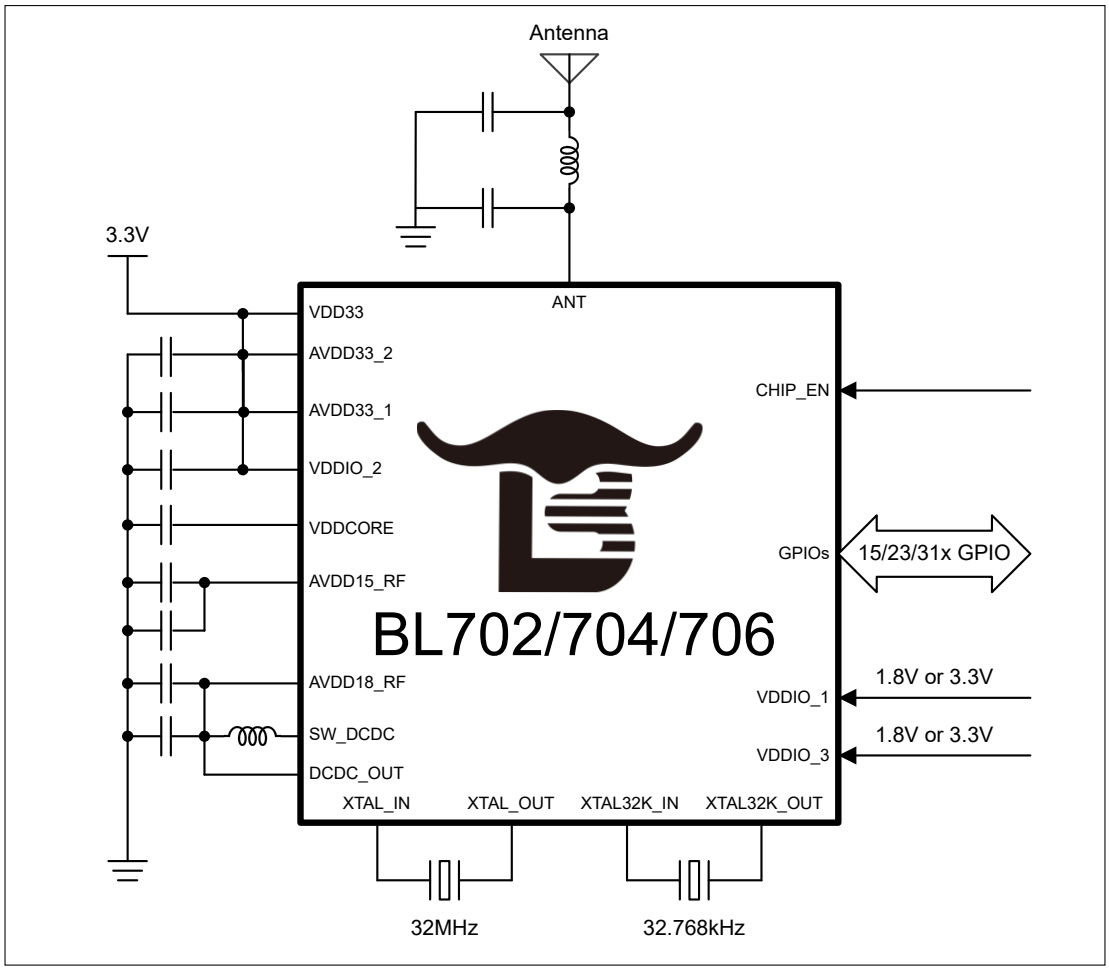

Fig. 6.1: Reference Design

7 Package Information(QFN32)

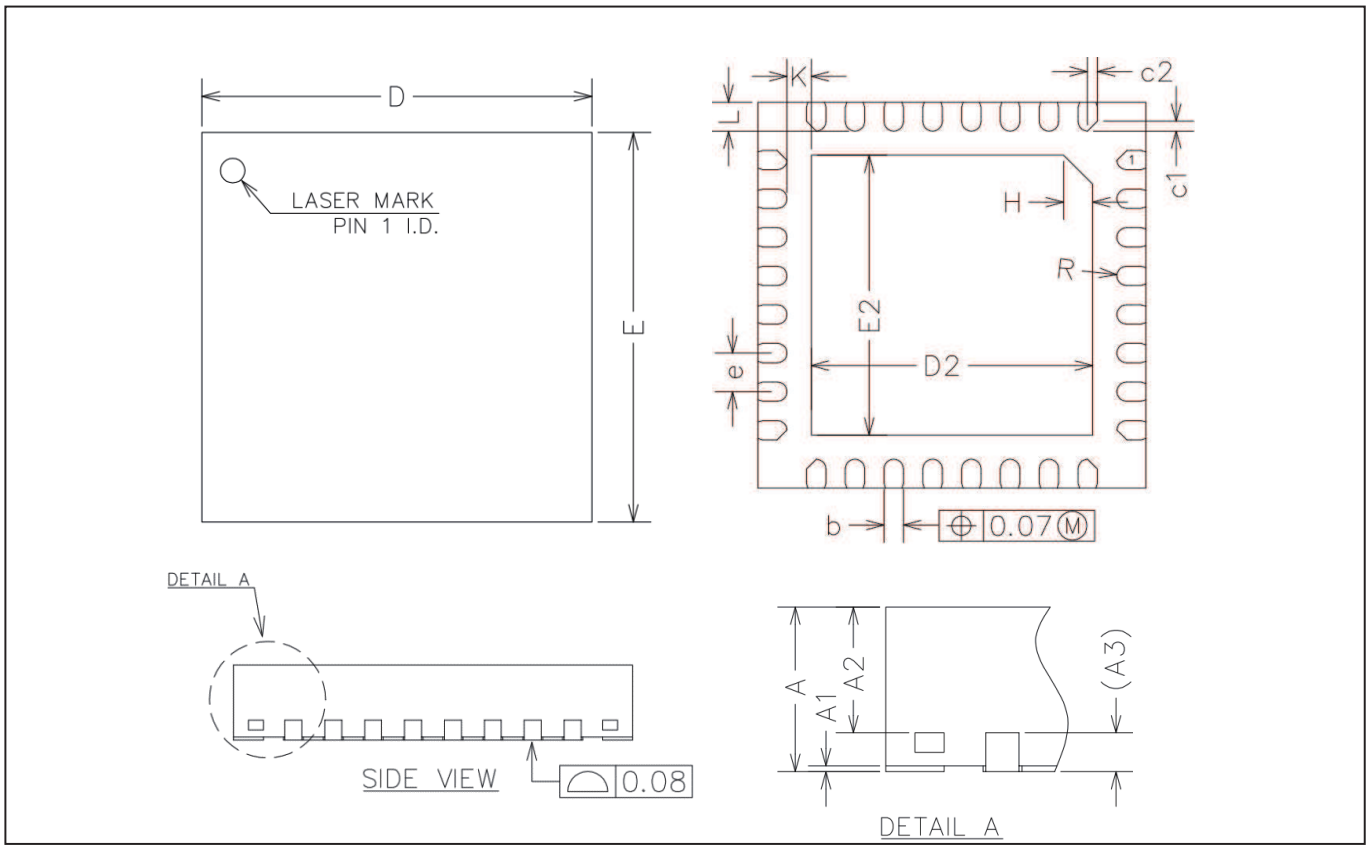

Fig. 7.1: QFN32 Package drawing

Table 7.1: QFN32 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05

Table 7.1: QFN32 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30REF		
K	0.25REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

8 Package Information(QFN40)

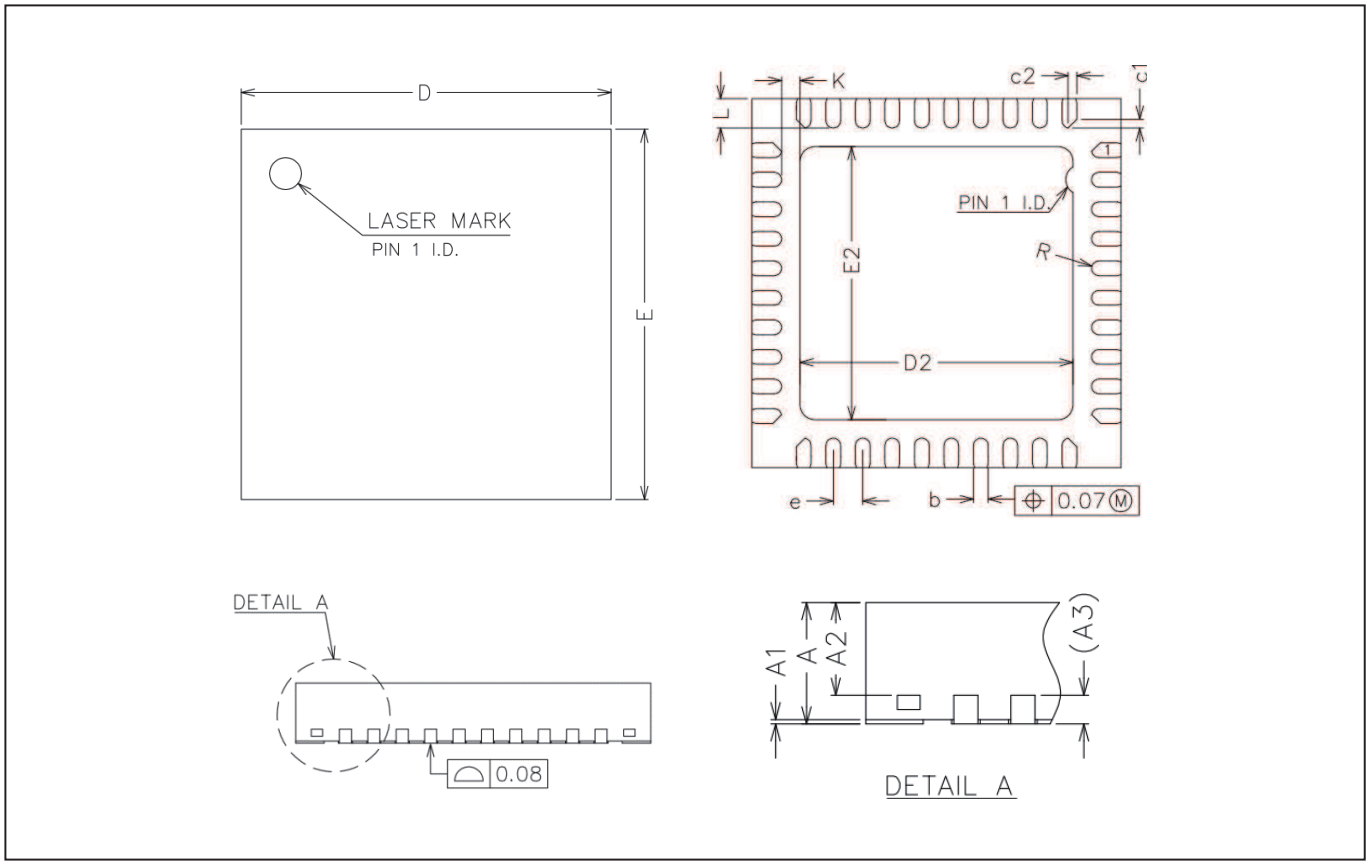

Fig. 8.1: QFN40 Package drawing

Table 8.1: QFN40 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05

Table 8.1: QFN40 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A2	0.60	0.65	0.70
A3	0.20REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
C1	-	0.12	-
C2	-	0.12	-

9 Package Information(QFN48)

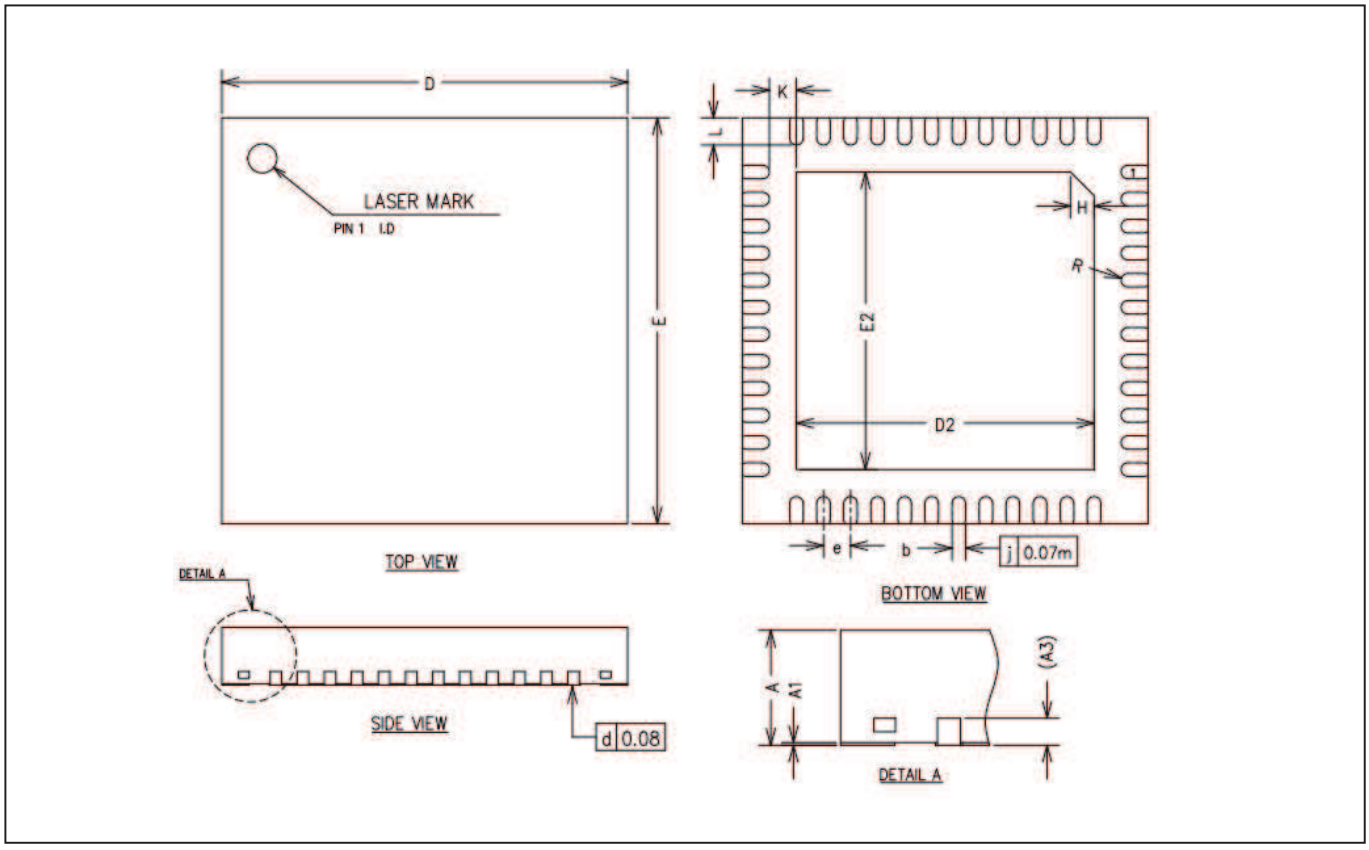

Fig. 9.1: QFN48 Package drawing

Table 9.1: QFN48 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05

Table 9.1: QFN48 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A3	0.20REF		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.30	4.40	4.50
E2	4.30	4.40	4.50
e	0.30	0.40	0.50
H	0.35REF		
K	0.30	0.40	0.50
L	0.30	0.40	0.50
R	0.075	-	-

10 Top Marking Definition

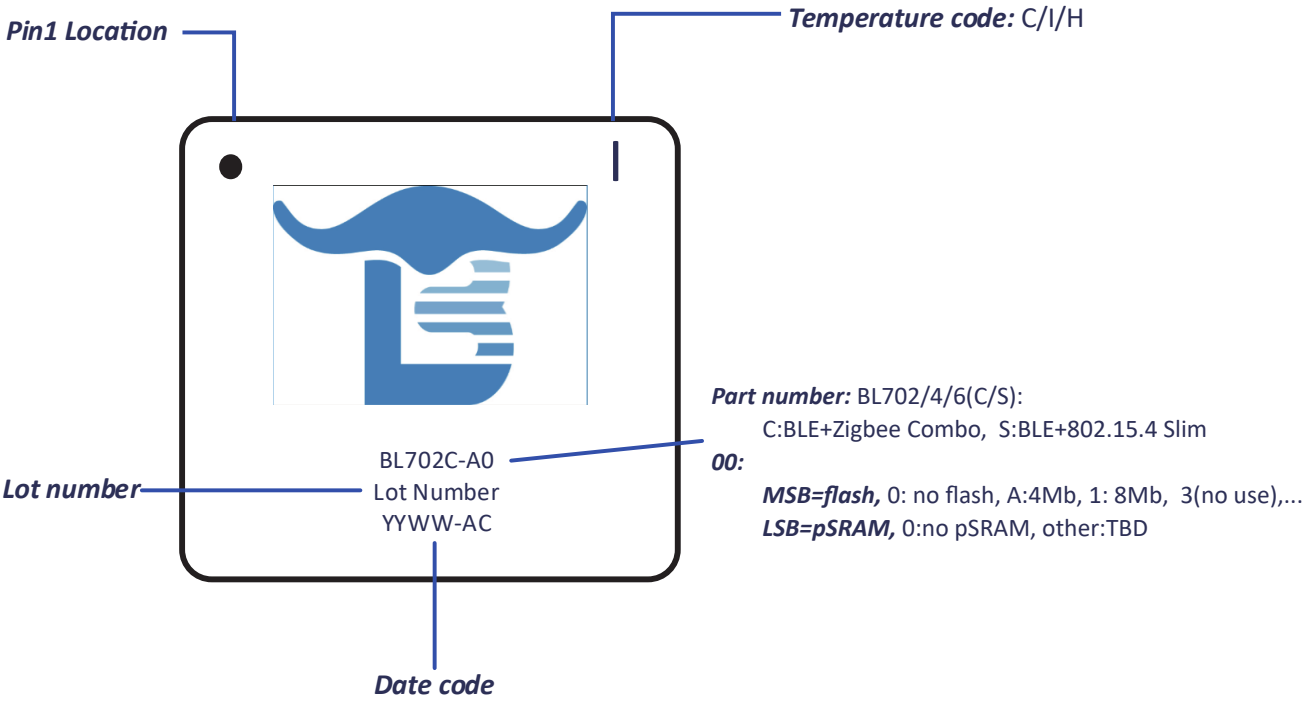

Fig. 10.1: Top Marking Definition

11 Ordering Information

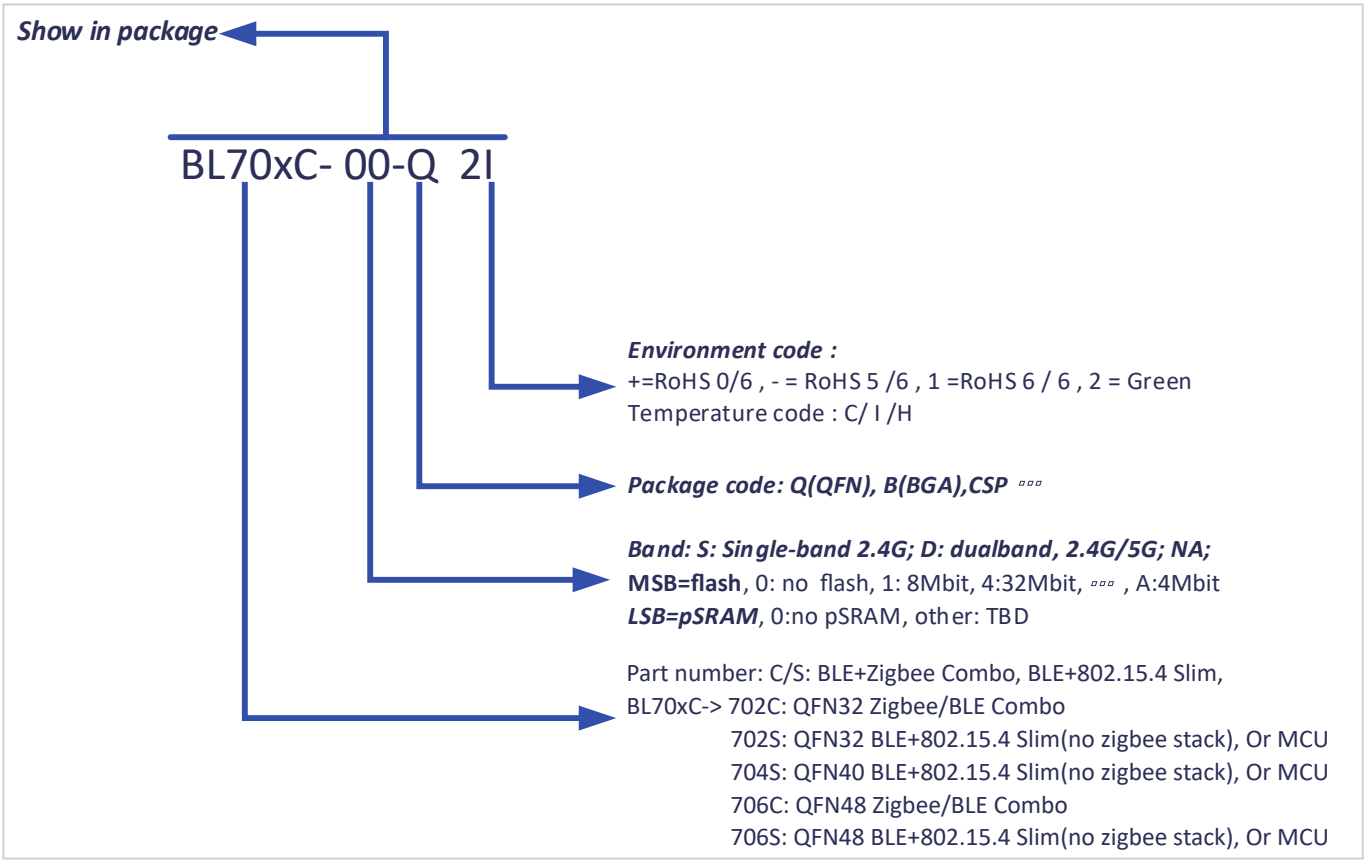

Fig. 11.1: Part Number

Table 11.1: Part Order Options

Product No.	Description
BL702S-A0-Q2I	BLE+802.15.4 Slim, MCU, QFN32, 4Mb flash
BL702C-10-Q2H	Zigbee+BLE Combo, QFN32, 8Mb flash

Table 11.1: Part Order Options

Product No.	Description
BL704S-10-Q2I	BLE+802.15.4 Slim, MCU, QFN40, 8Mb flash
BL706C-10-Q2I	Zigbee+BLE Combo, QFN48, 8Mb flash
BL706S-10-Q2I	BLE+802.15.4 Slim, MCU, QFN48, 8Mb flash

12 Revision history

Table 12.1: Document revision history

Date	Revision	Changes
2020/9/15	1.0	Initial release
2020/9/22	1.1	Add package information(QFN48)
2020/10/20	1.2	Modify the number of TIMER
2020/12/4	1.4	Differentiate different package information
2021/1/11	1.5	Add GPIO Muxed Pins
2021/1/22	1.6	Add Reference design
2021/3/16	1.7	Add Product use, ADC characteristics, modify the default function of SPI pins
2021/4/9	1.8	Add peripheral introduction
2021/5/27	1.9	Modify Pinmux description and minimum temperature value
2021/6/9	2.0	Update product number
2021/7/1	2.1	Modify the description of embedded pad