NCP2811

NOCAP™ Advanced Stereo Headphone Amplifier

NCP2811 is a dual audio power amplifier designed for portable communication device applications such as mobile phones. This part is capable of delivering 27 mW of continuous average power into a 16 Ω load from a 2.7 V power supply with a THD+N of 1%.

Based on the power supply delivered to the device, an internal power management block generates a symmetrical positive and negative voltage. Thus, the internal amplifiers provide outputs referenced to Ground. In this True Ground configuration, the two external heavy coupling capacitors can be removed. It offers significant space and cost savings compared to a typical stereo application.

NCP2811 is available with an external adjustable gain (version A), or with an internal gain of −1.5 V/V (version B). It reaches a superior −100 dB PSRR and noise floor. Thus, it offers high fidelity audio sound, as well as a direct connection to the battery. It contains circuitry to prevent from “Pop & Click” noise that would otherwise occur during turn−on and turn−off transitions. The device is available in 12 bump CSP package (2 x 1.5 mm) which help to save space on the board. It is also available in WQFN12 and TSSOP−14 packages.

Features

- True Ground Configuration Output Eliminates DC−Blocking Capacitors:
  - Save Board Area
  - Save Component Cost
  - No Low−Frequency Response Attenuation
- High PSRR (−100 dB): Direct Connection to the Battery
- “Pop and Click” Noise Protection Circuitry
- Internal Gain (−1.5 V/V) or External Adjustable Gain
- Ultra Low Current Shutdown Mode
- 2.7 V – 5.0 V Operation
- Thermal Overload Protection Circuitry
- CSP 2 x 1.5 mm
- WQFN12 3 x 3 mm
- TSSOP−14
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Headset Audio Amplifier for
  - Cellular Phones
  - MP3 Player
  - Personal Digital Assistant and Portable Media Player
  - Portable Devices

ON Semiconductor®

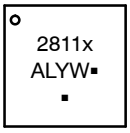
http://onsemi.com

MARKING DIAGRAMS

12 PIN CSP
FC SUFFIX
CASE 499AZ

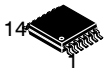
x = A for NCP2811A
= B for NCP2811B
z = C for backside laminate
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

WQFN12
MT SUFFIX
CASE 510AH

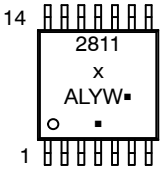


x = A for NCP2811A
= B for NCP2811B
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)



TSSOP−14
DTB SUFFIX
CASE 948G



x = A for NCP2811A
= B for NCP2811B
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

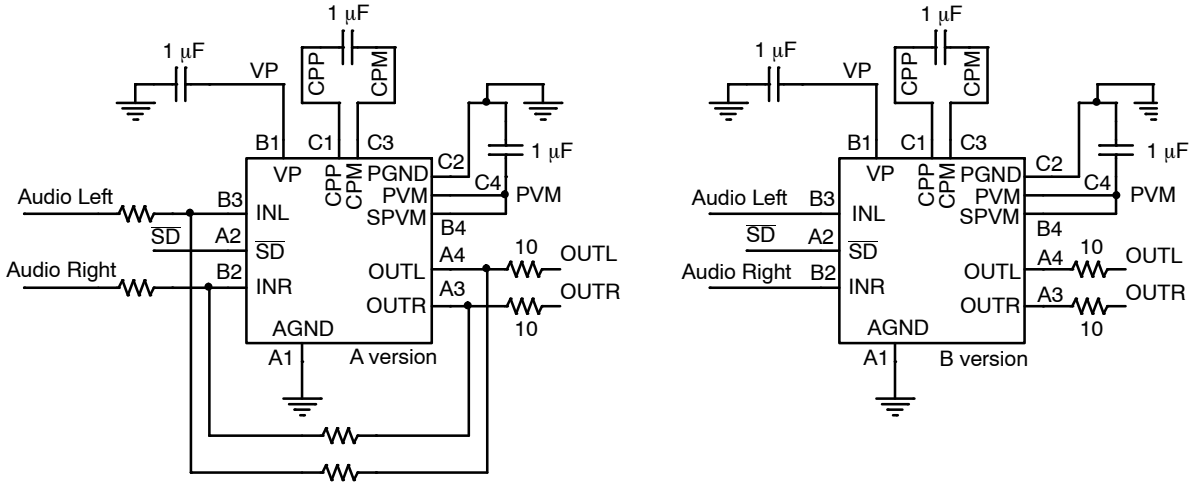


Figure 1. Application Schematics

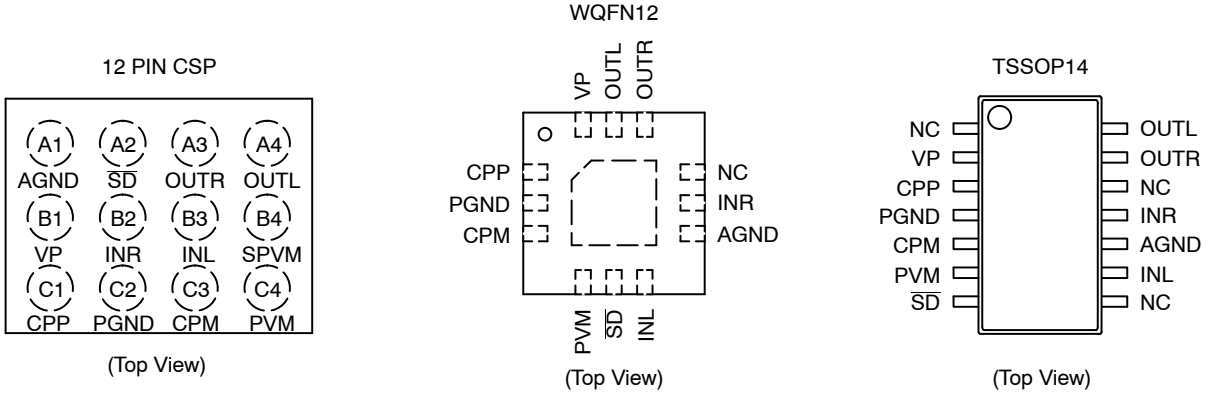


Figure 2. Pin Configurations

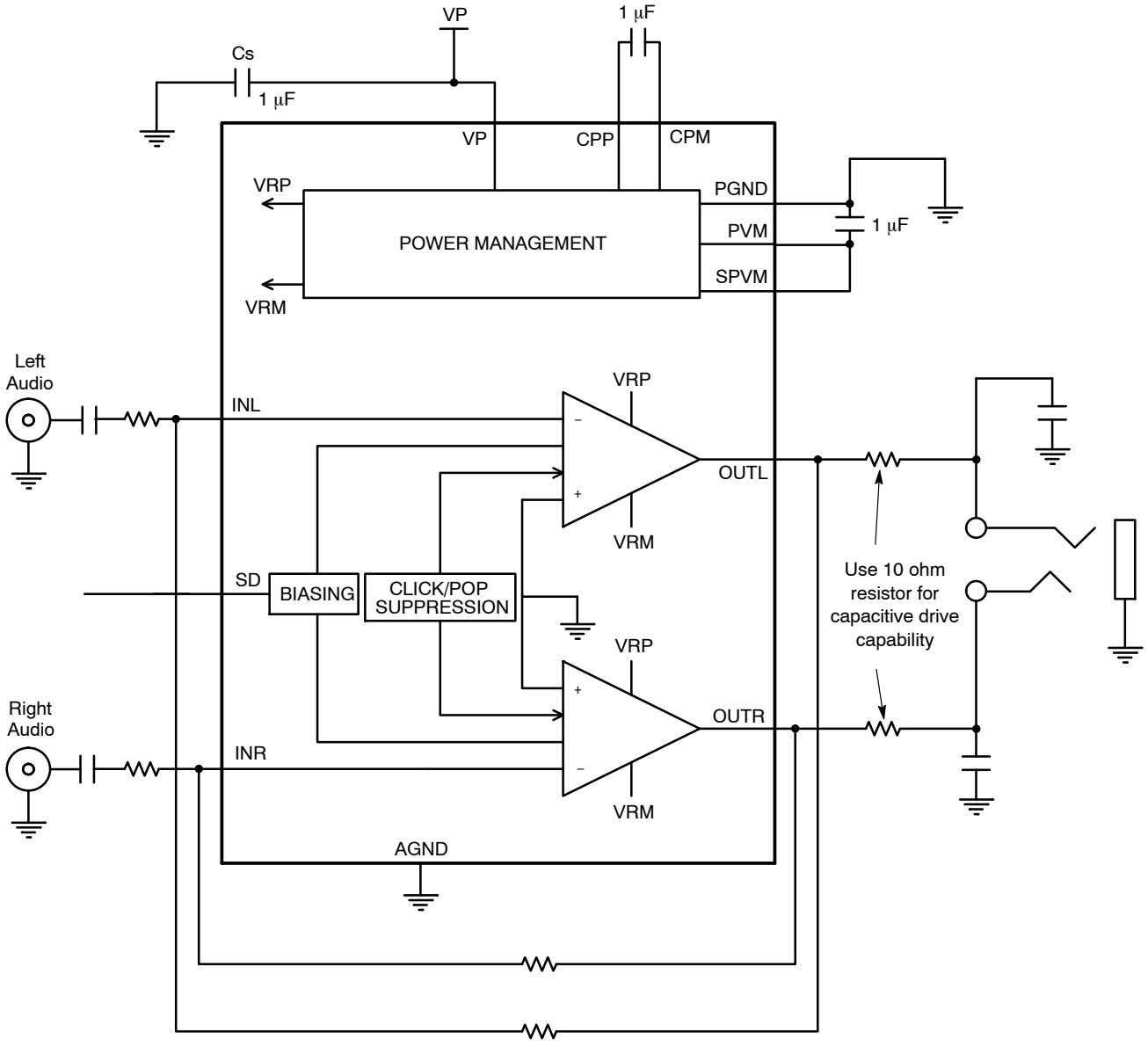


Figure 3. Typical Application Schematic version A

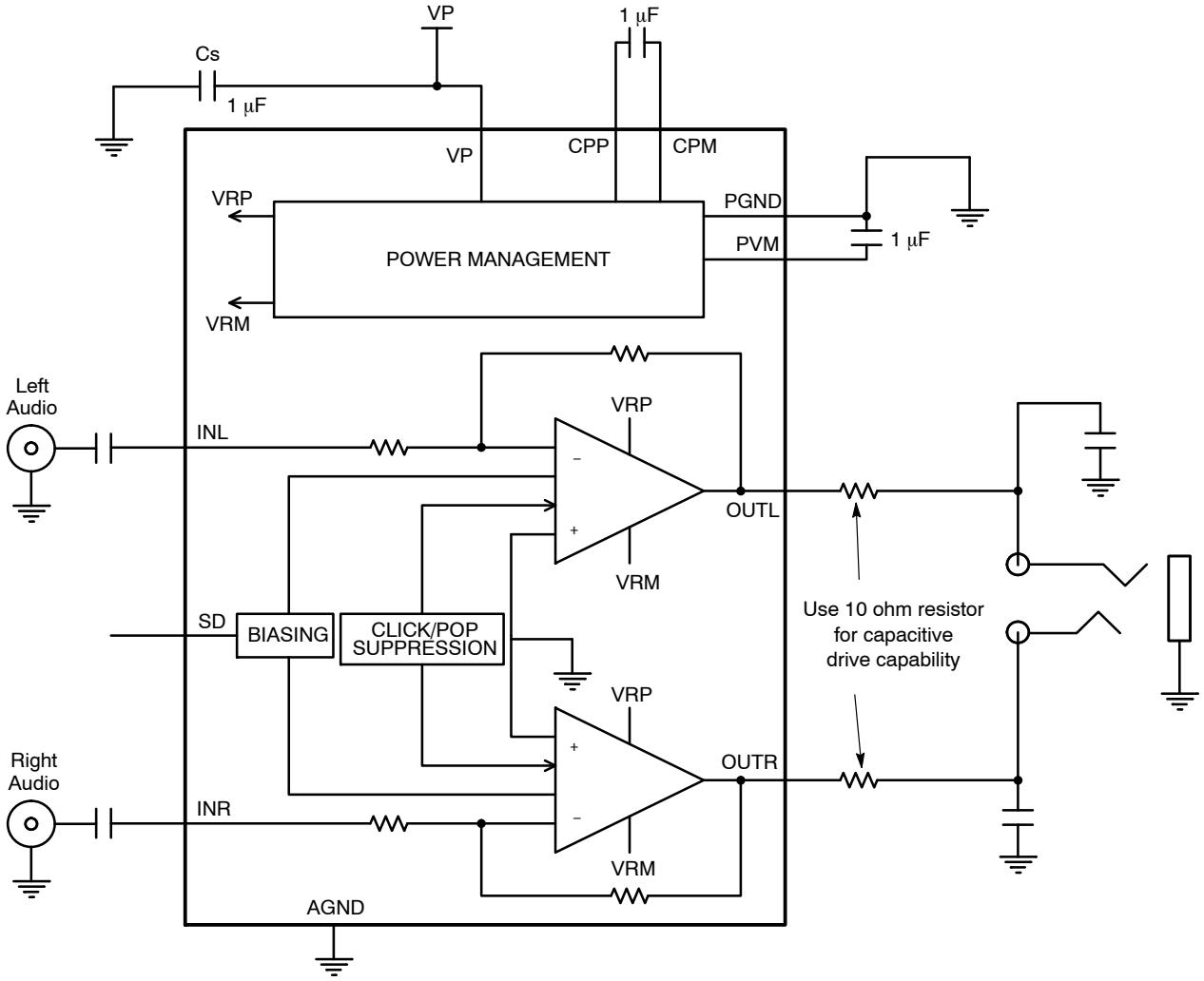


Figure 4. Typical Application Schematic version B

Table 1. PIN FUNCTION DESCRIPTION

PIN CSP	PIN TQFN	PIN TS-SOP	PIN NAME	TYPE	DESCRIPTION
A1	7	10	AGND	GROUND	Analog ground. Connect to ground reference
A2	5	7	$\overline{SD}$	INPUT	Enable activation
A3	10	13	OUTR	OUTPUT	Right audio channel output signal
A4	11	14	OUTL	OUTPUT	Left audio channel output signal
B1	12	2	VP	POWER	Positive supply voltage. It can be connected for example to a Lithium/Ion battery
B2	8	11	INR	INPUT	Right input of the first audio source
B3	6	9	INL	INPUT	Left input of the first audio source
B4	–	–	SPVM	POWER	Amplifier negative power supply voltage. Connect to PVM
C1	1	3	CPP	INPUT/ OUTPUT	Charge pump flying capacitor positive terminal. A 1 μF ceramic filtering capacitor to CPM is needed
C2	2	4	PGND	GROUND	Power ground, connect to ground reference
C3	3	5	CPM	INPUT	Charge pump flying capacitor negative terminal. A 1 μF ceramic filtering capacitor to CPP is needed
C4	4	6	PVM	OUTPUT	Charge pump output. A 1 μF ceramic filtering capacitor to ground is needed

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
AVIN, PVIN Pins: Power Supply Voltage (Note 2)	V_P	– 0.3 to + 6.0	V
INL, INR Pins: Input (Note 2) A version B version	V_{IN}	 $-V_P - 0.3$ to $V_P + 0.3$ –2 to +2	V
$\overline{SD}$ Pin: Input (Note 2)	V_{YY}	–0.3 to V_P + 0.3	V
Human Body Model (HBM) ESD Rating are (Note 3)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 3)	ESD MM	200	V
CSP 1.5 x 2.0 mm package (Notes 6 and 7) Thermal Resistance Junction to Case	$R_{\theta JC}$	(Note 7)	°C/W
Operating Ambient Temperature Range	T_A	–40 to + 85	°C
Operating Junction Temperature Range	T_J	–40 to + 125	°C
Maximum Junction Temperature (Note 6)	T_{JMAX}	+ 150	°C
Storage Temperature Range	T_{STG}	–65 to + 150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Notes:
1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22–A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22–A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22–A115 for all pins.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J–STD–020A.
6. The thermal shutdown set to 150°C (typical) avoids irreversible damage on the device due to power dissipation.
7. The R_{JA} is highly dependent of the PCB Heatsink area. For example, R_{JA} can equal 195°C/W with 50 mm^2 total area and also 135°C/W with 50 mm^2. The bumps have the same thermal resistance and all need to be connected to optimize the power dissipation.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC}$$

Table 3. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 2.7 V to 5.0 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_P	Operational Power Supply		2.7		5.0	V
I_{DD}	Supply quiescent current	Both channels enabled		6.0		mA
I_{SD}	Shutdown current	V_P = 2.7 V to 5.0 V			1	μA
V_{OS}	Output offset voltage	V_P = 2.7 V to 5.0 V		±1		mV
V_{IH}	High−Level input voltage SD pin		1.2			V
V_{IL}	Low−Level input voltage SD pin				0.4	V
R_{SD}	SD pin pull−down impedance			190		KΩ
T_{WU}	Turning on time			1		ms
T_{SD}	Thermal shutdown temperature			160		°C
V_{LP}	Max output swing (peak value)	V_P = 2.9 V to 5.0 V Headset ≥ 16 Ω THD+N = 1%	1			V_{RMS}
P_O	Max output power (output in phase)	V_P = 2.7V, THD+N = 1% Headset = 16 Ω V_P = 2.7V, THD+N = 1% Headset = 32 Ω V_P = 3.6V, THD+N = 1% Headset = 16 Ω V_P = 3.6V, THD+N = 1% Headset = 32 Ω V_P = 5.0V, THD+N = 1% Headset = 16 Ω V_P = 5.0V, THD+N = 1% Headset = 32 Ω		27 37 90 64 110 64		mW
	Crosstalk (Note 8)	Headset ≥ 16 Ω		−80	−60	dB
PSRR	Power supply rejection ratio (Note 8)	V_P = 2.7 V to 5.0 V Input shorted to ground F = 217 Hz F = 1 kHz		 −106 −95		dB
THD+N	Total harmonic distortion + noise (Note 8)	Headset = 16 Ω P_{OUT} = 25 mW		0.01		%
V_N	Output noise voltage (Note 8)	A−Weighting filter		7		$μV_{RMS}$
Z_{IN}	Input impedance	B version only		20		KΩ
Z_{SD}	Output impedance in shutdown mode			10		KΩ
UVLO	UVLO threshold	Falling edge		2.3		V
$UVLO_{HYST}$	UVLO hysteresis			100		mV
Av	Voltage Gain	B version only	−1.53	−1.5	−1.48	V/V

8. Guaranteed by design and characterized.

TYPICAL OPERATING CHARACTERISTICS

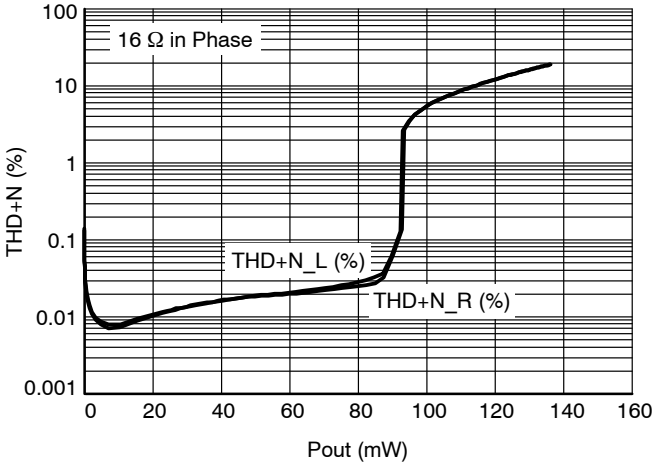


Figure 5. THD+N vs. Pout @ Vp = 3.6 V

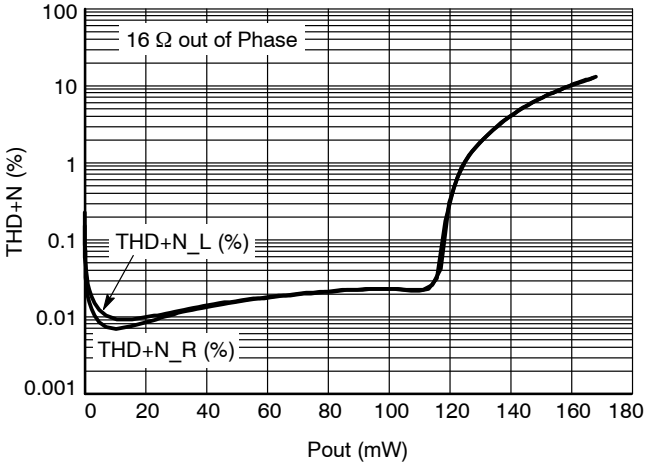


Figure 6. THD+N vs. Pout @ Vp = 3.6 V

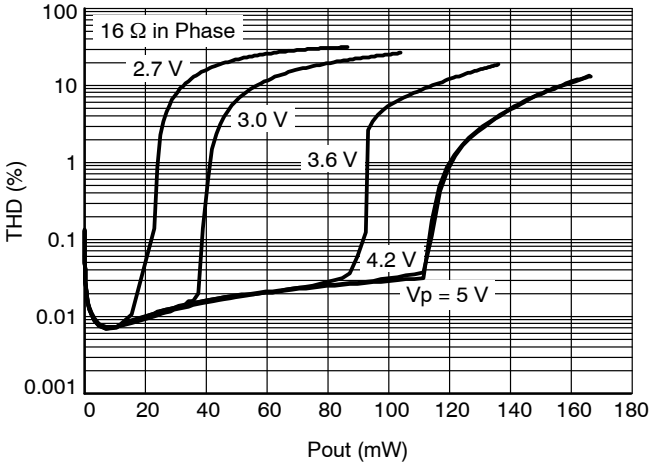


Figure 7. THD+N vs. Pout LEFT

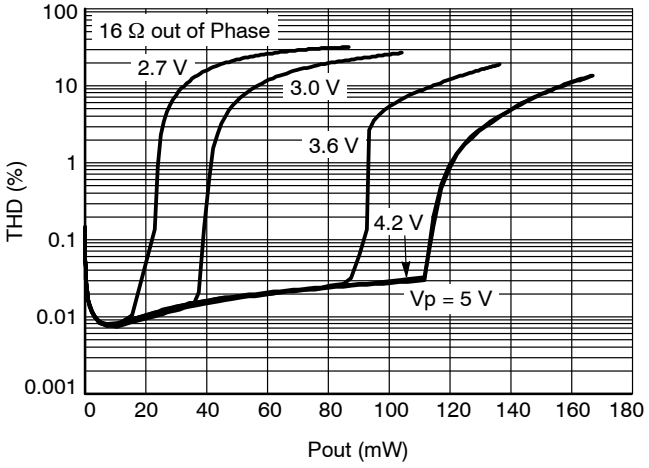


Figure 8. THD+N vs. Pout RIGHT

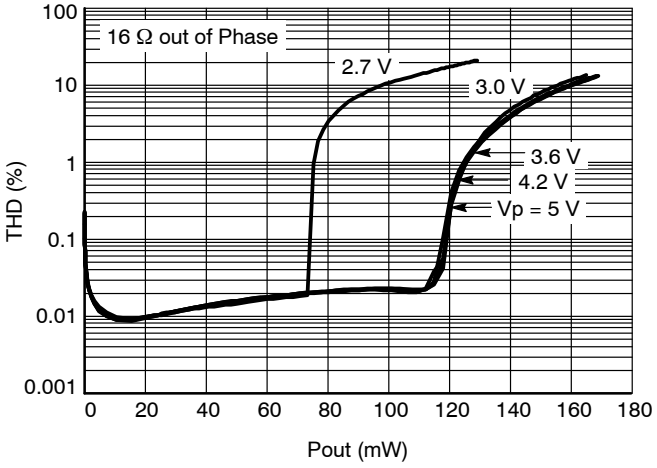


Figure 9. THD+N vs. Pout LEFT

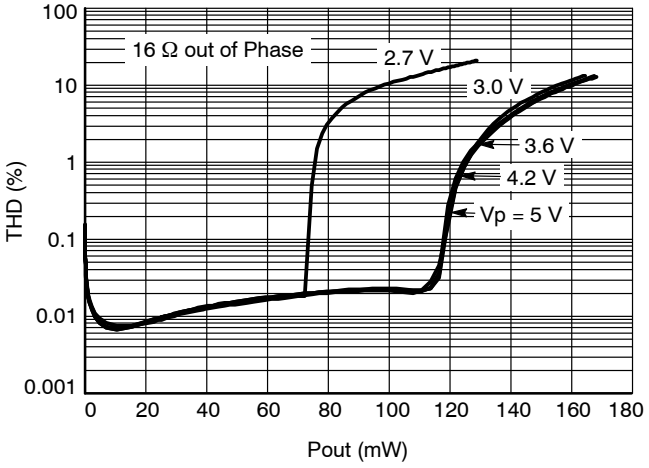


Figure 10. THD+N vs. Pout RIGHT

TYPICAL OPERATING CHARACTERISTICS

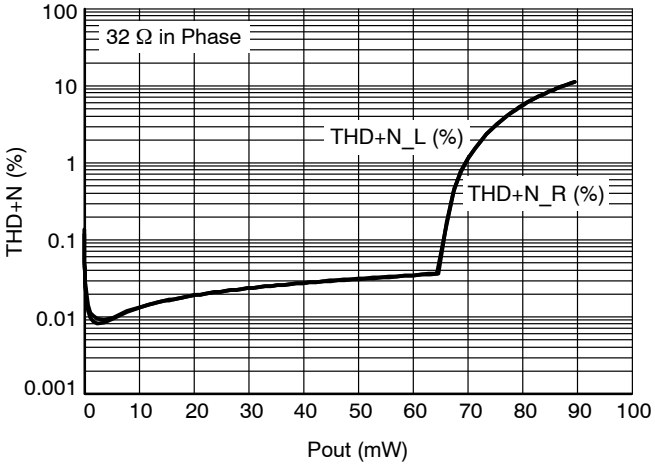


Figure 11. THD+N vs. Pout @ Vp = 3.6 V

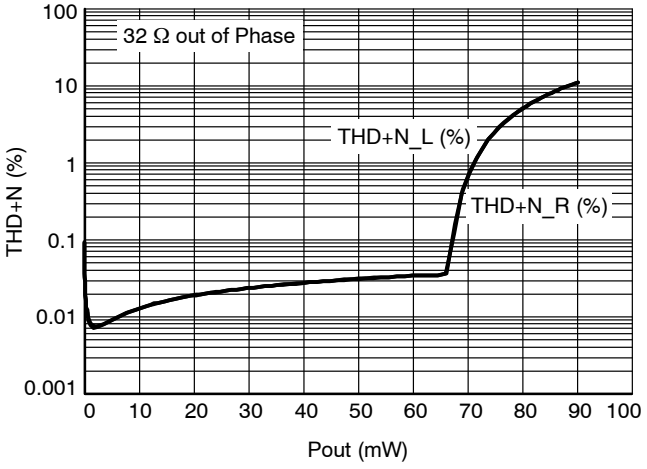


Figure 12. THD+N vs. Pout @ Vp = 3.6 V

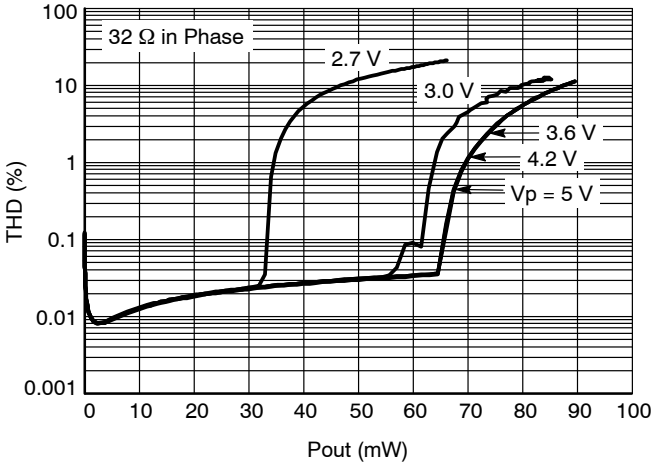


Figure 13. THD+N vs. Pout LEFT

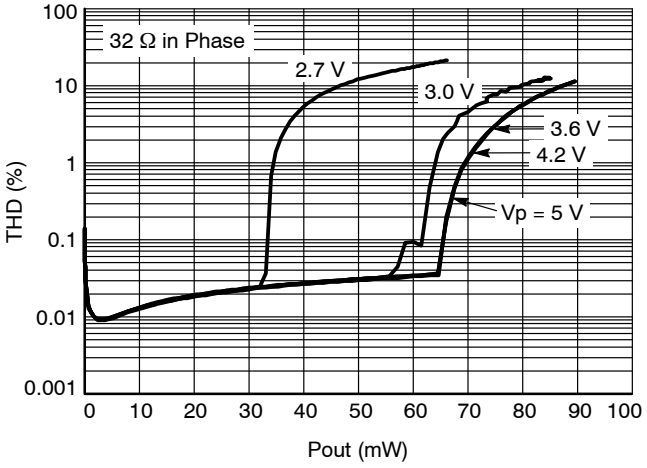


Figure 14. THD+N vs. Pout RIGHT

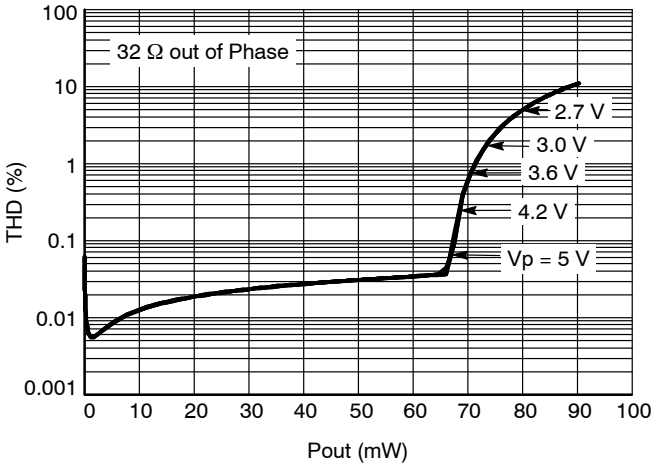


Figure 15. THD+N vs. Pout LEFT

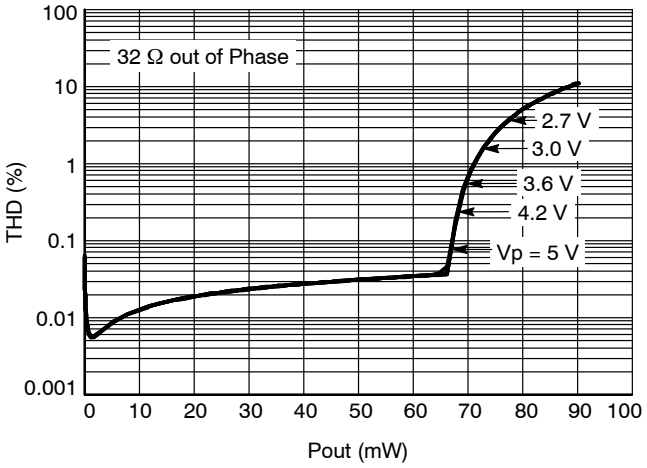


Figure 16. THD+N vs. Pout RIGHT

TYPICAL OPERATING CHARACTERISTICS

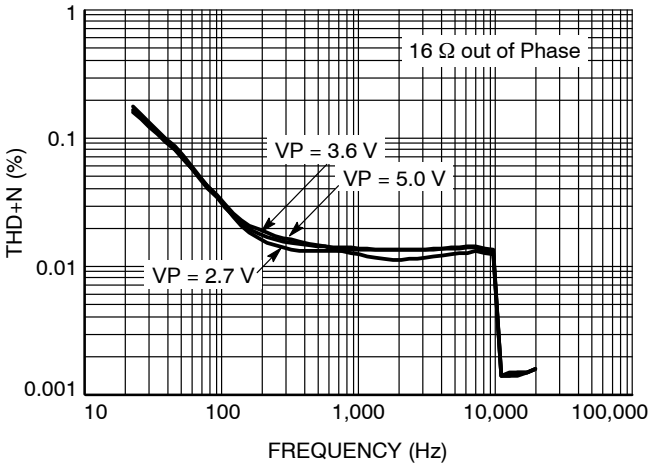


Figure 17. THD vs. Frequency LEFT @ Pout = 32 mW

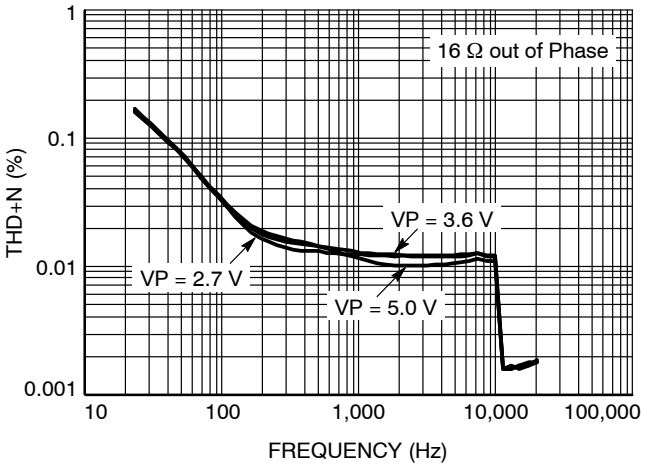


Figure 18. THD vs. Frequency RIGHT @ Pout = 32 mW

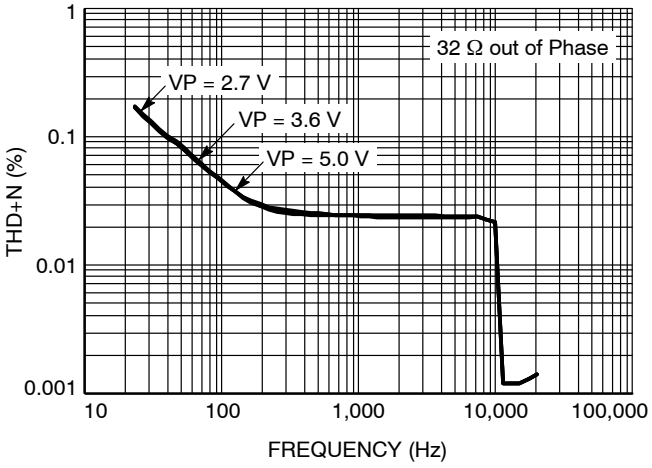


Figure 19. THD vs. Frequency LEFT @ Pout = 32 mW

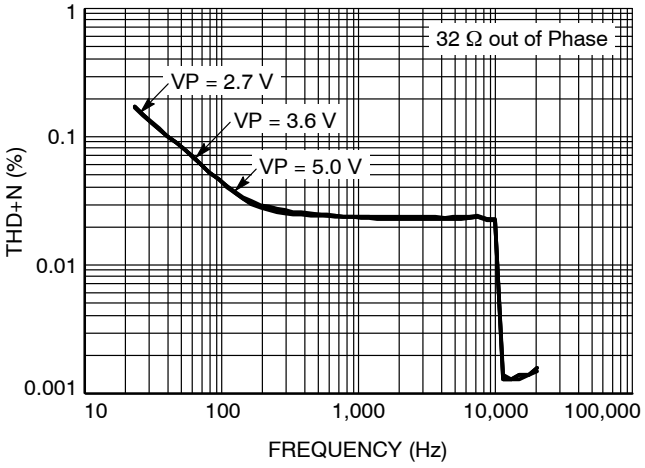


Figure 20. THD vs. Frequency RIGHT @ Pout = 32 mW

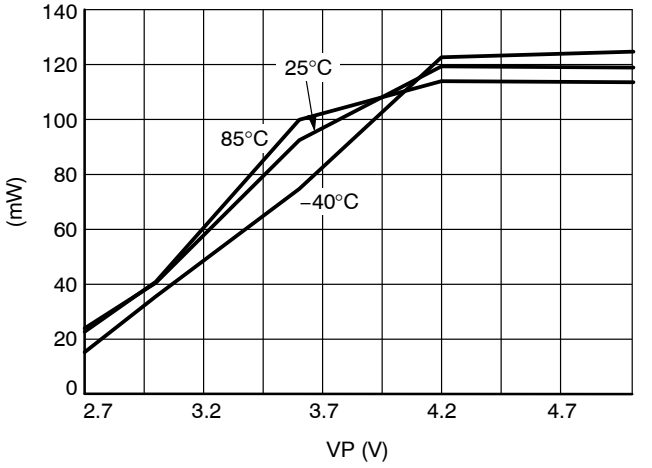


Figure 21. Maximum Output Power LEFT vs. VP (THD+N < 1%)

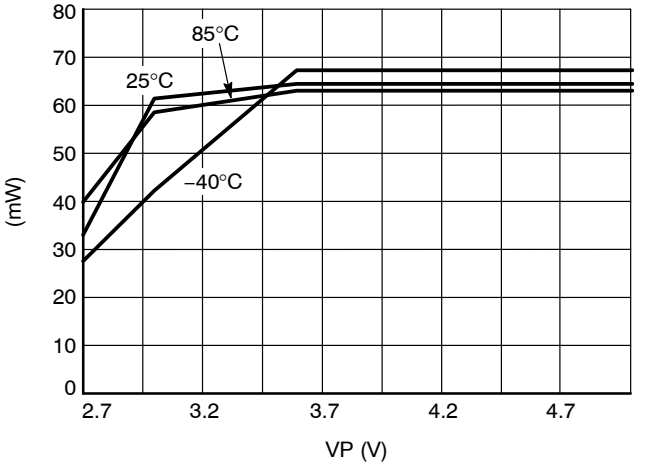


Figure 22. Maximum Output Power LEFT vs. VP (THD+N < 0.1%)

TYPICAL OPERATING CHARACTERISTICS

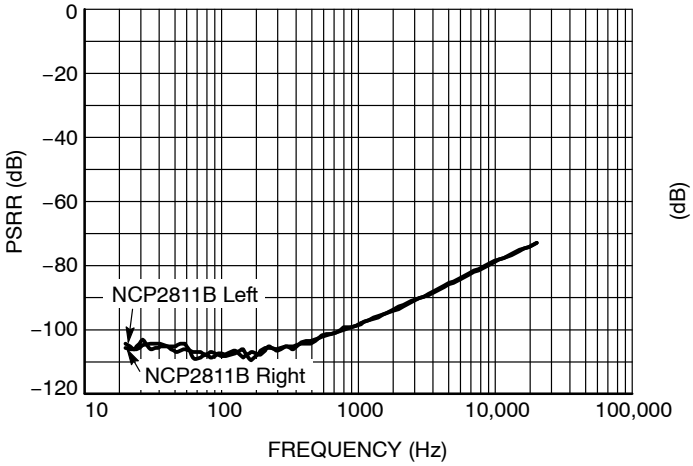


Figure 23. PSRR at Vp = 3.6 V

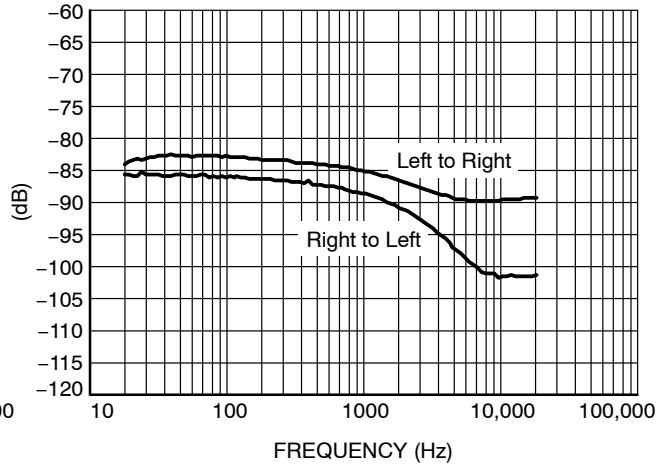


Figure 24. Crosstalk vs. Frequency @ Vp = 3.6 V

DETAIL OPERATING DESCRIPTION

Detailed Descriptions

The NCP2811 is a stereo headphone amplifier with a true ground architecture. This architecture eliminates the need to use 2 external big capacitors required by conventional headphone amplifier.

The structure of the NCP2811 is basically composed of 2 true ground amplifiers, an UVLO, a short circuit protection and also a thermal shutdown. A special circuitry is embedded to eliminate any pop and click noise that occurs during turn on and turn off time. The A version has an external gain selectable by two resistor, B version has a gain of 1.5 V/V.

NOCAP™

NOCAP™ is a patented architecture which requires only 2 small ceramic capacitors. It generates a symmetrical positive and negative voltage and it allows the output of the amplifiers to be biased around the ground.

Current Limit Protection Circuit

The NCP2811 embed a protection circuitry against short to ground. When an output is shorted to GND and when a signal appears at the input, the current is limited to 300 mA.

Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceed 160°C, and will be switch on again when the temperature decrease below 140°C.

Under Voltage Lockout

When the battery voltage decreases below 2.3 V, the amplifiers are turned off. The hysteresis to turn on it again is 100 mV.

Pop and Click Suppression Circuitry

The NCP2811 includes a special circuitry to eliminate any pop and click noise during turn on and turn off time. Basic amplifier creates an offset during these transitions at the output which give a parasitic noise called “pop and click noise”. The NCP2811 eliminates this problem.

Gain Setting Resistor Selection (Rin & Rf, A version only)

R_{in} and R_f set the closed loop gain of the amplifier. A low gain configuration (close to 1) minimizes the THD + noise values and maximizes the signal to noise ratio.

A closed loop gain in the range of 1 to 10 is recommended to optimize overall system performance.

The formula to calculate the gain is:

$$Av = -\frac{R_f}{R_{in}}$$

Input Capacitor Selection

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with R_{in} (externally selectable for A version, 20 kΩ for B version).

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation in the audio bandwith (20 Hz – 20 kHz).

The cut off frequency for the input high−pass filter is:

$$F_c = \frac{1}{2\pi R_{in} C_{in}}$$

A F_c < 20 Hz is recommended.

Charge Pump Capacitor Selection

Use ceramic capacitor with low ESR for better performances. X5R / X7R capacitor is recommended.

The flying capacitor (C2) serves to transfer charge during the generation of the negative voltage.

The CPVM capacitor (C3) must be equal at least to the CFly capacitor to allow maximum transfer charge. The CPVM value must not exceed 1 μF. Higher capacitor value can damage the part.

Table 4 suggests typical value and manufacturer:

Table 4.

Value	Reference	Package	Manufacturer
1 μF	C1005X5R0J105K	0402	TDK
1 μF	GRM155R60J105K19	0402	Murata

Lower value of capacitors can be used but the maximum output power is reduced and the device may not operate to specifications.

Power Supply Decoupling Capacitor (C1)

The NCP2811 is a True Ground amplifier which requires the adequate decoupling capacitor to reduce noise and THD+N. Use X5R / X7R ceramic capacitor and place it closed to the CPVDD pin. A value of 1 μF is recommended.

Shutdown Function

The device enters in shutdown mode when shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 500 nA. In this configuration, the output impedance is 10 kΩ on each output.

Output Resistor for Capacitive Drive Capability

Under normal operation, NCP2811 maximum direct capacitive load is in the 80 pF range. If, for any reason, high value capacitive loads should be connected to NCP2811 outputs, an additional 10 Ω resistor should be placed between the NCP2811 output and the capacitive load to ensure amplifier stability.

Layout Recommendation

Connect C1 as close as possible of the Vp pin.

Connect C2 and C3 as close as possible of the NCP2811.

Route audio signal and AGND far from Vp, CPP, CPM, PVM and PGND to avoid any perturbation due to the switching.

Table 5. ORDERING INFORMATION

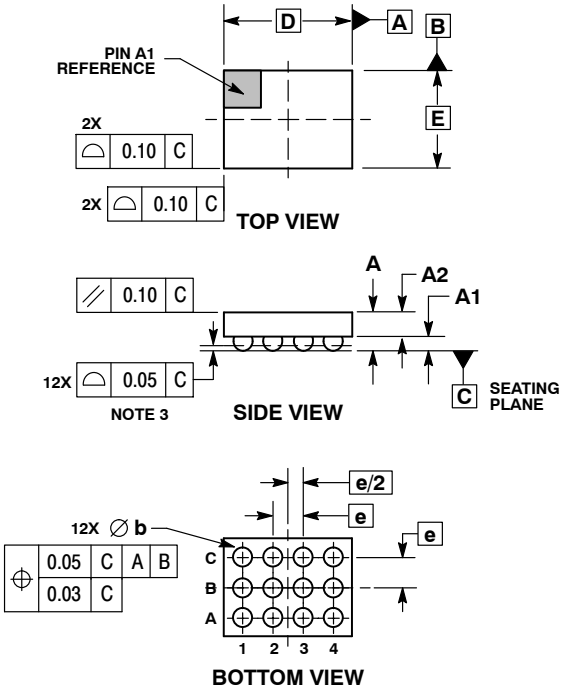
Device	Package	Shipping†
NCP2811ADTBR2G	TSSOP−14 (Pb−Free)	2500/Tape & Reel
NCP2811BDTBR2G	TSSOP−14 (Pb−Free)	2500/Tape & Reel
NCP2811AFCT1G	Flip−Chip 12 (Pb−Free)	3000/Tape & Reel
NCP2811BFCT1G	Flip−Chip 12 (Pb−Free)	3000/Tape & Reel
NCP2811BFCCT1G	Flip−Chip 12 (Backside Laminate Coating) (Pb−Free)	3000/Tape & Reel
NCP2811AMTTXG	WQFN12 (Pb−Fre)	3000/Tape & Reel
NCP2811BMTTXG	WQFN12 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

12 PIN FLIP−CHIP, 2.0x1.5, 0.5P
CASE 499AZ−01
ISSUE O

DATE 20 MAY 2008

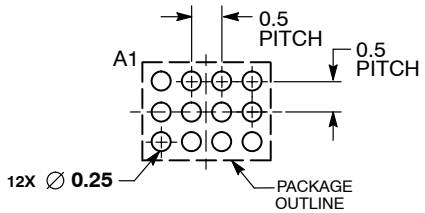
SCALE 4:1



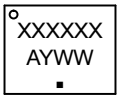
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.54	0.60
A1	0.21	0.27
A2	0.33	0.39
b	0.29	0.34
D	2.00 BSC	
E	1.50 BSC	
e	0.50 BSC	

SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

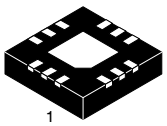
DOCUMENT NUMBER:	**98AON30285E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**12 PIN FLIP−CHIP, 2.0 X 1.5, 0.5P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

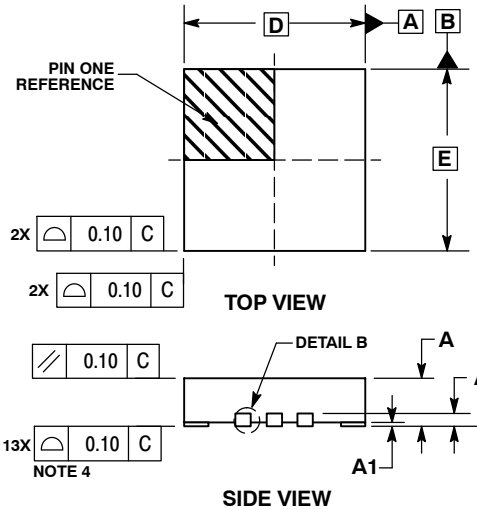
ON Semiconductor®

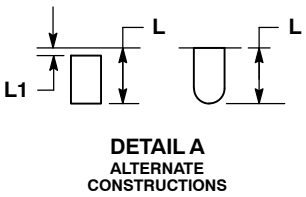
WQFN12 3x3, 0.5P
CASE 510AH−01
ISSUE O

DATE 20 JAN 2009

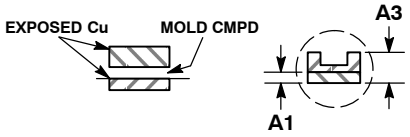


SCALE 4:1

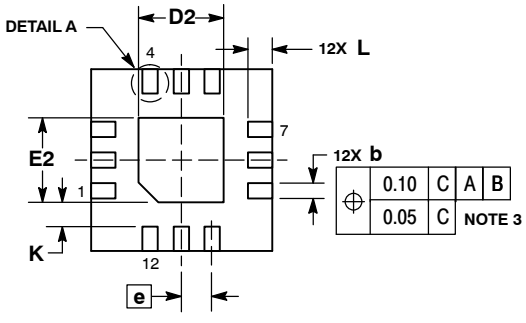




DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

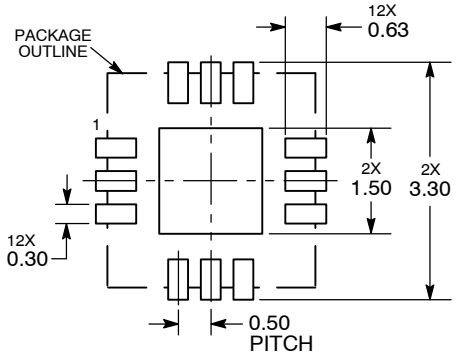
	MILLIMETERS	
DIM	MIN	MAX
A	0.65	0.85
A1	0.00	0.05
A3	0.22 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.30	1.50
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	WQFN12, 3X3, 0.5P		PAGE 1 OF 2

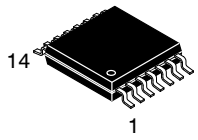
ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY J. SAMUDIO.	20 JAN 2009

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

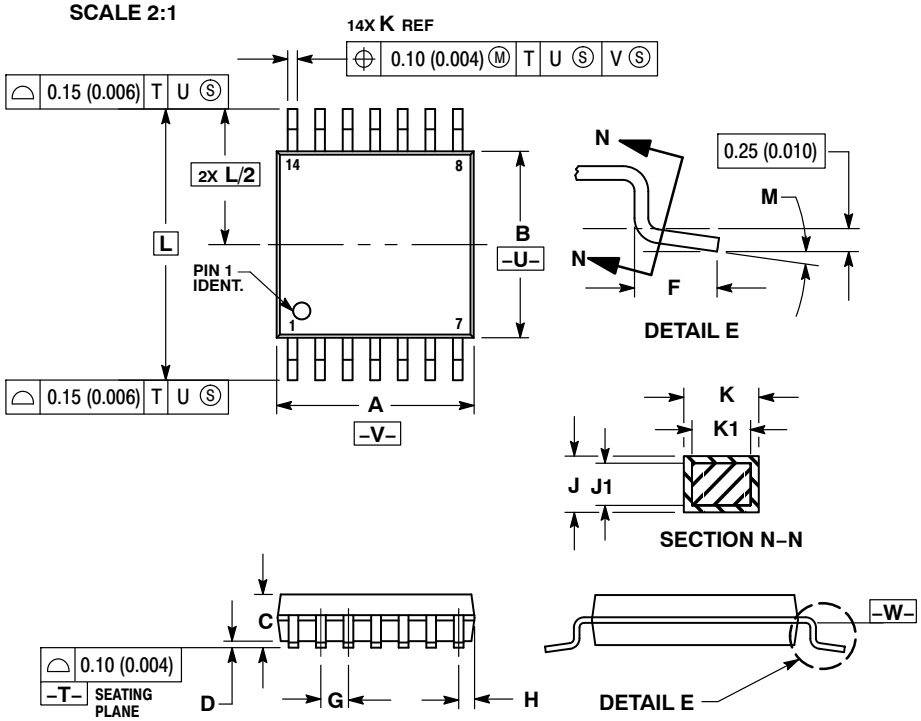
ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



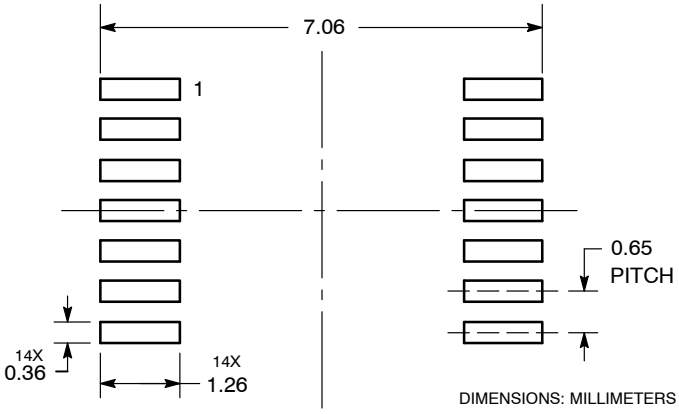
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

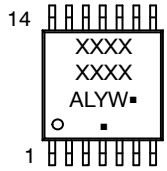
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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