MC10H125

Quad MECL-to-TTL Translator

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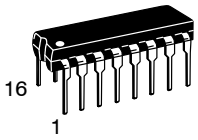
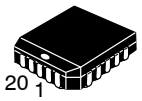


PDIP–16
P SUFFIX
CASE 648–08



PLLC–20
FN SUFFIX
CASE 775–02

Description

The MC10H125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10H part is a functional/pinout duplication of the standard MECL 10K™ family part, with 100% improvement in propagation delay, and no increase in power-supply current.

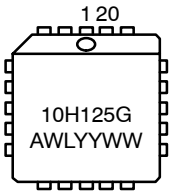
Outputs of unused translators will go to low state when their inputs are left open.

Features

- Propagation Delay, 2.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV
  (Over Operating Voltage and Temperature Range)
- MECL 10K Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAMS*

PDIP–16



PLLC–20

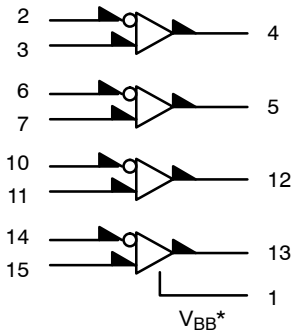
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC10H125FNG	PLLC–20 (Pb-Free)	46 Units / Tube
MC10H125FNR2G	PLLC–20 (Pb-Free)	500 Tape & Reel
MC10H125PG	PDIP–16 (Pb-Free)	25 Units / Tube

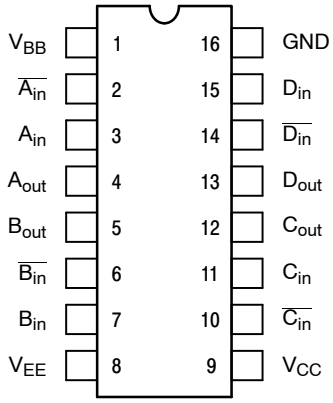
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



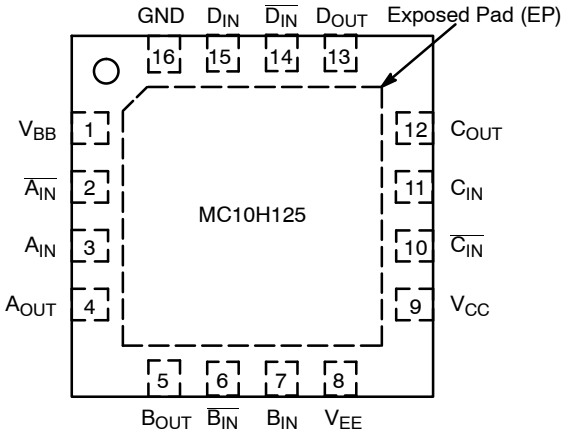
GND = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

*V_{BB} to be used to supply bias to the MC10H125 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

Figure 1. Logic Diagram



Pin assignment is for Dual−in−Line Package.
For PLCC pin assignment, see the Pin Conversion Tables.



Pin assignment for QFN16 Package.

Figure 2. Pin Assignment

Table 1. DIP CONVERSION TABLES

16−Pin DIL to 20−Pin PLCC

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16				
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20				

20−Pin DIL to 20−Pin PLCC

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Table 2. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 5.0 V)	−8.0 to 0	Vdc
V_{CC}	Power Supply (V_{EE} = −5.2 V)	0 to +7.0	Vdc
V_I	Input Voltage (V_{CC} = 5.0 V)	0 to V_{EE}	Vdc
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	 −55 to +150 −55 to +165	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V +5%; V_{CC} = 5.0 V + 5.0 %) (Note 2)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Negative Power Supply Drain Current	–	44	–	40	–	44	mA
I_{CCH}	Positive Power Supply Drain Current	–	63	–	63	–	63	mA
I_{CCL}		–	40	–	40	–	40	mA
I_{inH}	Input Current	–	225	–	145	–	145	μA
I_{CBO}	Input Leakage Current	–	1.5	–	1.0	–	1.0	μA
V_{OH}	High Output Voltage I_{OH} = −1.0 mA	2.5	–	2.5	–	2.5	–	Vdc
V_{OL}	Low Output Voltage I_{OL} = +20 mA	–	0.5	–	0.5	–	0.5	Vdc
V_{IH}	High Input Voltage (Note 1)	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
V_{IL}	Low Input Voltage (Note 1)	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc
I_{OS}	Short Circuit Current	60	150	60	150	50	150	mA
V_{BB}	Reference Voltage	−1.38	−1.27	−1.35	−1.25	−1.31	−1.19	Vdc
V_{CMR}	Common Mode Range (Note 3)	–	–	−2.85 to +0.3				V
		Typical						
V_{PP}	Input Sensitivity (Note 4)	150						mV

1. When V_{BB} is used as the reference voltage.
2. Each MECL 10H™ series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
3. Differential input not to exceed 1.0 Vdc.
4. 150 mV_{p-p} differential input required to obtain full logic swing on output.

Table 4. AC CHARACTERISTICS

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
t_{pd}	Propagation Delay	0.8	3.3	0.85	3.35	0.9	3.4	ns
t_r	Rise Time (Note 1)	0.3	1.2	0.3	1.2	0.3	1.2	ns
t_f	Fall Time (Note 1)	0.3	1.2	0.3	1.2	0.3	1.2	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Output Voltage = 1.0 V to 2.0 V. R_L = 500 Ω to GND and C_L = 25 pF to GND. Refer to Figure 1.

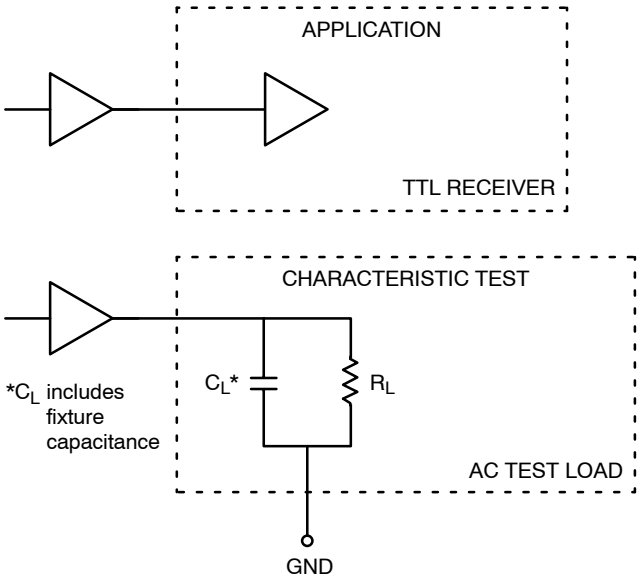


Figure 1. TTL Output Loading Used for Device Evaluation

APPLICATION INFORMATION

The MC10H125 incorporates differential inputs and Schottky TTL “totem pole” outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low-logic level whenever the inputs are left floating, and a high-logic output level is achieved with a minimum input level of 150 mV_{p-p}.

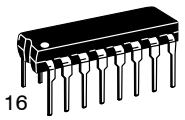
An advantage of this device is that MECL-level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 V and −5.2 V.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

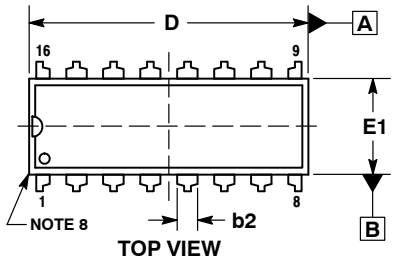
ON Semiconductor®

PDIP−16
CASE 648−08
ISSUE V

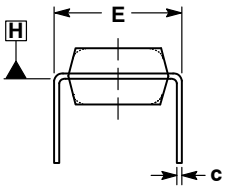
DATE 22 APR 2015



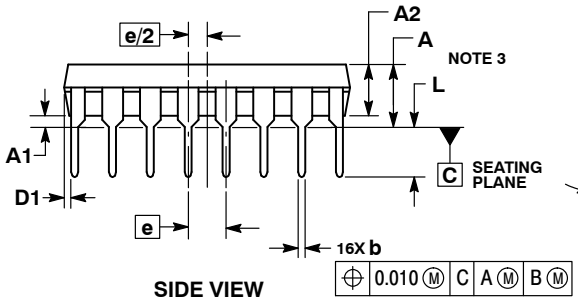
SCALE 1:1



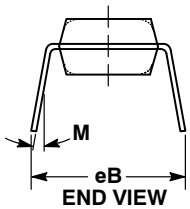
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



END VIEW
NOTE 6

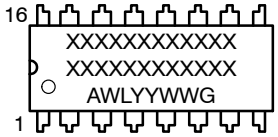
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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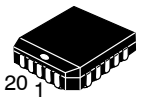
DESCRIPTION:	PDIP−16	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

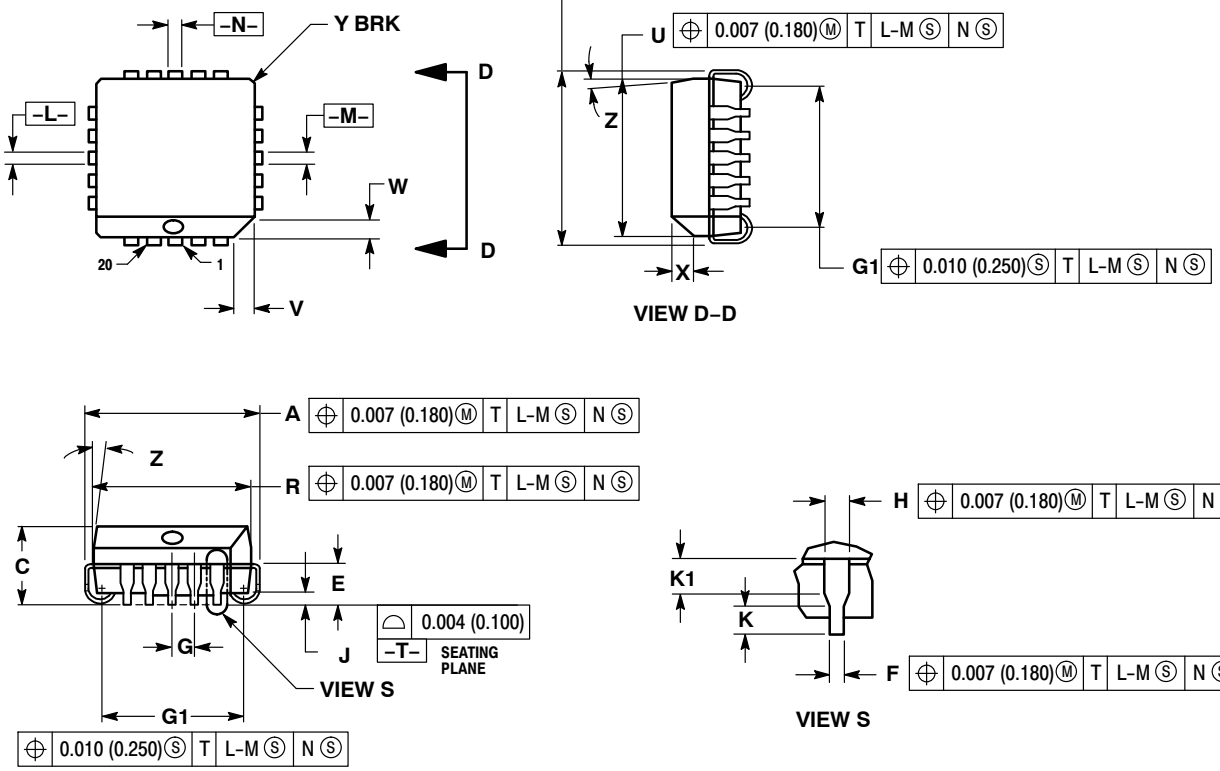
ON Semiconductor®



SCALE 1:1

20 LEAD PLCC
CASE 775–02
ISSUE G

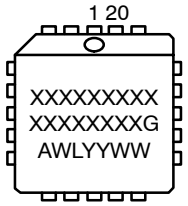
DATE 06 APR 2021



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS IN INCHES.
3. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

GENERIC MARKING DIAGRAM*



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DESCRIPTION:	**20 LEAD PLCC**	**PAGE 1 OF 1**

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