ON Semiconductor

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MOSFET, N-Channel, POWERTRENCH®

80 V, 80 A, 4.5 m Ω

FDWS86368-F085

Features

- Typical $R_{DS(on)} = 3.7 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- Typical $Q_{g(tot)}$ = 57 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- Wettable Flanks for Automatic Optical Inspection (AOI)
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

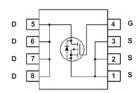
Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems



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DFN8 5.1x6.3, 1.27P CASE 506DW

MARKING DIAGRAM

O \$Y&Z&3&K FDWS86368

\$Y = ON Semiconductor Logo &Z = Assembly Plant Code &3 = Numeric Date Code &K = Lot Code

FDWS86368 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_J = 25°C, Unless otherwise noted)

Symbol	Parameter		Ratings	Units	
V _{DSS}	Drain-to-Source Voltage		80	V	
V_{GS}	Gate-to-Source Voltage		±20	V	
I _D	Drain Current —Continuous (V _{GS} = 10 V) (Note 1)	T _C = 25°C	80	А	
	-Pulsed	T _C = 25°C	See Figure 4		
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	82	mJ	
P _D	Power Dissipation		214	W	
	Derate Above 25°C		1.43	W/°C	
TJ, T _{STG}	Operating and Storage Temperature		-55 to +175	°C	
ReJC	Thermal Resistance, Junction to Case		0.7	°C/W	
RθJA	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	50	°C/W	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Current is limited by bondwire configuration.
- Starting T_J = 25°C, L = 40 μH, I_{AS} = 64 A, V_{DD} = 80 V during inductor charging and V_{DD} = 0 V during time in avalanche.
 RθJA is the sum of the junction–to–case and case–to–ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. Reuc is guaranteed by design, while Reua is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
FDWS86368	FDWS86368-F085	DFN8 5.1x6.3, 1.27P (Pb-Free)	3000 units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

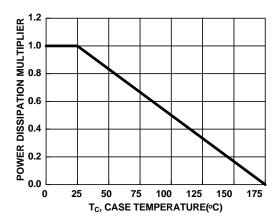
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Units
OFF CHAR	ACTERISTICS				-	•	
B _{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		80			V
I _{DSS}	Drain-to-Source Leakage	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 25^{\circ}\text{C}$ $V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 175^{\circ}\text{C} \text{ (Note 4)}$				1	μΑ
	Current					1	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V				±100	nA
ON CHAR	ACTERISTICS						
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$		2.0	3.0	4.0	V
R _{DS(on)}	Drain to Source On Resistance	I _D = 80 A, V _{GS} = 10 V, T _J = 25°C			3.7	4.5	mΩ
		I _D = 80 A, V _{GS} = 10 V, T _J = 175°C (Note 4)			7.4	9.0	
YNAMIC	CHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ $f = 1 \text{ MHz}$			4350		pF
C _{oss}	Output Capacitance				636		pF
C _{rss}	Reverse Transfer Capacitance				20		pF
R _g	Gate Resistance				2.5		Ω
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V	$V_{DD} = 64 \text{ V}, I_D = 80 \text{ A}$		57	75	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 V to 2 V]		8		nC
Q _{gs}	Gate-to-Source Gate Charge				23		nC
Q _{gd}	Gate-to-Drain "Miller" Charge				11		nC
WITCHIN	G CHARACTERISTICS						
t _{on}	Turn-On Time	$V_{DD} = 40 \text{ V}, I_D = 80 \text{ A},$	V_{GS} = 10V, R_{GEN} = 6 Ω			60	ns
t _{d(on)}	Turn-On Delay				23		ns
t _r	Rise Time				22		ns
t _{d(off)}	Turn-Off Delay				32		ns
t _f	Fall Time				13		ns
t _{off}	Turn-Off Time					59	ns
RAIN-SC	URCE DIODE CHARACTERISTI	cs					
V _{SD}	Source-to-Drain Diode Voltage	V _{GS} = 0 V, I _{SD} = 80 A V _{GS} = 0 V, I _{SD} = 40 A				1.25 1.2	V
t _{rr}	Reverse–Recovery Time	$I_F = 80 \text{ A}, \Delta I_{SD}/\Delta t = 100 \text{ A/}\mu\text{s}, V_{DD} = 64 \text{ V}$			58	75	ns
		<u>.</u>			i .	•	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS



200 CURRENT LIMITED $V_{GS} = 10V$ 175 BY PACKAGE € 150 CURRENT LIMITED BY SILICON ID, DRAIN CURRENT 125 100 75 50 25 O 75 100 125 150 175 T_C, CASE TEMPERATURE(°C) 25 200

Figure 1. Normalized Power Dissipation vs.

Case Temperature

Figure 2. Maximum Continuous Drain Current vs. Case Temperature

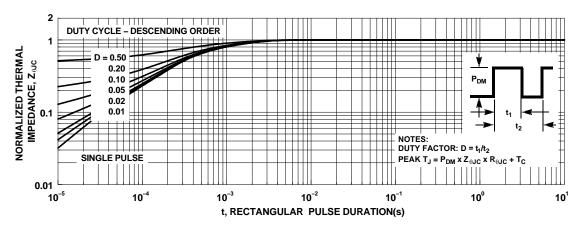


Figure 3. Normalized Maximum Transient Thermal Impedance

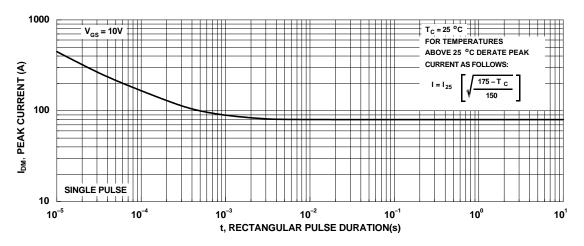


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

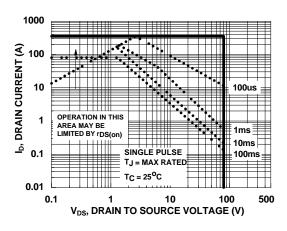


Figure 5. Forward Bias Safe Operating Area

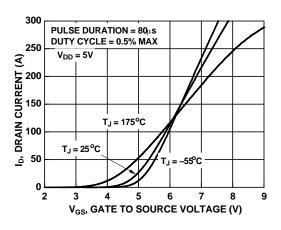


Figure 7. Transfer Characteristics

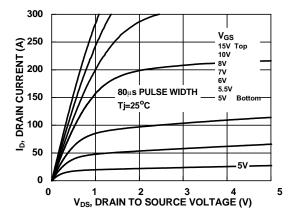
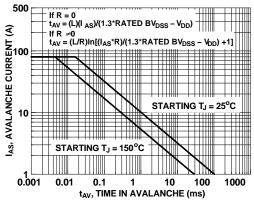


Figure 9. Saturation Characteristics



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

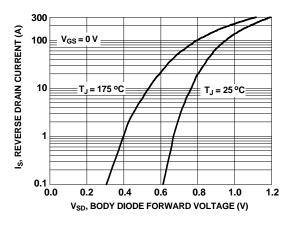


Figure 8. Forward Diode Characteristics

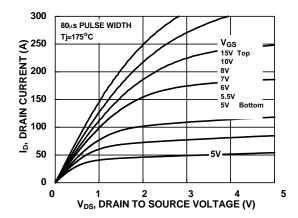


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

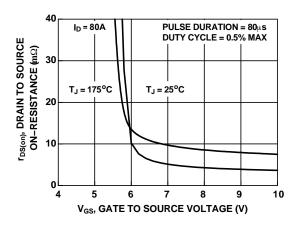


Figure 11. R_{DSON} vs. Gate Voltage

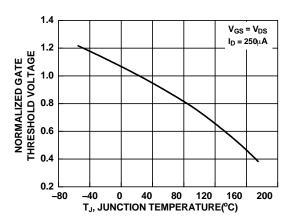


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

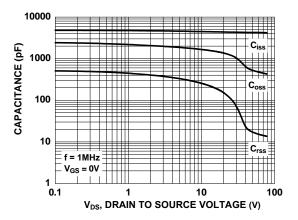


Figure 15. Capacitance vs. Drain to Source Voltage

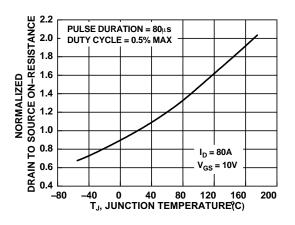


Figure 12. Normalized R_{DSON} vs. Junction Temperature

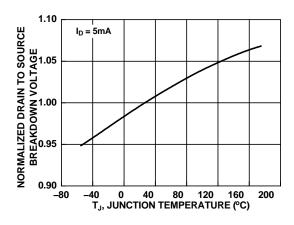


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

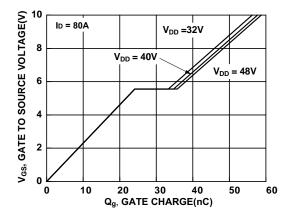


Figure 16. Single Pulse Maximum Power Dissipation

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS





// 0.10 C

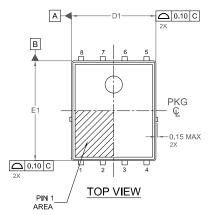
○ 0.10 C

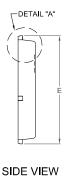
DFN8 5.1x6.3, 1.27PCASE 506DW ISSUE A

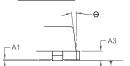
DATE 02 JUL 2021

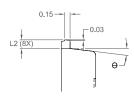
NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- 4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- 6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



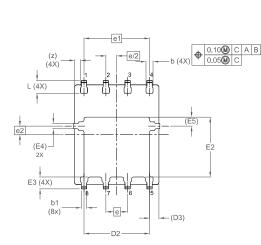






DETAIL "B"

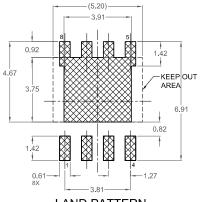
DETAIL "A"



BOTTOM VIEW

FRONT VIEW

DETAIL "B'



SEATING

LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS				
UIIVI	MIN.	NOM.	MAX.		
Α	0.90	1.00	1.10		
A1	0.00	-	0.05		
A3	0.20	0.25	0.30		
b	0.36	0.41	0.46		
b1	0.26	0.31	0.36		
D	4.90	5.00	5.20		
D1	4.80	4.90	5.00		
D2	3.72	3.82	3.92		
D3	0.54 REF				
Е	6.20	6.30	6.40		
E1	5.70	5.80	5.90		
E2	3.38	3.48	3.58		
E3	0.59	0.69	0.79		
E4	0.30 REF				
E5	0.52 REF				
е	1.27 BSC				
e/2	0.635 BSC				
e1	3.81 BSC				
e2	0.50 BSC				
L	0.64	0.74	0.84		
L2	0.15	0.25	0.35		
z	0.34 REF				
θ	0°	· - 7°			

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