Features

- Up to 96% Efficiency
- Up to 2.5A Max Output Current
- 1.2MHz Frequency
- PFM Mode for High Eff. in Light Load
- No Schottky Diode Required
- Tiny SOT23-5L Package
- Over Temperature Protected
- Short Circuit Protection
- Low Quiescent Current: 60uA
- Inrush Current Limit and Soft Start

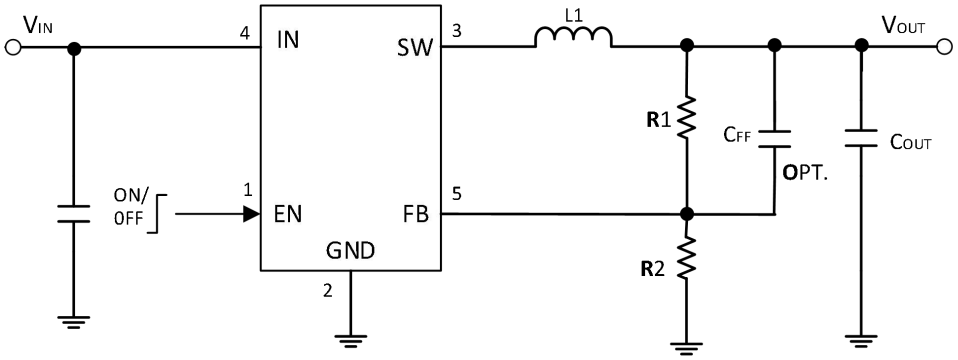
Applications

- MIDs, Tablet PC
- Set Top Boxes
- USB ports/Hubs
- Hot Swaps
- Cellphones
- PC Cards

Description

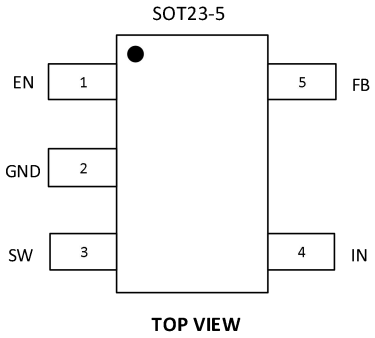
The HM8089 is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 2.5A of output current. The devices operate from an input voltage range of 2.5V to 5.5V and provide output voltages from 0.6V to VIN, making the HM8089 ideal for low voltage power conversions. Running at a fixed frequency of 1.2MHz allows the use of small inductance value and low DCR inductors, thereby achieving higher efficiencies. Other external components, such as ceramic input and output caps, can also be small due to higher switching frequency, while maintaining exceptional low noise output voltages. PWM/PFM mode operation provides very low output ripple voltage for noise sensitive applications. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability. HM8089 is housed in a tiny SOT23-5L package.

Typical Application Circuit



Basic Application Circuit

Pin Configuration



Order Information

PART No.	PACKAGE	Tape & Reel
HM8089	SOT23-5	3000/Reel

Absolute Maximum Ratings

Supply Voltage V_{IN} ..... –0.3V to +6.0V
Enable Voltage V_{EN} ..... –0.3V to V_{IN}V
Switch Node V_{SW} ..... –0.3V to V_{IN}+0.3V
Peak SW Sink and Source Current 3A
Thermal Resistance (θ_{JA}).....170°C/W
Thermal Resistance (θ_{JC}).....130°C/W

Operating Temperature Range...–40°C to +85°C
Junction Temperature .....+150°C
Lead Temperature ..... +260°C
Storage Temperature Range.... –65°C to +150°C
ESD, HBM 2KV
ESD, MM..... 200V

Electrical Characteristics

(V_{IN} = 5V, unless otherwise specified. Typical values are at TA = 25℃)

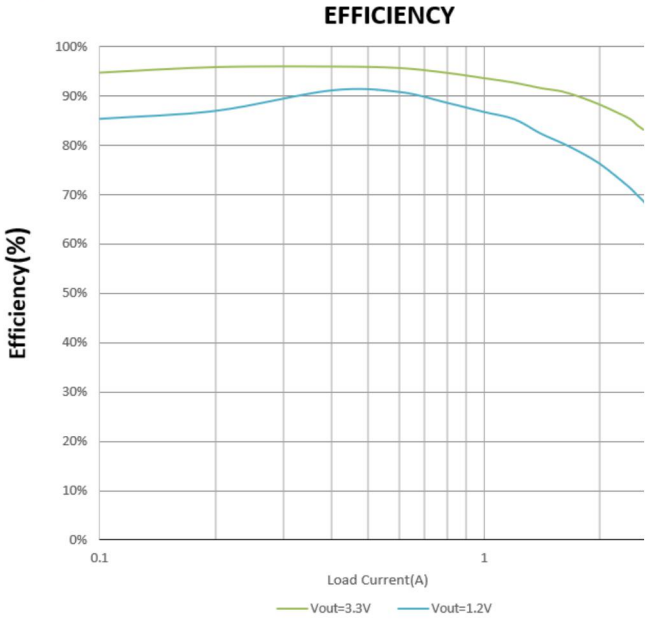
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	Vin		2.5		5.5	V
UVLO Threshold	Vuvlo			2.4		V
FB Feedback Voltage	Vref	V_{IN} =5V	0.586	0.6	0.614	V
Feedback Leakage current	Ifb			0.1		uA
Quiescent Current	Iq	V_{FB} =0.65V		60		uA
		Shutdown			1	uA
Line Regulation	LnReg	V_{IN} =2.5 to 5.5V		0.1	0.2	%/V
Load Regulation	LdReg	$I_{OUT=}$ 0.01A to 2.5A		0.1	0.2	%/A
Switching Frequency	Fsoc			1.2		MHz
PMOS Rdson	RdsonP			120		mΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NMOS Rdson	RdsonN			90		mΩ
Peak Current Limit	Ilimit			3.8		A
SW Leakage Current	Iswlk				1	uA
EN Leakage Current	Ienlk				1	uA
EN Input High Voltage	Vh_en		1.5			V
EN Input Low Voltage	Vl_en				0.5	V
Soft-Start				120		uS
Thermal Shutdown				160		℃
Thermal Hysteresis				20		℃

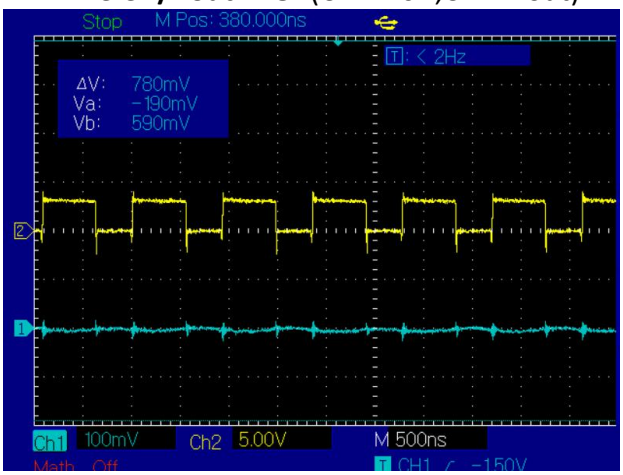
Pin Description

Pin	Name	Function
1	EN	Enable pin for the IC. Drive this pin high to enable the part, low to disable.
2	GND	Ground
3	SW	Inductor Connection. Connect an inductor Between SW and the regulator output.
4	IN	Supply Voltage. Bypass with a 10µF ceramic capacitor to GND
5	FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.6V and VIN

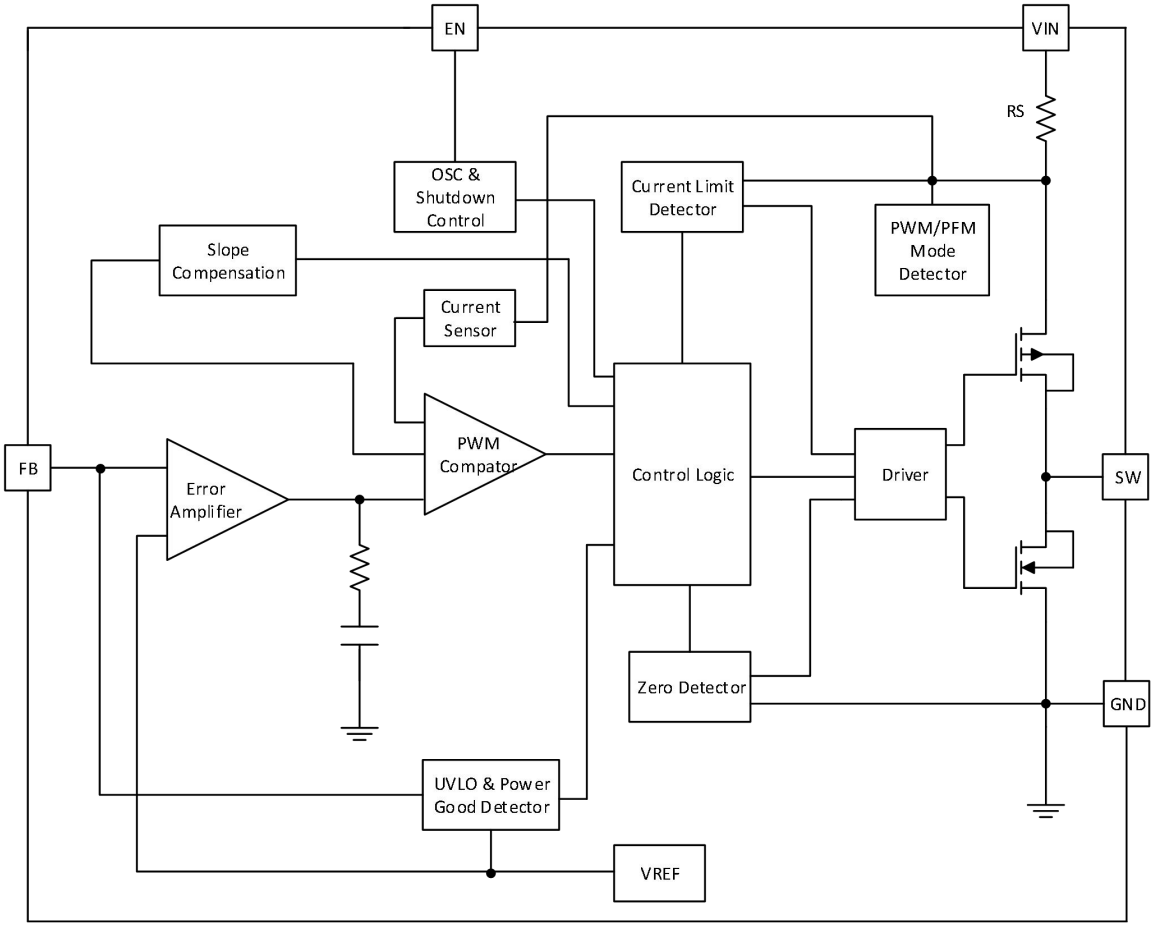
Typical Characteristics



Output Ripple and SW at 2.0A load
Vin=3.3V/Vout=1.8V(Ch1=Vsw,Ch2=Vout)



Block Diagram



Block Diagram

Function Description

The HM8089 high efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 2.5A of output current. The device operates in pulse-width modulation (PWM) at 1.5MHz from a 2.6V to 6V input voltage and provides an output voltage from 0.6V to VIN, making the HM8089 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

Loop Operation

HM8089 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET. When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. HM8089 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to I_{PEAK} and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

HM8089 has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the l soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If IN drops below 2.4V, the UVLO circuit inhibits switching. Once IN rises above 2.6V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Design Procedure

Setting Output Voltages

Output voltages are set by external resistors. The FBthreshold is 0.6V.

$R_{TOP} = R_{BOTTOM} x[(V_{OUT} / 0.6) - 1]$

Input Capacitor and Output Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. Input ripple with a ceramiccapacitor is approximately as follows:

$V_{RIPPLE} = IL_{(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{IN})]$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$V_{RIPPLE(ESR)} = IL_{(PEAK)} \times ESR$

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance.

Inductor Selection

A reasonable inductor value (LIDEAL) can be derived from the following:

L_{IDEAL} = [2(VIN) x D(1 - D)] / I_{OUT} x f_{OSC}

PCB Layout Guide

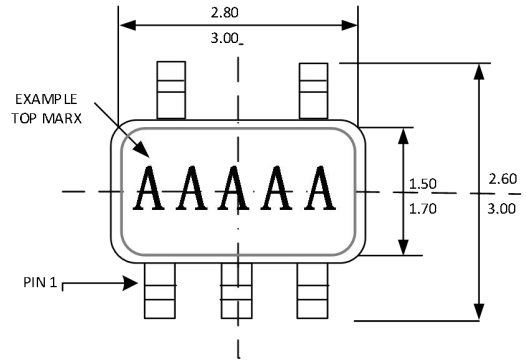
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary,please follow these guidelines.

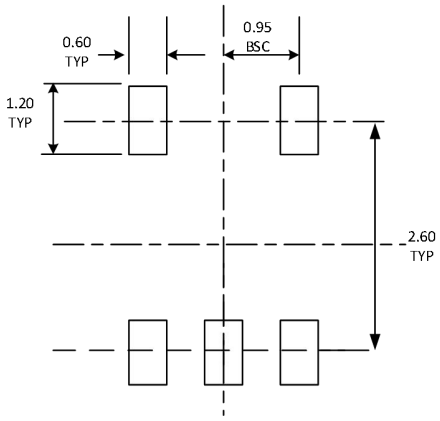
1) Keep the path of switching current short and minimize the loop area formed by input cap,high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the Vin pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Rout SW away from sensitive analog areas such as FB.
5) Connect IN,SW,and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

Package Outline

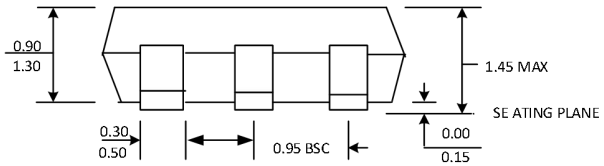
SOT23-5 PACKAGE OUTLINE AND DIMENSIONS



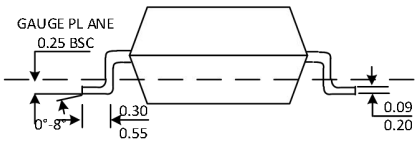
TOP VIEW



RECOMMEND ED PAD LAYOUT



FRONT VIEW



SIDE VIEW

NOTE:

1.CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.

2.PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

3.PACKAGE WIDTH DOES NOT INCLUDE INTERLEAN FLASH OR PROTRUSIONS.

4.LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004'' INCHES MAX.

5.DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.

6.DRAWING NOT TO SCALE.