DESCRIPTION

PT6315 is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/4 to 1/12 duty factor. Sixteen segment output lines, 4 grid output lines, 8 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6315 via a three-line serial interface. It is housed in a 44-pin LQFP.

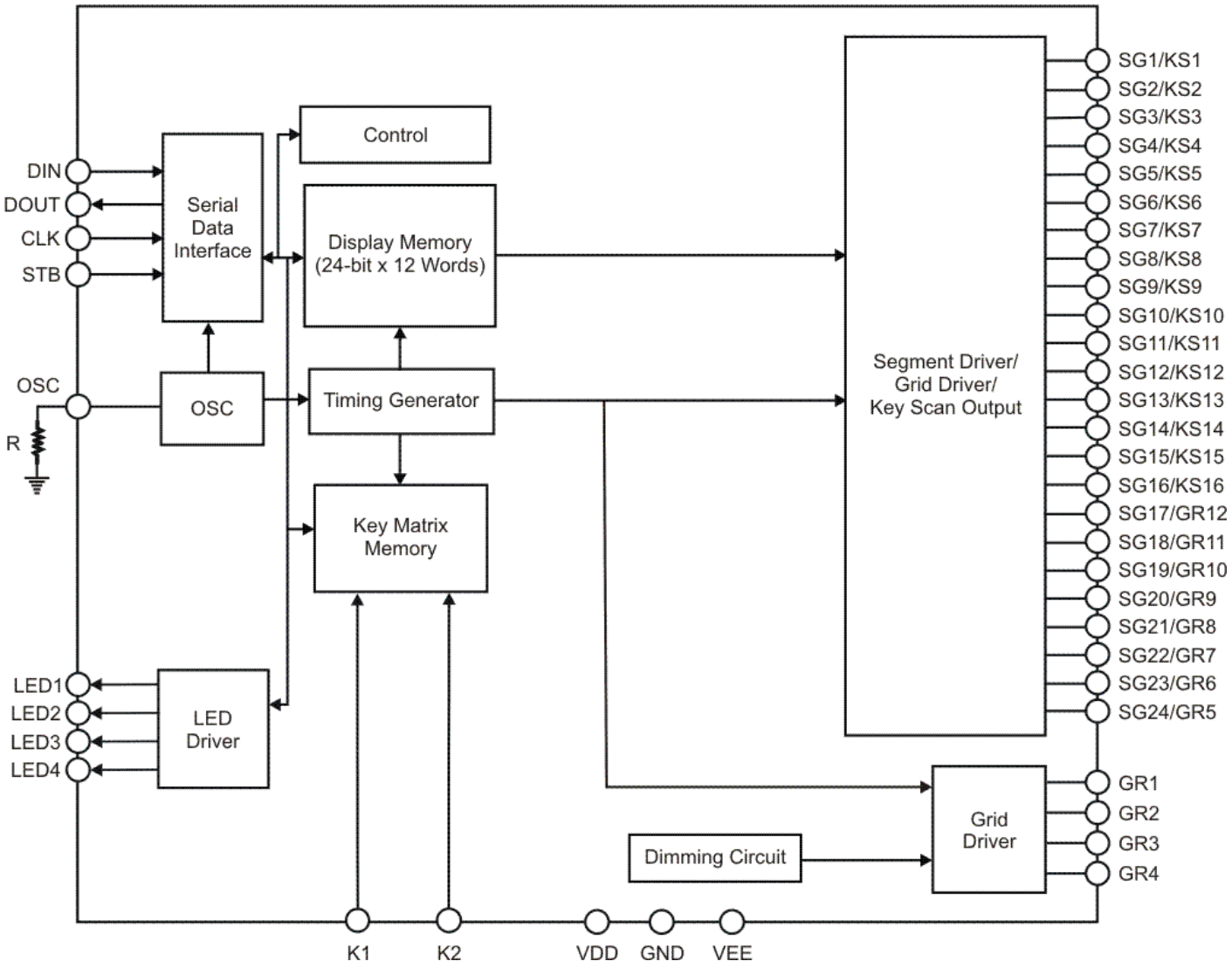
FEATURES

- CMOS Technology
- Low Power Consumption
- Key Scanning (16 x 2 matrix)
- Multiple Display Modes: (16 segments, 12 digits to 24 segments, 4 digits)
- 8-Step Dimming Circuitry
- LED Ports Provide (4 channels, 20mA max.)
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
- Available in 44-pin LQFP

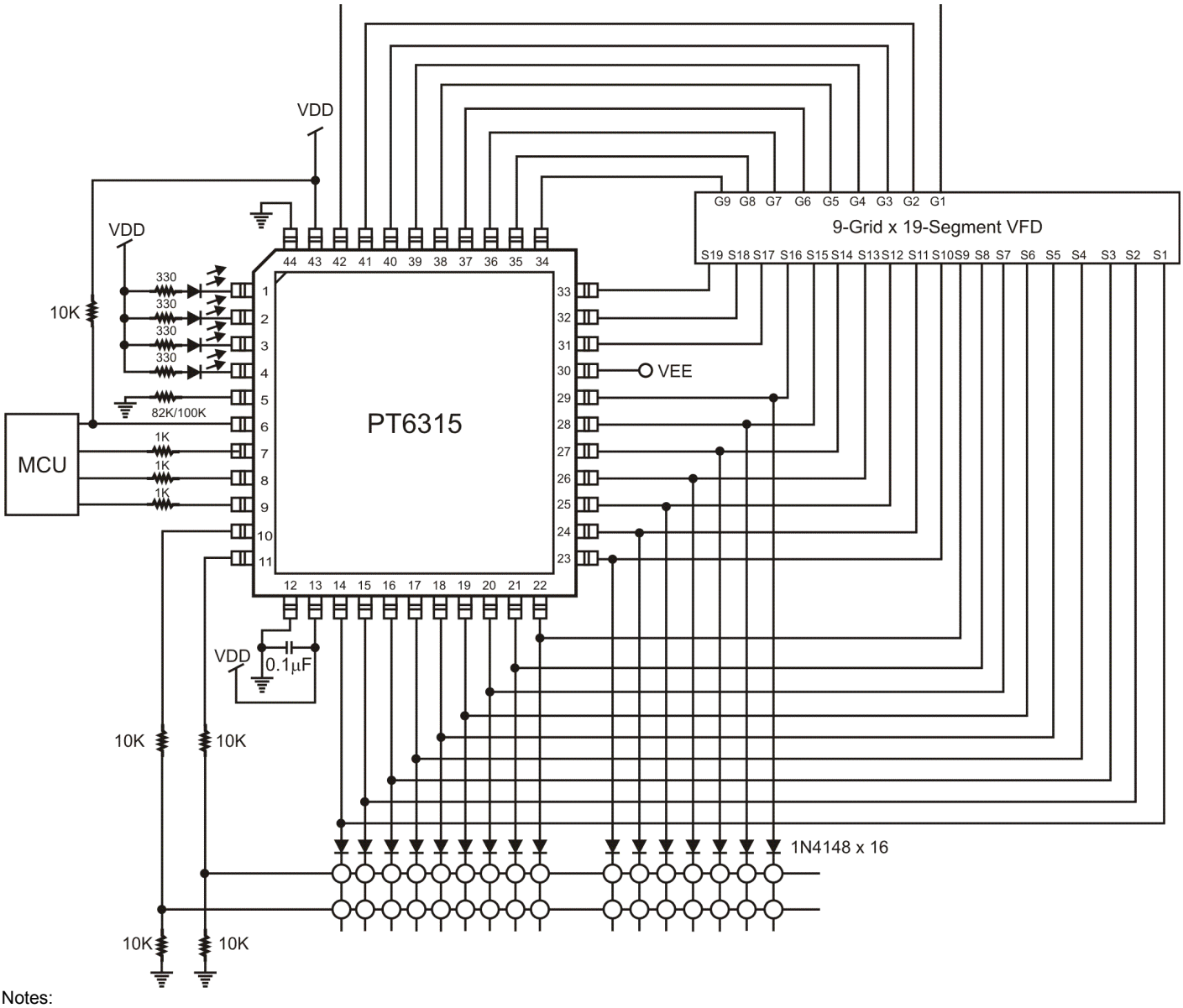
APPLICATION

- Microcomputer Peripheral Devices

BLOCK DIAGRAM



APPLICATION CIRCUIT

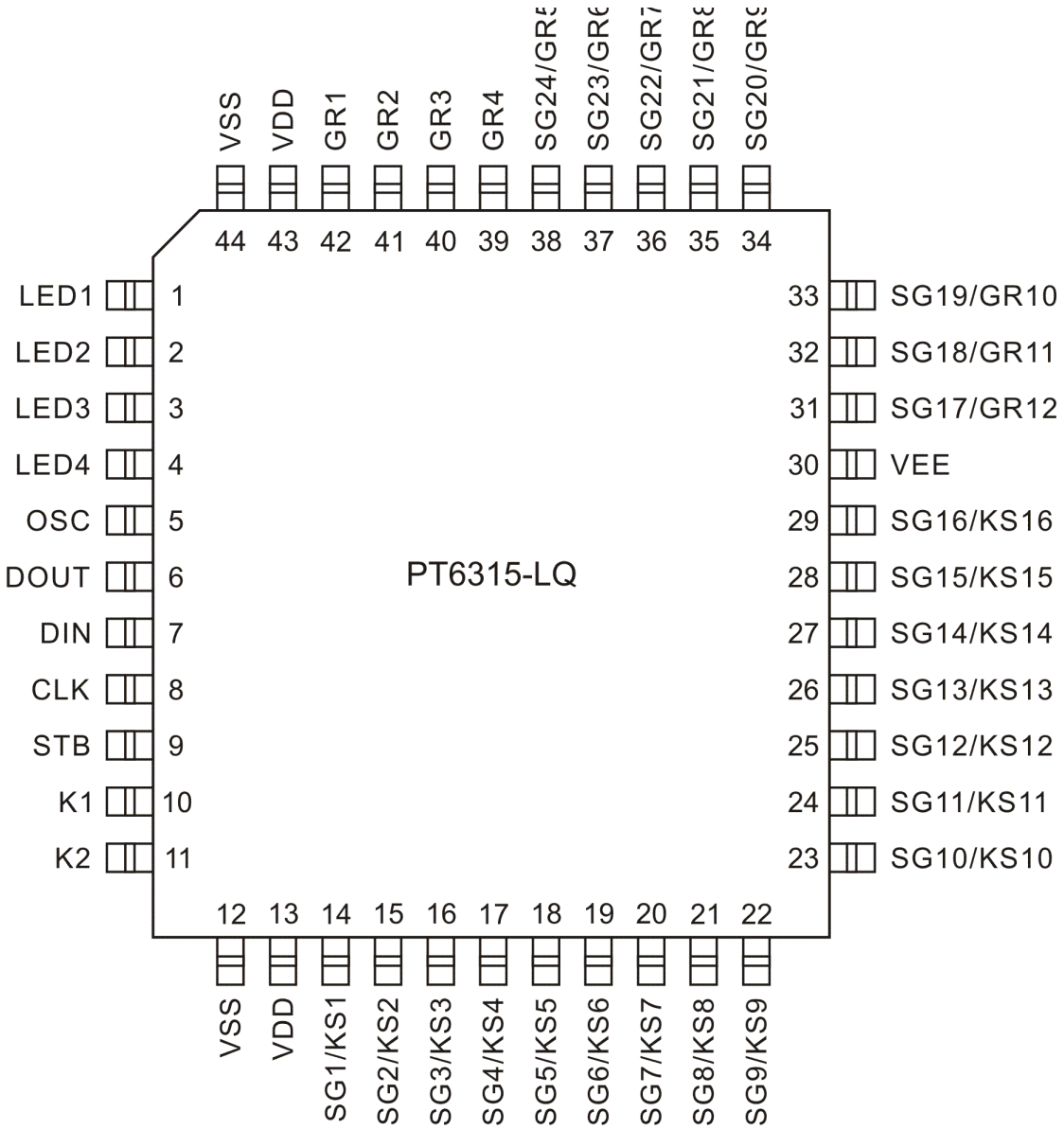


Notes:
1. The capacitor (0.1μF) connected between the GND and the VDD pins must be located as close as possible to the PT6315 chip.
2. Noise solution adds additional 1KΩ to avoid noise interruption at input pin.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6315	44-pin, LQFP	PT6315-LQ

PIN CONFIGURATION



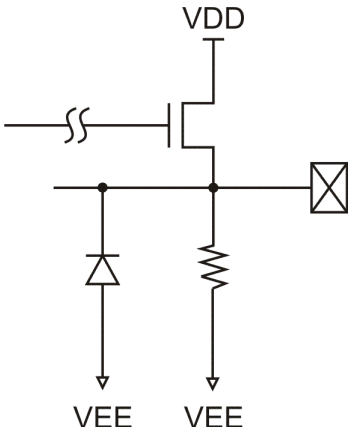
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
LED1 to LED4	O	LED Output Pin	1 to 4
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency.	5
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	6
DIN (Schmitt Trigger)	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit).	7
CLK (Schmitt Trigger)	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	8
STB (Schmitt Trigger)	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this in is “HIGH”, CLK is ignored.	9
K1, K2	I	Key Data Input Pins The data inputted to these pins is latched at the end of the display cycle.	10, 11
VSS	-	Logic Ground Pin	12, 44
VDD	-	Logic Power Supply	13, 43
SG1/KS1 to SG16/KS16	O	High-Voltage Segment Output Pins Also acts as the Key Source.	14 to 29
VEE	-	Pull-Down Level	30
SG17/GR12 to SG24/GR5	O	High-Voltage Segment/Grid Output Pins	31 to 38
GR4 to GR1	O	High-Voltage Grid Output Pins	39 to 42

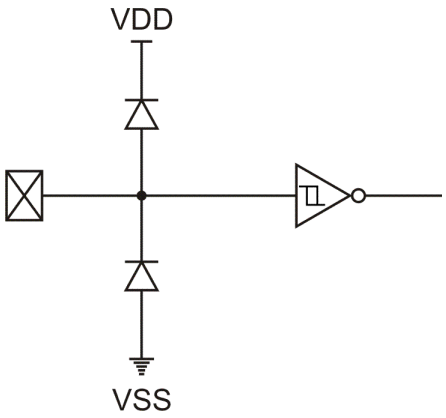
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

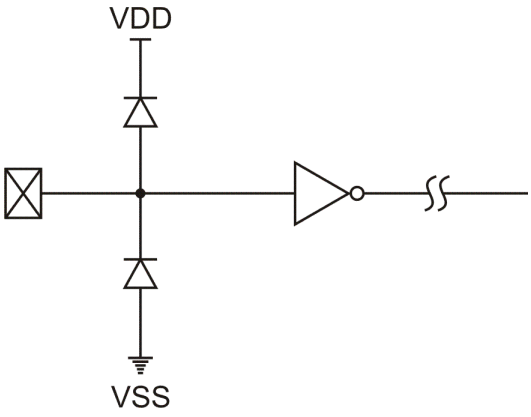
OUTPUT PINS: SGn, GRn



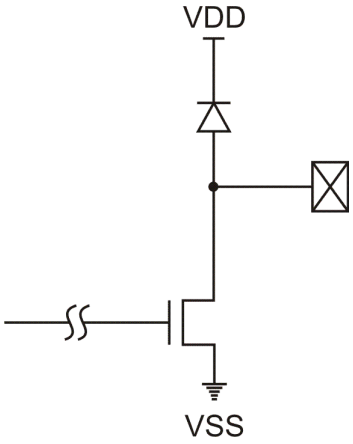
INPUT PINS: DIN, CLK, STB



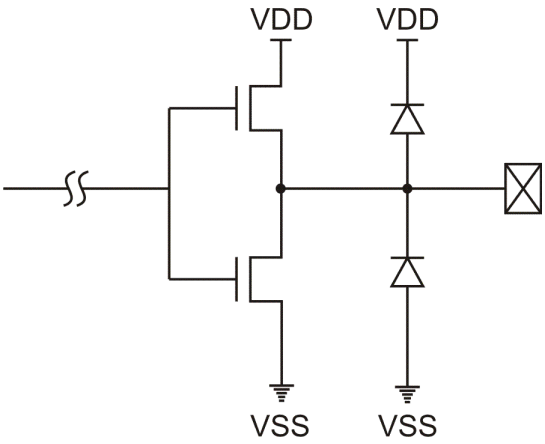
INPUT PINS: K1, K2



OUTPUT PIN: DOUT



OUTPUT PINS: LED1 TO LED4



FUNCTION DESCRIPTION

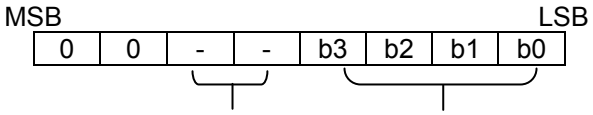
COMMANDS

Commands determine the display mode and status of PT6315. A command is the first byte (b0 to b7) inputted to PT6315 via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6315 provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6315 via the DIN Pin when STB is “LOW”. However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of “0”.
The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/12 duty, 16 to 24 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display command “ON” must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the 12-digit, 16-segment modes is selected.

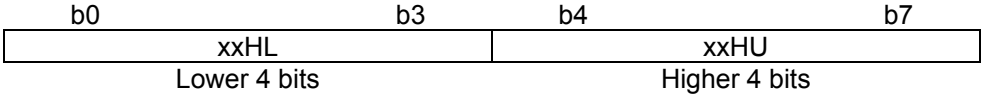


Display Mode Settings:
0000: 4 digits, 24 segments
0001: 5 digits, 23 segments
0010: 6 digits, 22 segments
0011: 7 digits, 21 segments
0100: 8 digits, 20 segments
0101: 9 digits, 19 segments
0110: 10 digits, 18 segments
0111: 11 digits, 17 segments
1XXX: 12 digits, 16 segments

DISPLAY MODE AND RAM ADDRESS

Data transmitted from an external device to PT6315 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6315 are given below in 8 bits unit.

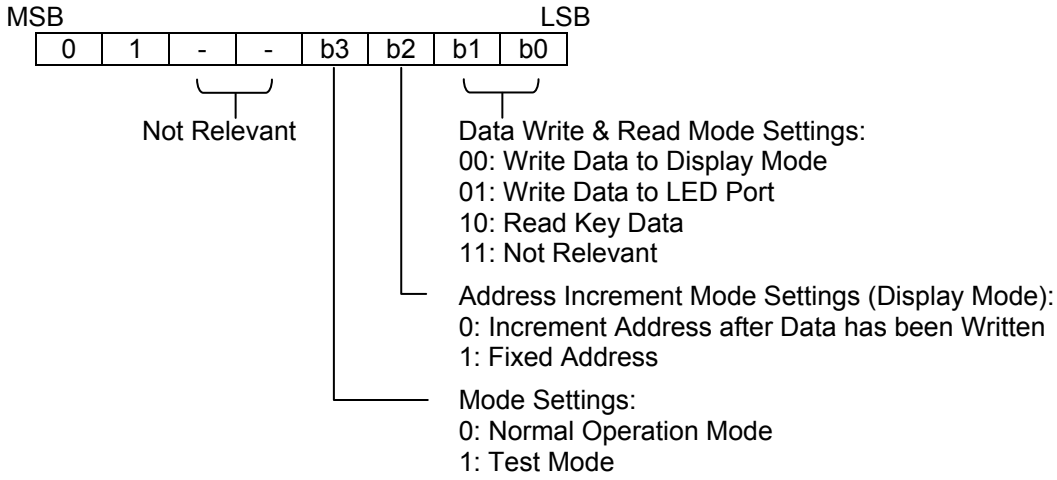
SG1 SG4	SG5 SG8	SG9 SG12	SG13 SG16	SG17 SG20	SG21 SG24	
00HL	00HU	01HL	01HU	02HL	02HU	DIG1
03HL	03HU	04HL	04HU	05HL	05HU	DIG2
06HL	06HU	07HL	07HU	08HL	08HU	DIG3
09HL	09HU	0AHL	0AHU	0BHL	0BHU	DIG4
0CHL	0CHU	0DHL	0DHU	0EHL	0EHU	DIG5
0FHL	0FHU	10HL	10HU	11HL	11HU	DIG6
12HL	12HU	13HL	13HU	14HL	14HU	DIG7
15HL	15HU	16HL	16HU	17HL	17HU	DIG8
18HL	18HU	19HL	19HU	1AHL	1AHU	DIG9
1BHL	1BHU	1CHL	1CHU	1DHL	1DHU	DIG10
1EHL	1EHU	1FHL	1FHU	20HL	20HU	DIG11
21HL	21HU	22HL	22HU	23HL	23HU	DIG12



COMMAND 2: DATA SETTING COMMANDS

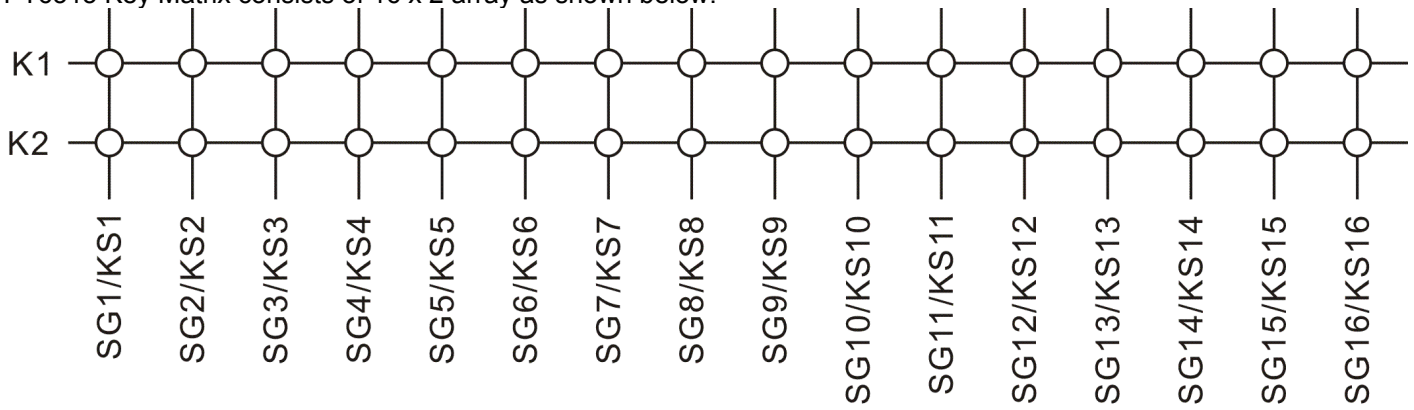
The Data Setting Commands executes the Data Write or Data Read Modes for PT6315. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of “1” while bit 8 (b7) is given the value of “0”. Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of “0”.



PT6315 KEY MATRIX & KEY INPUT DATA STORAGE RAM

PT6315 Key Matrix consists of 16 x 2 array as shown below:



Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG16, b7) has been read, the least significant bit of the next data (SG1, b0) is read.

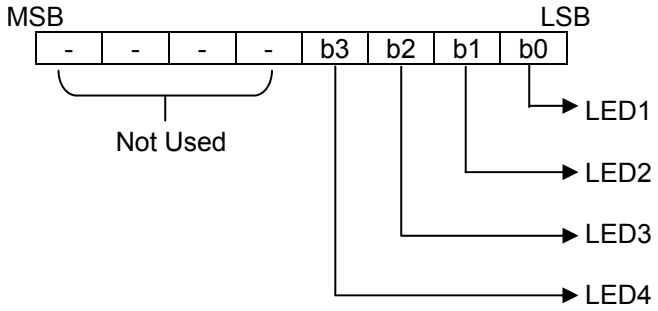
K1……K2	K1……K2	K1……K2	K1……K2
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8
SG9/KS9	SG10/KS10	SG11/KS11	SG12/KS12
SG13/KS13	SG14/KS14	SG15/KS15	SG16/KS16
b0……b1	b2……b3	b4……b5	b6……b7

Reading Sequence

LED DISPLAY

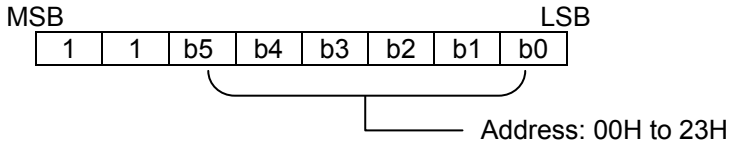
PT6315 provides 4 LED Display Terminals, namely LED1 to LED4. Data is written to the LED Port starting from the least significant bit (b0) of the port using a WRITE Command. Each bit starting from the least significant (b0) activates a specific LED Display Terminal -- b0 corresponds LED1 Display, b1 activates LED2 and so forth. Since there are only 4 LED display terminals, bits 5 to 8 (b4 ~ b7) are not used and therefore ignored. This means that b4 to b7 does NOT in anyway activate any LED Display, they are totally ignored.

When a bit (b0 ~ b3) in the LED Port is "1", the corresponding LED is OFF. Conversely, when the bit is "0", the LED Display is turned ON. For example, Bit 1 (as designated by b0) has the value of "1", then this means that LED1 is OFF. It must be noted that when power is turned ON, bit 1 to bit 4 (b0 to b3) are given the value of "0" (all LEDs are turned ON). Please refer to the diagrams below.



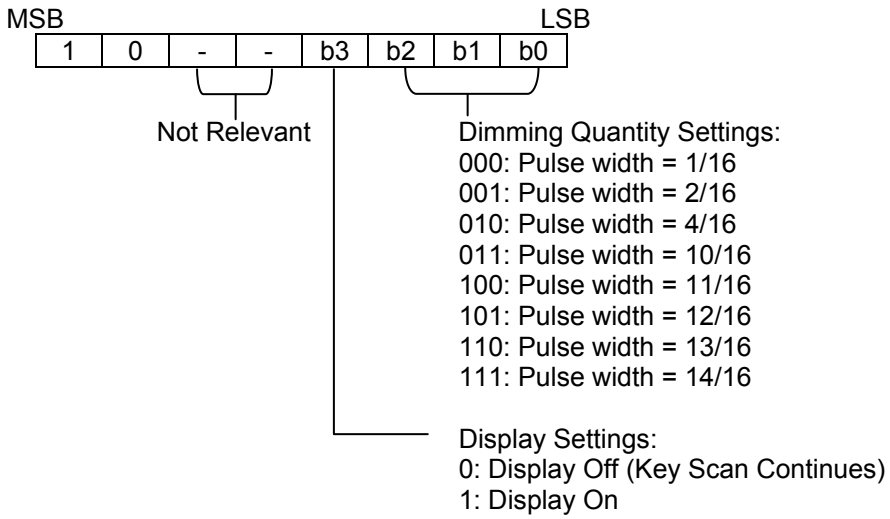
COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of "00H" to "23H". If the address is set to 24H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at "00H".
Please refer to the diagram below.



COMMAND 4: DISPLAY CONTROL COMMANDS

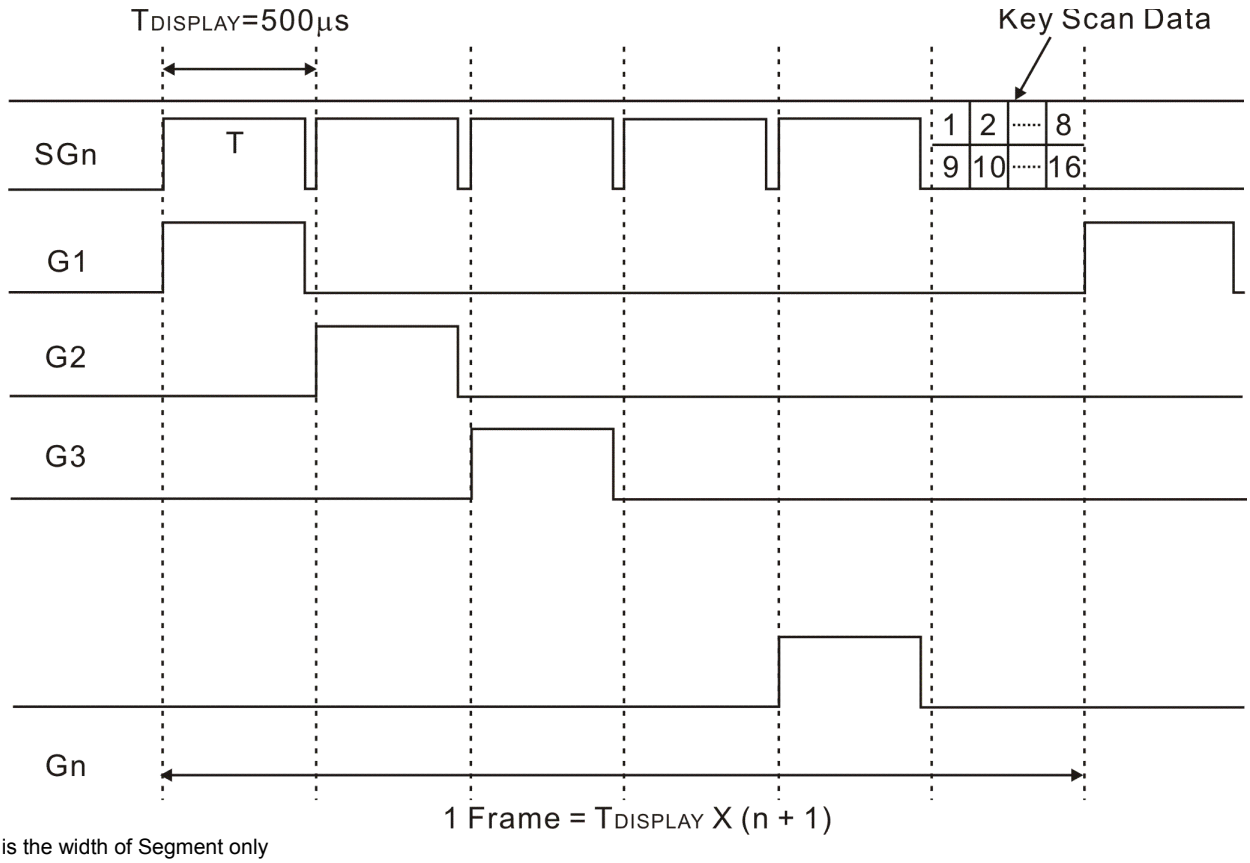
The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).



SCANNING AND DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 16 x 2 matrix is stored in the RAM.

Internal Operating Frequency (fosc) = 224/T

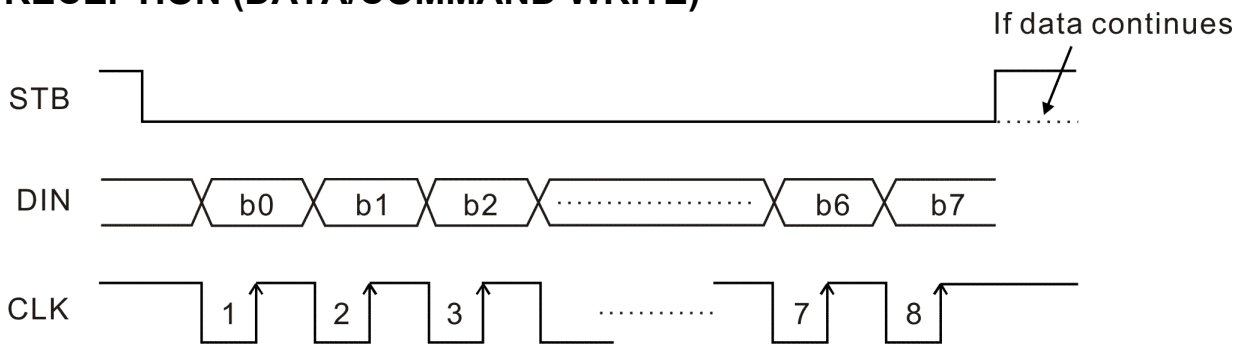


Note: T is the width of Segment only

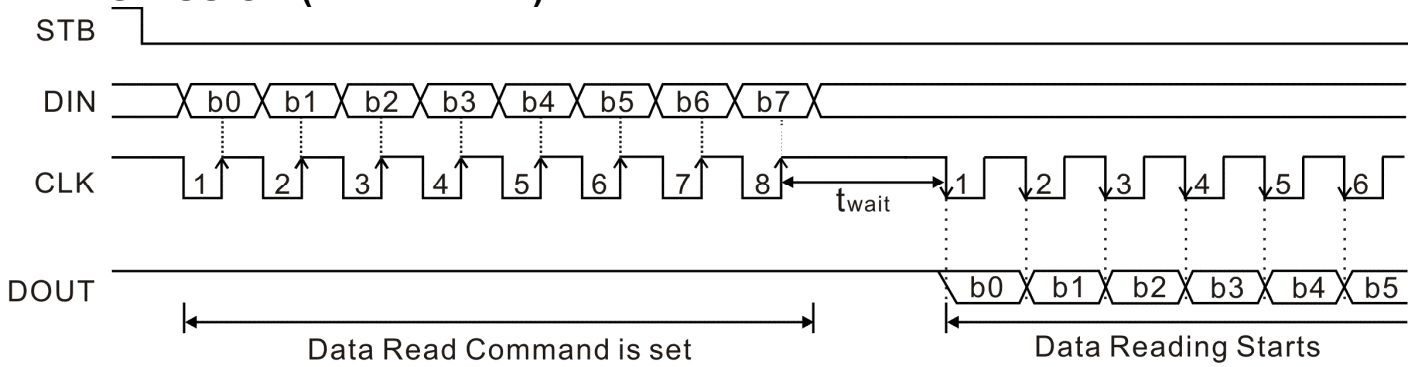
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6315 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1KΩ to 10KΩ) must be connected to DOUT.

RECEPTION (DATA/COMMAND WRITE)



TRANSMISSION (DATA READ)

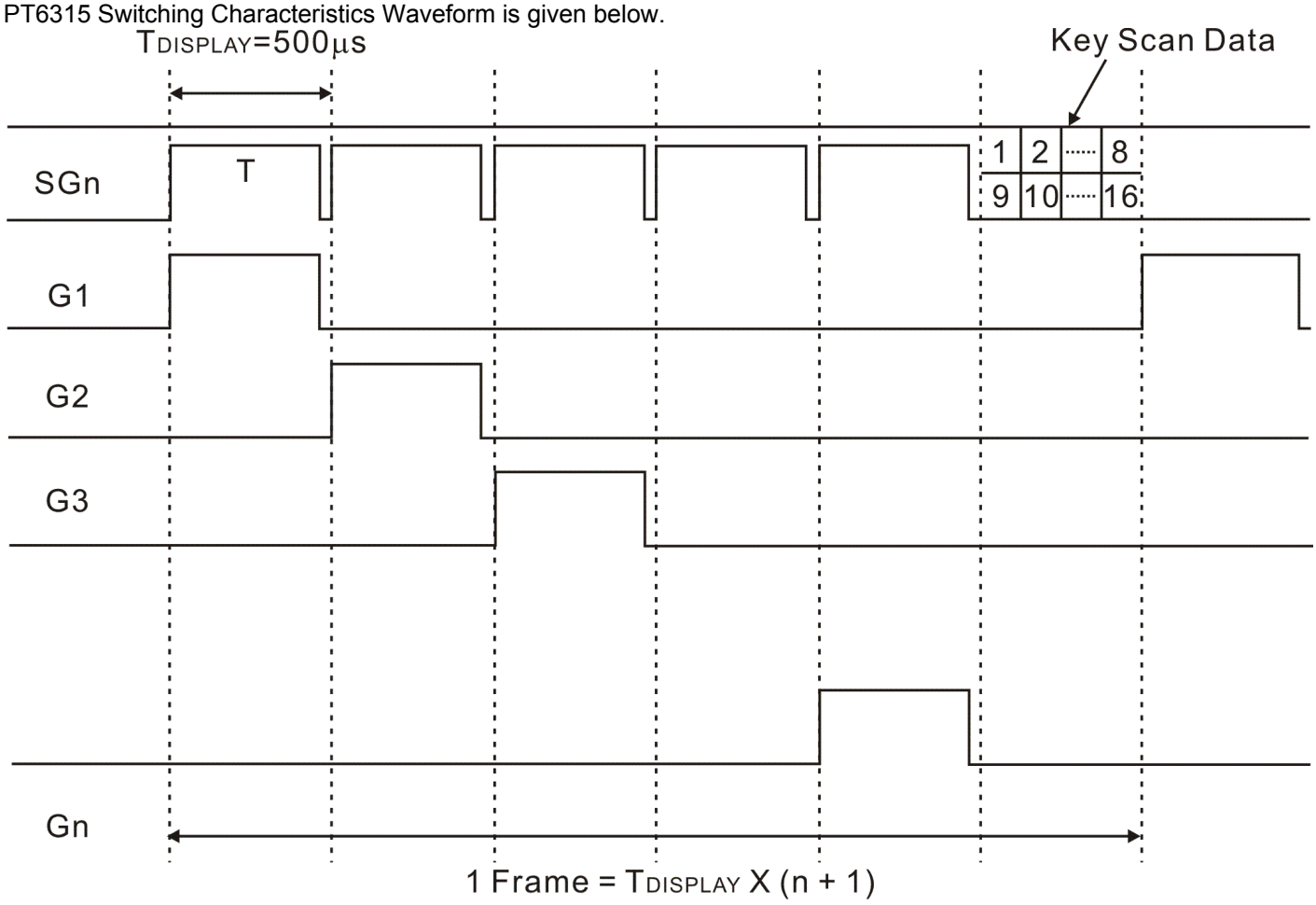


where: twait (waiting time) ≥ 1 μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1 μs.

SWITCHING CHARACTERISTIC WAVEFORM

PT6315 Switching Characteristics Waveform is given below.



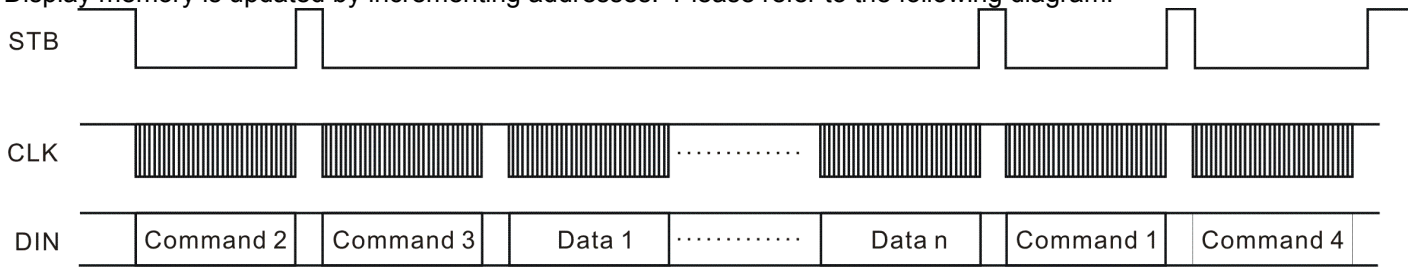
where:

fosc = Oscillation Frequency
PWSTB (Strobe Pulse Width) ≥ 1 µs
tsetup (Data Setup Time) ≥ 100 ns
tTZH1 (Segment Rise Time) ≤ 2.0 µs (VDD = 5 V)
tTZH2 (Grid Rise Time) ≤ 0.5 µs (VDD = 5 V)
tTHZ (Segment & Grid Fall Time) ≤ 150 µs
tPLZ (Propagation Delay Time) ≤ 400 ns (VDD = 5 V)

PWCLK (Clock Pulse Width) ≥ 400 ns
tCLK-STB (Clock - Strobe Time) ≥ 1 µs
thold (Data Hold Time) ≥ 100 ns
tTZH1 (Segment Rise Time) ≤ 4.0 µs (VDD = 3.3 V)
tTZH2 (Grid Rise Time) ≤ 1.2 µs (VDD = 3.3 V)
tPZL (Propagation Delay Time) ≤ 100 ns
tPLZ (Propagation Delay Time) ≤ 600 ns (VDD = 3.3 V)

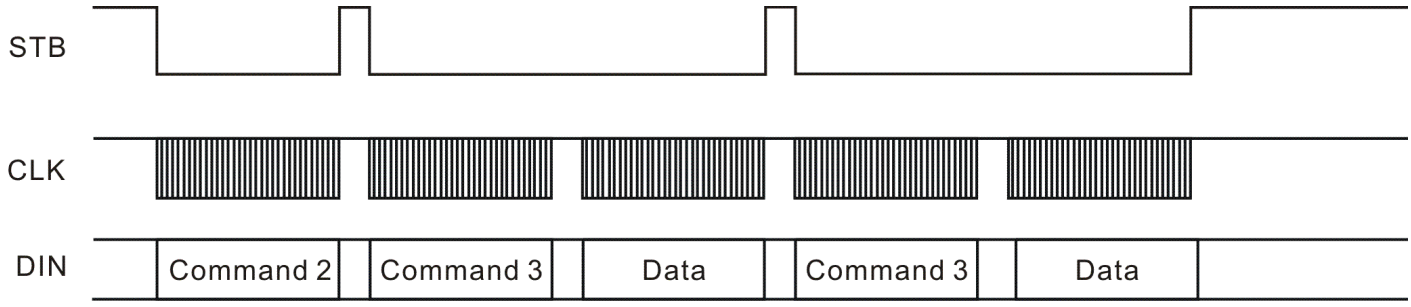
APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



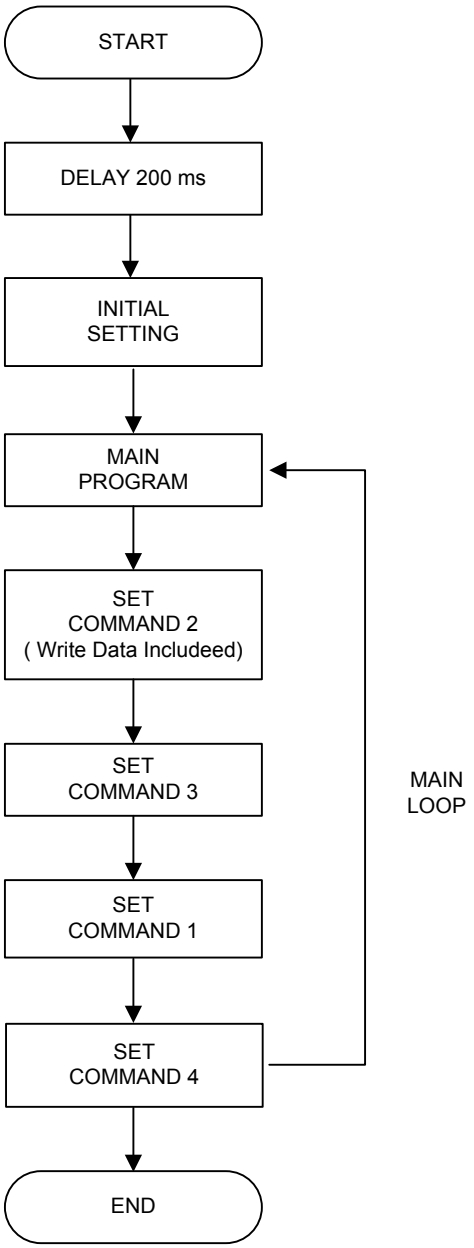
where:
Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n: Transfer Display Data (36 bytes max.)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.



where:
Command 2: Data Setting Command
Command 3: Address Setting Command
Data: Display Data

RECOMMENDED SOFTWARE FLOWCHART



Notes:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta = 25℃, GND = 0 V)

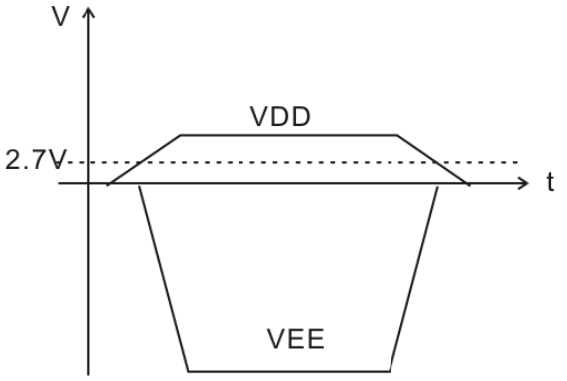
Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	VDD	-0.3 to +7	V
Logic Input Voltage	VI	-0.3 to VDD +0.3	V
VFD Driver Output Voltage	VO	VEE-0.3 to VDD +0.3	V
LED Driver Output Current	IOLED	±20	mA
VFD Driver Output Current	IOVFD	-40 (Grid) -15 (Segment)	mA
Operating Temperature	Topr	-40 to +85	℃
Storage Temperature	Tstg	-65 to +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta = 25℃, GND = 0 V)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Logic Supply Voltage	VDD	3.0	5	5.5	V
High-Level Input Voltage	VIH	0.7VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.3VDD	V
Driver Supply Voltage	VEE	VDD-35	-	0	V

POWER SUPPLY SEQUENCE



Note: The power on/off sequence suggestion:
Applications must observe the following sequence when turning the power on or off.

- At power on: First turn on the logic system power (VDD), and then turn on the driver power (VEE).
- At power off: First turn off the driver power (VEE), and then turn off the logic system power (VDD).

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD = 5 V, GND = 0 V, VEE = VDD-35 V, Ta = 25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Voltage	VOHLED	IOHLED = -12 mA LED1 to LED4	VDD-1	-	-	V
Low-Level Output Voltage	VOLLED	IOLLED = +15 mA LED1 to LED4	-	-	1	V
Low-Level Output Voltage	VOLDOUT	DOUT, IOLDOUT = 4 mA	-	-	0.4	V
High-Level Output Current	IOHSG	VO = VDD-2 V SG1/KS1 to SG16/KS16	-3	-	-	mA
High-Level Output Current	IOHGR	VO = VDD-2 V GR1 to GR4, SG17/GR12 to SG24/GR5	-15	-	-	mA
Oscillation Frequency	fosc	R = 82 KΩ	350	500	650	KHz
High Level Input Voltage	VIH	VDD = 5 V (DIN, CLK, STB)	0.7VDD	-	5	V
Low Level Input Voltage	VIL	VDD = 5 V (DIN, CLK, STB)	0	-	0.3VDD	V
Hysteresis Voltage	Vhys	VDD = 5 V (DIN, CLK, STB)	1.4	2.0	-	V
Input Current	II	VI = VDD or VSS	-	-	±1	μA
Dynamic Current Consumption	IDDdyn	Under no load, Display OFF	-	-	5	mA

Note: The frequency value is for PTC test condition: fosc = 224/T (see page 9 for detailed data)

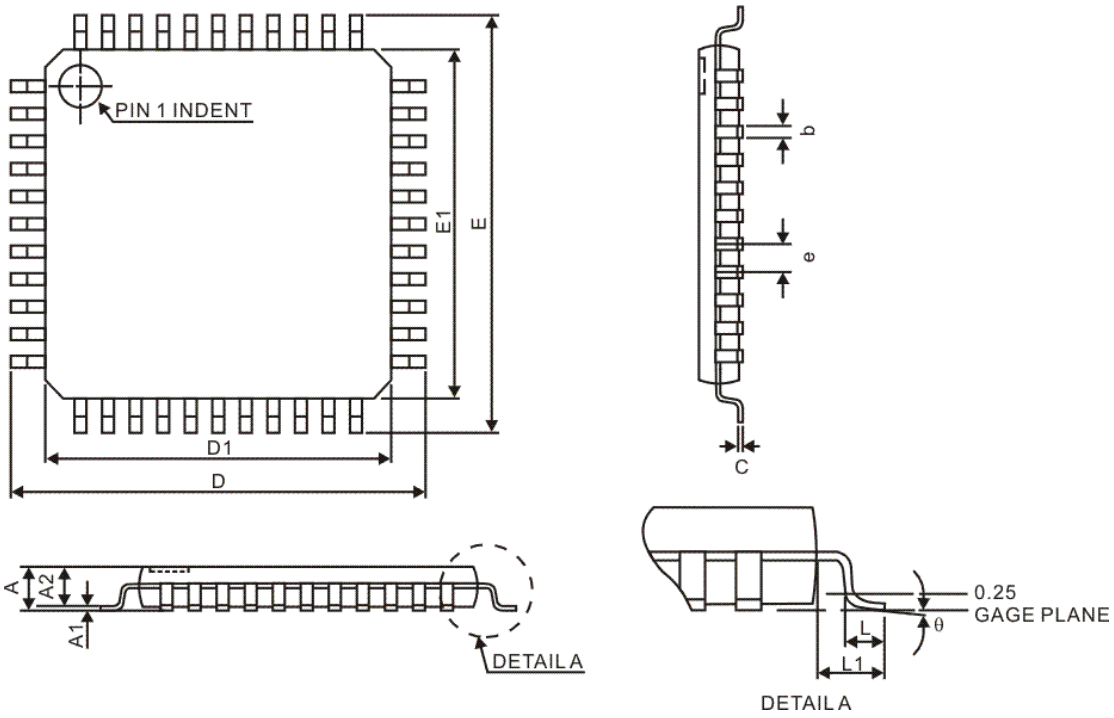
(Unless otherwise stated, VDD = 3.3 V, GND = 0 V, VEE = VDD-35 V, Ta = 25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Voltage	VOHLED	IOHLED = -6 mA LED1 to LED4	VDD-1	-	-	V
Low-Level Output Voltage	VOLLED	IOLLED = +15 mA LED1 to LED4	-	-	1	V
Low-Level Output Voltage	VOLDOUT	DOUT, IOLDOUT = 4 mA	-	-	0.4	V
High-Level Output Current	IOHSG	VO = VDD-2 V SG1/KS1 to SG16/KS16	-1.5	-	-	mA
High-Level Output Current	IOHGR	VO = VDD-2 V GR1 to GR4, SG17/GR12 to SG24/GR5	-6	-	-	mA
Oscillation Frequency	fosc	R = 100 KΩ	350	500	650	KHz
High Level Input Voltage	VIH	VDD = 3.3 V (DIN, CLK, STB)	0.7VDD	-	VDD	V
Low Level Input Voltage	VIL	VDD = 3.3 V (DIN, CLK, STB)	0	-	0.3VDD	V
Hysteresis Voltage	Vhys	VDD = 3.3 V (DIN, CLK, STB)	1.0	1.6	-	V
Input Current	II	VI = VDD or VSS	-	-	±1	μA
Dynamic Current Consumption	IDDdyn	Under no load, Display OFF	-	-	3	mA

Note: The frequency value is for PTC test condition: fosc = 224/T (see page 9 for detailed data)

PACKAGE INFORMATION

44-PIN, LQFP (BODY SIZE: 10MM X 10MM; PITCH: 0.80MM; THK BODY: 1.40MM)



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
C	0.09	-	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.8 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Notes:
1. All dimensions are in millimeters.
2. Refer to DEDEC MS-026BCB

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
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