



## Description

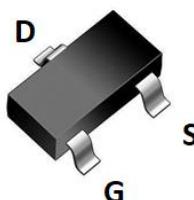
### JMT P-channel Enhancement Mode Power MOSFET

#### Features

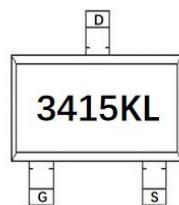
- $V_{DS} = -20V$ ,  $I_D = -4.1A$
- $R_{DS(ON)} < 40m\Omega$  @  $V_{GS} = -4.5V$
- $R_{DS(ON)} < 56m\Omega$  @  $V_{GS} = -2.5V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired
- ESD Rating: HBM 2.0KV

#### Application

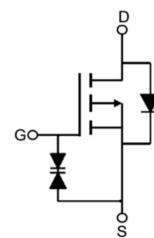
- PWM Applications
- Load Switch
- Power Management



SOT-23 top view



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
3415KL	JMTL3415KL	TAPING	SOT-23	7inch	3000	180000

## Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
$V_{DSS}$	Drain-Source Voltage		-20	V
$V_{GSS}$	Gate-Source Voltage		$\pm 10$	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ C$	-4.1	A
		$T_A = 100^\circ C$	-2.7	
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>		-16.4	A
$P_D$	Power Dissipation	$T_A = 25^\circ C$	1.1	W
$R_{QJA}$	Thermal Resistance, Junction to Ambient		114	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

**Electrical Characteristics** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

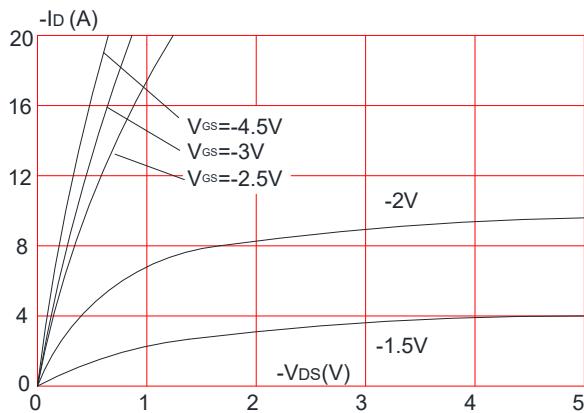
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D = -250\mu\text{A}$	-20	-	-	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V},$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 10\text{V}$	-	-	$\pm 10$	$\mu\text{A}$
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.4	-0.7	-1.0	V
$R_{DS(\text{on})}$ note2	Static Drain-Source on-Resistance	$V_{GS} = -4.5\text{V}, I_D = -4\text{A}$	-	31	40	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -3\text{A}$	-	40	56	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$	-	289	-	pF
$C_{oss}$	Output Capacitance		-	98	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	22	-	pF
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{V}, I_D = -4.1\text{A}, V_{GS} = -4.5\text{V}$	-	9	-	nC
$Q_{gs}$	Gate-Source Charge		-	1	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	2.6	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = -10\text{V}, R_G = 1\Omega, V_{GEN} = -4.5\text{V}, R_L = 1.2\Omega$	-	12	-	ns
$t_r$	Turn-on Rise Time		-	35	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	30	-	ns
$t_f$	Turn-off Fall Time		-	10	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_s$	Maximum Continuous Drain to Source Diode Forward Current	-	-	-4.1	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	-16.4	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_s = -4.1\text{A}$	-	-	-1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

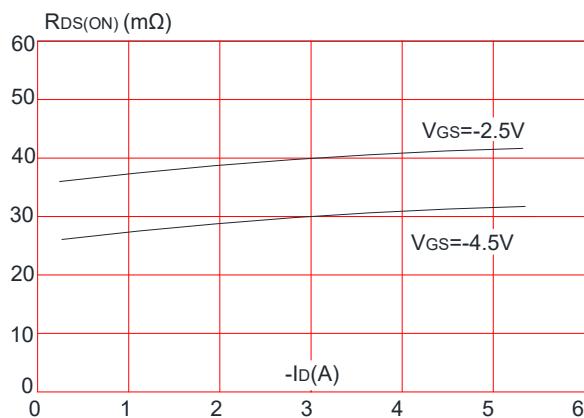
2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$ , Duty Cycle $\leq 2\%$

## Typical Performance Characteristics

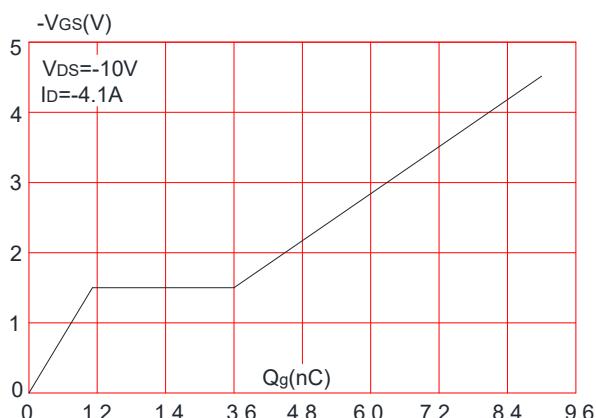
**Figure 1:** Output Characteristics



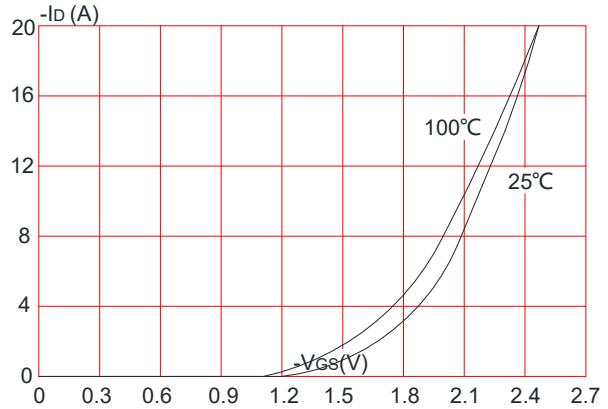
**Figure 3:** On-resistance vs. Drain Current



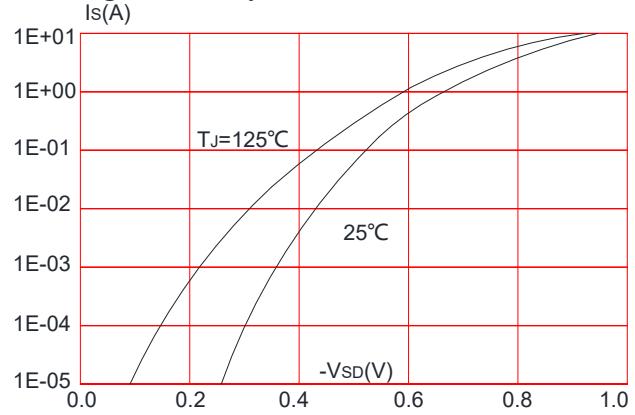
**Figure 5:** Gate Charge Characteristics



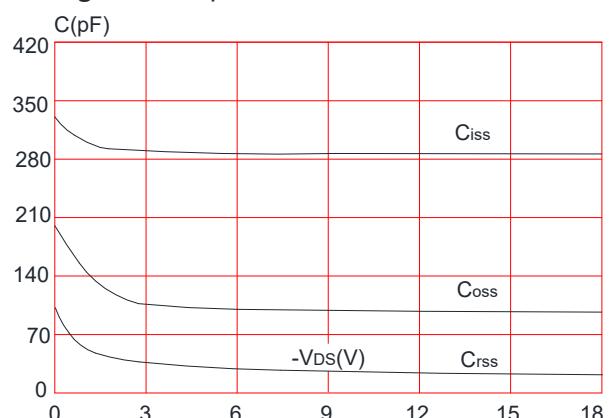
**Figure 2:** Typical Transfer Characteristics



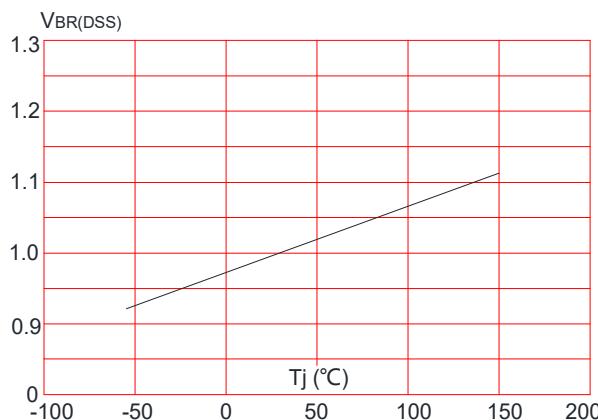
**Figure 4:** Body Diode Characteristics



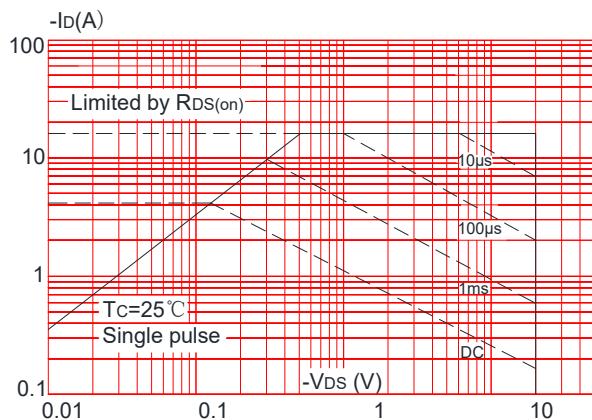
**Figure 6:** Capacitance Characteristics



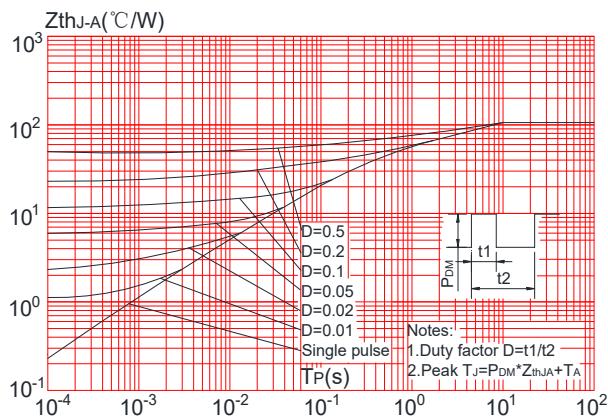
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



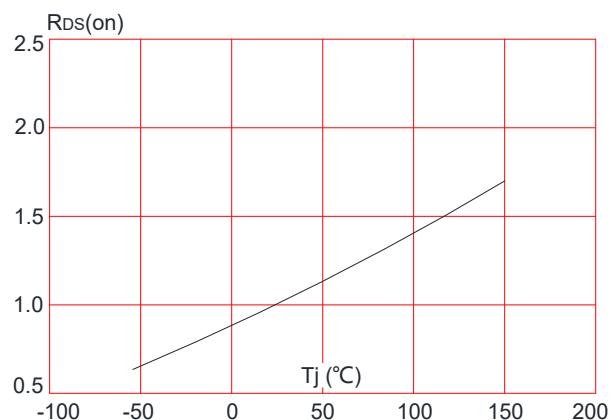
**Figure 9:** Maximum Safe Operating Area



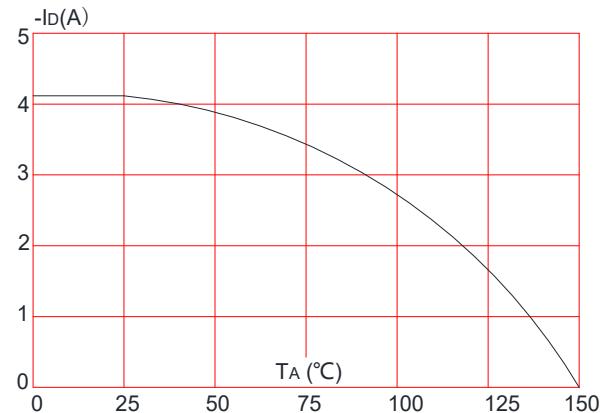
**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



**Figure 8:** Normalized on Resistance vs. Junction Temperature

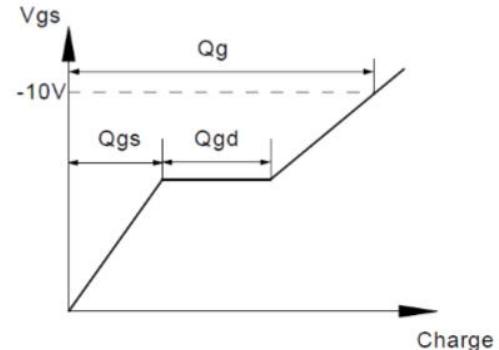
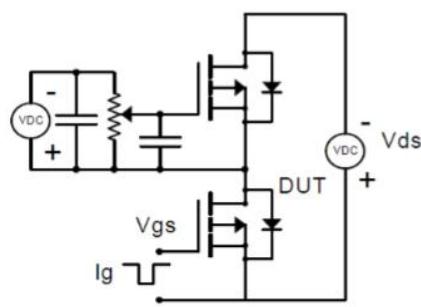


**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature

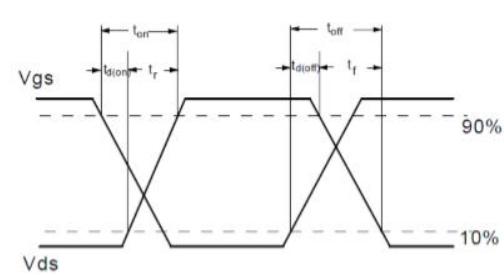
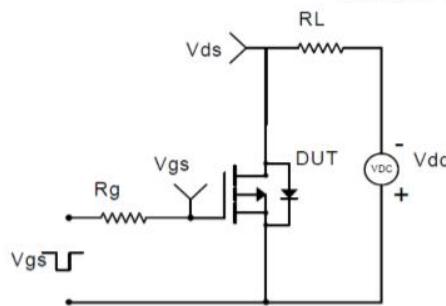


## Test Circuit

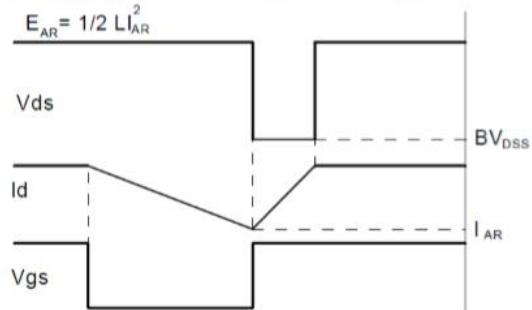
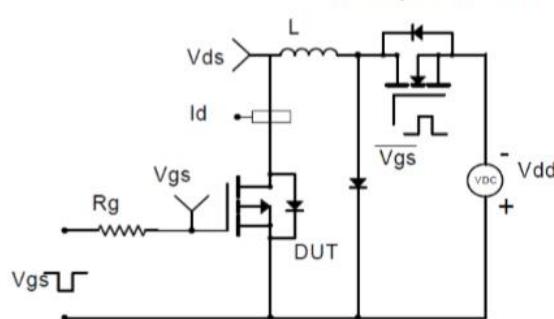
Gate Charge Test Circuit & Waveform



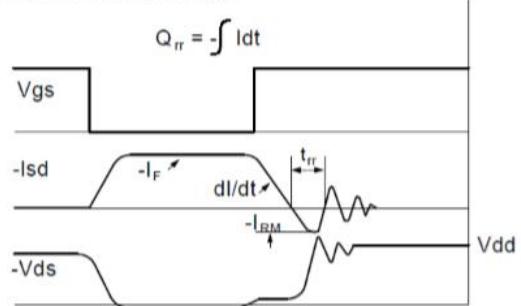
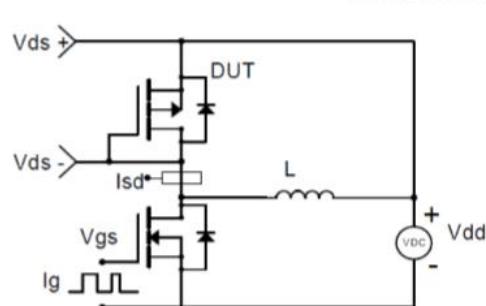
Resistive Switching Test Circuit & Waveforms



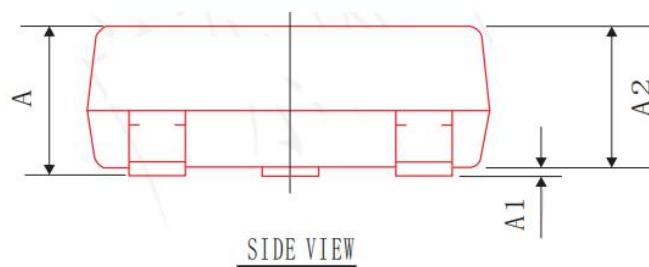
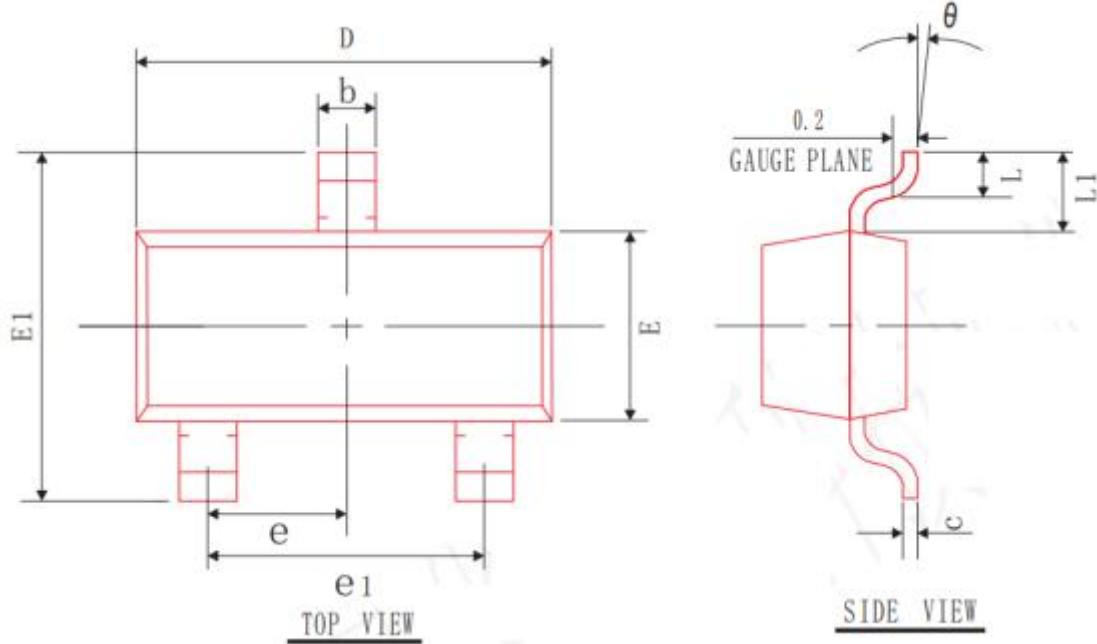
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



## Package Mechanical Data-SOT-23



SYMBOL	MIN	NOM	MAX
A	0.90	1.05	1.20
A <sub>1</sub>	0.00	0.05	0.10
A <sub>2</sub>	0.90	1.00	1.10
b	0.30	0.40	0.50
c	0.08	0.10	0.15
D	2.80	2.90	3.00
E	1.20	1.30	1.40
E <sub>1</sub>	2.30	2.40	2.50
L	0.30	0.40	0.50
θ	0°	5°	10°
L <sub>1</sub>	0.55 REF		
e	0.95 BSC		
e <sub>1</sub>	1.90 REF		



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