ALC5616E-CG
ALC5616E-CGT

Ultra-Low Power Audio CODEC
for Mobile Devices

Datasheet

Rev. 0.10

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5616E Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.10	2020/1/31	Preliminary version

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1. General Description

The ALC5616E is a high performance, low power, stereo channel I^{2}S interface audio CODEC. The data can be input from analog microphone interface and output to headphone or line_out interface.

The ALC5616E features a low power cap-free headphone amplifier. It consumes less than 6.5mW power during playback, providing mobile system longer battery life under headphone listening mode.

ALC5616E requires only two voltage supplies and consumes low power, making it ideal for portable devices.

2. Features

Analog Features:

- Digital-to-Analog Converter with 98dBA SNR
- Analog-to-Digital Converter with 94dBA SNR
- Single Ended/Differential analog microphone inputs with boost pre-amplifiers and low noise microphone bias
  - +20/+24/+30/+35/+40/+44/+50/+52 dB microphone boost gain
  - MIC input to ADC with 50dB boost gain, SNR > 66dBA and THD+N < -65dB
  - Adjustable MICBIAS(2.7V/2.4V/2.25V/1.8V)
- Stereo line outputs
  - DAC to line output with 0dB gain, SNR >= 98dBA, THD+N <= -86dB
- Stereo Cap-Free headphone amplifier with ultra low power consumption for playback
  - 20mW/CH (AVDD=CPVDD=1.8V, THD+N <= -80dB, 16Ohm Load)
  - Playback power consumption <= 6.5mW (AVDD=VBVDD=CPVDD=1.8V, 16Ohm, With I2S Clock, Playback Silence)
  - Playback power consumption <= 14mW (AVDD=VBVDD=CPVDD=1.8V, 16Ohm, With I2S Clock, Playback 1mW/CH)
- Audio jack detection
- Inside PLL can receiver wide range clock input

Digital Features:

- One 24bit/8kHz ~ 192kHz I^2S/PCM interface for stereo DAC and stereo ADC
- I^2C control interface
- One wind noise reduction filter
- Zero detection and soft volume for pop noise suppression

3. System Application

- Smart Phones
- Tablet

4. Function Block and Mixer Path

4.1. Function Block

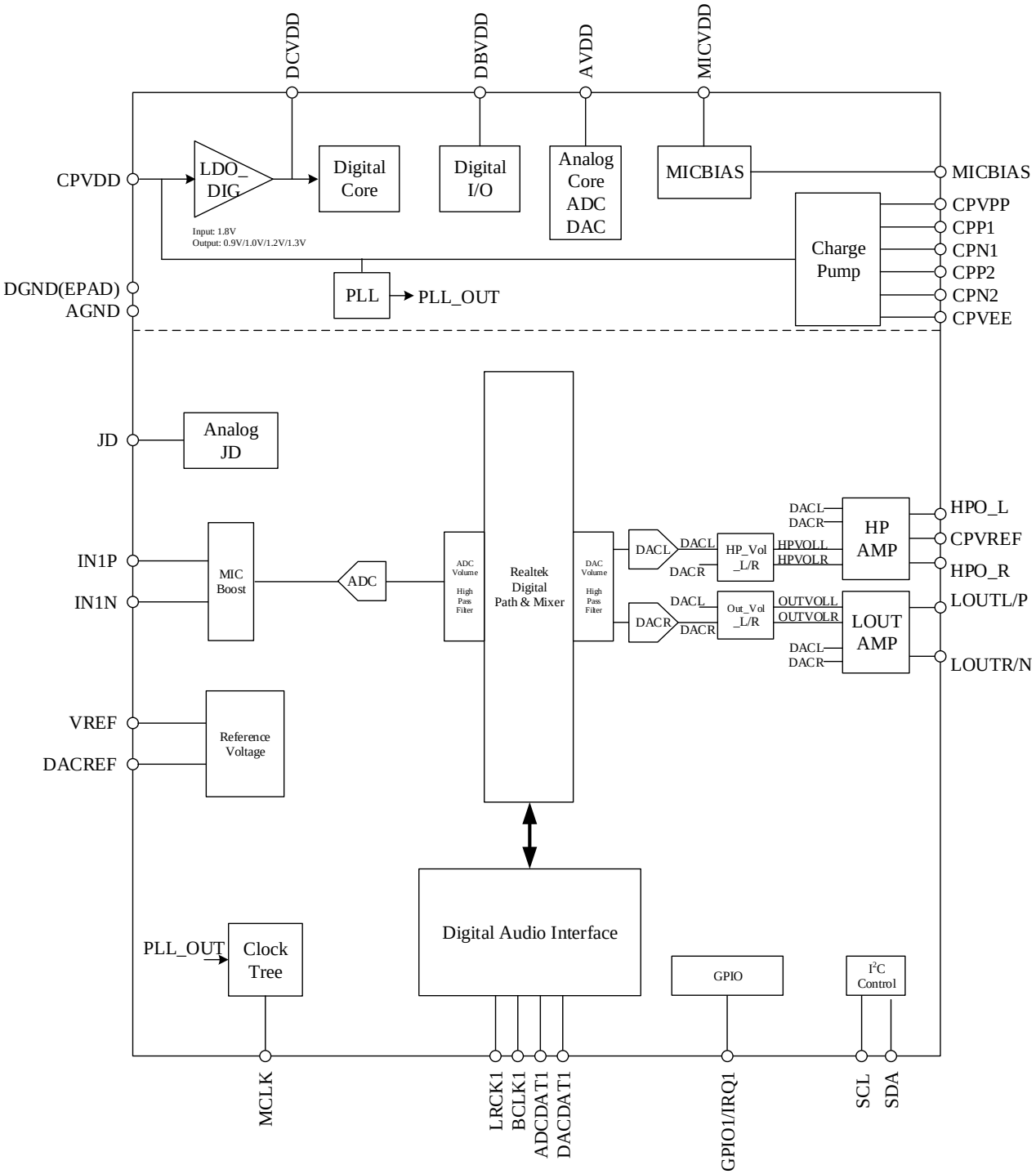


Figure 1. Block Diagram

4.2. Audio Mixer Path

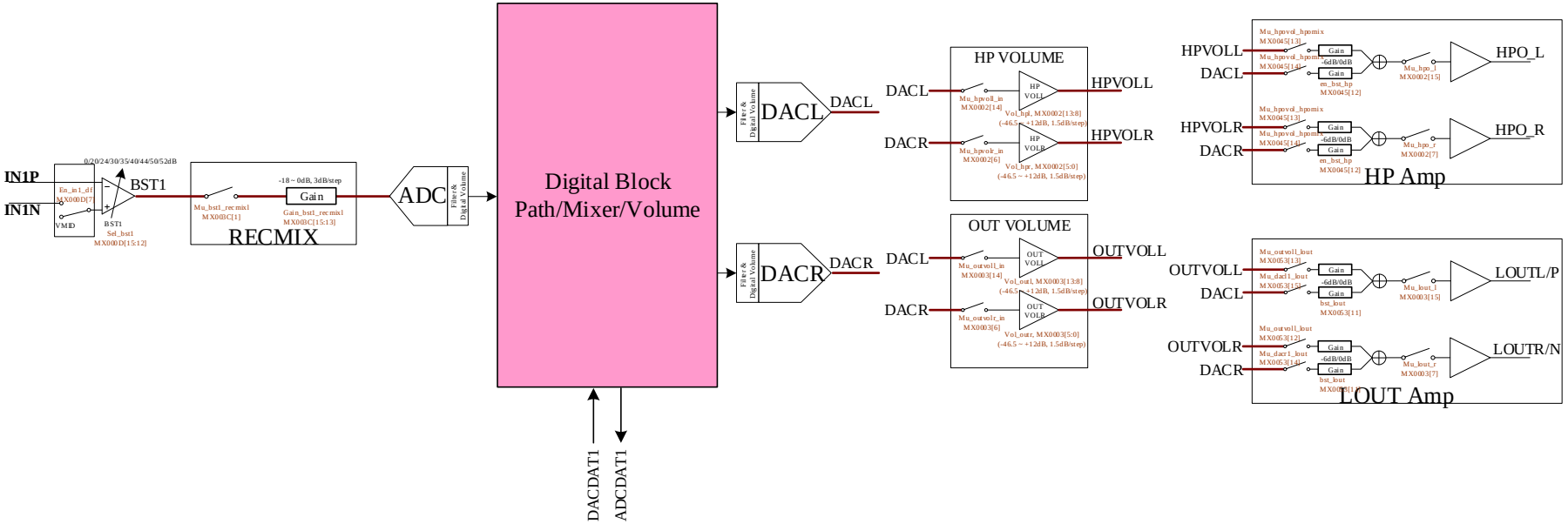


Figure 2. Audio Mixer Path

4.3. Digital Mixer Path

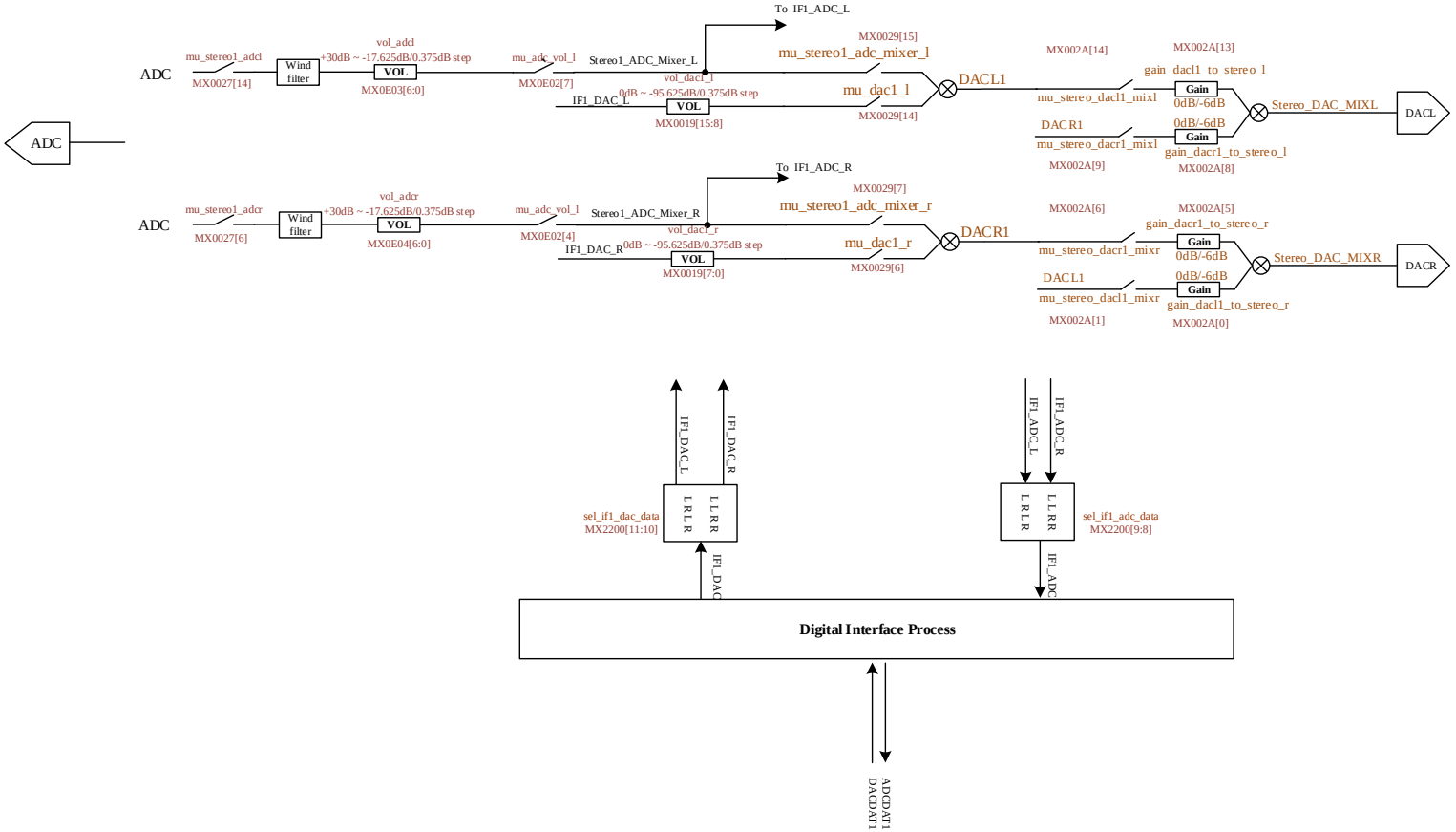
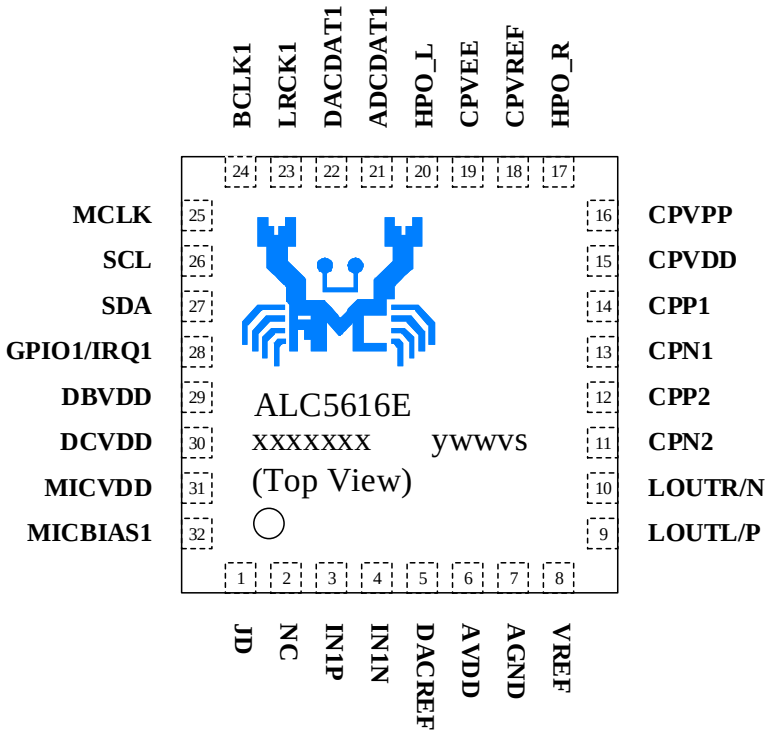


Figure 3. Digital Mixer Path

5. Pin Assignments

QFN32 (4x4mm^2)

Pitch 0.4mm



EPAD: DGND

Figure 4. Pin Assignment

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
DACDAT1	I	22	First I2S interface serial data input	Vt = 0.5*DBVDD
ADCDAT1	O	21	First I2S interface serial data output	V_{OL}=0.1*DBVDD, V_{OH}=0.9*DBVDD
BCLK1	I/O	24	First I2S interface serial bit clock	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Vt = 0.5*DBVDD
LRCK1	I/O	23	First I2S interface synchronous signal	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Vt = 0.5*DBVDD
SDA	I/O	27	I2C interface serial data	Open drain structure
SCL	I	26	I2C interface clock input	Open drain structure
MCLK	I	25	I2S interface master clock input	Vt = 0.5*DBVDD
GPIO1/IRQ	I/O	28	General purpose input and output Interrupt output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Vt = 0.5*DBVDD
				Total: 8 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LOUTR/N	O	10	Line output type Right channel single-end output Negative channel differential output	Analog output
LOUTL/P	O	9	Line output type Left channel single-end output Positive channel differential output	Analog output
IN1P	I	3	Positive differential input for microphone	Analog input
IN1N	I	4	Negative differential input for microphone	Analog input
JD	I	1	Jack detection pin	JD Threshold: 2.7V(Default Setting)
HPO_L	O	20	Headphone amplifier output Left channel	Analog output
HPO_R	O	17	Headphone amplifier output Right channel	Analog output
				Total: 7 Pins

6.3. Filter/Reference/NC

Table 3. Filter/Reference/NC

Name	Type	Pin	Description	Characteristic Definition
MICBIAS	O	32	Bias voltage output for microphone	Programmable analog DC output
VREF	O	8	Internal reference voltage	4.7uF capacitor to analog ground
CPVREF	-	18	Headphone reference ground	Headphone ground
CPN1	-	13	First charge pump bucket capacitor	2.2uf capacitor to CPP1
CPP1	-	14	First charge pump bucket capacitor	2.2uf capacitor to CPN1
CPN2	-	11	Second charge pump bucket capacitor	2.2uf capacitor to CPP2
CPP2	-	12	Second charge pump bucket capacitor	2.2uf capacitor to CPN2
NC	-	2	No connection pin	
				Total: 8 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
MICVDD	P	31	Analog power for MICBIAS	3.0V ~ 3.3V (Default 3.3V is recommended)
AVDD	P	6	Analog power	1.71V ~ 1.9V (Default 1.8V is recommended)
DACREF	P	5	Analog power	1.71V ~ 1.9V (Default 1.8V is recommended)
AGND	P	7	Analog ground	
CPVDD	P	15	Analog power for headphone charge pump	1.71V ~ 1.9V (Default 1.8V is recommended)
CPVEE	P	19	Charge pump negative voltage output	2.2uf capacitor to analog ground
CPVPP	P	16	Charge pump positive voltage output	2.2uf capacitor to analog ground
DCVDD	P	30	Digital power for digital core.	Internal LDO generated
DBVDD	P	29	Digital power for digital I/O buffer	1.71V~3.3V (Default 1.8V is recommended)
DGND	P	EPAD	Charge pump ground Digital ground	Exposed-Pad
				Total: 9 Pins

7. Function Description

7.1. Power

There are different power types in ALC5616E. DBVDD is for digital I/O power, DCVDD is for digital core power, AVDD and DACREF are for analog power, CPVDD is for charge pump power, MICVDD is for MICBIAS power.

The power supplier limit condition are MICVDD > AVDD = DACREF = CPVDD, and for the best performance, our design setting is show on below.

Table 5. Power Supply for Best Performance

Power	DBVDD	DCVDD	AVDD	DACREF	CPVDD	MICVDD
Setting	1.8V	1.2V	1.8V	1.8V	1.8V	3.3V

*1.2V DCVDD was generated by internal LDO.

To prevent all power down leakage, needs keep all power supply on.

Table 6. Power Supply Condition for Power Down Leakage

Power	DBVDD	AVDD	DACREF	CPVDD	MICVDD
Setting	Supplied	Supplied	Supplied	Supplied	Supplied

7.2. Power Supply On/Off Sequence

To prevent pop noise and make sure function work normally, following power on and off sequence are recommended.

Power On Sequence: (Sequentially turn on power pins)

1. DBVDD/AVDD/DACREF/CPVDD power supply on (If DBVDD=1.8V).
2. DBVDD power supply on (If DBVDD > 1.8V).
3. MICVDD power supply on.
4. Software starts to initialize ALC5616E.

Power Off Sequence: (Sequentially turn off power pins)

1. Power down all Codec function (Write 0x0000'h to register MX-00'h).
2. MICVDD power supply off.
3. DBVDD power supply off (If DBVDD > 1.8V).
4. DBVDD/AVDD/DACREF/CPVDD power supply off (If DBVDD=1.8V).

7.3. Reset

There are 2 types of reset operation: power on reset (POR) and register reset.

Table 7. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write MX-0000h	Reset all registers to default values except some specify control registers and logic.

7.3.1. Power-On Reset (POR)

When powered on, DCVDD passes through the V_{POR} band of the ALC5616E (V_{POR_ON} ~V_{POR_OFF}). A power on reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 8. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	-	0.8	-	V
V_{POR_OFF}	-	0.52	-	V

Note:
1.V_{POR_OFF} must be below V_{POR_ON}
2. T°C = 25°C
3. When DCVDD is supplied 1.2V

7.3.2. Software Reset

When MX-0000h is wrote, all registers become to default value.

7.4. Clocking

The Figure 5 shown the clock tree. The system clock of ALC5616E can be selected from MCLK or PLL. MCLK is always provided externally while the reference clock of PLL can be selected from MCLK, BCLK1. The driver should arrange the clock of each block and setup each divider.

The clock source of analog DAC/ADC and digital ADC/DAC filter can be selected by clock mux. When ALC5616E at I^{2}S master mode, the clock source also can be selected by clock mux.

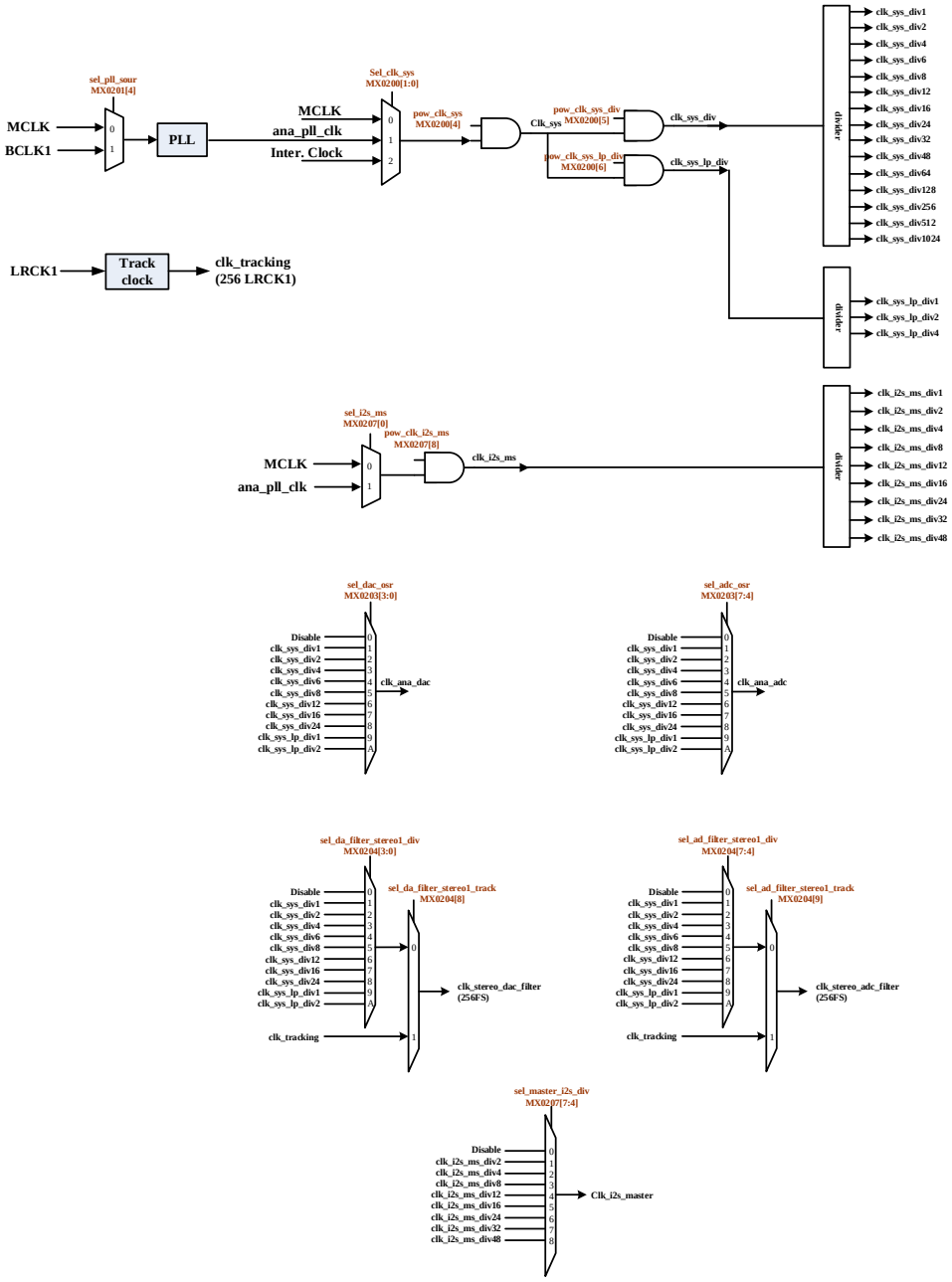


Figure 5. Clock Tree

7.4.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. The source of the PLL can be set to MCLK, BCLK1 by setting register.

The S/W driver can set up the PLL to output a frequency to match the requirement of system clock.

The PLL transmit formula as below:

$F_{OUT} = [F_{IN} * (N+2)] / [(M+2) * (K+2)]$ {Note: M = -1 is bypass, K = -1 is bypass}

Table 9. PLL Clock Setting Table for 48K (Unit: MHz)

F_{IN} (MHz)	M	N	K	F_{OUT} (MHz)
1.536	Bypass	78	3	24.5760
2.048	Bypass	58	3	24.5760
3.072	Bypass	38	3	24.5760
4.096	Bypass	28	3	24.5760

*The recommended Fvco range of PLL1 is from 50MHz to 150MHz.

Table 10. PLL Clock Setting Table 44.1K (Unit: MHz)

F_{IN} (MHz)	M	N	K	F_{OUT} (MHz)
1.4112	Bypass	78	3	22.5792
2.8224	Bypass	38	3	22.5792

*The recommended Fvco range of PLL1 is from 50MHz to 150MHz.

7.5. Digital Data Interface

7.5.1. Two I²S/PCM Interface

The two I2S/PCM interface can be configured as master mode or slave mode. Four audio data formats are supported:

- PCM mode
- Left justified mode
- I²S mode

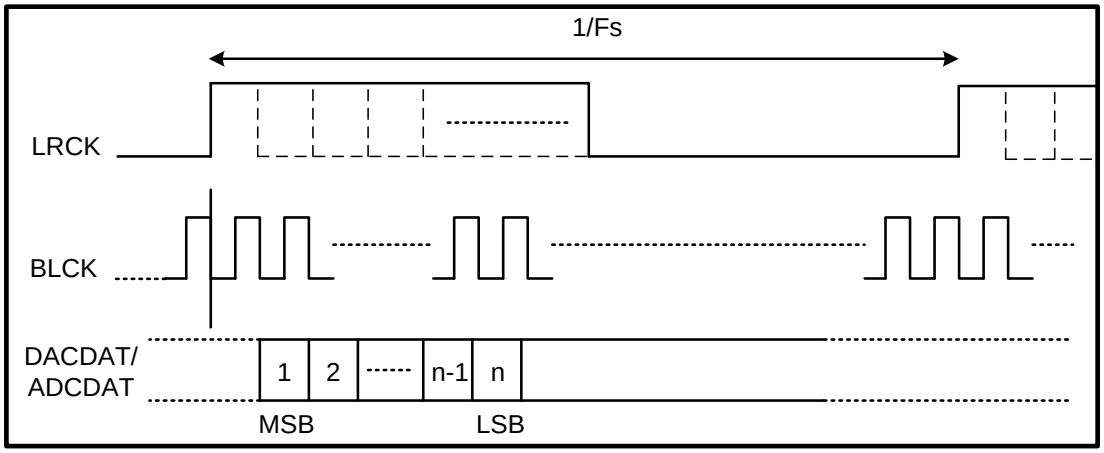


Figure 6. PCM MONO Data Mode A Format (BCLK POLARITY=0)

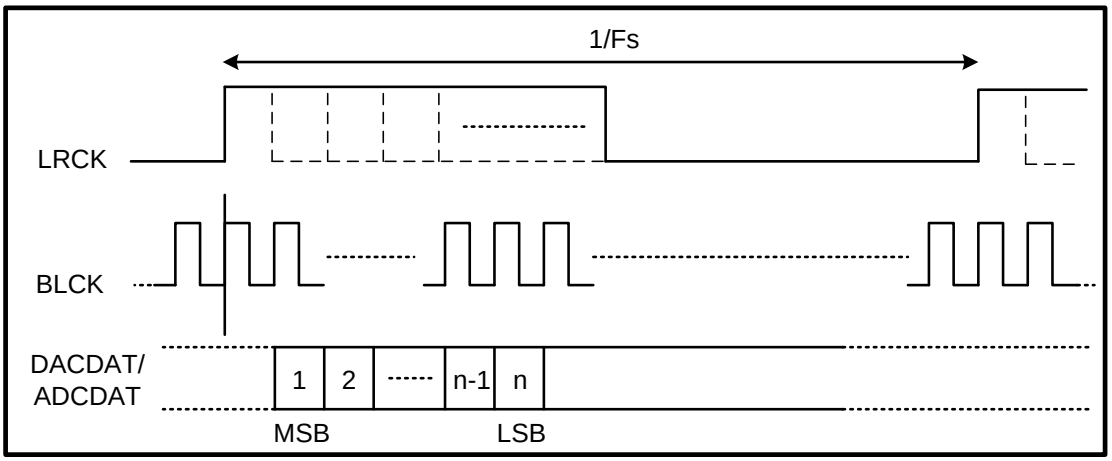


Figure 7. PCM MONO Data Mode A Format (BCLK POLARITY=1)

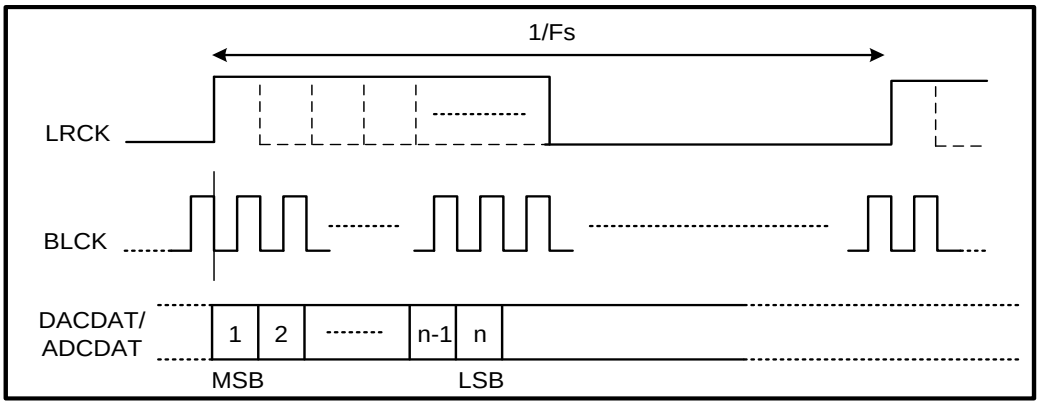


Figure 8. PCM MONO Data Mode B Format (BCLK POLARITY=0)

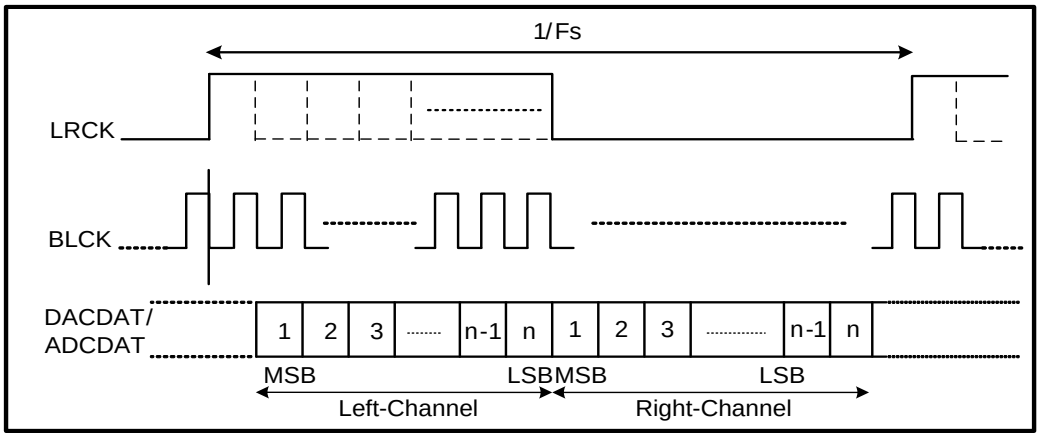


Figure 9. PCM Stereo Data Mode A Format (BCLK POLARITY=0)

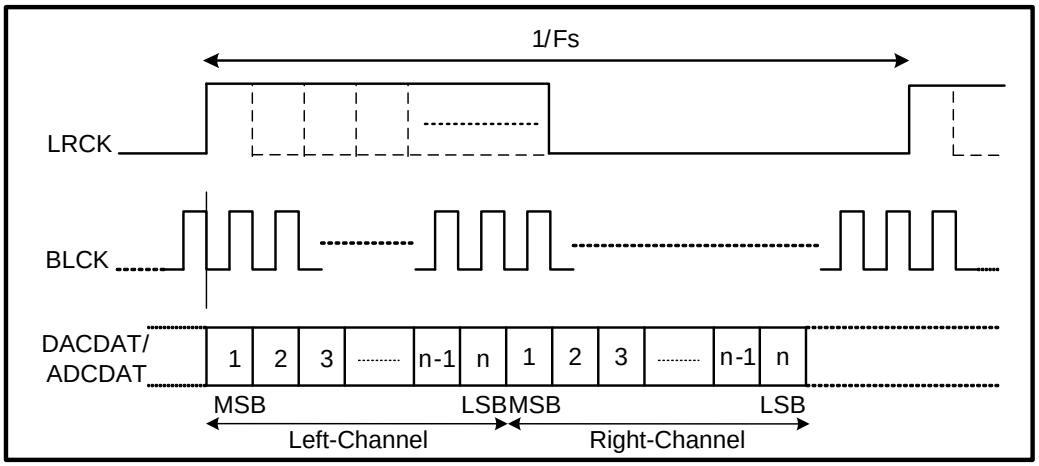


Figure 10. PCM Stereo Data Mode B Format (BCLK POLARITY=0)

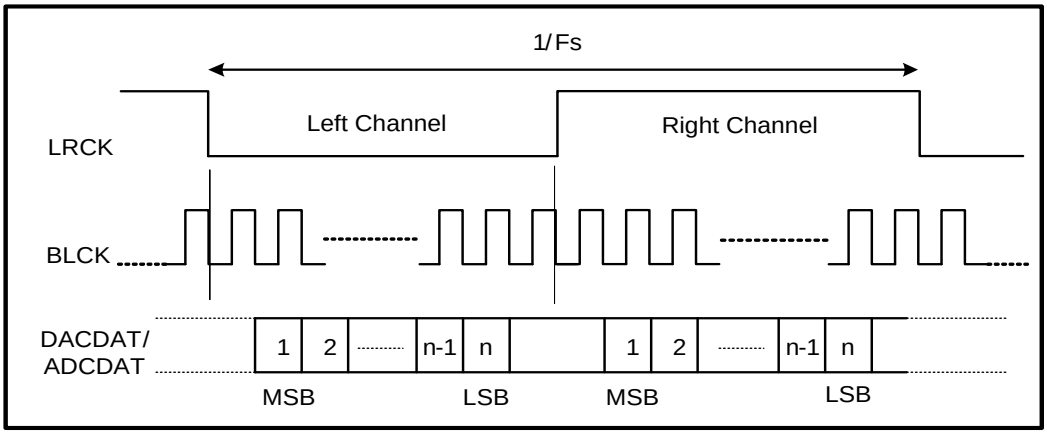


Figure 11. I²S Data Format (BCLK POLARITY=0)

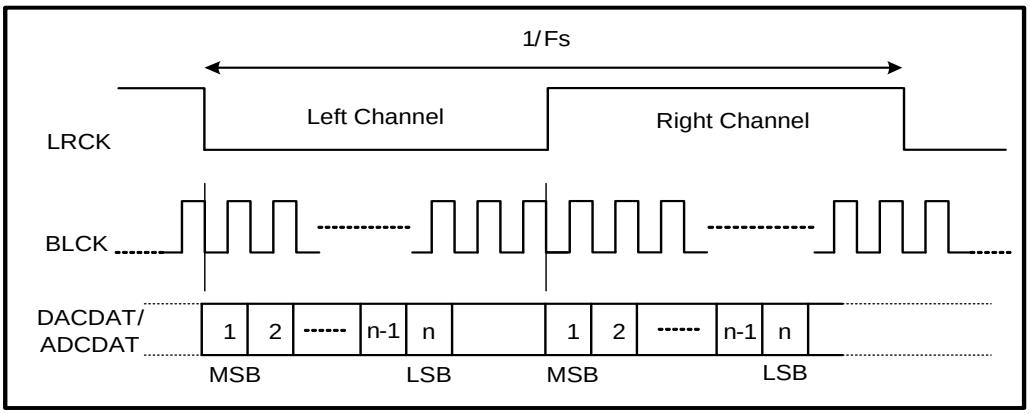


Figure 12. Left-Justified Data Format (BCLK POLARITY=0)

7.6. Audio Data Path

The ALC5616E provides stereo-channel analog DACs for playback and mono-channel analog ADCs for recording.

7.6.1. Mono Analog ADC Record Path

There is analog ADC and with mono-channel recording path. You can use mono analog microphones pass to analog ADC.

The full scale input of analog ADC with 0dB path setting is around 0.55Vrms. In order to save power, the analog ADC can be powered down by setting pow_adc (MX-0061[2]). And the volume control of the stereo ADC is also separately controlled by vol_adcl (MX-0E03[6:0]) and vol_adcr (MX-0E04[6:0]).

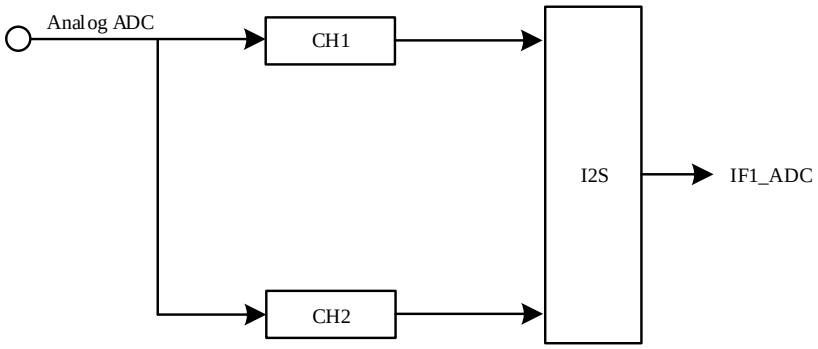


Figure 13. Mono AMIC Recording Path

7.6.2. Stereo Analog DACs with Playback Path

There are two analog DACs and with 2-channel playback path. The stereo analog DACs can output audio signal to headphone output or line output.

The full scale output of analog DAC with 0dB path setting is around 1Vrms at line output port. In order to save power, the two analog DACs can be powered down separately by setting pow_dac_l_1 (MX-0061[12]), pow_dac_r_1 (MX-0061[11]). And the two digital volume controls are also separately controlled by vol_dac1_l (MX-0019[15:8]) and vol_dac1_r (MX-0019[7:0]).

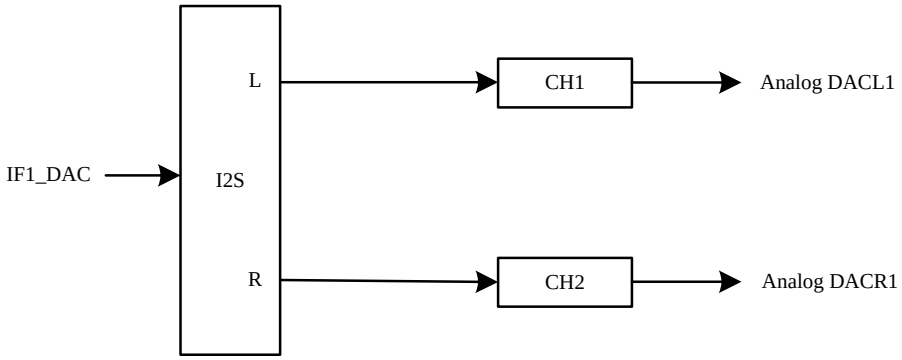


Figure 14. 4-Channel Playback Path

7.7. Analog Audio Input Port

The ALC5616E has one analog mic input ports:

- **IN1P/N**

  The IN1P/N is a microphone input. Microphone input can be configured to differential input or single-ended input by MX-000D[7]. Multi-steps microphone boost gain set by sel_bst1 (MX-000D[15:12]) is easy to use for microphone application. Pow_bst1 can be used to power down the MIC boost.

7.8. Analog Audio Output Port

The ALC5616E supports two type output ports:

- **HPO_L/R**

  The headphone output of ALC5616E is a stereo output with cap-free type headphone amplifier. It does not need to connect external capacitor and can connect to earphone device directly. The headphone output source can mix from HP Volume (HPVOLL/R) or DACL/R by setting MX-0045. The front stage of headphone output has volume control and gain control. The volume range is from +12dB to -46.5dB with 1.5dB/step by MX-0002.
  En_l_hp and en_r_hp (MX-0063[7/6]) can be used to power on/off Headphone Amplifier, and pow_hpo_voll and pow_hpo_volr (MX-0066[11/10]) can be used to power on/off headphone volume control. In addition, pow_pump_hp (MX-008E[3]) can be used to power on/off charge pump circuit for Headphone Amplifier.

- **Line_OUT_L/R/P/N**

  The output type is line type output. The output is a stereo single ended output or mono differential output. The input can be selected from OUTVOLL/R or DACL/R output by setting MX-0053[15:12]. The front stage of LOUT output has gain control for attenuation. The gain control is 0dB or -6dB by MX-0053[11].

7.9. Multi-Function Pins

There is multi-function pin in ALC5616E. For different function on pin is controlled by register. You need to set the right register settings for multi-function pin by your application.

- **GPIO1/IRQ – Pin 28**

The pin default is GPIO function. If want to change to IRQ output, write MX-0304[8] to 1'b that will switch to IRQ function.

7.10. Wind Filter with Dynamic Wind Noise Detector

7.10.1. Wind Filter

The wind filter is implemented by a high pass filter. The wind filter is mainly for ADC recording used. The cut-off frequency of wind filter is programmable and is varied according to different sample rate. The filter is used to remove DC offset at normal condition, and to remove wind noise at application mode.

Wind filter setting procedure:

Step1: Disable wind filter – MX-0E05[7]

Step2: Select target sample rate – MX-0E05[2:0] and MX-0E07[2:0]

Step3: Fine tune wind filter Fc – MX-0E06[5:0] and MX-0E08[5:0]

Step4: Enable wind filter – MX-0E05[7]

The following table (Table 11~Table 15.) is shown the Fc with sample rate selection.
For the formula of Fc calculation is also shown as:

$Fc = (Fs * \tan^{-1}(a/(2-a))) / \pi$

Where:
When MX-0E05[2:0] and MX-0E007[2:0]=000'b , $a = 2^{-6} + n * 2^{-6}$ (n is MX-0E06[5:0] & MX-0E08[5:0])
When MX-0E05[2:0] and MX-0E007[2:0]=001'b , $a = 2^{-7} + n * 2^{-7}$ (n is MX-0E06[5:0] & MX-0E08[5:0])
When MX-0E05[2:0] and MX-0E007[2:0]=010'b , $a = 2^{-8} + n * 2^{-8}$ (n is MX-0E06[5:0] & MX-0E08[5:0])
When MX-0E05[2:0] and MX-0E007[2:0]=011'b , $a = 2^{-9} + n * 2^{-9}$ (n is MX-0E06[5:0] & MX-0E08[5:0])
When MX-0E05[2:0] and MX-0E007[2:0]=100'b , $a = 2^{-10} + n * 2^{-10}$ (n is MX-0E06[5:0] & MX-0E08[5:0])

Table 11. Stereo ADC 1 Filter Wind Filter Fc Selection when MX0E05[2:0] and MX0E007[2:0]=000'b

MX0E06[5:0] MX0E08[5:0]		L & R Channel Sampling Rate Setting (Hz)				
		8000	16000	32000	44100	48000
n(HEX)	n(DEC)	Fc (Hz)				
000000	0	20.05062	40.10124	80.20248	110.529	120.3037
000001	1	40.41694	80.83389	161.6678	222.7984	242.5017
000010	2	61.10382	122.2076	244.4153	336.8348	366.6229
000011	3	82.11608	164.2322	328.4643	452.6649	492.6965
000100	4	103.4585	206.9171	413.8341	570.3152	620.7512
000101	5	125.136	250.2719	500.5438	689.812	750.8157
000110	6	147.1531	294.3062	588.6123	811.1814	882.9185
000111	7	169.5146	339.0292	678.0583	934.4491	1017.087
001000	8	192.2251	384.4501	768.9003	1059.641	1153.35
001001	9	215.2891	430.5782	861.1563	1186.781	1291.735
001010	10	238.7111	477.4222	954.8443	1315.895	1432.266
001011	11	262.4954	524.9908	1049.982	1447.006	1574.972
001100	12	286.6462	573.2925	1146.585	1580.137	1719.877
001101	13	311.1677	622.3354	1244.671	1715.312	1867.006
001110	14	336.0638	672.1275	1344.255	1852.552	2016.383
001111	15	361.3382	722.6764	1445.353	1991.877	2168.029
010000	16	386.9946	773.9891	1547.978	2133.308	2321.967
010001	17	413.0363	826.0726	1652.145	2276.863	2478.218
010010	18	439.4665	878.9331	1757.866	2422.559	2636.799
010011	19	466.2883	932.5765	1865.153	2570.414	2797.73
010100	20	493.5041	987.0083	1974.017	2720.441	2961.025
010101	21	521.1165	1042.233	2084.466	2872.655	3126.699
010110	22	549.1276	1098.255	2196.51	3027.066	3294.765
010111	23	577.539	1155.078	2310.156	3183.684	3465.234
011000	24	606.3523	1212.705	2425.409	3342.517	3638.114
011001	25	635.5684	1271.137	2542.274	3503.571	3813.411
011010	26	665.1881	1330.376	2660.752	3666.849	3991.129
011011	27	695.2115	1390.423	2780.846	3832.354	4171.269
011100	28	725.6385	1451.277	2902.554	4000.082	4353.831
011101	29	756.4684	1512.937	3025.874	4170.032	4538.811
011110	30	787.7001	1575.4	3150.8	4342.197	4726.2
011111	31	819.3318	1638.664	3277.327	4516.566	4915.991
100000	32	851.3613	1702.723	3405.445	4693.129	5108.168

100001	**33**	883.7859	1767.572	3535.143	4871.87	5302.715
100010	**34**	916.6022	1833.204	3666.409	5052.769	5499.613
100011	**35**	949.8062	1899.612	3799.225	5235.807	5698.837
100100	**36**	983.3935	1966.787	3933.574	5420.957	5900.361
100101	**37**	1017.359	2034.717	4069.435	5608.19	6104.152
100110	**38**	1051.696	2103.392	4206.784	5797.474	6310.176
100111	**39**	1086.399	2172.798	4345.596	5988.774	6518.393
101000	**40**	1121.46	2242.92	4485.84	6182.049	6728.761
101001	**41**	1156.872	2313.743	4627.487	6377.255	6941.23
101010	**42**	1192.625	2385.25	4770.501	6574.346	7155.751
101011	**43**	1228.711	2457.422	4914.844	6773.27	7372.266
101100	**44**	1265.119	2530.239	5060.478	6973.971	7590.716
101101	**45**	1301.839	2603.679	5207.358	7176.39	7811.037
101110	**46**	1338.86	2677.719	5355.439	7380.464	8033.158
101111	**47**	1376.168	2752.336	5504.672	7586.127	8257.009
110000	**48**	1413.752	2827.504	5655.007	7793.307	8482.511
110001	**49**	1451.597	2903.195	5806.389	8001.93	8709.584
110010	**50**	1489.691	2979.381	5958.762	8211.919	8938.143
110011	**51**	1528.017	3056.033	6112.066	8423.192	9168.1
110100	**52**	1566.56	3133.12	6266.241	8635.663	9399.361
110101	**53**	1605.305	3210.611	6421.222	8849.246	9631.832
110110	**54**	1644.236	3288.471	6576.943	9063.849	9865.414
110111	**55**	1683.334	3366.668	6733.336	9279.379	10100
111000	**56**	1722.583	3445.166	6890.332	9495.739	10335.5
111001	**57**	1761.965	3523.93	7047.859	9712.831	10571.79
111010	**58**	1801.461	3602.922	7205.844	9930.554	10808.77
111011	**59**	1841.053	3682.107	7364.213	10148.81	11046.32
111100	**60**	1880.723	3761.445	7522.891	10367.48	11284.34
111101	**61**	1920.45	3840.9	7681.8	10586.48	11522.7
111110	**62**	1960.216	3920.432	7840.865	10805.69	11761.3
111111	**63**	2000.002	4000.003	8000.007	11025.01	12000.01

Table 12. Stereo ADC 1 Filter Wind Filter Fc Selection when MX0E05[2:0] and MX0E007[2:0]=001'b

MX0E06[5:0] MX0E08[5:0]		L & R Channel Sampling Rate Setting (Hz)				
		8000	16000	32000	44100	48000
n(HEX)	n(DEC)	Fc (Hz)				
000000	0	9.98615	19.9723	39.9446	55.04865	59.9169
000001	1	20.05062	40.10124	80.20248	110.529	120.3037
000010	2	30.19401	60.38803	120.7761	166.4445	181.1641
000011	3	40.41694	80.83389	161.6678	222.7984	242.5017
000100	4	50.72001	101.44	202.88	279.5941	304.3201
000101	5	61.10382	122.2076	244.4153	336.8348	366.6229
000110	6	71.56898	143.138	286.2759	394.524	429.4139
000111	7	82.11608	164.2322	328.4643	452.6649	492.6965
001000	8	92.74574	185.4915	370.9829	511.2609	556.4744
001001	9	103.4585	206.9171	413.8341	570.3152	620.7512
001010	10	114.2551	228.5102	457.0203	629.8311	685.5305
001011	11	125.136	250.2719	500.5438	689.812	750.8157
001100	12	136.1018	272.2035	544.4071	750.261	816.6106
001101	13	147.1531	294.3062	588.6123	811.1814	882.9185
001110	14	158.2905	316.581	633.162	872.5763	949.743
001111	15	169.5146	339.0292	678.0583	934.4491	1017.087
010000	16	180.8259	361.6518	723.3037	996.8029	1084.955
010001	17	192.2251	384.4501	768.9003	1059.641	1153.35
010010	18	203.7126	407.4252	814.8504	1122.966	1222.276
010011	19	215.2891	430.5782	861.1563	1186.781	1291.735
010100	20	226.9551	453.9101	907.8202	1251.09	1361.73
010101	21	238.7111	477.4222	954.8443	1315.895	1432.266
010110	22	250.5577	501.1153	1002.231	1381.199	1503.346
010111	23	262.4954	524.9908	1049.982	1447.006	1574.972
011000	24	274.5247	549.0495	1098.099	1513.318	1647.148
011001	25	286.6462	573.2925	1146.585	1580.137	1719.877
011010	26	298.8604	597.7208	1195.442	1647.468	1793.162
011011	27	311.1677	622.3354	1244.671	1715.312	1867.006
011100	28	323.5687	647.1374	1294.275	1783.672	1941.412
011101	29	336.0638	672.1275	1344.255	1852.552	2016.383
011110	30	348.6535	697.3069	1394.614	1921.952	2091.921
011111	31	361.3382	722.6764	1445.353	1991.877	2168.029
100000	32	374.1184	748.2368	1496.474	2062.328	2244.71

100001	**33**	386.9946	773.9891	1547.978	2133.308	2321.967
100010	**34**	399.9671	799.9341	1599.868	2204.818	2399.802
100011	**35**	413.0363	826.0726	1652.145	2276.863	2478.218
100100	**36**	426.2027	852.4053	1704.811	2349.442	2557.216
100101	**37**	439.4665	878.9331	1757.866	2422.559	2636.799
100110	**38**	452.8283	905.6566	1811.313	2496.216	2716.97
100111	**39**	466.2883	932.5765	1865.153	2570.414	2797.73
101000	**40**	479.8468	959.6935	1919.387	2645.155	2879.081
101001	**41**	493.5041	987.0083	1974.017	2720.441	2961.025
101010	**42**	507.2606	1014.521	2029.042	2796.274	3043.564
101011	**43**	521.1165	1042.233	2084.466	2872.655	3126.699
101100	**44**	535.0721	1070.144	2140.288	2949.585	3210.433
101101	**45**	549.1276	1098.255	2196.51	3027.066	3294.765
101110	**46**	563.2831	1126.566	2253.133	3105.098	3379.699
101111	**47**	577.539	1155.078	2310.156	3183.684	3465.234
110000	**48**	591.8953	1183.791	2367.581	3262.823	3551.372
110001	**49**	606.3523	1212.705	2425.409	3342.517	3638.114
110010	**50**	620.9099	1241.82	2483.64	3422.766	3725.46
110011	**51**	635.5684	1271.137	2542.274	3503.571	3813.411
110100	**52**	650.3278	1300.656	2601.311	3584.932	3901.967
110101	**53**	665.1881	1330.376	2660.752	3666.849	3991.129
110110	**54**	680.1494	1360.299	2720.597	3749.323	4080.896
110111	**55**	695.2115	1390.423	2780.846	3832.354	4171.269
111000	**56**	710.3746	1420.749	2841.499	3915.94	4262.248
111001	**57**	725.6385	1451.277	2902.554	4000.082	4353.831
111010	**58**	741.0032	1482.006	2964.013	4084.78	4446.019
111011	**59**	756.4684	1512.937	3025.874	4170.032	4538.811
111100	**60**	772.0341	1544.068	3088.137	4255.838	4632.205
111101	**61**	787.7001	1575.4	3150.8	4342.197	4726.2
111110	**62**	803.466	1606.932	3213.864	4429.106	4820.796
111111	**63**	819.3318	1638.664	3277.327	4516.566	4915.991

Table 13. Stereo ADC 1 Filter Wind Filter Fc Selection when MX0E05[2:0] and MX0E007[2:0]=010'b

MX0E06[5:0] MX0E08[5:0]		L & R Channel Sampling Rate Setting (Hz)				
		8000	16000	32000	44100	48000
n(HEX)	n(DEC)	Fc (Hz)				
000000	0	4.983323	9.966646	19.93329	27.47057	29.89994
000001	1	9.98615	19.9723	39.9446	55.04865	59.9169
000010	2	15.00856	30.01711	60.03423	82.73467	90.05134
000011	3	20.05062	40.10124	80.20248	110.529	120.3037
000100	4	25.11241	50.22483	100.4497	138.4322	150.6745
000101	5	30.19401	60.38803	120.7761	166.4445	181.1641
000110	6	35.2955	70.591	141.182	194.5664	211.773
000111	7	40.41694	80.83389	161.6678	222.7984	242.5017
001000	8	45.55842	91.11684	182.2337	251.1408	273.3505
001001	9	50.72001	101.44	202.88	279.5941	304.3201
001010	10	55.90178	111.8036	223.6071	308.1586	335.4107
001011	11	61.10382	122.2076	244.4153	336.8348	366.6229
001100	12	66.32619	132.6524	265.3048	365.6231	397.9572
001101	13	71.56898	143.138	286.2759	394.524	429.4139
001110	14	76.83225	153.6645	307.329	423.5378	460.9935
001111	15	82.11608	164.2322	328.4643	452.6649	492.6965
010000	16	87.42055	174.8411	349.6822	481.9058	524.5233
010001	17	92.74574	185.4915	370.9829	511.2609	556.4744
010010	18	98.0917	196.1834	392.3668	540.7305	588.5502
010011	19	103.4585	206.9171	413.8341	570.3152	620.7512
010100	20	108.8463	217.6926	435.3852	600.0152	653.0778
010101	21	114.2551	228.5102	457.0203	629.8311	685.5305
010110	22	119.6849	239.3699	478.7398	659.7632	718.1096
010111	23	125.136	250.2719	500.5438	689.812	750.8157
011000	24	130.6082	261.2164	522.4328	719.9777	783.6492
011001	25	136.1018	272.2035	544.4071	750.261	816.6106
011010	26	141.6167	283.2334	566.4668	780.662	849.7002
011011	27	147.1531	294.3062	588.6123	811.1814	882.9185
011100	28	152.711	305.422	610.844	841.8193	916.2659
011101	29	158.2905	316.581	633.162	872.5763	949.743
011110	30	163.8917	327.7833	655.5667	903.4528	983.35
011111	31	169.5146	339.0292	678.0583	934.4491	1017.087
100000	32	175.1593	350.3186	700.6372	965.5657	1050.956

100001	**33**	180.8259	361.6518	723.3037	996.8029	1084.955
100010	**34**	186.5145	373.029	746.0579	1028.161	1119.087
100011	**35**	192.2251	384.4501	768.9003	1059.641	1153.35
100100	**36**	197.9578	395.9155	791.831	1091.242	1187.747
100101	**37**	203.7126	407.4252	814.8504	1122.966	1222.276
100110	**38**	209.4897	418.9794	837.9588	1154.812	1256.938
100111	**39**	215.2891	430.5782	861.1563	1186.781	1291.735
101000	**40**	221.1109	442.2217	884.4434	1218.874	1326.665
101001	**41**	226.9551	453.9101	907.8202	1251.09	1361.73
101010	**42**	232.8218	465.6436	931.2871	1283.43	1396.931
101011	**43**	238.7111	477.4222	954.8443	1315.895	1432.266
101100	**44**	244.623	489.246	978.4921	1348.484	1467.738
101101	**45**	250.5577	501.1153	1002.231	1381.199	1503.346
101110	**46**	256.5151	513.0302	1026.06	1414.04	1539.091
101111	**47**	262.4954	524.9908	1049.982	1447.006	1574.972
110000	**48**	268.4986	536.9971	1073.994	1480.098	1610.991
110001	**49**	274.5247	549.0495	1098.099	1513.318	1647.148
110010	**50**	280.5739	561.1479	1122.296	1546.664	1683.444
110011	**51**	286.6462	573.2925	1146.585	1580.137	1719.877
110100	**52**	292.7417	585.4834	1170.967	1613.739	1756.45
110101	**53**	298.8604	597.7208	1195.442	1647.468	1793.162
110110	**54**	305.0024	610.0047	1220.009	1681.326	1830.014
110111	**55**	311.1677	622.3354	1244.671	1715.312	1867.006
111000	**56**	317.3565	634.7129	1269.426	1749.427	1904.139
111001	**57**	323.5687	647.1374	1294.275	1783.672	1941.412
111010	**58**	329.8044	659.6089	1319.218	1818.047	1978.827
111011	**59**	336.0638	672.1275	1344.255	1852.552	2016.383
111100	**60**	342.3468	684.6935	1369.387	1887.187	2054.081
111101	**61**	348.6535	697.3069	1394.614	1921.952	2091.921
111110	**62**	354.9839	709.9678	1419.936	1956.849	2129.903
111111	**63**	361.3382	722.6764	1445.353	1991.877	2168.029

Table 14. Stereo ADC 1 Filter Wind Filter Fc Selection when MX0E05[2:0] and MX0E007[2:0]=011'b

MX0E06[5:0] MX0E08[5:0]		L & R Channel Sampling Rate Setting (Hz)				
		8000	16000	32000	44100	48000
n(HEX)	n(DEC)	Fc (Hz)				
000000	0	2.489228	4.978456	9.956913	13.72187	14.93537
000001	1	4.983323	9.966646	19.93329	27.47057	29.89994
000010	2	7.482294	14.96459	29.92917	41.24614	44.89376
000011	3	9.98615	19.9723	39.9446	55.04865	59.9169
000100	4	12.4949	24.9898	49.9796	68.87814	74.96941
000101	5	15.00856	30.01711	60.03423	82.73467	90.05134
000110	6	17.52713	35.05425	70.1085	96.61828	105.1628
000111	7	20.05062	40.10124	80.20248	110.529	120.3037
001000	8	22.57904	45.15809	90.31618	124.467	135.4743
001001	9	25.11241	50.22483	100.4497	138.4322	150.6745
001010	10	27.65073	55.30147	110.6029	152.4247	165.9044
001011	11	30.19401	60.38803	120.7761	166.4445	181.1641
001100	12	32.74227	65.48453	130.9691	180.4917	196.4536
001101	13	35.2955	70.591	141.182	194.5664	211.773
001110	14	37.85372	75.70744	151.4149	208.6686	227.1223
001111	15	40.41694	80.83389	161.6678	222.7984	242.5017
010000	16	42.98517	85.97035	171.9407	236.9558	257.911
010001	17	45.55842	91.11684	182.2337	251.1408	273.3505
010010	18	48.1367	96.27339	192.5468	265.3535	288.8202
010011	19	50.72001	101.44	202.88	279.5941	304.3201
010100	20	53.30837	106.6167	213.2335	293.8624	319.8502
010101	21	55.90178	111.8036	223.6071	308.1586	335.4107
010110	22	58.50026	117.0005	234.0011	322.4827	351.0016
010111	23	61.10382	122.2076	244.4153	336.8348	366.6229
011000	24	63.71246	127.4249	254.8498	351.2149	382.2748
011001	25	66.32619	132.6524	265.3048	365.6231	397.9572
011010	26	68.94503	137.8901	275.7801	380.0595	413.6702
011011	27	71.56898	143.138	286.2759	394.524	429.4139
011100	28	74.19805	148.3961	296.7922	409.0167	445.1883
011101	29	76.83225	153.6645	307.329	423.5378	460.9935
011110	30	79.47159	158.9432	317.8864	438.0871	476.8295
011111	31	82.11608	164.2322	328.4643	452.6649	492.6965
100000	32	84.76573	169.5315	339.0629	467.2711	508.5944

100001	**33**	87.42055	174.8411	349.6822	481.9058	524.5233
100010	**34**	90.08055	180.1611	360.3222	496.569	540.4833
100011	**35**	92.74574	185.4915	370.9829	511.2609	556.4744
100100	**36**	95.41612	190.8322	381.6645	525.9813	572.4967
100101	**37**	98.0917	196.1834	392.3668	540.7305	588.5502
100110	**38**	100.7725	201.545	403.09	555.5085	604.635
100111	**39**	103.4585	206.9171	413.8341	570.3152	620.7512
101000	**40**	106.1498	212.2996	424.5992	585.1508	636.8988
101001	**41**	108.8463	217.6926	435.3852	600.0152	653.0778
101010	**42**	111.5481	223.0961	446.1922	614.9087	669.2884
101011	**43**	114.2551	228.5102	457.0203	629.8311	685.5305
101100	**44**	116.9674	233.9347	467.8695	644.7826	701.8042
101101	**45**	119.6849	239.3699	478.7398	659.7632	718.1096
101110	**46**	122.4078	244.8156	489.6312	674.773	734.4468
101111	**47**	125.136	250.2719	500.5438	689.812	750.8157
110000	**48**	127.8694	255.7388	511.4777	704.8802	767.2165
110001	**49**	130.6082	261.2164	522.4328	719.9777	783.6492
110010	**50**	133.3523	266.7046	533.4093	735.1047	800.1139
110011	**51**	136.1018	272.2035	544.4071	750.261	816.6106
110100	**52**	138.8566	277.7131	555.4262	765.4467	833.1393
110101	**53**	141.6167	283.2334	566.4668	780.662	849.7002
110110	**54**	144.3822	288.7644	577.5288	795.9069	866.2932
110111	**55**	147.1531	294.3062	588.6123	811.1814	882.9185
111000	**56**	149.9293	299.8587	599.7174	826.4855	899.576
111001	**57**	152.711	305.422	610.844	841.8193	916.2659
111010	**58**	155.498	310.9961	621.9921	857.1829	932.9882
111011	**59**	158.2905	316.581	633.162	872.5763	949.743
111100	**60**	161.0884	322.1767	644.3535	887.9996	966.5302
111101	**61**	163.8917	327.7833	655.5667	903.4528	983.35
111110	**62**	166.7004	333.4008	666.8016	918.936	1000.202
111111	**63**	169.5146	339.0292	678.0583	934.4491	1017.087

Table 15. Stereo ADC 1 Filter Wind Filter Fc Selection when MX0E05[2:0] and MX0E007[2:0]=100'b

MX0E06[5:0] MX0E08[5:0]		L & R Channel Sampling Rate Setting (Hz)				
		8000	16000	32000	44100	48000
n(HEX)	n(DEC)	Fc (Hz)				
000000	0	1.244006	2.488013	4.976025	6.857585	7.464038
000001	1	2.489228	4.978456	9.956913	13.72187	14.93537
000010	2	3.735667	7.471333	14.94267	20.59286	22.414
000011	3	4.983323	9.966646	19.93329	27.47057	29.89994
000100	4	6.232198	12.4644	24.92879	34.35499	37.39319
000101	5	7.482294	14.96459	29.92917	41.24614	44.89376
000110	6	8.73361	17.46722	34.93444	48.14403	52.40166
000111	7	9.98615	19.9723	39.9446	55.04865	59.9169
001000	8	11.23991	22.47983	44.95965	61.96002	67.43948
001001	9	12.4949	24.9898	49.9796	68.87814	74.96941
001010	10	13.75112	27.50223	55.00446	75.80302	82.50669
001011	11	15.00856	30.01711	60.03423	82.73467	90.05134
001100	12	16.26723	32.53445	65.06891	89.67309	97.60336
001101	13	17.52713	35.05425	70.1085	96.61828	105.1628
001110	14	18.78826	37.57651	75.15303	103.5703	112.7295
001111	15	20.05062	40.10124	80.20248	110.529	120.3037
010000	16	21.31421	42.62843	85.25686	117.4946	127.8853
010001	17	22.57904	45.15809	90.31618	124.467	135.4743
010010	18	23.84511	47.69022	95.38044	131.4462	143.0707
010011	19	25.11241	50.22483	100.4497	138.4322	150.6745
010100	20	26.38095	52.76191	105.5238	145.425	158.2857
010101	21	27.65073	55.30147	110.6029	152.4247	165.9044
010110	22	28.92175	57.84351	115.687	159.4312	173.5305
010111	23	30.19401	60.38803	120.7761	166.4445	181.1641
011000	24	31.46752	62.93504	125.8701	173.4647	188.8051
011001	25	32.74227	65.48453	130.9691	180.4917	196.4536
011010	26	34.01826	68.03652	136.073	187.5257	204.1096
011011	27	35.2955	70.591	141.182	194.5664	211.773
011100	28	36.57399	73.14797	146.2959	201.6141	219.4439
011101	29	37.85372	75.70744	151.4149	208.6686	227.1223
011110	30	39.13471	78.26941	156.5388	215.7301	234.8082
011111	31	40.41694	80.83389	161.6678	222.7984	242.5017
100000	32	41.70043	83.40086	166.8017	229.8736	250.2026

100001	**33**	42.98517	85.97035	171.9407	236.9558	257.911
100010	**34**	44.27117	88.54234	177.0847	244.0448	265.627
100011	**35**	45.55842	91.11684	182.2337	251.1408	273.3505
100100	**36**	46.84693	93.69386	187.3877	258.2437	281.0816
100101	**37**	48.1367	96.27339	192.5468	265.3535	288.8202
100110	**38**	49.42772	98.85545	197.7109	272.4703	296.5663
100111	**39**	50.72001	101.44	202.88	279.5941	304.3201
101000	**40**	52.01356	104.0271	208.0542	286.7247	312.0813
101001	**41**	53.30837	106.6167	213.2335	293.8624	319.8502
101010	**42**	54.60444	109.2089	218.4178	301.007	327.6267
101011	**43**	55.90178	111.8036	223.6071	308.1586	335.4107
101100	**44**	57.20039	114.4008	228.8016	315.3172	343.2023
101101	**45**	58.50026	117.0005	234.0011	322.4827	351.0016
101110	**46**	59.80141	119.6028	239.2056	329.6553	358.8084
101111	**47**	61.10382	122.2076	244.4153	336.8348	366.6229
110000	**48**	62.4075	124.815	249.63	344.0214	374.445
110001	**49**	63.71246	127.4249	254.8498	351.2149	382.2748
110010	**50**	65.01869	130.0374	260.0748	358.4155	390.1121
110011	**51**	66.32619	132.6524	265.3048	365.6231	397.9572
110100	**52**	67.63497	135.2699	270.5399	372.8378	405.8098
110101	**53**	68.94503	137.8901	275.7801	380.0595	413.6702
110110	**54**	70.25636	140.5127	281.0254	387.2882	421.5382
110111	**55**	71.56898	143.138	286.2759	394.524	429.4139
111000	**56**	72.88287	145.7657	291.5315	401.7668	437.2972
111001	**57**	74.19805	148.3961	296.7922	409.0167	445.1883
111010	**58**	75.5145	151.029	302.058	416.2737	453.087
111011	**59**	76.83225	153.6645	307.329	423.5378	460.9935
111100	**60**	78.15128	156.3026	312.6051	430.8089	468.9077
111101	**61**	79.47159	158.9432	317.8864	438.0871	476.8295
111110	**62**	80.79319	161.5864	323.1728	445.3725	484.7591
111111	**63**	82.11608	164.2322	328.4643	452.6649	492.6965

7.11. I²C Control Interface

I²C is a 2-wire (SCL/SDA) half-duplex serial communication interface, supporting only slave mode. SCL is used for clock and SDA is for data. SCL clock supports up to 400kHz rate and SDA data is an open drain structure. The input has built-in spike filter and can remove less than 50ns spike at SCL and SDA.

7.11.1. Device Address Setting

Device address is 0x1B'h for 7 bits format definition

Table 16. 7 Bits Device Address Setting include the R/W bit (0x1B'h)

(MSB)			BIT			(LSB)
0	0	1	1	0	1	1

Device address is 0x36'h for 8 bits format definition

Table 17. 8 Bits Device Address Setting include the R/W bit (0x36'h)

(MSB)			BIT				(LSB)
0	0	1	1	0	1	1	R/W

7.11.2. Complete Data Transfer

Data Transfer over I²C Control Interface

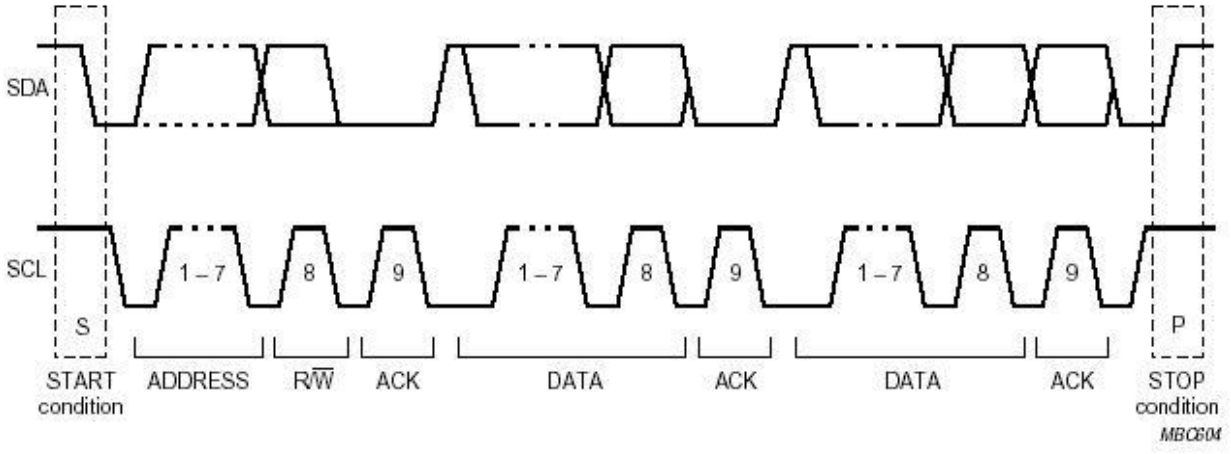
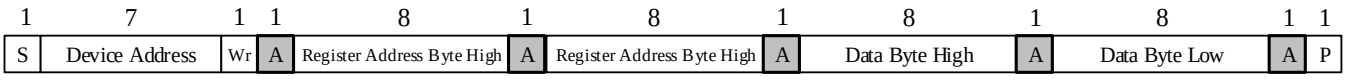
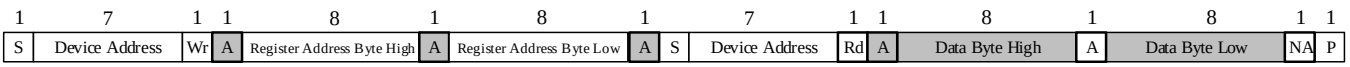


Figure 15. Data Transfer over I²C Control Interface

16 bits Register Address Write WORD Protocol:



16 bits Register Address Read WORD Protocol:



S**: Start Condition**

Slave Address: 7-bit Device Address

Wr: 0 for Write Command

Rd: 1 for Read Command

Command Code: 8-bit Mixer Address

A: **0 FOR ACK, 1 FOR NACK**

Register Address Byte: 16-bit Mixer data

Data Byte: 16-bit Mixer data

☐:Master-to-Slave

☐:Slave-to-Master

7.12. GPIO, Interrupt and Jack Detection

The ALC5616E supports one GPIO – GPIO1 and two jack detection pins.

For GPIO function, the GPIO can be configured to input or output. For input type, the internal circuit can read pin status and report to register table. For output type, the internal circuit can drive this pin to high or low to control external device. In GPIO function, the pin polarity can be controlled by register at output type.

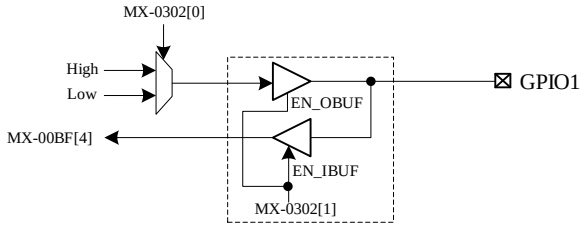


Figure 16. GPIO Function Block

For IRQ function is shown at Figure 17, the IRQ output source can be selected from, jack detection status, and MICBIAS Over-Current Status. When either status is triggered, the GPIO will output a flag as interrupt signal to external device.

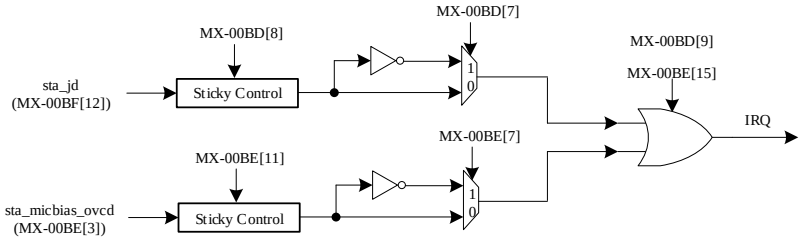
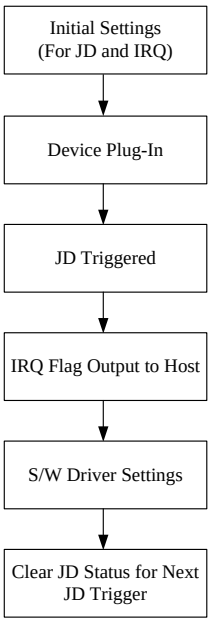


Figure 17. IRQ Function Block

In general, the IRQ output needs to combine with JD function. When JD is trigger, IRQ will output a flag to host to notice S/W driver. The S/W driver will do something by system design. The behavior flow chard as following:



The MICBIAS supports short detection function. When MICBIAS circuit is short, MICBIAS circuit will generate an over-current flag. The flag can generate an interrupt signal to notice host and let S/W do follow-up processes.

7.13. Power Management

ALC5616E detailed Power Management control registers are supported in MX-0061~0066h. Each particular block will only be active when each bit of each register is set to enable.

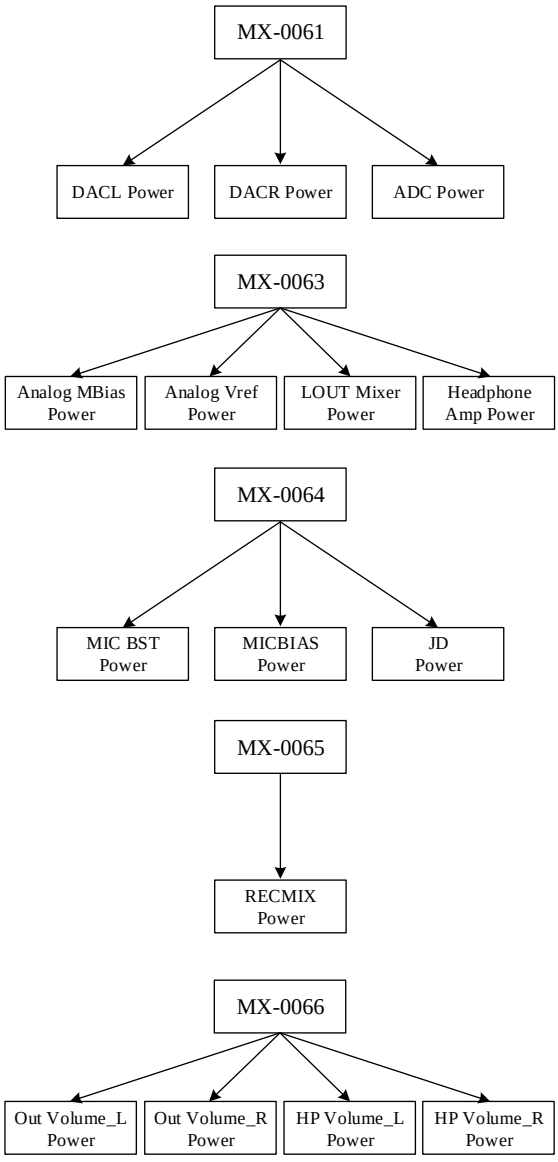


Figure 18. Power Management

8. Registers List

ALC5616E register map as shown as following and accessing unimplemented registers will return a 0.

8.1. Register Map

Table 18. Register Map

Type	Name	Description	Register Address	Reset State
Reset	S/W Reset	S/W Reset & Device ID	MX-0000h	0x0000'h
Analog Input/Output	HPOUT	Headphone Output Volume & Mute/Un-Mute	MX-0002h	0xC8C8'h
	Line Output	Line Output Control 1	MX-0003h	0xC8C8'h
		Line Output Control 2	MX-0005h	0x0000'h
	MIC Input	IN1/2 Mode and Gain Boost Control	MX-000Dh	0x0000'h
Digital Gain/Volume	DACL1/R1	DACL1/R1 Digital Volume Control	MX-0019h	0xAFAF'h
	ADCL/R-1	ADC Boost Gain	MX-0E00h	0x0001'h
	ADCL/R-2	ADC Mute/Unmute	MX-0E02h	0x0000'h
	ADCL/R-3	ADC Lch Volume	MX-0E03h	0x002F'h
	ADCL/R-4	ADC Rch Volume	MX-0E04h	0x002F'h
Digital Mixer	ADC-1	ADC Stereo1 Digital Mixer Control	MX-0027h	0x6060'h
	ADC-2	ADC to DAC Digital Mixer Control	MX-0029h	0x8080'h
	DAC-1	DAC Stereo Digital Mixer Control	MX-002Ah	0x4242'h
Input Mixer	RECMIXL	RECMIXL Gain & Selection Control	MX-003Ch	0x006F'h
Output Mixer	HPOMIX	HPOMIX Gain & Selection Control	MX-0045h	0x6000'h
	LOUTMIX	LOUTMIX Control	MX-0053h	0xF000'h
Power Management	Management-1	DAC & ADC & Power Control	MX-0061h	0x0000'h
	Management-2	VREF & MBias & LOUTMIX & HP & LDO Power Control	MX-0062h	0x00C6'h
	Management-3	MICBST & MICBIAS & JD Power Control	MX-0063h	0x0000'h
	Management-4	OUTMIX & RECMIX Power Control	MX-0064h	0x0000'h
	Management-5	OUTVOL & HPOVOL & INVOL Power Control	MX-0065h	0x0000'h
	Management-6	Digital Filter Power Control	MX-0208h	0x0600'h
Digital Interface	I2S1 Port Ctrl	I2S-1 Interface Control	MX-2200h	0x0038'h
Global Clock	Global Clock	Global Clock Control 1	MX-0200h	0x0000'h
	Global Clock	Global Clock Control 2	MX-0201h	0x0000'h
	Global Clock	Global Clock Control 3	MX-0203h	0x0000'h
	Global Clock	Global Clock Control 4	MX-0204h	0x0000'h
	Global Clock	Global Clock Control 5	MX-0207h	0x0000'h
	PLL-1	PLL Control-1	MX-0081h	0x0000'h
	PLL-2	PLL Control-2	MX-0082h	0x0000'h
HP Amp	HP	HP Amp Control 1	MX-008Eh	0x0004'h
		HP Amp Control 2	MX-008Fh	0x1100'h
MICBIAS	MICBIAS	MICBIAS Control	MX-0093h	0x2000'h
Jack Detection	JD-1	Jack Detection Control-1	MX-00BBh	0x0000'h
	JD-2	Jack Detection Control-2	MX-00BCh	0x0000'h
IRQ	IRQ-1	IRQ Control-1	MX-00BDh	0x0000'h

Type	Name	Description	Register Address	Reset State
	IRQ-2	IRQ Control-2	MX-00BEh	0x0000’h
Flag Status	Status	GPIO & Internal Status	MX-00BFh	0x0000’h
GPIO	GPIO-1	GPIO Control-1	MX-0302h	0x0000’h
	GPIO-2	GPIO Control-2	MX-0304h	0x0055’h
Wind Filter	Control-1	Wind Filter Control 1	MX-0E05h	0x00F3’h
	Control-2	Wind Filter Control 2	MX-0E06h	0x0000’h
	Control-3	Wind Filter Control 3	MX-0E07h	0x0023’h
	Control-4	Wind Filter Control 4	MX-0E08h	0x0000’h
General Control	Digital	Digital Misc. Control	MX-00FAh	0x0090’h
	ADC/DAC	ADC/DAC RESET Control	MX-013Dh	0xA800’h
Vendor ID	ID	Vendor ID	MX-00FEh	0x10EC’h

8.2. MX-0000h: S/W Reset & Device ID

Default: 0000'h

Table 19. MX-0000h: S/W Reset & Device ID

Port Name	Bits	Read/Write	Reset State	Description
Reserved	15:0	R	0000’h	Reserved

Note: Writes any value to this register will reset all registers to their default values.

8.3. MX-0002h: Headphone Output Control

Default: C8C8'h

Table 20. MX-0002h: Headphone Output Control

Name	Bits	Read/Write	Reset State	Description
mu_hpo_l	15	R/W	1’h	Mute Control for Left Headphone Output Port (HPOL) 0’b: Un-Mute 1’b: Mute
Mu_hpovoll_in	14	R/W	1’h	Mute Control for Left Headphone Volume Channel (HPOVOLL) 0’b: Un-Mute 1’b: Mute
vol_hpol	13:8	R/W	8’h	Left Headphone Channel Volume Control (HPOVOLL) ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step

Name	Bits	Read/Write	Reset State	Description
mu_hpo_r	7	R/W	1'h	Mute Control Right Headphone Output Port (HPOR) 0'b: Un-Mute 1'b: Mute
Mu_hpovolr_in	6	R/W	1'h	Mute Control for Right Headphone Volume Channel (HPOVOLR) 0'b: Un-Mute 1'b: Mute
Vol_hpor	5:0	R/W	8'h	Right Headphone Channel Volume Control (HPOVOLR)❶ 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42
5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			
10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			
12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

8.4. MX-0003h: LINE Output Control 1

Default: C8C8'h

Table 21. MX-0003h: LINE Output Control 1

Name	Bits	Read/Write	Reset State	Description
Mu_lout_l	15	R/W	1'h	Mute Control for Left Line Output Port(LOUTL) 0'b: Un-Mute 1'b: Mute
Mu_outvoll_in	14	R/W	1'h	Mute Control for Left Output Volume Channel (OUTVOLL) 0'b: Un-Mute 1'b: Mute
Vol_outl	13:8	R/W	08'h	Left Output Volume Control (OUTVOLL) ❶ 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step
Mu_lout_r	7	R/W	1'h	Mute Control for Right Line Output Port (LOUTR) 0'b: Un-Mute 1'b: Mute
Mu_outvolr_in	6	R/W	1'h	Mute Control for Right Output Volume Channel (OUTVOLR) 0'b: Un-Mute 1'b: Mute
Vol_outr	5:0	R/W	08'h	Right Output Volume Control ❶ 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42

5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			
10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			
12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

8.5. MX-0005h: LINE Output Control 2

Default: 0000'h

Table 22. MX-0005h: LINE Output Control 2

Name	Bits	Read/Write	Reset State	Description
En_dfo	15	R/W	0’h	Enable Differential Line Output 0’b: Disable 1’b: Enable (LP / RN)
reserved	14:0	R	0’h	Reserved

8.6. MX-000Dh: IN1 Input Control

Default: 0000'h

Table 23. MX-000Dh: IN1 Input Control

Name	Bits	Read/Write	Reset State	Description
Sel_bst1	15:12	R/W	0’h	IN1 Boost Control (BST1) 0000’b: Bypass 0001’b: +20dB 0010’b: +24dB 0011’b: +30dB 0100’b: +35dB 0101’b: +40dB 0110’b: +44dB 0111’b: +50dB 1000’b: +52dB Others : Reserved
reserved	14:0	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
En_in1_df	7	R/W	0’h	IN1 Input Mode Control 0’b: Single Ended Mode 1’b: Differential Mode
reserved	6:0	R	0’h	Reserved

8.7. MX-0019h: DACL1/R1 Digital Volume

Default: FFFF'h

Table 24. MX-0019h: DACL1/R1 Digital Volume

Name	Bits	Read/Write	Reset State	Description
vol_dac1_l	15:8	R/W	AF’h	DAC1 Left Channel Digital Volume 00’h: -95.625dB … FF’h: 0dB, with 0.375dB/Step
vol_dac1_r	7:0	R/W	AF’h	DAC1 Right Channel Digital Volume 00’h: -95.625dB … FF’h: 0dB, with 0.375dB/Step

8.8. MX-0027h: Stereo1 ADC Digital Mixer Control

Default: 6060'h

Table 25. MX-0027h: Stereo1 ADC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0’h	reserved
mu_stereo1_adcl	14	R/W	1’h	Mute Control for Stereo1 ADC1 Left Channel 0’b: Un-Mute 1’b: Mute
reserved	13:7	R	40’h	Reserved
mu_stereo1_adcr	6	R/W	1’h	Mute Control for Stereo1 ADC1 Right Channel 0’b: Un-Mute 1’b: Mute
reserved	5:0	R	20’h	reserved

8.9. MX-0029h: Stereo ADC to DAC Digital Mixer Control

Default: 8080'h

Table 26. MX-0029h: Stereo ADC to DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
mu_stereo1_adc_mixer_l	15	R/W	1'h	Mute Control for Stereo1 ADC Left Channel to DAC 0'b: Un-Mute 1'b: Mute
mu_dac1_l	14	R/W	0'h	Mute Control for I2S-1 to DAC Left Channel 0'b: Un-Mute 1'b: Mute
Reserved	13:8	R	0'h	Reserved
mu_stereo1_adc_mixer_r	7	R/W	1'h	Mute Control for Stereo1 ADC Right Channel to DAC 0'b: Un-Mute 1'b: Mute
mu_dac1_r	6	R/W	0'h	Mute Control for I2S-1 to DAC Right Channel 0'b: Un-Mute 1'b: Mute
reserved	5:0	R	0'h	reserved

8.10. MX-002Ah: Stereo DAC Digital Mixer Control

Default: 4242'h

Table 27. MX-002Ah: Stereo DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	reserved
mu_stereo_dacl1_mixl	14	R/W	1'h	Mute Control for DACL1 to Stereo DAC Left Mixer 0'b: Un-Mute 1'b: Mute
gain_dacl1_to_stereo_l	13	R/W	0'h	Gain Control for DACL1 to Stereo DAC Left Mixer 0'b: 0dB 1'b: -6dB
Reserved	12:10	R	0'h	reserved
mu_stereo_dacr1_mixl	9	R/W	1'h	Mute Control for DACR1 to Stereo DAC Left Mixer 0'b: Un-Mute 1'b: Mute
gain_dacr1_to_stereo_l	8	R/W	0'h	Gain Control for DACR1 to Stereo DAC Left Mixer 0'b: 0dB 1'b: -6dB
Reserved	7	R	0'h	reserved
mu_stereo_dacr1_mixr	6	R/W	1'h	Mute Control for DACR1 to Stereo DAC Right Mixer 0'b: Un-Mute 1'b: Mute
gain_dacr1_to_stereo_r	5	R/W	0'h	Gain Control for DACR1 to Stereo DAC Right Mixer 0'b: 0dB 1'b: -6dB

Name	Bits	Read/Write	Reset State	Description
reserved	4:2	R	0’h	reserved
mu_stereo_dacl1_mixr	1	R/W	1’h	Mute Control for DACL1 to Stereo DAC Right Mixer 0’b: Un-Mute 1’b: Mute
gain_dacl1_to_stereo_r	0	R/W	0’h	Gain Control for DACL1 to Stereo DAC Right Mixer 0’b: 0dB 1’b: -6dB

8.11. MX-003Ch: RECMIX Control

Default: 006F'h

Table 28. MX-003Ch: RECMIXL Control

Name	Bits	Read/Write	Reset State	Description
Gain_bst1_recmixl	15:13	R/W	0’h	Gain Control for BST1 to RECMIXL 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: Reserved
reserved	12:2	R	1B’h	reserved
Mu_bst1_recmixl	1	R/W	1’h	Mute Control for BST1 to RECMIXL 0’b: Un-Mute 1’b: Mute
Reserved	0	R	1’h	Reserved

8.12. MX-0045h: HPOMIX Control

Default: 6000'h

Table 29. MX-0045h: HPOMIX Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0’h	Reserved
mu_dac1_hpomix	14	R/W	1’h	Mute Control for DAC1 to HPOMIX 0’b: Un-Mute 1’b: Mute
mu_hpovol_hpomix	13	R/W	1’h	Mute Control for HPOVOL to HPOMIX 0’b: Un-Mute 1’b: Mute

Name	Bits	Read/Write	Reset State	Description
Gain_hpomix	12	R/W	0’h	Gain Control for HPOMIX 0’b: 0dB 1’b: -6dB
Reserved	11:0	R	0’h	Reserved

8.13. MX-0053h: LOUTMIX Control

Default: F000'h

Table 30. MX-0053h: LOUTMIX Control

Name	Bits	Read/Write	Reset State	Description
Mu_dacl1_lout	15	R/W	1’h	Mute DACL1 to LOUT Mixer 0’b: Un-Mute 1’b: Mute
Mu_dacr1_lout	14	R/W	1’h	Mute DACR1 to LOUT Mixer 0’b: Un-Mute 1’b: Mute
Mu_outvoll_lout	13	R/W	1’h	Mute OUTVOLL to LOUT Mixer 0’b: Un-Mute 1’b: Mute
Mu_outvolr_lout	12	R/W	1’h	Mute OUTVOLR to LOUT Mixer 0’b: Un-Mute 1’b: Mute
Bst_lout	11	R/W	0’h	Gain Control for LOUT Mixer 0’b: 0dB 1’b: -6dB
reserved	10:0	R	0’h	Reserved

8.14. MX-0061h: Power Management Control 1

Default: 0000'h

Table 31. MX-0061h: Power Management Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R/W	0’h	Reserved
Pow_dac_l_1	12	R/W	0’h	Analog DACL1 Power Control 0’b: Power Down 1’b: Power On
Pow_dac_r_1	11	R/W	0’h	Analog DACR1 Power Control 0’b: Power Down 1’b: Power On
reserved	10:3	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
Pow_adc	2	R/W	0’h	Analog ADC Power Control 0’b: Power Down 1’b: Power On
Reserved	1:0	R	0’h	Reserved

8.15. MX-0063h: Power Management Control 2

Default: 00C6'h

Table 32. MX-0063h: Power Management Control 2

Name	Bits	Read/Write	Reset State	Description
Pow_vref1	15	R/W	0’h	VREF1 Power Control 0’b: Power Down 1’b: Power On
En_fastb1	14	R/W	0’h	VREF1 Fast Mode Control 0’b: Fast VREF 1’b: Slow VREF, (For good analog performance)
Pow_main_bias	13	R/W	0’h	MBIAS Power Control 0’b: Power Down 1’b: Power On
Pow_lout	12	R/W	0’h	LOUTMIX Power Control 0’b: Power Down 1’b: Power On
Pow_bg_bias	11	R/W	0’h	MBIAS Bandgap Power Control 0’b: Power Down 1’b: Power On
reserved	10:8	R	0’h	Reserved
En_l_hp	7	R/W	1’h	Left Headphone Amp Power Control 0’b: Power Down 1’b: Power On
En_r_hp	6	R/W	1’h	Right Headphone Amp Power Control 0’b: Power Down 1’b: Power On
En_amp_hp	5	R/W	0’h	Improve HP Amp Driving 0’b: Disable 1’b: Enable
Pow_vref2	4	R/W	0’h	VREF2 Power Control 0’b: Power Down 1’b: Power On
En_fastb2	3	R/W	0’h	VREF2 Fast Mode Control 0’b: Fast VREF 1’b: Slow VREF, (For good analog performance)
Reserved	2	R	1’h	Reserved
Ldo_dvo	1:0	R/W	2’h	LDO Output Control 00’b: 1.1V 01’b: 1.2V 10’b: 1.3V 11’b: 1.4V

8.16. MX-0064h: Power Management Control 3

Default: 0000'h

Table 33. MX-0064h: Power Management Control 3

Name	Bits	Read/Write	Reset State	Description
Pow_bst1	15	R/W	0'h	MIC BST1 Power Control 0'b: Power Down 1'b: Power On
Reserved	14:12	R	0'h	Reserved
Pow_micbias	11	R/W	0'h	MICBIAS Power Control 0'b: Power Down 1'b: Power On
reserved	10:6	R/W	0'h	reserved
Pow_bst1_op2	5	R/W	0'h	MIC1 SE Mode Control 0'b: For differential mode 1'b: For single-end mode
Pow_bst2_op2	4	R/W	0'h	MIC2 SE Mode Control 0'b: For differential mode 1'b: For single-end mode or line-input mode
Reserved	3	R	0'h	Reserved
Pow_jd	2	R/W	0'h	JD Power Control 0'b: Power down 1'b: Power on
Reserved	1:0	R	0'h	Reserved

8.17. MX-0065h: Power Management Control 4

Default: 0000'h

Table 34. MX-0065h: Power Management Control 4

Name	Bits	Read/Write	Reset State	Description
reserved	15:12	R	0'h	Reserved
Pow_recmix	11	R/W	0'h	RECMIXL Power Control 0'b: Power Down 1'b: Power On
reserved	10:0	R	0'h	Reserved

8.18. MX-0066h: Power Management Control 5

Default: 0000'h

Table 35. MX-0066h: Power Management Control 5

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
Pow_outvoll	13	R/W	0’h	OUTVOLL Power Control 0’b: Power Down 1’b: Power On
Pow_outvolr	12	R/W	0’h	OUTVOLR Power Control 0’b: Power Down 1’b: Power On
Pow_hpovoll	11	R/W	0’h	HPOVOLL Power Control 0’b: Power Down 1’b: Power On
Pow_hpovolr	10	R/W	0’h	HPOVOLR Power Control 0’b: Power Down 1’b: Power On
reserved	9:0	R	0’h	Reserved

8.19. MX-0081h: PLL Control 1

Default: 0000'h

Table 36. MX-0081h: PLL Control 1

Name	Bits	Read/Write	Reset State	Description
Pll_n_code	15:7	R/W	0’h	PLL N[8:0] Code 000000000’b: Div 2 000000001’b: Div 3 … 111111111’b: Div 513
Reserved	6:5	R	0’h	Reserved
Pll_k_code	4:0	R/W	0’h	PLL K[4:0] Code 00000’b: Div 2 00001’b: Div 3 … 11111’b: Div 33

8.20. MX-0082h: PLL Control 2

Default: 0000'h

Table 37. MX-0082h: PLL Control 2

Name	Bits	Read/Write	Reset State	Description
Pll_m_code	15:12	R/W	0'h	PLL M[3:0] Code 0000'b: Div 2 0001'b: Div 3 … 1111'b: Div 17
Pll_m_bypass	11	R/W	0'h	Bypass PLL M Code 0'b : No bypass 1'b : Bypass
Reserved	10:0	R	0'h	Reserved

8.21. MX-008Eh: HP Amp Control 1

Default: 0004'h

Table 38. MX-008Eh: HP Amp Control 1

Name	Bits	Read/Write	Reset State	Description
Smttrig_hp	15	R/W	0'h	Enable Softgen Trigger for Soft Mute Depop 0'b: Disable 1'b: Enable
reserved	14:10	R/W	0'h	Reserved
En_smt_l_hp	9	R/W	0'h	Enable HP_L Mute/Un-Mute Depop 0'b: Disbale 1'b: Enable
En_smt_r_hp	8	R/W	0'h	Enable HP_R Mute/Un-Mute Depop 0'b: Disbale 1'b: Enable
Pdn_hp	7	R/W	0'h	Capless Depop Power Down Control 0'b: Disbale 1'b: Enable
Softgen_rstn	6	R/W	0'h	Reset Softgen to Initialize SOFTP=1 0'b: Disbale 1'b: Reset
Softgen_rstp	5	R/W	0'h	Reset Softgen to Initialize SOFTP=0 0'b: Disbale 1'b: Reset
En_out_hp	4	R/W	0'h	Enable Headphone Output 0'b: Disable 1'b: Enable
Pow_pump_hp	3	R/W	0'h	Charge Pump Power Control 0'b: Power Down 1'b: Power On
En_softgen_hp	2	R/W	1'h	Power On Soft Generator 0'b: Power down 1'b: Power on

Name	Bits	Read/Write	Reset State	Description
reserved	1	R/W	0’h	Reserved
Pow_capless	0	R/W	0’h	HP Amp All Power On Control 0’b: Power Down 1’b: Power On

8.22. MX-008Fh: HP Amp Control 2

Default: 1100'h

Table 39. MX-008Fh: HP Amp Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
Depop_mode_hp	13	R/W	0’h	Select HP Depop Mode 0’b: Depop mode 1 1’b: Depop mode 2
reserved	12:7	R/W	22’h	Reserved
En_depop_mode1	6	R/W	0’h	HP Depop Mode 1 Control 0’b: Disbale 1’b: Enable
reserved	5:0	R/W	0’h	Reserved

8.23. MX-0091h: HP Amp Control 3

Default: 0C00'h

Table 40. MX-0091h: HP Amp Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15:10	R	3’h	Reserved
Sel_pm_hp	9:8	R/W	0’h	Select HP Capless Power Mode 00’b: 0.6V 01’b: 0.9V 10’b: 1.8V 11’b: Reserved
reserved	7:0	R	0’h	Reserved

8.24. MX-0093h: MICBIAS Control

Default: 2000'h

Table 41. MX-0093h: MICBIAS Control

Name	Bits	Read/Write	Reset State	Description
Sel_micbias	15:14	R/W	0'h	MICBIAS Output Voltage Control 00'b: 2.7V 01'b: 2.4V 10'b: 2.25V 11'b: 1.8V
reserved	13:12	R/W	2'h	Reserved
Pow_mic_ovcd	11	R/W	0'h	MICBIAS Short Current Detector Control 0'b: Disable 1'b: Enable
Mic_ovcd_th_sel	10:9	R/W	0'h	MICBIAS Short Current Detector Threshold 00'b: 600uA 01'b: 1500uA 1x'b: 2000uA Note: tolerance is 200uA
reserved	8:0	R/W	0'h	reserved

8.25. MX-00BBh: Jack Detection Control 1

Default: 0000'h

Table 42. MX-00BBh: Jack Detection Control 1

Name	Bits	Read/Write	Reset State	Description
sel_gpio_jd	15:13	R/W	0'h	Jack Detect Selection 000'b: OFF 001'b: GPIO1 Others: Reserved
reserved	12	R	0'h	Reserved
en_jd_hpo	11	R/W	0'h	Enable Jack Detect Trigger HPOUT 0'b: Disable 1'b: Enable
polarity_jd_tri_hpo	10	R/W	0'h	Select Jack Detect Polarity Trigger HPOUT 0'b: Low trigger 1'b: High trigger
reserved	9:4	R	0'h	Reserved
en_jd_lout	3	R/W	0'h	Enable Jack Detect Trigger LOUT 0'b: Disable 1'b: Enable
polarity_jd_tri_lout	2	R/W	0'h	Select Jack Detect Polarity Trigger LOUT 0'b: Low trigger 1'b: High trigger
reserved	1:0	R/W	0'h	reserved

8.26. MX-00BCh: Jack Detection Control 2

Default: 0000'h

Table 43. MX-00BCh: Jack Detection Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:10	R	0'h	Reserved
Sel_jd_trigger	9	R/W	0'h	JD Trigger Source Selection 0'b: From sta_gpio_jd 1'b: From sta_jd
reserved	8:0	R	0'h	Reserved

8.27. MX-00BDh: IRQ Control 1

Default: 0000'h

Table 44. MX-00BDh: IRQ Control 1

Name	Bits	Read/Write	Reset State	Description
en_irq_gpio_jd	15	R/W	0'h	IRQ Output Source Configure of GPIO Jack Detection Status 0'b: Disable 1'b: Enable
Reserved	14	R	0'h	Reserved
en_gpio_jd_sticky	13	R/W	0'h	Sticky Control for GPIO Jack Detect 0'b: Disable 1'b: Enable
Reserved	12	R	0'h	Reserved
inv_gpio_jd	11	R/W	0'h	GPIO Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
reserved	10	R	0'h	Reserved
en_irq_jd	9	R/W	0'h	IRQ Output Source Configure of Jack Detection Status 0'b: Disable 1'b: Enable
en_jd_sticky	8	R/W	0'h	Sticky Control for Jack Detect 0'b: Disable 1'b: Enable
inv_jd	7	R/W	0'h	Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
Reserved	6:0	R	0'h	Reserved

8.28. MX-00BEh: IRQ Control 2

Default: 0000'h

Table 45. MX-00BEh: IRQ Control 2

Name	Bits	Read/Write	Reset State	Description
en_irq_micbias1_ovcd	15	R/W	0’h	IRQ Output Source Configure of MICBIAS1 Over Current Status 0’b: Disable 1’b: Enable
reserved	14:12	R/W	0’h	Reserved
en_micbias1_ovcd_sticky	11	R/W	0’h	Sticky Control for MICBIAS1 Over Current 0’b: Disable 1’b: Enable
reserved	10:8	R/W	0’h	Reserved
inv_micbias1_ovcd	7	R/W	0’h	MICBIAS1 over current status polarity 0’b: Normal 1’b: Output Invert
reserved	6:4	R	0’h	Reserved
Ovc_micbias1	3	R	0’h	MICBIAS1 Over Current Status Read: return status of each status pin Write: Write ‘0’ to clear stick bit
Reserved	2:0	R	0’h	Reserved

8.29. MX-00BFh: GPIO and Internal Status

Default: 0000'h

Table 46. MX-00BFh: GPIO and Internal Status

Name	Bits	Read/Write	Reset State	Description
Reserved	15:14	R	0’h	Reserved
sta_jd	12	R/W0C	0’h	JD Pin Status Read: return status of JD Write: Write ‘0’ to clear stick bit
Reserved	11:5	R	0’h	Reserved
sta_gpio_jd	4	R/W0C	0’h	GPIO_JD Status Read: Return status of Jack Detect Select output Write: Write ‘0’ to clear stick bit
reserved	3:0	R	0’h	Reserved

8.30. MX-00FAh: Digital Misc. Control

Default: 0090'h

Table 47. MX-00FAh: Digital Misc. Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:1	R	48’h	Reserved
Digital_gate_ctrl	0	R/W	0’h	Clock Gating Control 0’b: Gating 1’b: No Gating

8.31. MX-00FEh: Vendor ID

Default: 10EC'h

Table 48. MX-00FEh: Vendor ID

Name	Bits	Read/Write	Reset State	Description
Vendor_id	15:0	R	10EC’h	Vendor ID

8.32. MX-013Dh: ADC/DAC Reset Control

Default: A800'h

Table 49. MX-013Dh: ADC/DAC Reset Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	5’h	Reserved
en_ckgen_adc	12	R/W	0’h	Enable Clock Generation of ADC 0’b: Disable, 1’b: Enable
Reserved	11:10	R/W	2’h	Reserved

Name	Bits	Read/Write	Reset State	Description
en_ckgen_dac	9	R/W	0’h	Enable Clock Generation of DAC 0’b: Disable, 1’b: Enable
reserved	8:0	R	0’h	reserved

8.33. MX-0200h: Global Clock Control 1

Default: 0000'h

Table 50. MX-0200h: Global Clock Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15:7	R	0’h	Reserved
pow_clk_sys_lp_div	6	R/W	0’h	clk_sys_lp_div gating control 0’b: disable 1’b: enable
pow_clk_sys_div	5	R/W	0’h	clk_sys_div gating control 0’b: disable 1’b: enable
pow_clk_sys	4	R/W	0’h	clk_sys gating control 0’b: disable 1’b: enable
Reserved	3:2	R	0’h	Reserved
sel_sysclk	1:0	R/W	0’h	clk_sys source selection 00’b: MCLK 01’b: PLL 10’b: RC Clock (12MHz) 11’b: Reserved

8.34. MX-0201h: Global Clock Control 2

Default: 0000'h

Table 51. MX-0201h: Global Clock Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:5	R	0’h	Reserved
sel_pll_sour	4	R/W	0’h	PLL reference clock selection 0’b: MCLK 1’b: BCLK
Reserved	3:1	R	0’h	Reserved
pow_pll	0	R/W	0’h	PLL power control 0’b: power off 1’b: power on

8.35. MX-0203h: Global Clock Control 3

Default: 0000'h

Table 52. MX-0203h: Global Clock Control 3

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	0’h	Reserved
sel_adc_osr	7:4	R/W	0’h	ADC over sample rate 0’h: disable 1’h: clk_sys_div1 2’h: clk_sys_div2 3’h: clk_sys_div4 4’h: clk_sys_div6 5’h: clk_sys_div8 6’h: clk_sys_div12 7’h: clk_sys_div16 8’h: clk_sys_div24 9’h: clk_sys_lp_div1 A’h: clk_sys_lp_div2 B’h: Reserved C’h: Reserved D’h: Reserved E’h: Reserved F’h: Reserved
sel_dac_osr	3:0	R/W	0’h	DAC over sample rate 0’h: disable 1’h: clk_sys_div1 2’h: clk_sys_div2 3’h: clk_sys_div4 4’h: clk_sys_div6 5’h: clk_sys_div8 6’h: clk_sys_div12 7’h: clk_sys_div16 8’h: clk_sys_div24 9’h: clk_sys_lp_div1 A’h: clk_sys_lp_div2 B’h: Reserved C’h: Reserved D’h: Reserved E’h: Reserved F’h: Reserved

8.36. MX-0204h: Global Clock Control 4

Default: 0000'h

Table 53. MX-0204h: Global Clock Control 4

Name	Bits	Read/Write	Reset State	Description
Reserved	15:10	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
sel_ad_filter_stereo1_track	9	R/W	0’h	ADC Filter tracking clock selection 0’b: From clk_sys divider 1’b: From tracking clock
sel_da_filter_stereo1_track	8	R/W	0’h	DAC Filter tracking clock selection 0’b: From clk_sys divider 1’b: From tracking clock
sel_ad_filter_stereo1_div	7:4	R/W	0’h	ADC Filter clock 0’h: Disable 1’h: clk_sys_div1 2’h: clk_sys_div2 3’h: clk_sys_div4 4’h: clk_sys_div6 5’h: clk_sys_div8 6’h: clk_sys_div12 7’h: clk_sys_div16 8’h: clk_sys_div24 9’h: clk_sys_lp_div1 A’h: clk_sys_lp_div2 B’h: Reserved C’h: Reserved D’h: Reserved E’h: Reserved F’h: Reserved
sel_da_filter_stereo1_div	3:0	R/W	0’h	DAC Filter clock 0’h: disable 1’h: clk_sys_div1 2’h: clk_sys_div2 3’h: clk_sys_div4 4’h: clk_sys_div6 5’h: clk_sys_div8 6’h: clk_sys_div12 7’h: clk_sys_div16 8’h: clk_sys_div24 9’h: clk_sys_lp_div1 A’h: clk_sys_lp_div2 B’h: Reserved C’h: Reserved D’h: Reserved E’h: Reserved F’h: Reserved

8.37. MX-0207h: Global Clock Control 5

Default: 0000'h

Table 54. MX-0207h: Global Clock Control 5

Name	Bits	Read/Write	Reset State	Description
Reserved	15:10	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
en_i2s1	9	R/W	0’h	I2S enable control 0’b: I2S disable 1’b: I2S enable
pow_clk_i2s_ms	8	R/W	0’h	clk_i2s_ms gating control 0’b: Disable 1’b: Enable
sel_master_i2s_div	7:4	R/W	0’h	I2S Master clock selection 0’h: Disable 1’h: clk_i2s_ms_div2 2’h: clk_i2s_ms_div4 3’h: clk_i2s_ms_div8 4’h: clk_i2s_ms_div12 5’h: clk_i2s_ms_div16 6’h: clk_i2s_ms_div24 7’h: clk_i2s_ms_div32 8’h: clk_i2s_ms_div48 9’h: Reserved A’h: Reserved B’h: Reserved C’h: Reserved D’h: Reserved E’h: Reserved F’h: Reserved
Reserved	3:2	R	0’h	Reserved
Reserved	1	R	0’h	Resrved
sel_i2s_ms	0	R/W	0’h	clk_i2s_ms source selection 0’b: MCLK 1’b: PLL

8.38. MX-0208h: Power Management Control 6

Default: 0000'h

Table 55. MX-0208h: Power Management Control 6

Name	Bits	Read/Write	Reset State	Description
Reserved	15:9	R	3’h	Reserved
pow_softvol	8	R/W	0’h	Soft volume power control 0’b: Power off 1’b: Power on
Reserved	7	R	0’h	Reserved
pow_hp_amp_detect	6	R/W	0’h	HP AMP Detect power control 0’b: Power off 1’b: Power on

Name	Bits	Read/Write	Reset State	Description
pow_stereo1_dac_mix	5	R/W	0’h	DAC Mixer power control 0’b: Power off 1’b: Power on
en_adc_track_stereo1	4	R/W	0’h	ADC tracking enable control for Stereo1 ADC path 0’b: Disable 1’b: Enable
sel_stereo1_dac_mode	3	R/W	0’h	DAC tracking enable control for Stereo1 DAC path 0’b: Disable 1’b: Enable
en_asrc	2	R/W	0’h	Tracking enable control 0’b: Tracking disabled 1’b: Tracking enabled
pow_adc_stereo1_filter	1	R/W	0’h	ADC Filter power control 0’b: Power off 1’b: Power on
pow_dac_stereo1_filter	0	R/W	0’h	DAC Filter power control 0’b: Power off 1’b: Power on

8.39. MX-0302h: GPIO Control 1

Default: 0000'h

Table 56. MX-0302h: GPIO Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15:2	R	0’h	Reserved
sel_gpio1	1	R/W	0’h	GPIO1 Pin Configuration 0’b: Input 1’b: Output
sel_gpio1_logic	0	R/W	0’h	GPIO1 Output Pin Control 0’b: Drive Low 1’b: Drive High

8.40. MX-0304h: GPIO Control 2

Default: 0055'h

Table 57. MX-0304h: GPIO Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	0’h	Reserved
sel_gpio1_type	8	R/W	0’h	GPIO1 Pin Function Select 0’b: GPIO1 1’b: IRQ output
Reserved	7:0	R/W	55’h	Reserved

8.41. MX-0E00h: ADC Digital Boost Gain Control

Default: 0001'h

Table 58. MX-0E00h: ADC Digital Boost Gain Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	0'h	Reserved
ad_bst_gain_l	7:6	R/W	0'h	ADC left channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
ad_bst_gain_r	5:4	R/W	0'h	ADC Right channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Reserved	3:0	R	1'h	Reserved

8.42. MX-0E02h: ADC Digital Mute/Unmute Control

Default: 0000'h

Table 59. MX-0E02h: ADC Digital Mute/Unmute Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	0'h	Reserved
mu_adc_vol_l	7	R/W	0'h	Digital Mute From ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute
Reserved	6:5	R	0'h	Reserved
mu_adc_vol_r	4	R/W	0'h	Digital Mute From ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute
Reserved	3:0	R	0'h	Reserved

8.43. MX-0E03h: ADC Lch Digital Volume Control

Default: 0000'h

Table 60. MX-0E03h: ADC Lch Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:7	R	0'h	Reserved
vol_adcl	6:0	R/W	2F'h	ADC left channel digital volume in 0.375 dB step❶

❶

00'h	*-17.625dB*
2F'h	*0dB*
7F'h	*+30 dB, with 0.375dB/step*

8.44. MX-0E04h: ADC Rch Digital Volume Control

Default: 0000'h

Table 61. MX-0E04h: ADC Rch Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:7	R	0'h	Reserved
vol_adcr	6:0	R/W	2F'h	ADC Right channel digital volume in 0.375 dB step❶

❶ *00'h -17.625dB*
2F'h 0dB
7F'h +30 dB, with 0.375dB/step

8.45. MX-0E05h: Wind Filter Control 1

Default: 00F3'h

Table 62. MX-0E05h: Wind Filter Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	0'h	Reserved
adj_hpf_l_en	7	R/W	1'h	Enable adjustable 2nd high pass filter for left channel. 0'b : Disable 1'b : Enable
ad_dchpf_l_en	6	R/W	1'h	Enable ADC narrow band high pass filter (7Hz) for left channel 0'b : Disable 1'b : Enable
adj_hpf_r_en	5	R/W	1'h	Enable adjustable 2nd high pass filter for right channel 0'b : Disable 1'b : Enable
ad_dchpf_r_en	4	R/W	1'h	Enable ADC narrow band high pass filter (7Hz) for right channel 0'b : Disable 1'b : Enable
Reserved	3	R	0'h	Reserved
adj_hpf_coef_l_sel	2:0	R/W	3'h	Left channel coefficient coarse select for Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved

8.46. MX-0E06h: Wind Filter Control 2

Default: 0000'h

Table 63. MX-0E06h: Wind Filter Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:6	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
adj_hpf_coef_l_num	5:0	R/W	0’h	Left channel coefficient fine select for Filter (0~63)

8.47. MX-0E07h: Wind Filter Control 3

Default: 0023'h

Table 64. MX-0E07h: Wind Filter Control 3

Name	Bits	Read/Write	Reset State	Description
Reserved	15:3	R	4’h	Reserved
adj_hpf_coef_r_sel	2:0	R/W	3’h	Right channel coefficient coarse select for Filter (If fs = 48kHz) 000’b : fc = 120.3~12000Hz 001’b : fc = 59.9~4915.9Hz 010’b : fc = 29.8~2168Hz 011’b : fc = 14.9~1017Hz 100’b : fc = 7.46~492.7Hz 101’b : Reserved 110’b : Reserved 111’b : Reserved

8.48. MX-0E08h: Wind Filter Control 4

Default: 0000'h

Table 65. MX-0E08h: Wind Filter Control 4

Name	Bits	Read/Write	Reset State	Description
Reserved	15:6	R	0’h	Reserved
adj_hpf_coef_r_num	5:0	R/W	0’h	Right channel coefficient fine select for Filter (0~63)

8.49. MX-2200h: I2S Interface Control

Default: 0000'h

Table 66. MX-2200h: I2S Interface Control

Name	Bits	Read/Write	Reset State	Description
sel_i2s_bclk_ms	15	R/W	0’h	Master Mode clock relative of BCLK and LRCK 0’b: 16Bits (32FS) 1’b: 32Bits (64FS)
Reserved	14	R	0’h	Reserved
inv_i2s_sclk	13	R/W	0’h	I2S BCLK Polarity Control 0’b: Normal 1’b: Invert
stereo_i2s_self_lpbk_en	12	R/W	0’h	DACDAT Loopback to ADCDAT 0’b: Loopback disable 1’b: Loopback enable
sel_i2s_tx_ch	11:10	R/W	0’h	Select Interface DAC Data Swap 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R

Name	Bits	Read/Write	Reset State	Description
sel_i2s_rx_ch	9:8	R/W	0'h	Select Interface ADC Data Swap 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
en_i2s_mono	7	R/W	0'h	Enable I2S PCM 17FS Mono mode 0'b: Disable 1'b: Enable
i2s_data_len_sel	6:4	R/W	3'h	I2S Data Length Selection 000'b : 8 bits 001'b : 16 bits 010'b : 20 bits 011'b : 24 bits 100'b : 32 bits Others: 8 bits
sel_i2s_ms	3	R/W	1'h	I2S Serial Data Port Mode Selection 0'b: Master 1'b: Slave
sel_i2s_format	2:0	R/W	0'h	I2S PCM Data Format Selection 000'b: I2S format 001'b: Left justified 010'b: PCM Mode A (LRCK One Plus at Master Mode) 011'b: PCM Mode B (LRCK One Plus at Master Mode) 100'b: Reserved 101'b: Reserved 110'b: PCM Mode A-N (LRCK One Plus at Master Mode) 111'b: PCM Mode B-N (LRCK One Plus at Master Mode)

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 67. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DBVDD	-0.3	-	3.63	V
Digital Core	DCVDD	-0.3	-	1.98	V
Analog	AVDD	-0.3	-	1.98	V
Analog	DACREF	-0.3	-	1.98	V
Headphone	CPVDD	-0.3	-	1.98	V
Micbias	MICVDD	-0.3	-	3.63	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

9.1.2. Recommended Operating Conditions

Table 68. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD	1.71	1.8	3.6	V
Digital Core	DCVDD	1.1	1.2	1.9	V
Analog	AVDD	1.71	1.8	1.9	V
Analog	DACREF	1.71	1.8	1.9	V
Headphone	CPVDD	1.71	1.8	1.9	V
Micbias	MICVDD	3.0	3.3	3.6	V

9.1.3. Static Characteristics

Table 69. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DBVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DBVDD	V
High Level Input Voltage	V_{IH}	0.65DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DBVDD	V
Output Buffer High Drive Current	-	0.6	1.8	4.3	mA
Output Buffer Low Drive Current	-	0.7	2.1	4.8	mA
Input Buffer Pull-Up Resistor	-	55	110	270	KΩ
Input Buffer Pull-Down Resistor	-	63	130	300	KΩ

Note: DBVDD=1.8V, DCVDD=1.2V, $T_{ambient}$=40°C.

9.2. Analog Performance Characteristics

Table 70. Analog Performance Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DAC to Headphone Output (Loading = 32 Ohm)						
Full Swing Output Voltage	FSOV	Digital Input=0dBFS	-	1	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSOV	-	98	-	dBrA
Dynamic Range	DNR	A-Weighting Reference: FSOV Input=-60dBFS,	-	98	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	Po=20mW	-	-82	-	dB
		Po=10mW	-	-82	-	dB
Crosstalk	Xtalk	Po=20mW	-	-100	-	dB
Output Noise Floor	N	A-Weighting	-	12.5	-	uV
Power Supply Rejection Ratio (1.8V Domain)	PSRR	100mVrms 217Hz~4kHz	60	-	78	dB
DAC to Headphone Output (Loading = 16 Ohm)						
Full Swing Output Voltage	FSOV	Digital Input=0dBFS	-	0.9	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSOV	-	98	-	dBrA
Dynamic Range	DNR	A-Weighting Reference: FSOV Input=-60dBFS,	-	98	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	Po=30mW	-	-82	-	dB
		Po=20mW	-	-82	-	dB
Crosstalk	Xtalk	Po=20mW	-	-100	-	dB
Output Noise Floor	N	A-Weighting	-	12.5	-	uV
Power Supply Rejection Ratio (1.8V Domain)	PSRR	100mVrms 217Hz~4kHz	60	-	78	dB
DAC to LOUT Output (Loading = 10k Ohm)						
Full Swing Output Voltage	FSOV	Digital Input=0dBFS	-	1	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSOV	-	98	-	dBrA
Dynamic Range	DNR	A-Weighting Reference: FSOV Input=-60dBFS,	-	98	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	Digital Input=0dBFS	-	-85	-	dB
Crosstalk	Xtalk	Output=1Vrms	-	-100	-	dB
Output Noise Floor	N	A-Weighting	-	12.5	-	uV
Power Supply Rejection Ratio (1.8V Domain)	PSRR	100mVrms 217Hz~4kHz	60	-	78	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Mic Input to ADC (Single Mode)						
Maximum Input Voltage	FSIV	Digital Input=0dBFS	-	0.6	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSIV BST Gain=0dB	-	94	-	dBrA
		A-Weighting Reference: FSIV BST Gain=20dB	-	89	-	dBrA
		A-Weighting Reference: FSIV BST Gain=40dB	-	78	-	dBrA
		A-Weighting Reference: FSIV BST Gain=50dB	-	68	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	-		83		dB
Power Supply Rejection Ratio (1.8V Domain)	PSRR	100mVrms 217Hz~4kHz	-	70	-	dB
Mic Input to ADC (Differential Mode)						
Maximum Input Voltage	FSIV	Digital Input=0dBFS	-	1.2	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSIV BST Gain=0dB	-	94	-	dBrA
		A-Weighting Reference: FSIV BST Gain=20dB	-	89	-	dBrA
		A-Weighting Reference: FSIV BST Gain=40dB	-	78	-	dBrA
		A-Weighting Reference: FSIV BST Gain=50dB	-	68	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	-	87	83	93	dB
Power Supply Rejection Ratio (1.8V Domain)	PSRR	100mVrms 217Hz~4kHz	-	70	-	dB

Note: Standard test conditions:
$T_{ambient}$=25℃
VVPD=5V
1kHz input sine wave; 24Bits Data Length PCM Sampling frequency=48kHz; Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation
dBA: with A-Weighting

9.3. Signal Timing

9.3.1. I²C Control Interface

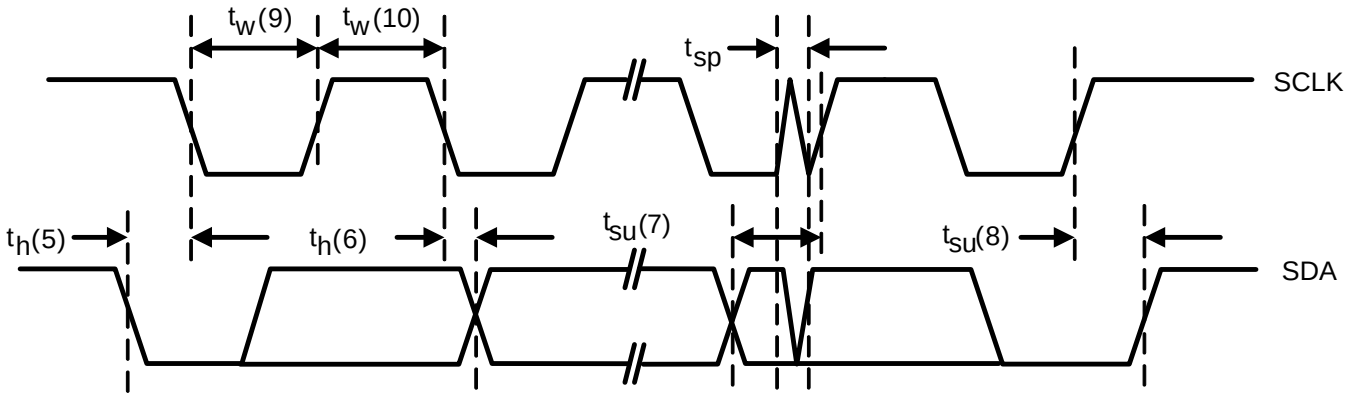


Figure 24. I²C Control Interface

Table 71. I²C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	$t_w(9)$	1.3	-	-	µs
Clock Pulse Duration	$t_w(10)$	600	-	-	ns
Clock Frequency	F	0	-	400K	Hz
Start Hold Time	$t_h(5)$	600	-	-	ns
Data Setup Time	$t_{su}(7)$	100	-	-	ns
Data Hold Time	$t_h(6)$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su}(8)$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

9.3.2. I²S/PCM Interface Master Mode

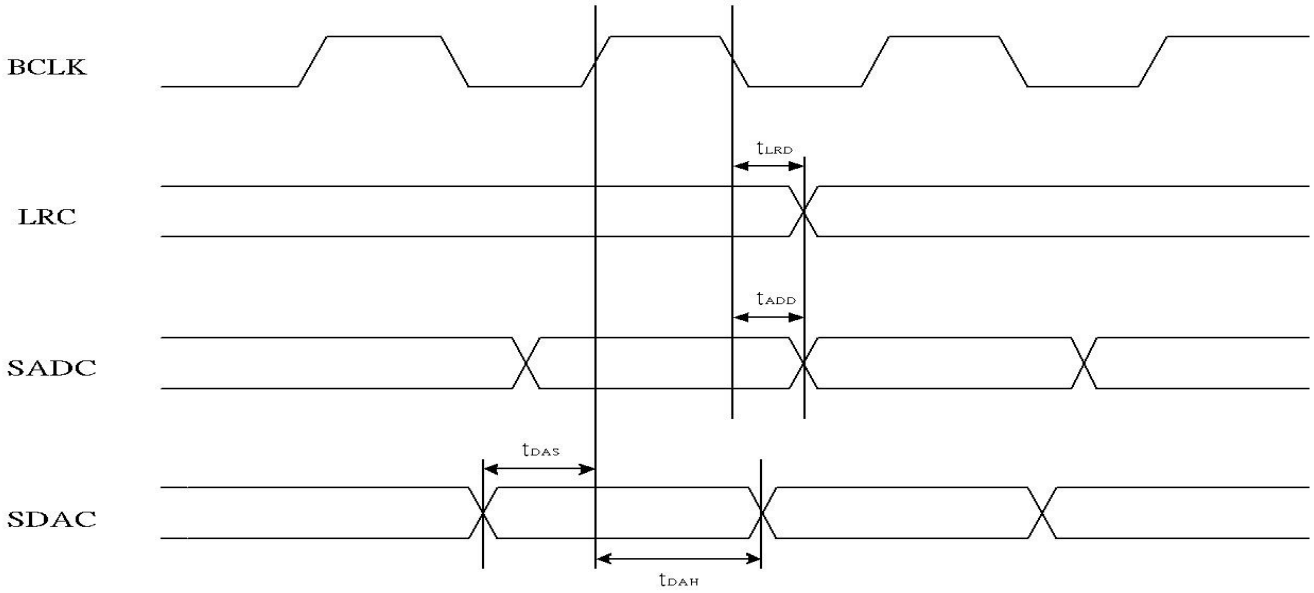
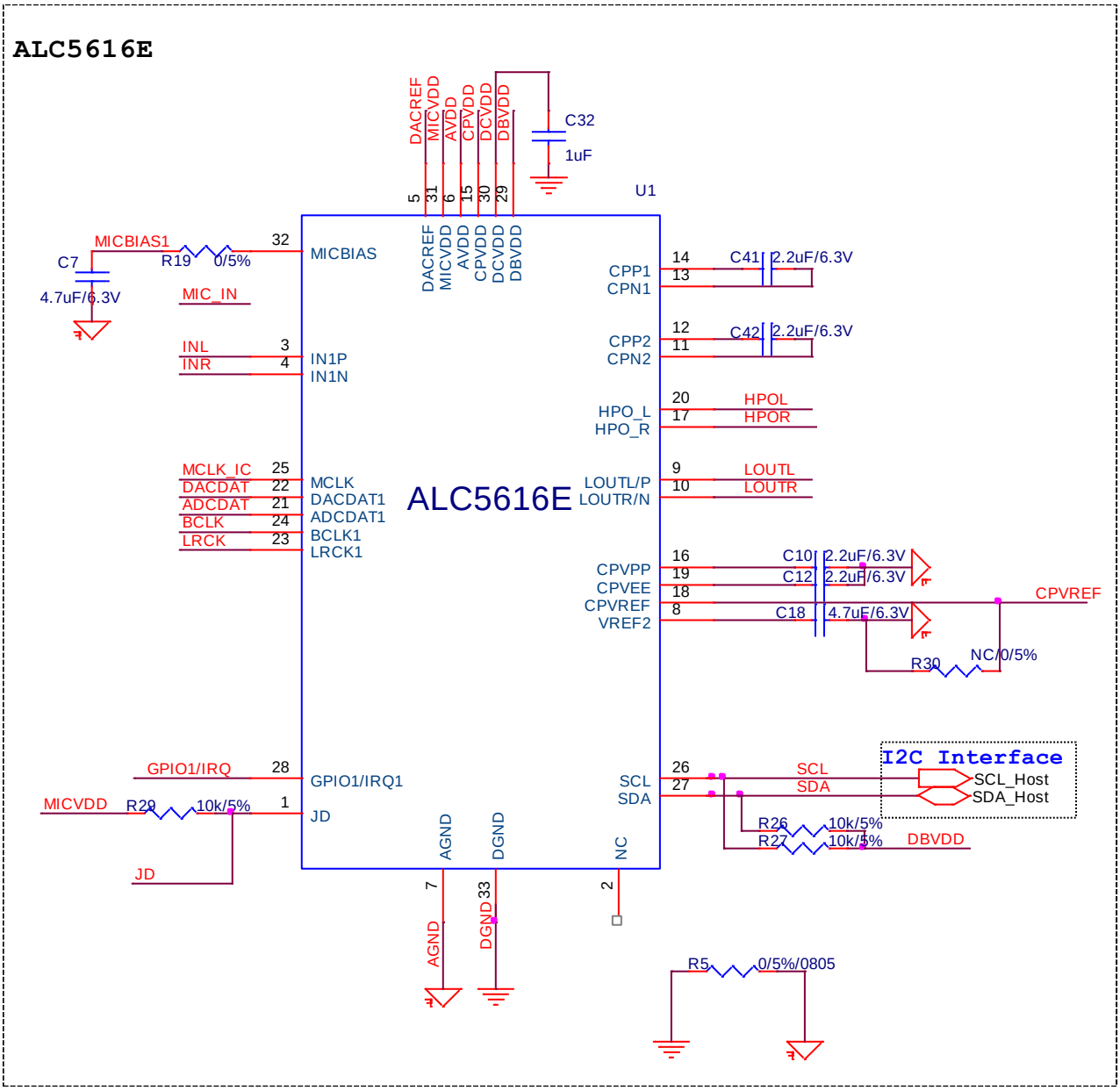


Figure 25. Timing of I²S/PCM Master Mode

Table 72. I2S/PCM Slave Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

10. Application Circuits



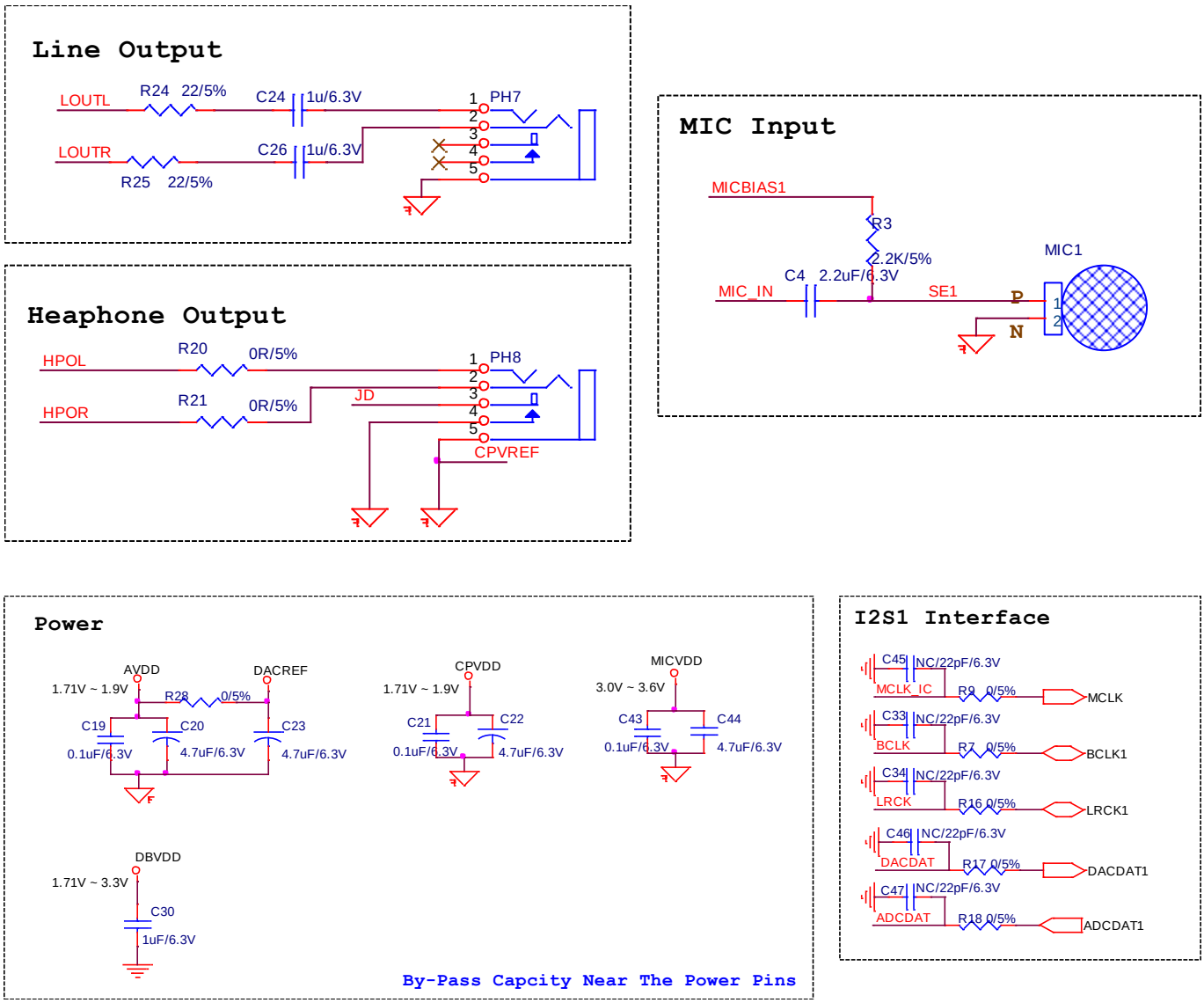
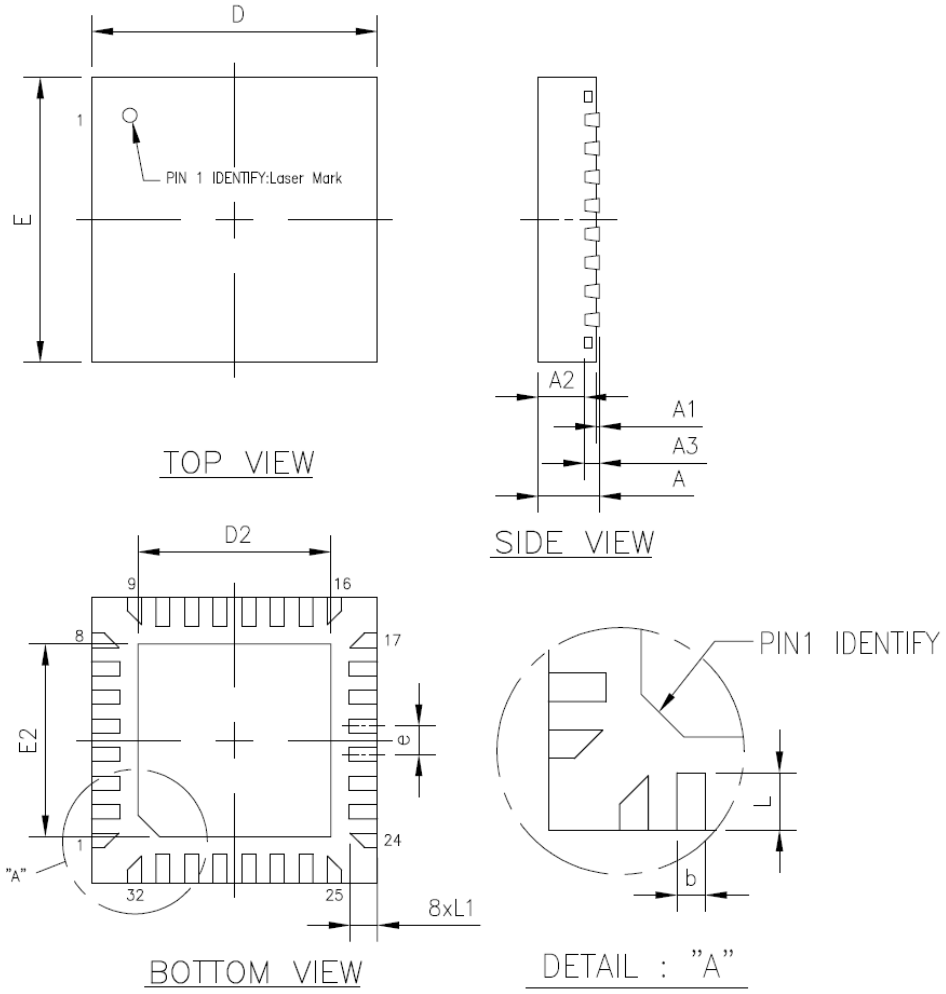


Figure 27. Application Circuit

11. Package Information

Plastic Quad Flat No-Lead Package 32 Leads 4x4mm^2 Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.65	0.70	—	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.080	0.010
D/E	4.00 BSC			0.157 BSC		
D2/E2	2.55	2.70	2.85	0.100	0.106	0.112
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.282	0.382	0.482	0.011	0.015	0.019

Notes··

1. CONTROLLING DIMENSION·· MILLIMETER(mm).
2. REFERENCE DOCUMENTL·· JEDEC MO-220.

Figure 28. Package Dimension

12. Ordering Information

Table 73. Ordering Information

Part Number	Package	Status
ALC5616E-CG	32-Pin QFN (4mm x 4mm) in 'Green' Package (Tray)	N/A
ALC5616E-CGT	32-Pin QFN (4mm x 4mm) in 'Green' Package (Tape & Reel)	N/A

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