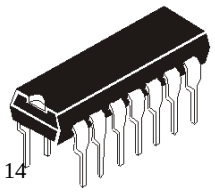
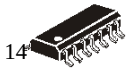
Low Power Quad Operational Amplifier

The HT324A contains four independent high gain operational amplifiers with internal frequency compensation. The op-amps operate over a wide voltage range. The device has low power supply current drain, regardless of the power supply voltage. The low power drain makes the HT324A a good choice for battery operation.

- Internally frequency compensated for unity gain
- Large DC voltage gain
- Single or split supply operation
- Input common-mode voltage range to ground
- Large output voltage swing: 0V DC to V_{CC}-1.5V DC
- Power drain suitable for battery operation
- Low input offset voltage and offset current
- Differential input voltage range equal to the power supply voltage



N SUFFIX
PLASTIC

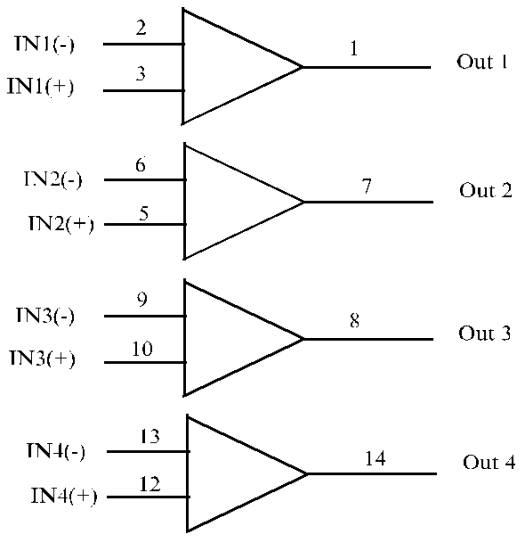


D SUFFIX
SOIC

ORDERING INFORMATION

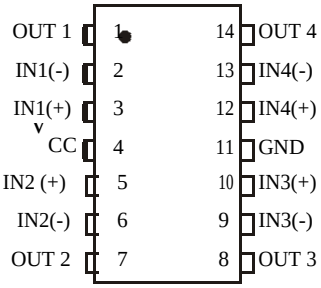
HT324AN	Plastic
HT324AR	SOIC
HT324AG	Chip

BLOCK DIAGRAM



PIN 4 = V_{CC}
PIN 11= GND

PIN ASSIGNMENT



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltages Single Supply Split Supplies	 32 ±16	 V
V_{IDR}	Input Differential Voltage Range (1)	±32	V
V_{ICR}	Input Common Mode Voltage Range	-0.3 to 32	V
t_S	Short-Circuit duration of Output	100	ms
T_J	Junction Temperature Plastic Packages	 150	 °C
Tstg	Storage Temperature Plastic Packages	 -55 to +125	°C
I_{IN}	Input Current, per pin (2)	50	mA
T_L	Lead Temperature, 1mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Notes:

1. Split Power Supplies.
2. V_{IN}<-0.3V.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	±2.5 or 5.0	±15 or 30	V
T_A	Operating Temperature, All Package Types	0	+70	°C

DC ELECTRICAL CHARACTERISTICS (T_A=0 to +70°C)

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V_{IO}	Maximum Input Offset Voltage	V_{CC}=5.0-30V;R_S=0Ω V_O=1.4V V_{ICR}=0V - (V_{CC}-1.5V)* V_{ICR}=0V - (V_{CC}-2.0V)		 7.0* 9.0	mV
I_{IO}	Maximum Input Offset Current	V_{CC}=5.0-30V, V_O =1.4V		±50* ±150	nA
I_{IB}	Maximum Input Bias Current	V_{CC}=5.0-30V, V_O =1.4V		-250* -500	nA
V_{ICR}	Input Common Mode Voltage Range	V_{CC}=30V	0	V_{CC}-1.5V V_{CC}-2.0V	V
I_{CC}	Maximum Power Supply Current	R_L=∞,V_{CC}=5V, V_0=2.5V R_L=∞,V_{CC}=30V, V_0=15V		1.2 3.0	mA
A_{VOL}	Minimum Large Signal Open-Loop Voltage Gain	V_{CC}=15V, R_L≥2KΩ	25* 15		V/mV
V_{OH}	Minimum Output High-Level Voltage Swing	V_{CC}=5V,R_L=2KΩ V_{CC}=30V,R_L=2KΩ V_{CC}=30V,R_L=10KΩ	3.3 26 27		V
V_{OL}	Maximum Output Low-Level Voltage Swing	V_{CC}=5V,R_L=10KΩ		20	mV
CMR	Common Mode Rejection	Ω V_{CC}=5-30V, R_S=10K	65*		dB
PSR	Power Supply Rejection	V_{CC}=5-30V	65*		dB
I_{SC}	Maximum Output Short Circuit to GND	V_{CC}=5.0V, V_O=0V		60*	mA
I_{O+}	Minimum Output Source Current	V_{CC}=15V, V_{ID-}=1.0V,	20*		mA
I_{O--}	Minimum Output Sink Current	V_{ID}=-1.0V, V_{CC}=15V, V_O=15V V_{ID}=-1.0V, V_{CC}=15V, V_O=0.2V	10* 5 12*		mA mA µA
V_{IDR}	Differential Input Voltage Range	All V_{IN}≥GND or V-Supply (if used)		V_{CC}*	V

* T_A = +25°C

NOTE: Guaranteed Limits of DC Electrical Characteristics are given for T_A=0, +70°C as the information for chips.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A= +25°C)

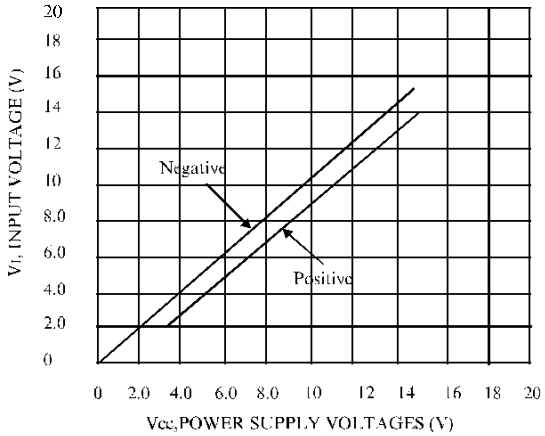


Figure 1.Input Voltage Range

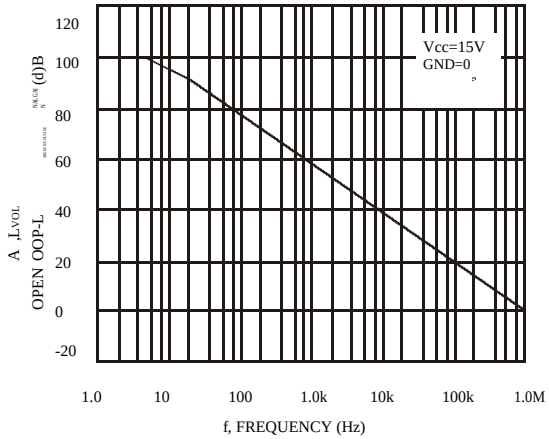


Figure 2. Open-Loop Frequency

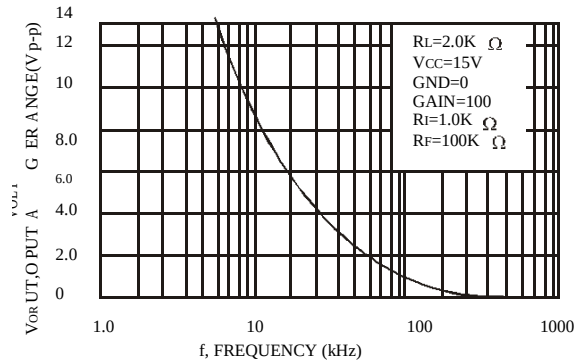


Figure 3. Large-Signal Frequency Response

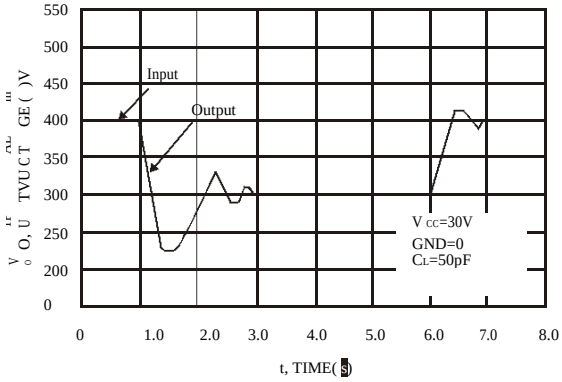


Figure 4. Small-Signal Voltage Follower Pulse Response (Noninverting)

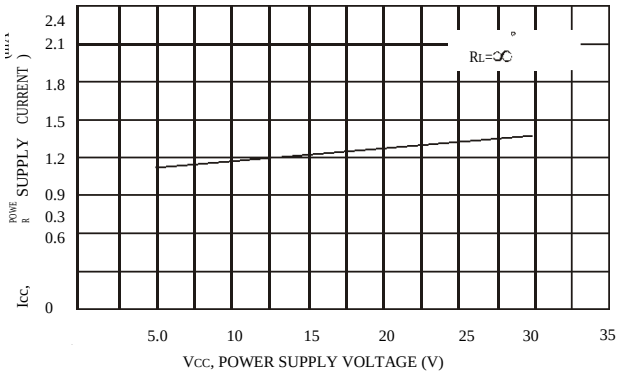


Figure 5. Power Supply Current versus Power Supply Voltage

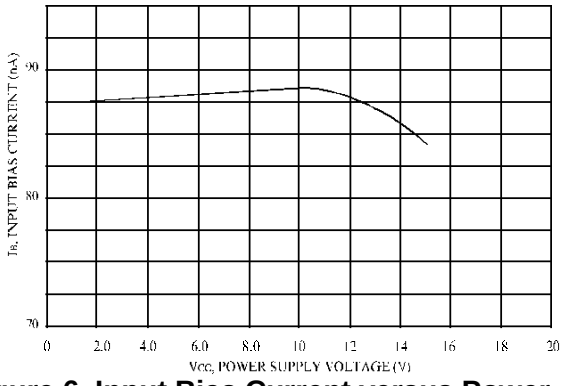


Figure 6. Input Bias Current versus Power Supply Voltage

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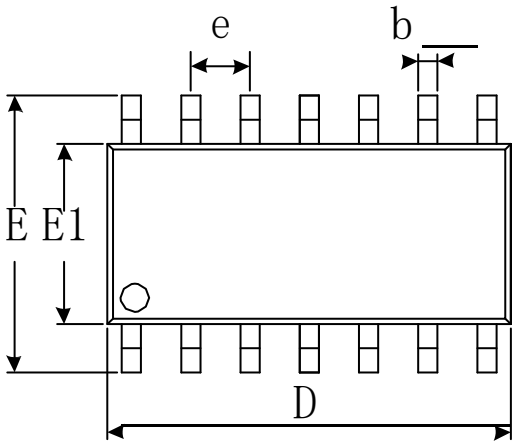
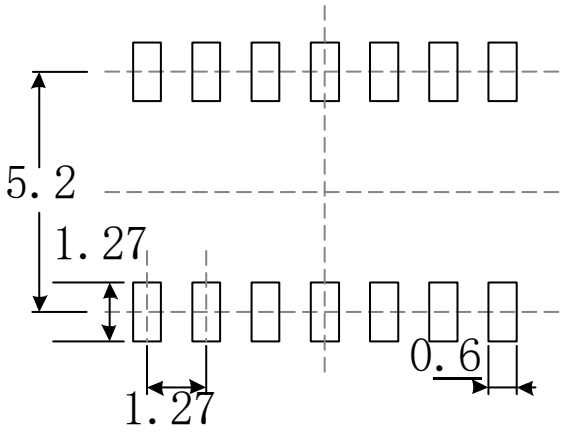
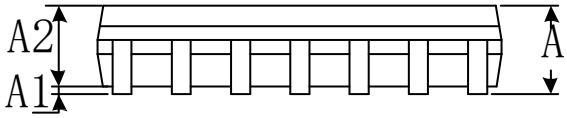
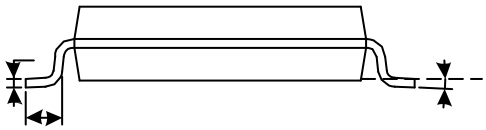




RECOMMENDED LAND PATTERN (Unit: mm)

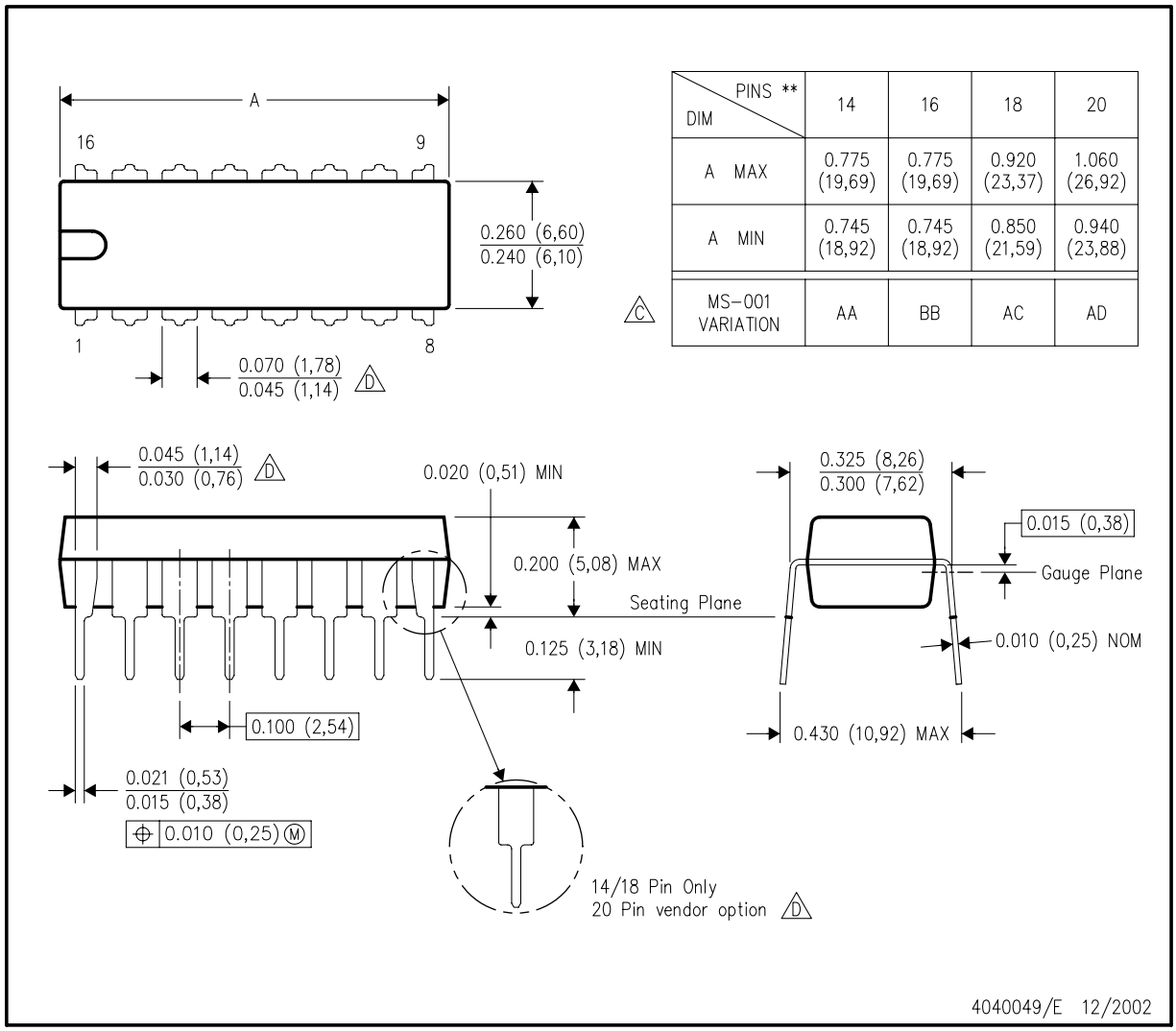




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP-14

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.