DESCRIPTION

The LTP31xx series of low - dropout (LDO), low - power linear regulators offer very high power supply rejection ratio (PSRR) while maintaining very low 14 µA ground current, suitable for RF applications. The family uses an advanced CMOS process and a P - MOSFET pass device to achieve fast start - up, very low noise, excellent transient response, and excellent PSRR performance.

The LTP31xx is stable with a 1.0 µF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from T_J = – 40°C to +125°C, and is available in small UTDFN1.0×1.0 - 4L, DFN1.0×1.0 - 4L and SOT23 - 5L packages, which is ideal for small form factor portable equipments such as wireless handsets and PDAs.

FEATURES

- Wide Input Voltage Range: 1.9V to 5.5V
- Up to 300mA Load Current
- Fixed Output Voltages: 1.2V to 4.5V
- More Output Voltage Options Available on Requested
- Very Low IQ: 14µA
- Low Dropout: 180mV Typically at 3.3V
- Very High PSRR: 90dB at 1kHz
- Ultra Low Noise: 10µV_{RMS} at 3.3V Output and I_{LOAD}=1mA
- Excellent Load and Line Transient Response
- Line Regulation: 0.02%/V Typically
- Short Circuit Protection: 500mA Typically (Current at Short Mode)
- With Auto Discharge

APPLICATIONS

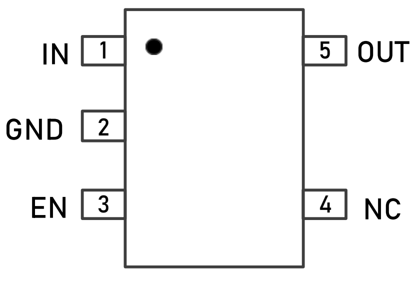
- Smart Phones and Cellular Phones
- Modems
- Security and Surveillance
- Hand-Held Instruments
- Battery-Powered Equipments

ORDER INFORMATION

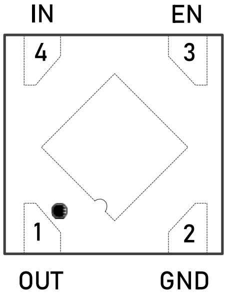
Model Note1	Package	Ordering Number Note1	Packing Option
LTP31xx	SOT23-5L	LTP31xxXT5	Tape and Reel, 3000
	DFN1.0×1.0-4L	LTP31xxXF4	Tape and Reel, 10000
	UTDFN1.0×1.0-4L	LTP31xxXFU4	Tape and Reel, 10000

Note1: xx stands for output voltage, e.g. if xx = 18, the output voltage is 1.8V; if xx = 30, the output voltage is 3.0V.

PIN CONFIGURATION (Top View)



SOT23-5L

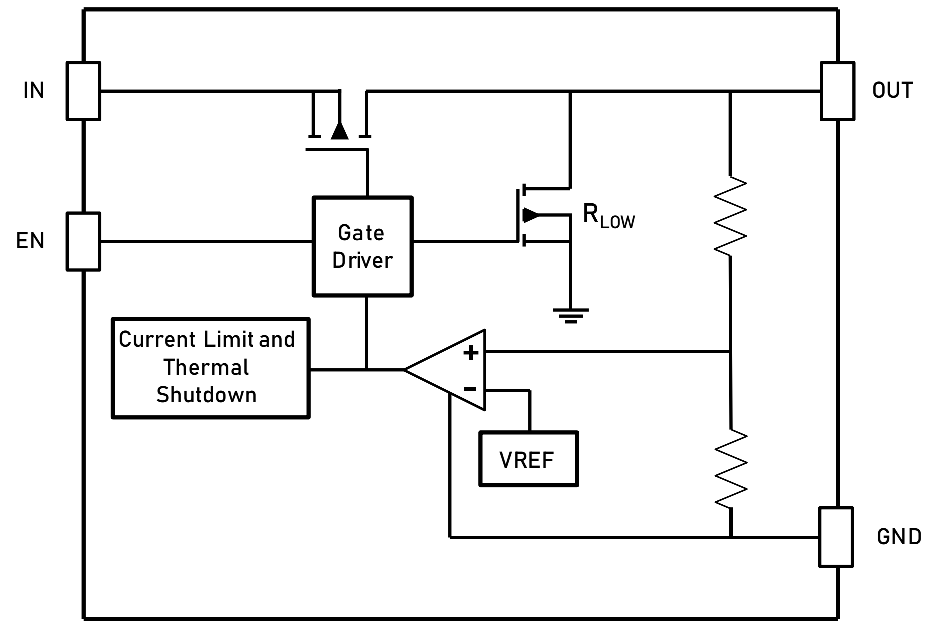


UTDFN1.0×1.0-4L / DFN1.0×1.0-4L

PIN DESCRIPTIONS

Pin		Symbol	Descriptio
SOT23-5L	UTDFN1.0×1.0-4L DFN1.0×1.0-4L		
1	4	IN	Supply input pin. Must be closely decoupled to GND with a 1μFor greater ceramic capacitor.
2	2	GND	Ground.
3	3	EN	Enable control input, active high. Do not leave EN floating.
4		NC	No Connection.
5	1	OUT	Output pin. Bypass a 1μF ceramic capacitor from this pin to ground.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input Capacitor

A 1 µF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 µF to 10 µF, Equivalent Series Resistance (ESR) is from 5 mΩ to 500 mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins. With a reasonable PCB layout, the single 1 µF ceramic output capacitor can be placed up to 10 cm away from the LTP31xx devices.

ON/OFF Input Operation

The LTP31xx EN pin is internally held LOW by a 1 MΩ resistor to ground. The LTP31xx is turned on by setting the EN-pin higher than V_{IH} threshold, and is turned off by pulling it lower than V_{IL} threshold. If this feature is not used, the EN pin should be tied to IN-pin to keep the regulator output on at all time.

High PSRR and Low Noise

RF circuits such as low noise amplifier (LNA), up/down converter, mixer, PLL, VCO, and IF stage, require low noise and high PSRR LDOs. The temperature-compensated crystal oscillator circuit requires very high PSRR at RF power amplifier burst frequency. For instance, minimum 65 dB PSRR at 217 Hz is recommended for the wireless handsets.

In order to provide good audio quality, the audio power supply for hand-free, game, MP3, and multimedia applications in cellular phones, require low-noise and high PSRR at audio frequency range (20 Hz to 20 kHz). The LTP31xx, with PSRR of 90 dB at 1 kHz, is suitable for most of these applications that require high PSRR and low noise.

Output Automatic Discharge

The LTP31xx output employs an internal 230 Ω (typically) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

Remote Output Capacitor Placement

The LTP31xx requires at least a 1 µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

Fast Transient Response

Fast transient response LDOs can also extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100 µA to 100 mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDOs.

The LTP31xx 's fast transient response from 0 to 300 mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Low Quiescent Current

Cellular phone baseband internal digital circuits typically operate all the time. That requires LDO stays on at all times. However, in the standby mode, the microprocessor consumes only around 100~300 µA. Since the phone stays in standby for the longest percentage of time, using a 14µA quiescent current LDO, instead of 100 µA, saves 88 µA and can substantially extends the battery standby time.

The LTP31xx, consuming only 14 µA quiescent current, provides great power saving in portable and low power applications.

Minimum Operating Input Voltage (V_{IN})

The LTP31xx does not include any dedicated UVLO circuitry. The LTP31xx internal circuitry is not fully functional until V_{IN} is at least 1.8V. The output voltage is not regulated until V_{IN} has reached at least the greater of 1.8 V or (V_{OUT} + V_{DO}).

Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the current limit protection will be triggered and clamp the output current to approximately 500 mA to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Overload Protection (TSD)

Thermal shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the LTP31xx has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the LTP31xx device into thermal shutdown may degrade the device reliability.

ABSOLUTE MAXIIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
IN Voltage	V_{IN}	-0.3	6.0	V
Other Pin Voltage		-0.3	V_{IN} + 0.3	V
Maximum Load Current		Internal Limited		mA
Operating Junction Temperature	T_{OP}	-40	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Lead Temperature(Soldering, 10 sec)	T_L		300	°C

NOTE:Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. LINEARIN recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

LINEARIN reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact LINEARIN sales office to get the latest datasheet.

ELECTRICAL CHARACTERISTICS

T_A = +25°C, C_{IN} = 1µF, C_{OUT} = 1µF, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		1.9		5.5	V
ΔV_{OUT}	Output Voltage Tolerance	V_{IN} = 2.8 V to 5.5 V, I_{OUT} = 1 mA to 300mA	–2		2	$\%V_{OUT}$
	Line Regulation	V_{IN} = 2.8 V to 5.5 V, I_{OUT} = 1 mA		0.02		%mA
	Load Regulation	I_{OUT} = 1 mA to 300 mA		0.001		%mA
I_{LOAD}	Load Current		0		300	mA
I_{SHDN}	Input Shutdown Quiescent Current	Disabled, V_{EN} = 0 V		0.2	1	µA
I_Q	Input Quiescent Current	V_{IN} > 1.9 V, V_{EN} > 1.2 V, I_{OUT} = 0 mA		14	25	µA
$I_{standby}$	Standby Current	V_{EN} = 0 V		0.2	1	µA
V_{DROP}	Dropout Voltage (1)	I_{OUT} = 100 mA		50	100	mV
		I_{OUT} = 300 mA		180	300	mV
I_{LMT}	Short Circuit Current Limit	T_A = 25°C	300	500		mA
PSRR	Power Supply Rejection Ratio	f = 100 Hz, I_{OUT} = 1 mA		94		dB
		f = 1 kHz, I_{OUT} = 1 mA		90		dB
		f = 10 kHz, I_{OUT} = 1 mA		84		dB
		f = 100 kHz, I_{OUT} = 1 mA		71		dB
		f = 1 MHz, I_{OUT} = 1 mA		60		dB
		f = 100 Hz, I_{OUT} = 20 mA		84		dB
		f = 1 kHz, I_{OUT} = 20 mA		83		dB
		f = 10 kHz, I_{OUT} = 20 mA		77		dB
		f = 100 kHz, I_{OUT} = 20 mA		60		dB
		f = 1 MHz, I_{OUT} = 20 mA		58		dB
e_N	Output Noise Voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 1 mA		10		μV_{RMS}
		BW = 10 Hz to 100 kHz, I_{OUT} = 300 mA		6.5		μV_{RMS}
$R_{Dischrg}$	Output Discharge FET R_{DSON}	V_{EN} < V_{IL} (output disable)	20	30	40	Ω
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 1.8 V to 5.5 V, V_{EN} falling until the output is disabled			0.4	V
V_{IH}	EN Input Logic High Voltage	VIN = 1.8 V to 5.5 V, VEN risinguntil the output is enabled	1			V
I_{EN}	EN Input leakage current	V_{IN} = 5.5 V ,V_{EN} = 0 V		0.01	1	µA
		V_{IN} = 5.5 V ,V_{EN} = 5.5 V		5.5		µA
T_{SHDN}	Thermal shutdown threshold	V_{IN} = 2.8 V, T_J rising		155		°C
T_{HYS}	Thermal shutdown hysteresis	V_{IN} = 2.8 V, T_J falling from shutdown		15		°C

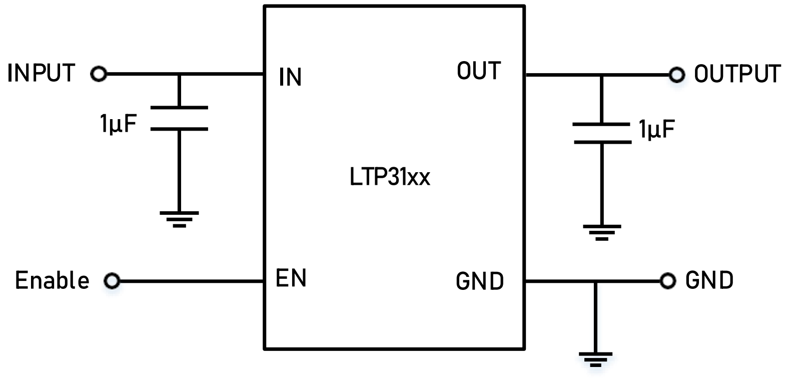
Note: (1) V_{DROP} is measured for devices with $V_{OUT} \geq 1.5V$.

ELECTRICAL CHARACTERISTICS (Continued)

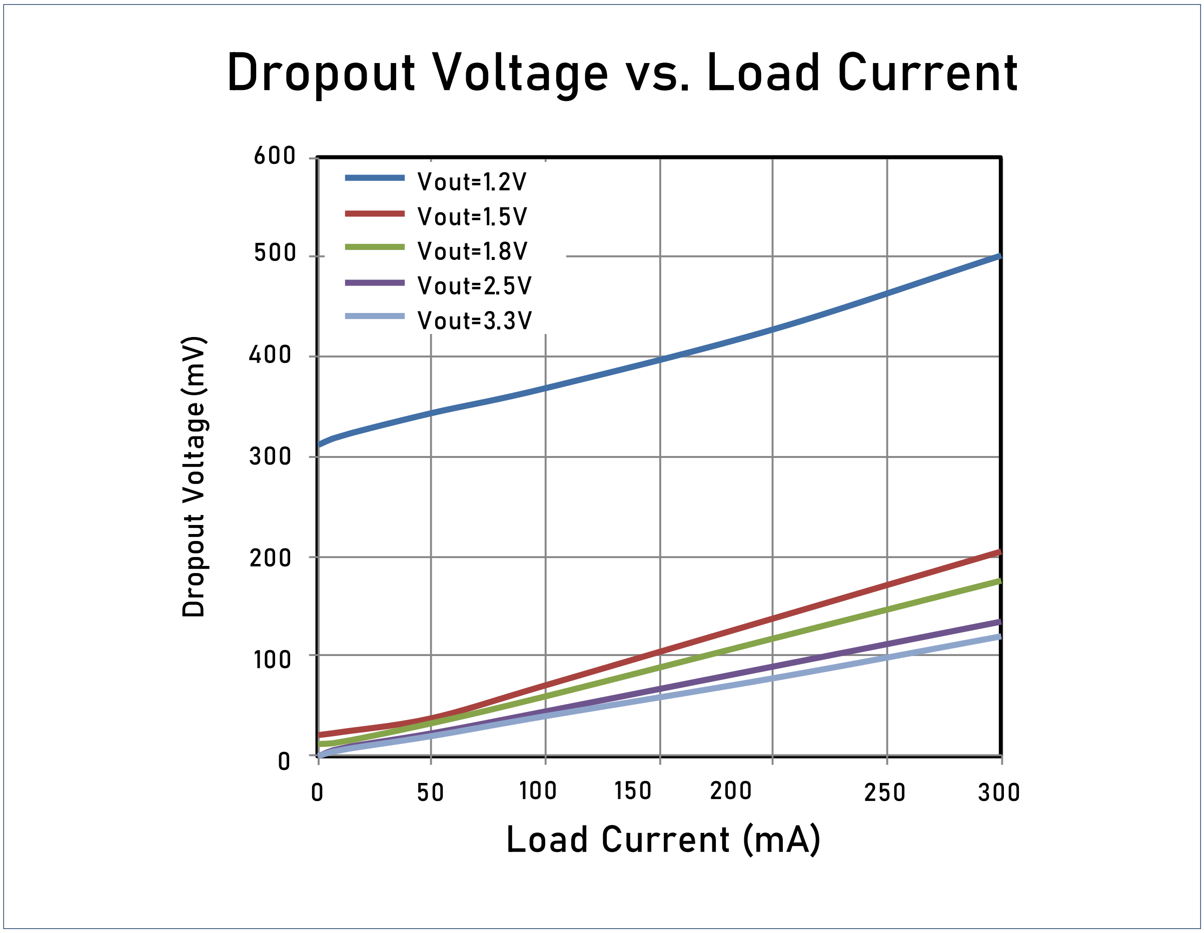
T_A = +25°C, C_{IN} = 1µF, C_{OUT} = 1µF, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔV_{OUT}	Line transient	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 1.6V) in 10 µs		10		mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$ + 1 V) in 10 µs		10		mV
	Load transient	I_{OUT} = 1 mA to 300 mA in 10 µs		20		mV
		I_{OUT} = 300 mA to 1 mA in 10 µs		20		mV
Overshoot	Overshoot on start-up	Stated as percentage of $V_{OUT(NOM)}$			5	%
$T_{D(ON)}$	Output Turn-on Delay Time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$		150	250	µs

APPLICATION CIRCUITS

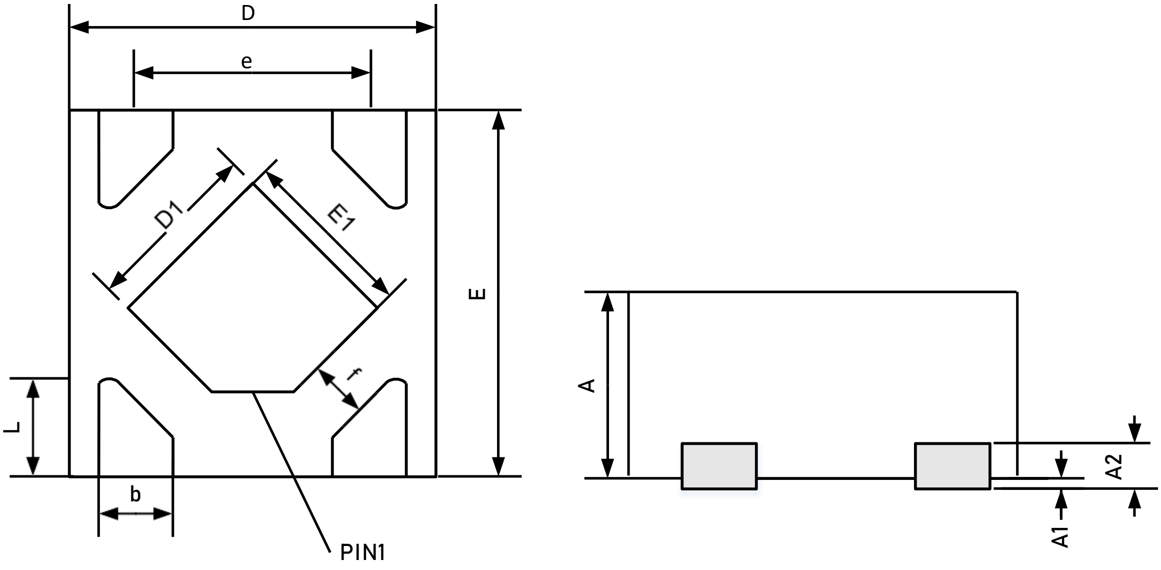


TYPICAL PERFORMANCE CHARACTERISTICS



PACKAGE OUTLINE

UTDFN1.0×1.0-4L

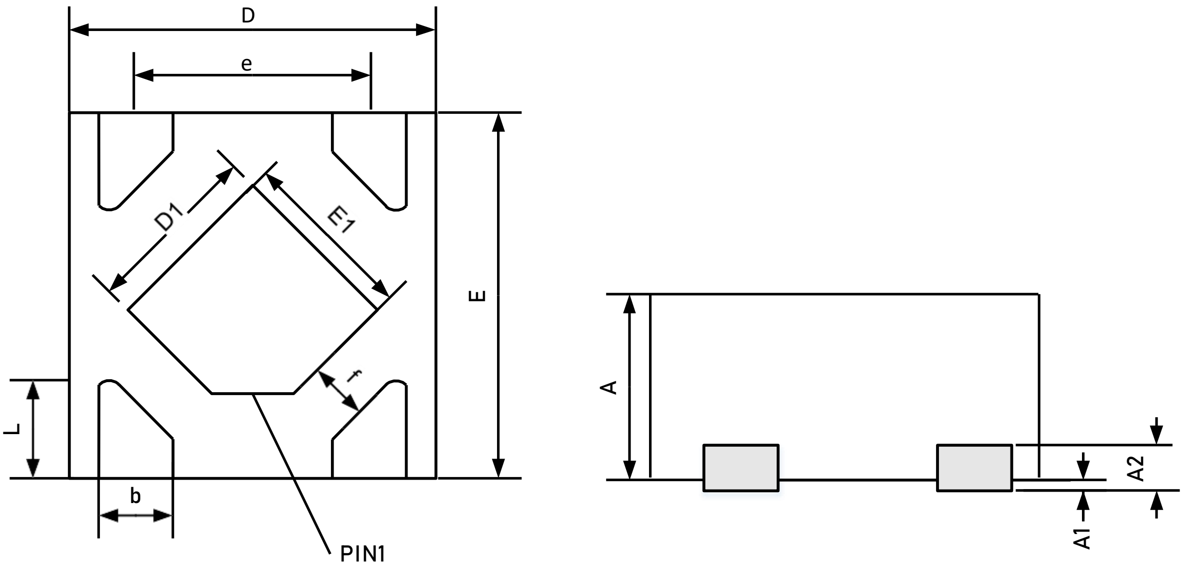


Unit: mm

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.340	0.370	0.400
A1	0.000	0.020	0.050
A2	0.100REF		
D	0.950	1.000	1.050
D1	0.430	0.480	0.530
E	0.950	1.000	1.050
E1	0.430	0.480	0.530
b	0.170	0.220	0.270
e	0.650BSC		
f	0.190	0.195	0.200
L	0.200	0.250	0.300

PACKAGE OUTLINE

DFN1.0×1.0-4L

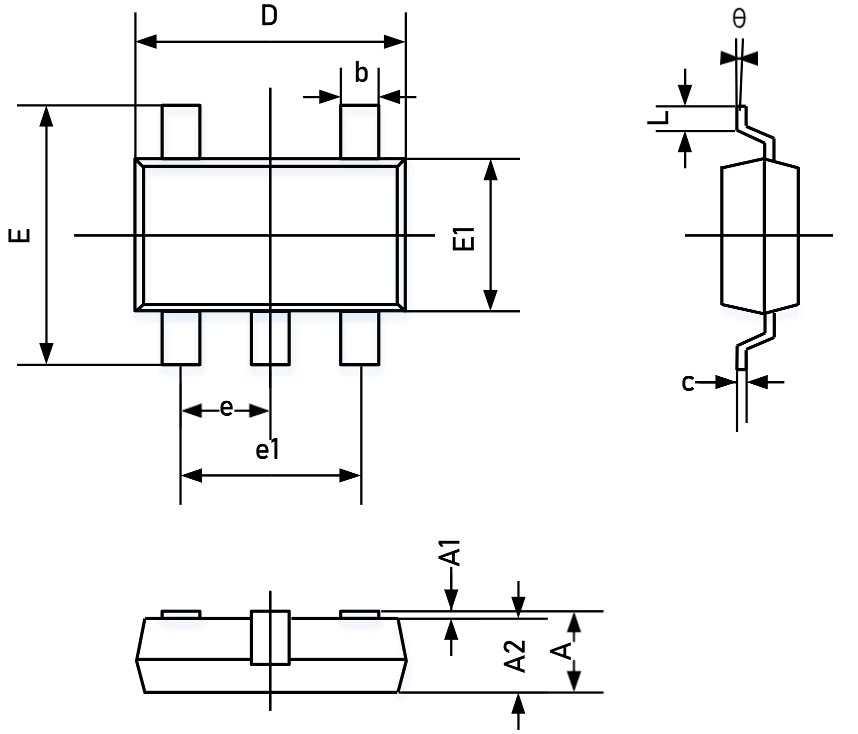


Unit: mm

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.450	0.500	0.550
A1	0.000	0.025	0.050
A2	0.125REF		
D	0.950	1.000	1.050
D1	0.380	0.480	0.580
E	0.950	1.000	1.050
E1	0.380	0.480	0.580
b	0.150	0.200	0.250
e	0.650BSC		
f	0.190	0.195	0.200
L	0.150	0.250	0.350

PACKAGE OUTLINE

SOT23-5L



Unit: mm

Symbol	Dimensions In Millimeters	
	MIN	MAX
A	0.700	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.350	0.500
c	0.080	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.600	1.700
e	0.950BSC	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°