SYT16A03DVC

Ultra-Low Capacitance TVS Protection

Features

- Transient protection for high-speed data lines
  IEC 61000-4-2 (ESD) ±15kV (Air)
  ±15kV (Contact)
  IEC 61000-4-5 (Surge) 6A (8/20μs)
- For 3.3V and below operating voltage
- Ultra-small package (2.5mm*1.0mm*0.55mm)
- Protects four data lines
- Ultra Low capacitance: 0.3pF for each channel
- Low leakage current: 0.01μA @ V_{RWM} (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

Description

SYT16A03DVC is an ultra-low capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.3pF only, SYT16A03DVC is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), (±15kV air, ±15kV contact discharge), IEC 61000-4-5 (Surge) (6A, 8/20μs), etc.

SYT16A03DVC uses ultra-small DFN2.5*1.0-10L package. Each SYT16A03DVC device can protect four high-speed data lines. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make SYT16A03DVC ideal for high-speed data ports and high-frequency lines (e.g., USB3.0 & DVI) applications. The low clamping voltage of the SYT16A03DVC guarantees a minimum stress on the protected IC.

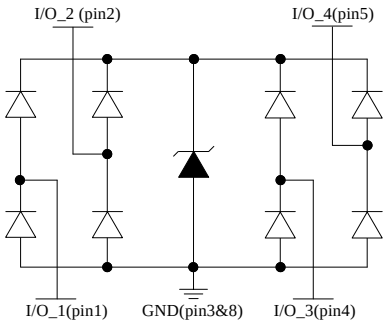
Applications

- USB2.0&3.x
- V-By-One
- SATA and eSATA interface
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- Display Ports
- Digital Visual Interfaces (DVI)

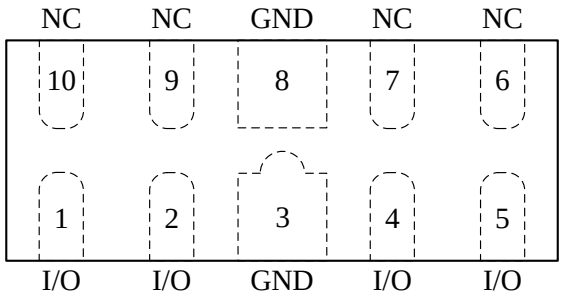
Mechanical Characteristics

- DFN2.5*1.0-10 package
- Marking: Device code, Date code
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



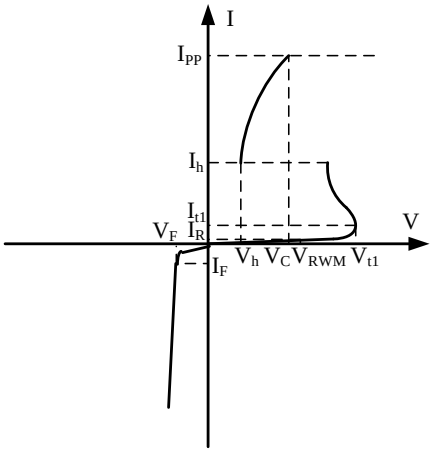
DFN2.5*1.0-10
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
I_{PP}	Maximum Peak Pulse Current (8/20μs)	6	A
P_{PK}	Maximum Peak Pulse Power (8/20μs)	40	Watts
V_{ESD}	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	±15 ±15	kV
T_{OPT}	Operating Temperature	-40/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C

Electrical Characteristics (T_A = 25°C)

Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{t1}	Reverse Triggering Voltage @ I_{t1}
I_{t1}	Test Current for Reverse Triggering
V_h	Holding Voltage
I_h	Holding Current
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Peak Pulse Current
C_{ESD}	Parasitic Capacitance
f	Small Signal Frequency
V_F	Forward Voltage
I_F	Forward Current



Uni-Directional TVS

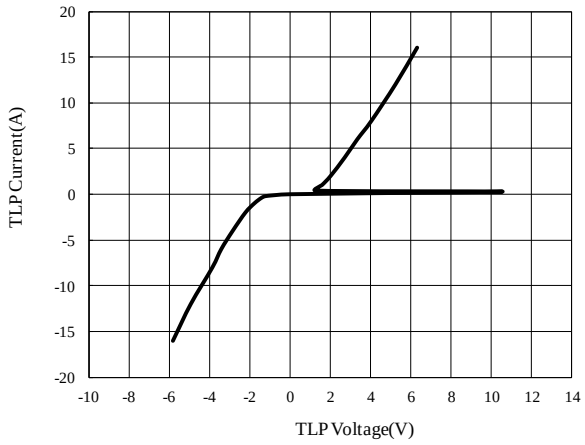
Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				3.3	V
I_R	V_{RWM} = 3.3V, T_A = 25°C		0.01	0.1	μA
V_{t1}	I_{t1} = 1mA	3.6			V
V_h[1]	I_h=100mA	0.8			V
V_C[1]	I_{PP} = 6A, t_p = 8/20μs		4.5	6.0	V
V_C[1]	I_{PP} = 16A, t_p = 10/100ns		6.5		V
R_{DYN}[1,2]	t_p = 10/100ns		0.35		Ω
C_{ESD}[1]	V_R = 3.3V, f = 1MHz		0.30	0.45	pF

NOTES

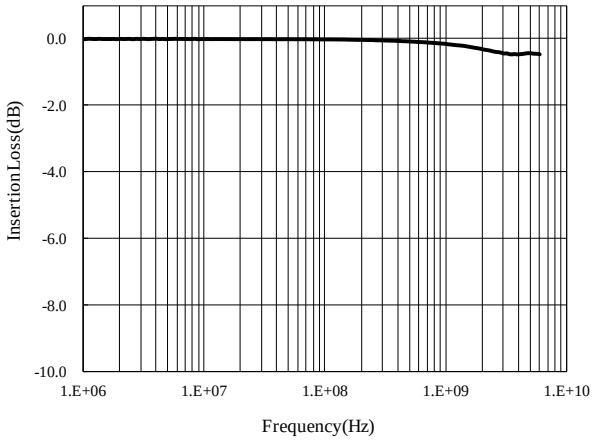
[1] Guaranteed by design and not subject to production test.

[2] R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

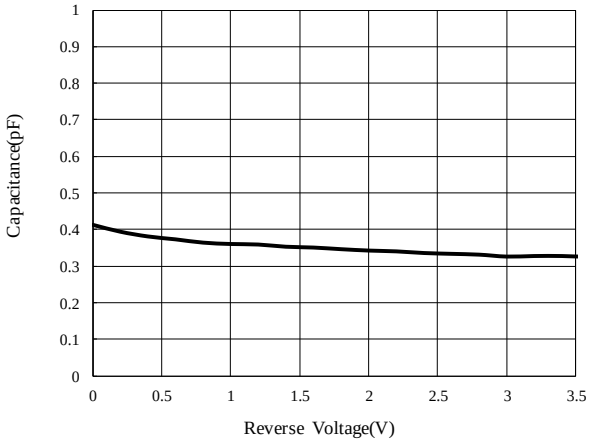
TLP Testing of I/O to GND



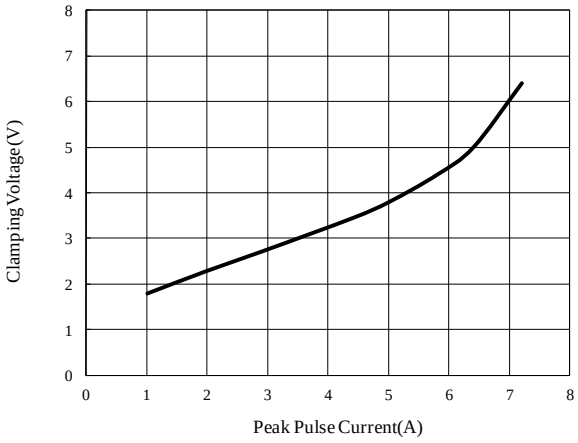
Insertion Loss S21 of I/O to GND



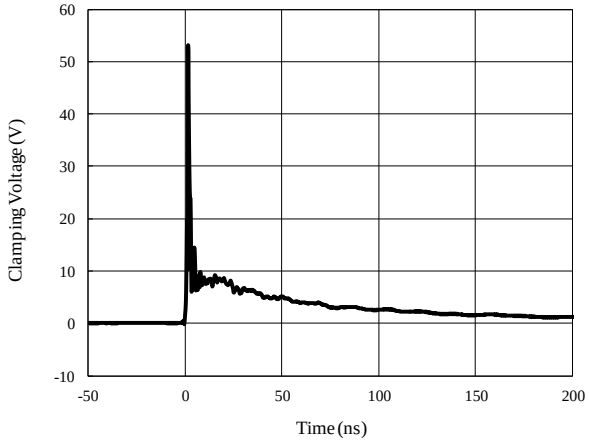
Capacitance vs. Voltage of I/O to GND



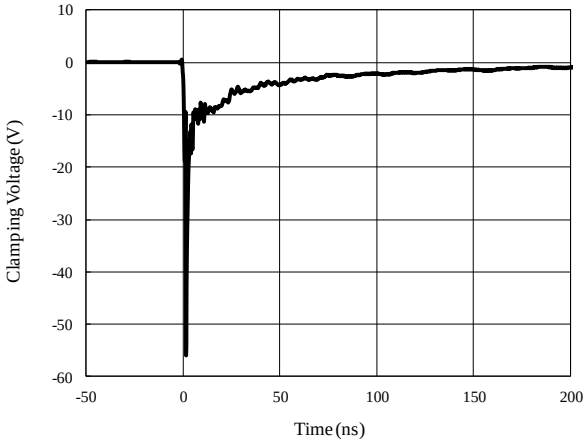
Clamping Voltage vs. Peak Pulse Current (8/20μs)



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

SYT16A03DVC provides ESD protection for four data lines simultaneously. The pin connection is shown in the figure below.

Four parallel data lines, from inner IC to I/O port connector, could connect to SYT16A03DVC four I/O pins directly. Pin 3&8 of SYT16A03DVC is the GND pin, which should connect to the GND of PCB. The wire should be as short as possible in order to minimize the parasitic inductance.

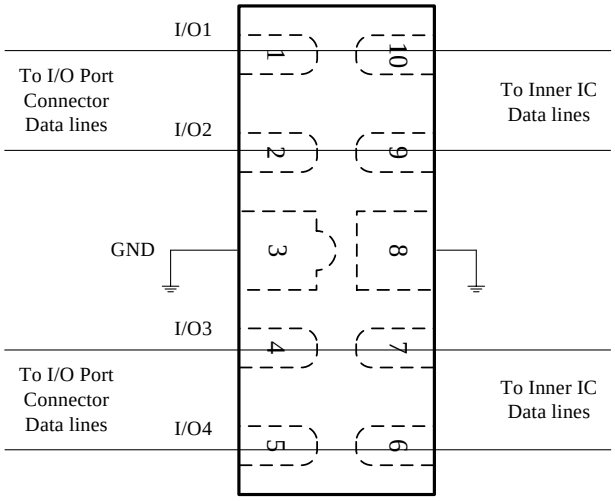


Figure 1 SYT16A03DVC pin connection in PCB

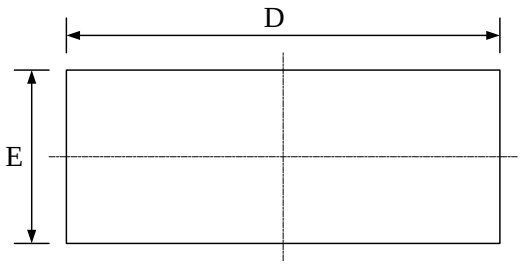
PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

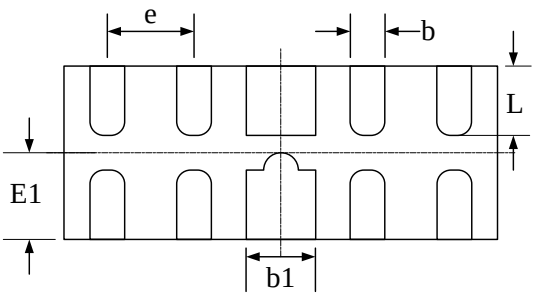
- SYT16A03DVC GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting SYT16A03DVC GND pins to the PCB GND should be wide.
- Place SYT16A03DVC as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

Package Outline

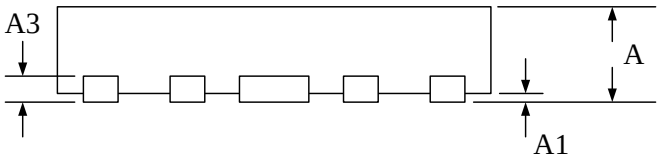
- DFN2.5*1.0-10



TOP VIEW



BOTTOM VIEW



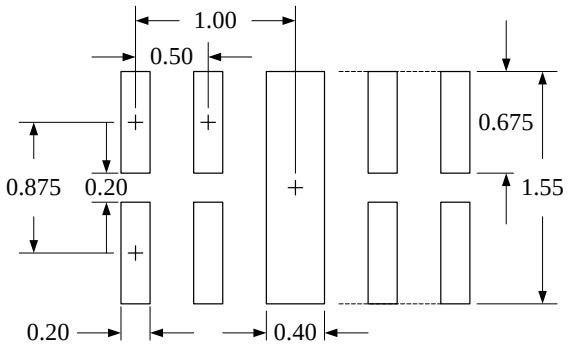
Side VIEW

Package Dimensions (Controlling dimensions are in millimeters)

Symbol	Dimensions (mm)	
	Minimum	Maximum
A	0.500	0.600
A1	0.000	0.050
A3	0.150REF.	
b	0.150	0.250
D1	0.350	0.450
E1	0.460	0.560
D	2.450	2.550
E	0.950	1.050
e	0.500 BSC	
L	0.330	0.430

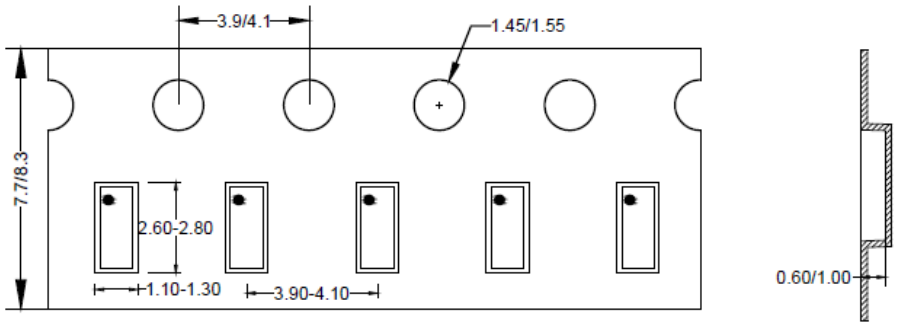
Notes: All dimension in millimeter and exclude mold flash & metal burr.

PCB Layout Pattern



Notes: All dimension in millimeter

Tape and Reel Specification



Feeding direction →

Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
DFN2.5*1.0-10	8	4	7"	400	400	3000

Marking Codes

Note:

(1) "Xa" is device code, fixed.

(2) "YWA" is date code.

Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
SYT16A03DVC	3.3V	3,000	7 Inch

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