

# TC7USB3212WBG

## 1. Functional Description

- Quad SPDT USB Switch

## 2. General

The TC7USB3212WBG is a 2 differential channel, 1-2 multiplexer/demultiplexer for USB3.0 (5Gbps), or other high-speed interface applications.

This device consists of four individual multiplexer/demultiplexer with common select input (SEL) and output enable ( $\overline{OE}$ ). The An+/An- inputs is connected to the Bn+/Bn- or Cn+/Cn- outputs determined by the combination both the select input (SEL) and output enable ( $\overline{OE}$ ). When the output enable ( $\overline{OE}$ ) input is held high level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

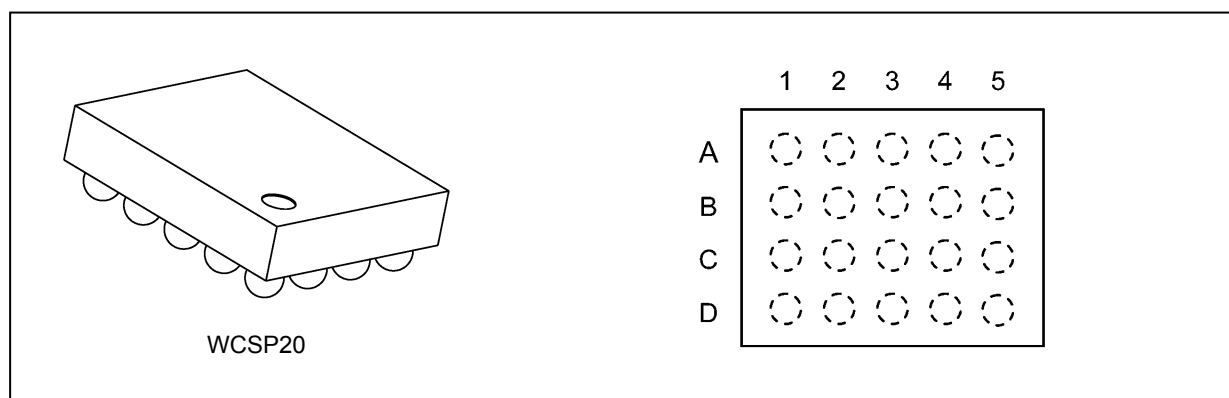
## 3. Features

- (1) Supply voltage:  $V_{CC} = 1.65$  to  $1.95$  V
- (2) ON-resistance:  $R_{ON} = 4.5 \Omega$  (typ.) @  $V_{CC} = 1.65$  V,  $V_{IS} = 0$  V
- (3) -3dB Bandwidth:  $BW = 8$  GHz (typ.) @  $V_{CC} = 1.8$  V
- (4) Insertion Loss:  $IL = -1$  dB (typ.) @  $V_{CC} = 1.8$  V,  $f = 2.5$  GHz,
- (5) Power-down protection provided on all inputs and outputs.
- (6) Package: WCSP20

Note: Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

## 4. Packaging and Pin Assignment (Top View)



### 4.1. Pin Assignment

|   | 1   | 2   | 3   | 4               | 5        |
|---|-----|-----|-----|-----------------|----------|
| A | A0+ | B0+ | B0- | B1+             | B1-      |
| B | A0- | GND | GND | GND             | $V_{CC}$ |
| C | A1+ | GND | GND | $\overline{OE}$ | SEL      |
| D | A1- | C0+ | C0- | C1+             | C1-      |

Start of commercial production

2014-07

## 5. Marking

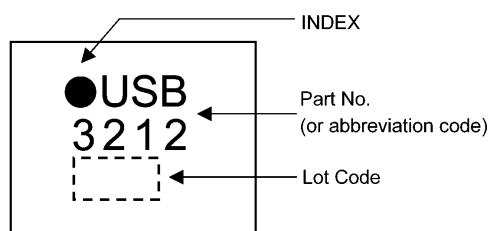


Fig. 5.1 Marking

## 6. System Diagram

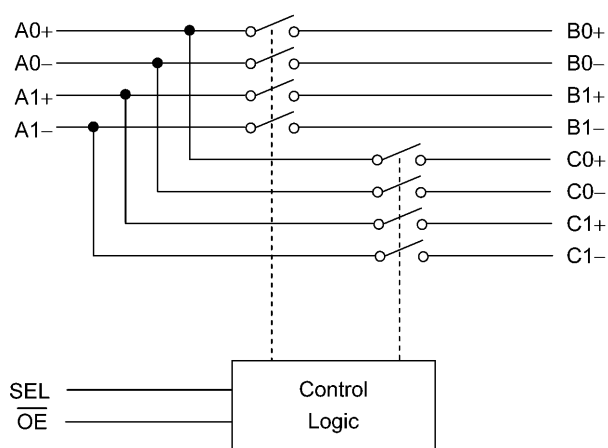


Fig. 6.1 Block Diagram

## 7. Principle of Operation

### 7.1. Truth Table

| Input<br>OE | Input<br>SEL | Function                                 |
|-------------|--------------|------------------------------------------|
| L           | L            | An+ port = Bn+ port, An- Port = Bn- Port |
| L           | H            | An+ port = Cn+ port, An- Port = Cn- Port |
| H           | X            | Disconnect                               |

X: Don't Care

## 8. Absolute Maximum Ratings (Note)

| Characteristics                        | Symbol           | Note | Test Condition               | Rating                 | Unit |
|----------------------------------------|------------------|------|------------------------------|------------------------|------|
| Supply voltage                         | $V_{CC}$         |      | —                            | -0.5 to 2.5            | V    |
| Input voltage ( $\overline{OE}$ , SEL) | $V_{IN}$         |      |                              | -0.5 to 2.5            |      |
| Switch I/O voltage                     | $V_S$            |      | $V_{CC} = 0$ V or Switch OFF | -0.5 to 2.5            |      |
|                                        |                  |      | Switch ON                    | -0.5 to $V_{CC} + 0.5$ |      |
| Switch I/O current                     | $I_S$            |      | —                            | 45                     | mA   |
| Power dissipation                      | $P_D$            |      |                              | 210                    | mW   |
| $V_{CC}$ /ground current               | $I_{CC}/I_{GND}$ |      |                              | $\pm 50$               | mA   |
| Storage temperature                    | $T_{stg}$        |      |                              | -55 to 125             | °C   |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 9. Operating Ranges (Note)

| Characteristics                        | Symbol    | Note | Test Condition               | Rating            | Unit |
|----------------------------------------|-----------|------|------------------------------|-------------------|------|
| Supply voltage                         | $V_{CC}$  |      | —                            | 1.65 to 1.95      | V    |
| Input voltage ( $\overline{OE}$ , SEL) | $V_{IN}$  |      |                              | 0 to 1.95         |      |
| Switch I/O voltage                     | $V_S$     |      | $V_{CC} = 0$ V or Switch OFF | -0.35 to 1.95     |      |
|                                        |           |      | Switch ON                    | -0.35 to $V_{CC}$ |      |
| Operating temperature                  | $T_{opr}$ |      | —                            | -40 to 85         | °C   |
| Input rise time                        | $dt/dv$   |      |                              | 0 to 10           | ns/V |
| Input fall time                        |           |      |                              | 0 to 10           |      |

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs and bus inputs must be tied to either  $V_{CC}$  or GND.

## 10. Electrical Characteristics

### 10.1. DC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to $85^\circ\text{C}$ )

| Characteristics                                   | Symbol                | Note     | Test Condition                                           | $V_{CC}$ (V) | Min                  | Typ. | Max                  | Unit          |
|---------------------------------------------------|-----------------------|----------|----------------------------------------------------------|--------------|----------------------|------|----------------------|---------------|
| High-level input voltage ( $\overline{OE}$ , SEL) | $V_{IH}$              |          | —                                                        | 1.65 to 1.95 | $0.75 \times V_{CC}$ | —    | —                    | V             |
| Low-level input voltage ( $\overline{OE}$ , SEL)  | $V_{IL}$              |          | —                                                        | 1.65 to 1.95 | —                    | —    | $0.35 \times V_{CC}$ | V             |
| Input leakage current ( $\overline{OE}$ , SEL)    | $I_{IN}$              |          | $V_{IN} = 0$ to 1.95 V                                   | 1.65 to 1.95 | —                    | —    | $\pm 5$              | $\mu\text{A}$ |
| Power-OFF leakage current                         | $I_{OFF}$             |          | $V_{IN} = V_{IS} = 0$ to 1.95 V                          | 0            | —                    | —    | $\pm 20$             | $\mu\text{A}$ |
| Switch OFF-state leakage current                  | $I_{SZ}$              |          | $V_{IS} = 0$ to $V_{CC}$ , $\overline{OE} = \text{GND}$  | 1.65 to 1.95 | —                    | —    | $\pm 5$              | $\mu\text{A}$ |
| ON-resistance                                     | $R_{ON}$              | (Note 1) | $V_{IS} = 0$ V, $I_{IS} = 30$ mA                         | 1.65         | —                    | 4.5  | 6                    | $\Omega$      |
|                                                   |                       |          | $V_{IS} = 0.5$ V, $I_{IS} = 30$ mA                       | 1.65         | —                    | 4.7  | 6.4                  |               |
|                                                   |                       |          | $V_{IS} = 1.65$ V, $I_{IS} = 30$ mA                      | 1.65         | —                    | 7.5  | 13                   |               |
| Difference of ON-resistance between switches      | $\Delta R_{ON}$       | (Note 1) | $V_{IS} = 0.5$ V, $I_{IS} = 30$ mA (bit to bit)          | 1.65         | —                    | 0.1  | —                    | $\Omega$      |
| ON-resistance flatness                            | $R_{ON(\text{flat})}$ | (Note 1) | $V_{IS} = 0$ V to 1.0 V, $I_{IS} = 30$ mA                | 1.65         | —                    | 1.0  | —                    | $\Omega$      |
| Quiescent supply current                          | $I_{CC}$              |          | $V_{IN} = V_{CC}$ or GND<br>$\overline{OE} = V_{CC}$     | 1.95         | —                    | —    | 25                   | $\mu\text{A}$ |
|                                                   |                       |          | $V_{IN} = V_{CC}$ or GND<br>$\overline{OE} = \text{GND}$ | —            | —                    | —    | 200                  |               |

Note: All typical values are at  $T_a = 25^\circ\text{C}$ .

Note 1: Measured by the voltage drop between An+/An- and Bn+/Bn-, Cn+/Cn- pins at the indicated current through the switch. On-resistance is determined by the lower of the voltages on the two pins.

### 10.2. AC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to $85^\circ\text{C}$ )

| Characteristics                                | Symbol            | Note     | Test Condition                                    | $V_{CC}$ (V)   | Min | Typ. | Max | Unit          |
|------------------------------------------------|-------------------|----------|---------------------------------------------------|----------------|-----|------|-----|---------------|
| Propagation delay time                         | $t_{PLH}/t_{PHL}$ | (Note 1) | $C_L = 5$ pF, See Fig. 11.1                       | $1.8 \pm 0.15$ | —   | 0.1  | —   | ns            |
| Turn-ON time (SEL, $\overline{OE}$ to output)  | $t_{on}$          |          | $R_L = 50$ $\Omega$ , $C_L = 5$ pF, See Fig. 11.2 |                | —   | 0.5  | 1   | $\mu\text{s}$ |
| Turn-OFF time (SEL, $\overline{OE}$ to output) | $t_{off}$         |          |                                                   |                | —   | 0.1  | 0.5 | $\mu\text{s}$ |
| Break before make                              | TBBM              |          | $R_L = 50$ $\Omega$ , $C_L = 5$ pF, See Fig. 11.3 |                | 200 | —    | 700 | ns            |
| Output skew (bit to bit)                       | $t_{SK(b)}$       | (Note 1) | $C_L = 5$ pF, See Fig. 11.4                       |                | —   | 1.5  | —   | ps            |
| Output skew (channel to channel)               | $t_{SK(CH)}$      | (Note 1) | $C_L = 5$ pF, See Fig. 11.5                       |                | —   | 9.5  | —   | ps            |

Note: All typical values are at  $T_a = 25^\circ\text{C}$ .

Note 1: Parameter guaranteed by design.

### 10.3. Analog Switch (Note) (Unless otherwise specified, $T_a = -40$ to $85^\circ\text{C}$ )

| Characteristics              | Symbol | Note | Test Condition                                     | $V_{CC}$ (V)   | Min | Typ. | Max | Unit |
|------------------------------|--------|------|----------------------------------------------------|----------------|-----|------|-----|------|
| OFF isolation (non-adjacent) | OIRR   |      | $R_T = 50$ $\Omega$ , $f = 2.5$ GHz, See Fig. 11.6 | $1.8 \pm 0.15$ | —   | -30  | —   | dB   |
| Crosstalk (non-adjacent)     | Xtalk  |      | $R_T = 50$ $\Omega$ , $f = 2.5$ GHz, See Fig. 11.7 |                | —   | -25  | —   |      |
| Insertion loss               | IL     |      | $R_T = 50$ $\Omega$ , $f = 2.5$ GHz, See Fig. 11.8 |                | —   | -1   | —   |      |
| -3dB Bandwidth               | BW     |      | $R_T = 50$ $\Omega$ , $C_L = 0$ pF, See Fig. 11.8  |                | —   | 8    | —   | GHz  |

Note: All typical values are at  $T_a = 25^\circ\text{C}$ . Parameter guaranteed by design.

# 11. AC Test Circuits and Waveforms

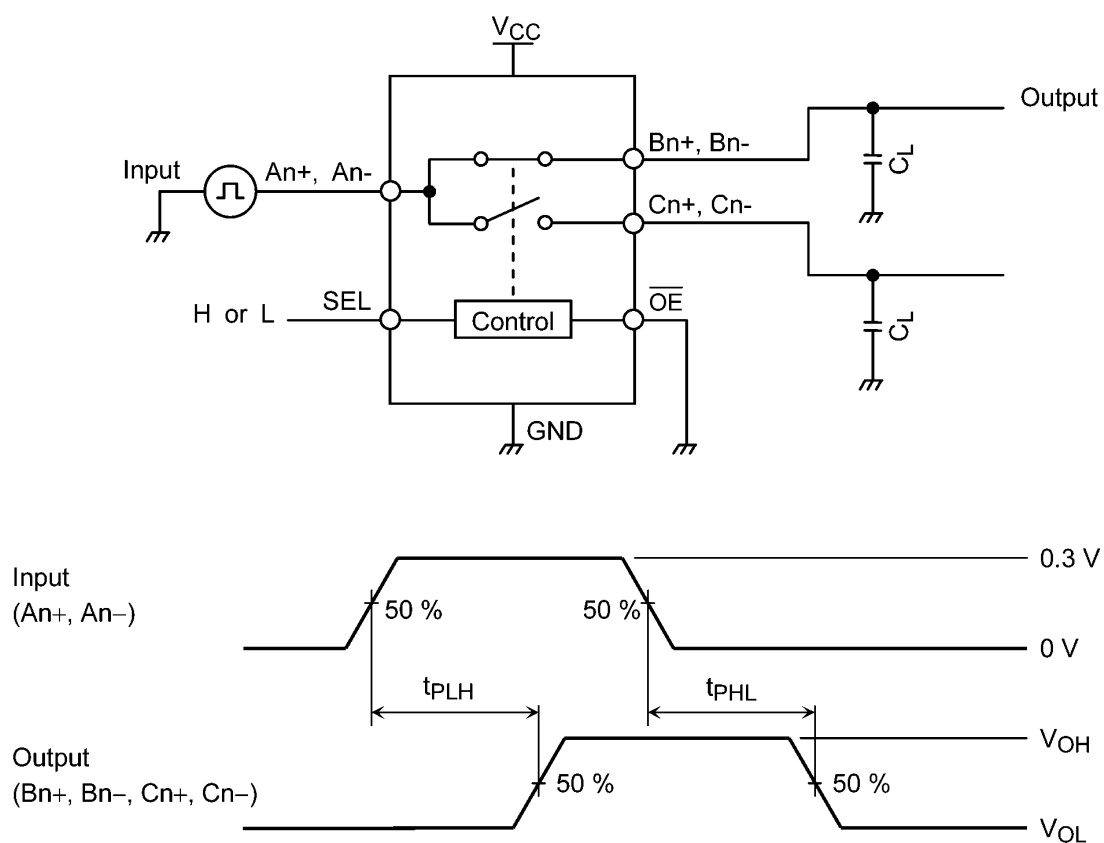
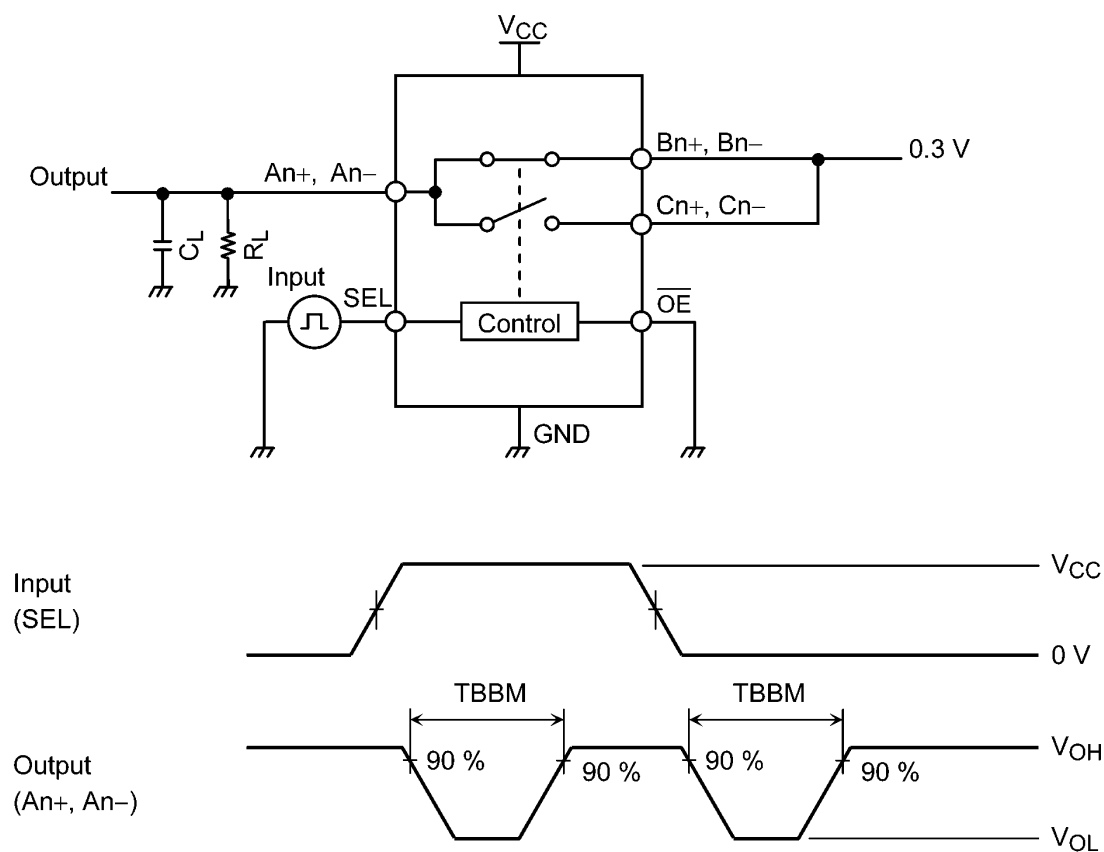
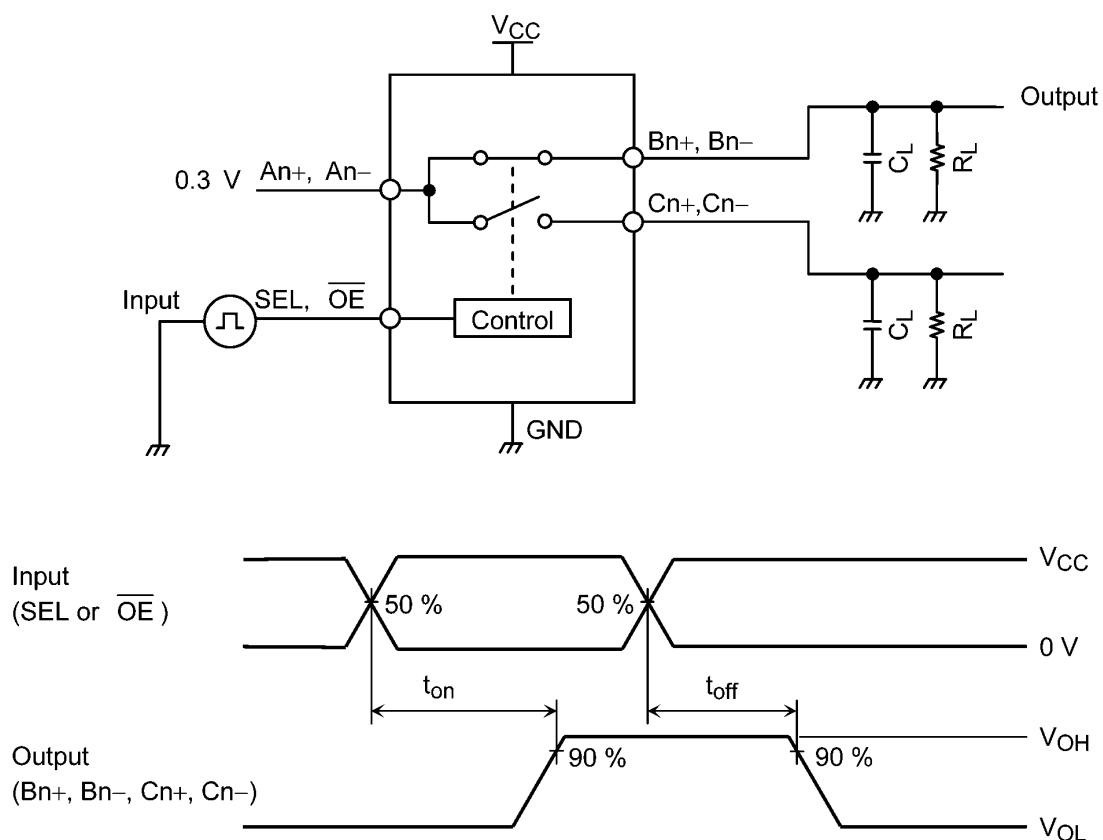


Fig. 11.1 Propagation Delay Time ( $t_{PLH}$ ,  $t_{PHL}$ )



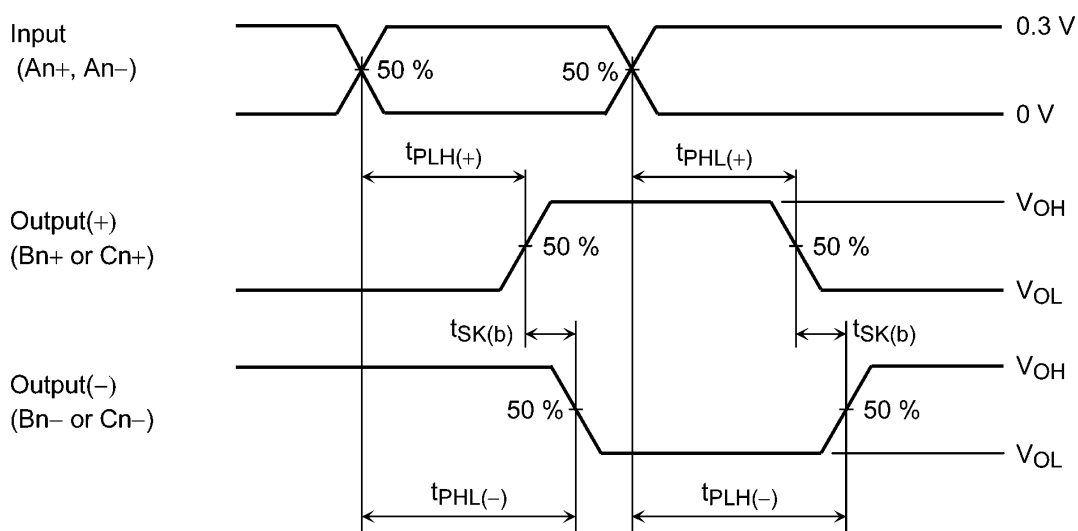
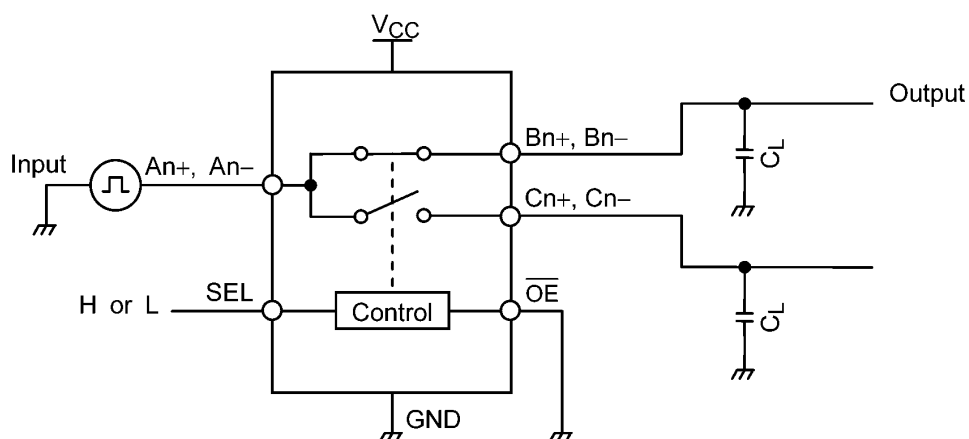


Fig. 11.4 Output Skew (bit to bit)

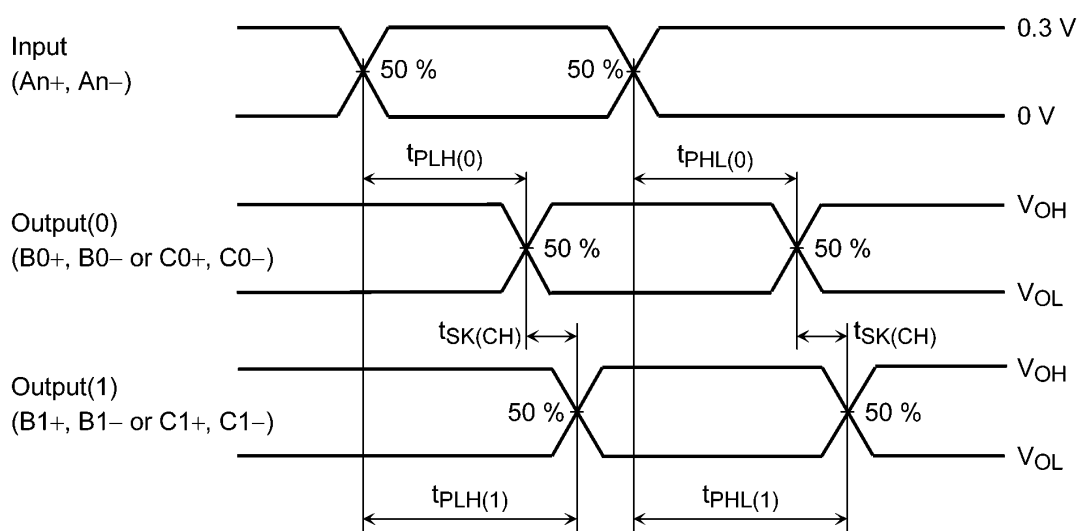
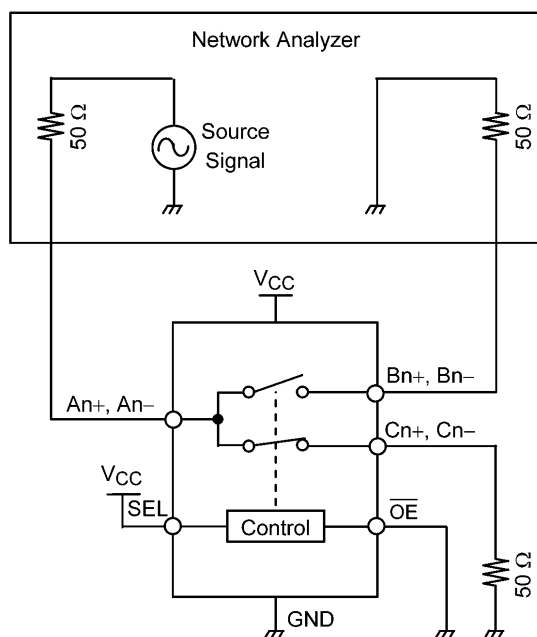
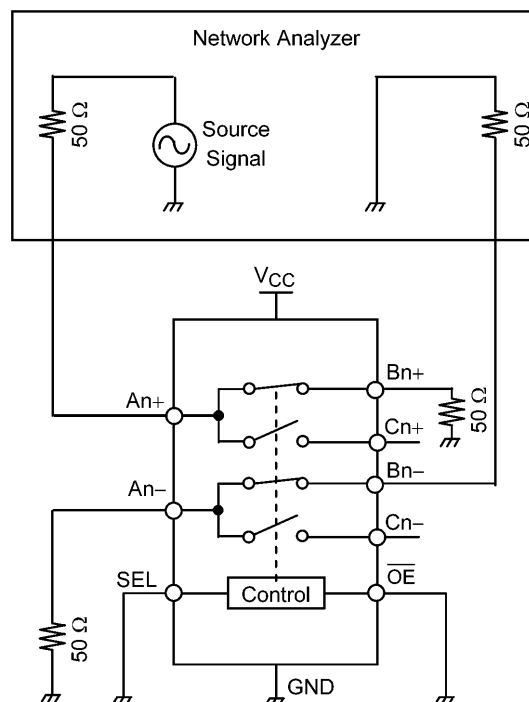


Fig. 11.5 Output Skew (channel to channel)



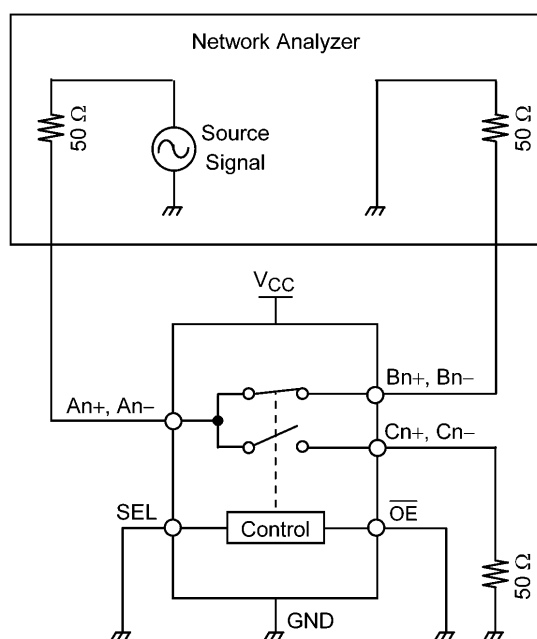
All unused ports are connected to GND through 50 Ω pull-down resistors.

**Fig. 11.6 OFF Isolation**



All unused ports are connected to GND through 50 Ω pull-down resistors.

**Fig. 11.7 Crosstalk**

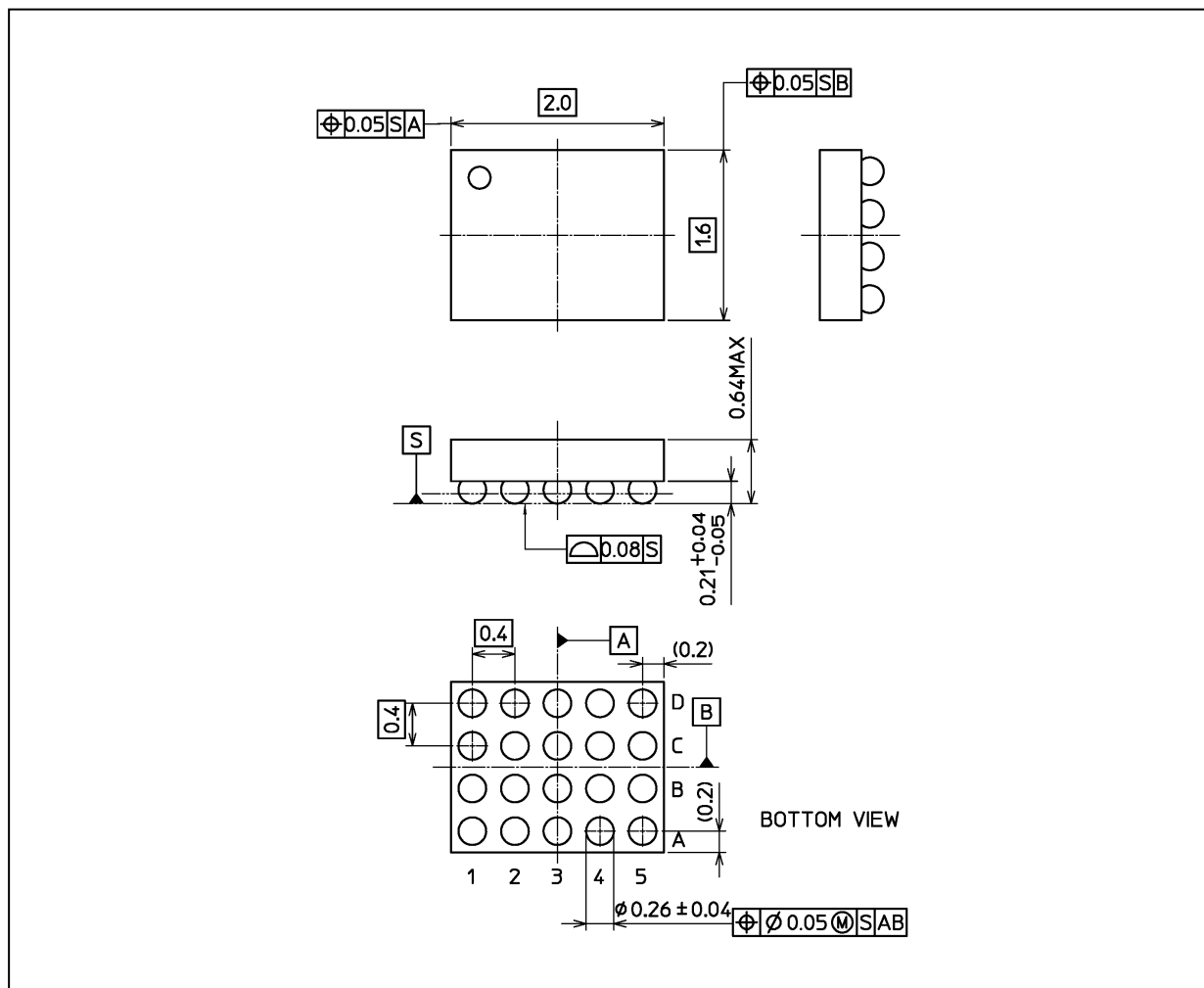


All unused ports are connected to GND through 50 Ω pull-down resistors.

**Fig. 11.8 Insertion loss, -3dB Bandwidth**

## Package Dimensions

Unit: mm



This resins used in this product include no flame retardants.

Weight: 0.005 g (typ.)

| Package Name(s)                  |
|----------------------------------|
| TOSHIBA: S-UFBGA20-0202-0.40-001 |
| Nickname: WCSP20                 |

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