Western Digital.

DATA SHEET

iNAND® 7250-B e.MMC 5.1 with HS400 Interface

(Re-branded as iNAND® CL EM122 EFD)

02-05-WW-04-00062

Revision History

Revision	Date	Description	Reference
1.0	January 28, 2019	Initial release.	

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1.0 INTRODUCTION

1.1 General Description

The iNAND 7250-B is an EFD (Embedded Flash Drive) designed for write-intensive applications in a wide range of home entertainment and security applications, such as Set-Top Box (STB), Over-The-Top (OTT), Home Gateways, Smart TV, Smart Security Cameras, etc. The device utilizes LDPC ECC and MLC memory to provide a robust, high performance, high quality and high endurance product. The LDPC engine significantly improves error correction, enabling longer device lifetime and an increased ability to handle operation at high temperature.

1.2 Capacities and Applications

The device is available in capacities of 8GB and supports e.MMC 5.1, making it the ideal choice to deliver high reliability and performance for storage applications such as imaging, video, music, GPS, gaming, email, office and new applications such as NOR replacement for embedded systems or other devices.

1.3 153-Ball Package

The design adheres to a JEDEC compatible 153-ball form factor measuring 11.5x13mm for all capacities to lower integration costs and accelerate time-to-market.

1.4 Architecture

The device combines an embedded thin flash controller with advanced Multi-Level Cell (MLC) NAND flash technology enhanced by embedded flash management software running as firmware on the controller. The device employs an industry-standard eMMC 5.1 (JESD84-B51 compatible) interface featuring Command-Queue, HS400, FFU, and legacy eMMC 4.51 features such as EUDA, Power-Off Notifications, Packed Commands, SLC Cache, Boot / RPMB partitions, HPI, and HW Reset, making it an optimal device for both reliable code and data storage.

The architecture and embedded firmware fully emulates a HDD (Hard Disk Drive) to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, The firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability while maximizing flash life expectancy.

1.5 Intelligent Controller

An intelligent controller manages the interface protocols, data storage and retrieval, ECC algorithms, defect handling and diagnostics, power management and the clock control.

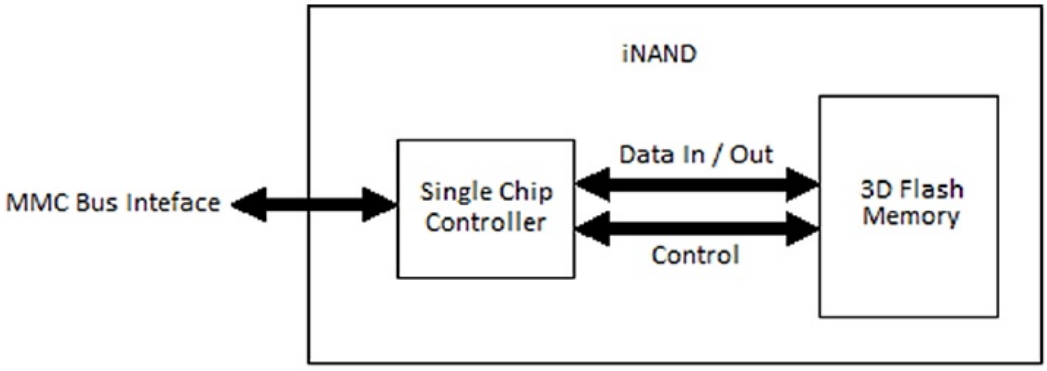
1.6 Plug-and-Play Integration

The device integrates plug-and-play support for multiple NAND technology transitions. The optimized architecture eliminates the need for complicated software integration and testing processes; the replacement of one iNAND device with another of a newer generation requires virtually no changes to the host. Manufactures can adopt advanced NAND flash technologies and update product lines with minimal integration or qualification efforts.

1.7 MMC Bus Interface

The MMC interface allows for easy integration regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device. Figure 1-1 shows a functional block diagram of the device with the MMC Bus interface.

Figure 1-1. iNAND with MMC Interface



1.8 Feature Overview

The iNAND 7250-B, with MMC interface, includes the following features:

- Memory Controller and NAND flash
- Mechanical design that is JEDEC compliant with specific optimizations for automotive applications.
- Offered in three TFBGA packages of e.MMC 5.1:
  - 11.5mm x 13mm x 0.8mm (8GB)
- Operating Temperature Range: -25°C to +85°C
- Dual Power System:
  - Core Voltage (VCC): 2.7-3.6 V
  - I/O (VCCQ) Voltage, either: 1.7-1.95V or 2.7-3.6V
- 8GB of data storage
- Supports three data bus widths: 1bit (default), 4bit, 8bit
- Complies with e.MMC Specification Version 5.1 HS400.
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200 MHz SDR (HS200), 0-200 MHz DDR (HS400)
- Up to 300 MB/s bus transfer rate, using 8 parallel data lines at 200 MHz, HS400 Mode.
- High data integrity with MLC memory, advanced LDPC ECC engine, automatic refresh, advanced power protection.
- Flexible EUDA, Fast Boot
- Up to 3K P/E cycles on MLC and 30K on SLC with a 1-year data retention @ 55°C and at least a 10-year data retention @ 55°C for fresh devices.

1.9 MMC Bus and Power Lines

The device interface supports the MMC protocol. For more information regarding these buses, refer to JEDEC Standard No. JESD84-B51. Table 1-1 lists the bus communication and power lines.

Table 1-1. MMC Bus and Power Lines

Line	Description
CMD	CMD, or Command, is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
DAT0-7	Data lines are bi-directional signals. The host and iNAND operate in push-pull mode.
CLK	Clock Input
RST_n	Hardware Reset Input
VCCQ_	VCCQ_is the power supply line for the host interface.
VCC	VCC is the power supply line for internal flash memory.
VDDi	VDDi is the internal power node of the device and not the power supply. A 0.1µ capacitor must be connected from VDDi to GND (Ground).
VSS, VSSQ_	Ground Lines
RCLK	Data Strobe
VSF	Vendor-Specific Function lines used for debugging purposes.

1.10 Bus Operating Conditions

Table 1-2. Bus Operating Conditions

Parameter	Minimum	Maximum	Unit
Peak voltage on all lines.	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors).	-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors).	-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors).	-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors).	-2	2	µA

Table 1-3. Power Supply Voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ_(Low)	1.7	1.95	V
	VCCQ_(High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ_	-0.3	0.3	V

2.0 e.MMC Selected Features Overview

2.1 Supported Features List

Table 2-1 shows the industrial iNAND 7250-B supported feature list.

Table 2-1. Proprietary Features List

e.MMC	Device Feature	Benefit	Support
N/A	INTERFACE	Speed	HS400
N/A	BUS SPEED	Maximum theoretical Speed	Up to 400MB/s
4.41	EUDA	Enhanced User Data Area for higher endurance	Yes
4.41	SECURE ERASE/TRIM	"True Wipe"	Yes
4.41	BOOT AND MASS STORAGE	One storage device (reduced BOM)	Yes
4.41	PARTITIONING AND PROTECTION	Flexibility	Yes
4.41	BACKGROUND OPERATIONS	Better User Experience (low latency)	Yes
4.41	POWER OFF NOTIFICATION	Faster Boot; Responsiveness	Yes
4.41	HARDWARE RESET	Robust System Design	Yes
4.41	HPI	Control Long Reads/Writes	Yes
4.41	RPMB	Secure Folders	Yes
4.5	EXTENDED PARTITION ATTRIBUTE	Flexibility	Yes
4.5	LARGE SECTOR SIZE	Potential performance	No
4.5	SANITIZE (4.51)	"True Wipe"	Yes
4.5	PACKED COMMANDS	Reduce Host Overhead	Yes
4.5	DISCARD	Improved Performance on Full Media	Yes
4.5	DATA TAG	Performance and/or Reliability	Yes (API only)
4.5	CONTEXT MANAGEMENT	Performance and/or Reliability	Yes (API only)
4.5	CACHE	Better Sequential & Random Writes	Yes
5.0	SECURED FIELD FIRMWARE UPGRADE (sFFU)	Enables feature enhancements in the field	Yes
5.0	PRODUCTION STATE AWARENESS	Different operation during production	Yes
5.0	DEVICE HEALTH	Vital NAND info	Yes
5.1	ENHANCE STROBE	Sync between Device and Host in HS400	Yes
5.1	COMMAND QUEUE	Responsiveness	Yes
5.1	RPMB THROUGHPUT	Faster RPMB write throughput	Yes
5.1	CACHE FLUSH AND BARRIER	Ordered Cache flushing	Yes
5.1	BKOPS CONTROLLER	Host control on BKOPs	Yes
5.1	SECURE WP	Secure Write Protect	Yes
5.1	PRE EOL	Pre-End-of-Life notification	Yes
Proprietary	VSF	Enables vendor on-board debugging	Yes
Proprietary	PNM	Special Product Name	Yes
Proprietary	DEVICE REPORT	Device Firmware Status	Yes
Proprietary	UNIFIED BOOT	Reports both boot partitions	Yes (only on CS2.2)
Proprietary	HARDWARE PIN SECURE BOOT	Enable Hardware Pin Secure Write Protect	Yes (only on CS2.2)

2.2 HS400 Interface

The device supports HS400 signaling to achieve a bus speed of 400 MB/s via a 200MHz dual data rate clock frequency. HS400 mode supports a 4bit or 8bit bus width and the 1.7 – 1.95 VCCQ option. The host may need to have an adjustable sampling point to reliably receive the incoming data due to the speed. Refer to the JESD84-B51 standard for information.

2.3 Enhanced User Data Area (EUDA)

For write intensive applications, there is a need for an area of higher endurance or performance. The device allows for the definition of an enhanced user data area as specified in the JESD84-B51 standard. This area is a true SLC partition. The EUDA is a designated area of the general User Data Area. The configuration is one-time programmable.

2.4 Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) allows for features enhancement in the field; the host will download the latest version of the firmware and then installs it on the device. The entire FFU process occurs in the background without affecting the user/OS data. The host can replace firmware files or single/all file systems during the FFU process.

The secure FFU (sFFU) usage model for firmware upgrades is as follows:

1. sFFU files are generated and signed at the laboratory.
2. The sFFU files are handed to the customer.
3. The customer can transparently push the firmware updates to their end-users.

NOTES:

- The sFFU process and sFFU files are protected against leakage to unauthorized entities.
- The host may retrieve the exact status of the process using the SMART Report feature.
- Refer to the JESD84-B51 standard and the application note on this subject for more information.

2.5 Cache

The eMMC cache is dedicated volatile memory with a size of 512KB. Caching is enabled to improve performance for both sequential and random access. Refer to the JESD84-B51 standard for additional information.

2.6 Discard

The device supports the Discard command as defined in the e.MMC 5.1 specification. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the media. It is highly recommended to use the Discard command to guarantee optimal performance and reduce amount of housekeeping.

2.7 Power-off Notifications

The device supports power off notifications as defined in e.MMC 5.1 specification. Power-off notification allows the device to shutdown properly and save important data for a faster boot time on the next power cycle, thereby improving the user experience during power-on.

Note: The device may enter Sleep Mode while power-off notification is enabled.

2.8 Packed Commands

To enable optimal system performance, the device supports packed commands (as defined in e.MMC 5.1 specification). The host can pack Read or Write commands into groups (of a single type of operation) and transfer the commands to the device in a single transfer on the bus, thereby reducing overall bus overheads.

2.9 Boot Partition

The device supports e.MMC 5.1 boot operation mode; the factory configuration supplies two boot partitions, each 4MB in size, for 8GB capacities.

2.10 RPMB Partition

The e.MMC 5.1 RPMB operation mode is supported; the factory configuration supplies one RPMB partition, 4MB in size, for 8GB capacities.

2.11 Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from Sleep Mode. The device enters Sleep Mode to conserve power upon completion of an operation if no further commands are received. The host does not have to take any action for this to occur; however, to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in Sleep Mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in Sleep Mode, any command issued to the device will cause it to immediately exit Sleep Mode.

2.12 Sleep (CMD5)

The device may be switched between a Sleep and a Standby state using SLEEP/AWAKE (CMD5). The power consumption is minimized and the device responds only to the RESET (CMD0) and SLEEP/AWAKE (CMD5) commands. All the other commands are ignored by the memory device.The VCC power supply may be switched off in Sleep state to enable further system power reduction. Refer to the JESD84-B51 specification for information.

2.13 Enhanced Reliable Write

The device supports Enhanced Reliable Write (as defined in the e.MMC 5.1 specification). Enhanced Reliable Write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, the data will remain valid even if a sudden power loss occurs during programming.

2.14 Sanitize

The Sanitize operation is used to permanently remove data from the device. The device will physically remove data from the unmapped user address space. The device will continue the Sanitize operation, with BUSY asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

Note: No data should remain in the unmapped host address space following the completion of a Sanitize operation.

2.15 Secure Erase

To ensure backward compatibility, the device supports the optional Secure Erase command (in addition to the standard Erase command). This command allows the host to erase a defined range of LBAs and ensure that no previous copies of this data exist in the flash.

2.16 Secure Trim

The device supports the Secure Trim command (to ensure backward compatibility). The Secure Trim command is like the Secure Erase command, but also performs a Secure Purge operation on write blocks instead of erase groups.

The Secure Trim command is performed in two steps:

1. Marks the LBA range as candidate for erasure.
2. Erases the marked address range and ensures no old copies of data remain.

2.17 Partition Management

It is possible for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models; the memory block area scan be classified as follows:

- Factory configuration supplies two boot partitions (refer to *Section 2.10 RPMB Partition on page 13*) implemented as enhanced storage media and one RPMB partitioning of 4MB in size (refer to *Section 2.11 Automatic Sleep Mode on page 13*); the two partitions are implemented as SLC.
- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size can be programmed once in the device life-cycle (one-time programmable). For the generic SKU, the partitions can only be set as a MLC block. If the host sets the GPP partitions as enhanced, it will remain as MLC.

2.18 Device Health

Device Health is like the SMART features of modern hard disks; it provides only vital NAND flash program/erase cycle information as percentage of the useful flash life span.

The host can query Device Health information utilizing standard MMC commands. To access the extended CSD structure:

- DEVICE_LIFE_TIME_EST_TYP_A[268]:
  The host may use it to query SLC device health information.
- DEVICE_LIFE_TIME_EST_TYP_B[269]:
  The host may use it to query MLC device health information

Note: Device Health will indicate a percentage (%) of the wear of the device in 10% increments.

2.19 EOL Status

EOL Status was implemented according to the eMMC 5.1 specification. One additional state (State 4) was added to the device to indicate that it is in EOL Mode.

2.20 Enhanced Write Protection

To allow the host to protect data against unauthorized erase or write, the device supports two levels of the Write Protect command:

- The entire device (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition), may be write-protected by setting the permanent or temporary write protect bits in the CSD.
- Specific segments of the device may be permanently, at power-on or temporarily, write protected; the Segment size can be programmed via the EXT_CSD register.

Note: Refer to the JESD84-B51 standard for information.

2.21 High Priority Interrupt (HPI)

The HPI (High Priority Interrupt) as defined in the JESD84-B51 standard enables a low read latency operation by suspending a lower priority operation before it is completed.

For example, the operating system usually employs demand-paging to launch a process requested by the user. If the host needs to fetch pages during a write operation, the request will be delayed until the completion of the Write command.

Note: Refer to JESD84-B51 for more information on the HPI function.

2.22 Hardware (H/W) Reset

Hardware Reset (H/W Reset) may be used by host to reset the device, moving the device to a pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted.

Note: Refer to JESD84-B51 for more information.

2.23 Host-Device Synchronization Flow (Enhanced STROBE)

The Enhanced STROBE feature as implemented in the device allows the utilization of STROBE to also synchronize the CMD response:

- CMD clocking stays SDR (much like legacy DDR52).
- Host commands are clocked out with the rising edge of the host clock (using the same method of legacy eMMC devices).
- The device will provide STROBE signaling synced with the CMD response in addition to DATA OUT.
- The host may use the STROBE signaling for DAT and CMD-Response capturing, eliminating the need for a tuning mechanism.

Note: This feature requires support by the host to enable faster and more reliable operation.

2.24 Command-Queue

Command Queue enables device visibility of the next series of commands and results in a performance improvement. The protocol allows the host to queue up to 32 data-transfer commands in the device by implementing five (5) new commands.

The benefits of command queuing are:

- Random Read performance improvement (higher IOPs)
- Reducing protocol overhead
- Command issuance allowed while data transfer is on-going
- Device order of the tasks according to best access to/from flash

3.0 Product Specifications

3.1 Typical Power Measurements

Table 3-1. Power Consumption Sleep (Ta=25°C@1.8V/3.3V)

	8GB	Units
HS400 Sleep (CMD5 – VCCQ, VCC off)	150	µA
HS200 Sleep (CMD5 – VCCQ, VCC off)	150	µA
DDR52 Sleep (CMD5 – VCCQ, VCC off)	150	µA

Table 3-2. Power Consumption Peak VCC / VCCQ (Ta=25°C@1.8V/3.3V)

		8GB	Units
Active HS400	Peak [2µs window] VCC	150	mA
	Peak [2µs window] VCCQ[1]	295	mA
Active HS200	Peak [2µs window] VCC	150	mA
	Peak [2µs window] VCCQ	210	mA
Active DDR52	Peak [2µs window] VCC	150	mA
	Peak [2µs window] VCCQ	200/165[2]	mA

[1] *The regulator must be able to supply the current as the peak value can last for up to 1ms.*
[2] *1.8V/3.3V.*

Table 3-3. Power Consumption RMS VCC / VCCQ (Ta=25°C@1.8V/3.3V)

			8GB	Units
Active HS400	Read	RMS [100ms window] VCC	60	mA
		RMS [100ms window] VCCQ	245	mA
	Write	RMS [100ms window] VCC	45	mA
		RMS [100ms window] VCCQ	135	mA
Active HS200	Read	RMS [100ms window] VCC	50	mA
		RMS [100ms window] VCCQ	145	mA
	Write	RMS [100ms window] VCC	50	mA
		RMS [100ms window] VCCQ	105	mA
Active DDR52	Read	RMS [100ms window] VCC	40	mA
		RMS [100ms window] VCCQ	110/140[1]	mA
	Write	RMS [100ms window] VCC	45	mA
		RMS [100ms window] VCCQ	95/100[1]	mA

[1] 1.8V/3.3V.

3.2 Operating Conditions

3.2.1 Operating and Storage Temperature

Table 3-4. Operating and Storage Temperatures

Operating Temperature	Storage (Non-Operating Temperature	Condition
-25°C (min) to 85°C (max)	-40°C (min) to 85°C (max)	Ambient Temperature (Ta)

3.2.2 Moisture Sensitivity Level (MSL)

The moisture sensitivity level for the device is MSL = 3.

3.2.3 Reliability

The device meets or exceeds Endurance and Data Retention requirements as per evaluated representative usage models for the designated market and relevant sections of JESD47I standard.

Table 3-5. Critical Reliability Characteristics

Reliability Characteristics	Description	Value
Uncorrectable Bit Error Rate (UBER)	The Uncorrectable Bit Error Rate (UBER) will not exceed one (1) sector in the specified number of bits read (in such rare events, data can be lost).	1 sector in 10^{15} bits read.
Write Endurance (TBW)	Write Endurance is commonly classified in Total Terabytes Written (TBW) to the device. This is the total amount of data that can be written to the device over its useful life time and is dependent on the workload. TBW is characterized according to a representative mobile workload as described below: ■ 70% Sequential Write, 30% Random Write. ■ Distribution of I/O Transaction Sizes: – <16KB: 77% - 86% – 16KB-128KB: 13% - 19% – >128KB: 1.5% - 4% ■ Cache On, Packed Off ■ Host data is 4K aligned	Total Terabytes Written [TBW] Per representative Android workload: ■ 8GB: 20 TBW
Data Retention (Years)	Fresh or Early Life Device: A device having a total number of write cycles to the flash that is less than 10% of the maximum endurance specification.	10 years[1] of Data Retention @ 55°C
	Cycled Device: A device having a total number of write cycles between 10% of the maximum write endurance and equal to or greater than the maximum write endurance specification.	1 year[1] of Data Retention @ 55°C

[1] *When power is off. In the case of power on, the automatic refresh will insure protection against data retention related loss of data.*

3.3 Typical System Performance[1]

Table 3-6. Sequential Performance [2,3]

	HS400		HS200		DDR52	
Capacity	**Write (MB/s)**	**Read (MB/s)**	**Write (MB/s)**	**Read (MB/s)**	**Write (MB/s)**	**Read (MB/s)**
8GB	35	270	35	170	35	90

Table 3-7. Sequential Performance - EUDA

	HS400		HS200		DDR52	
Capacity	**Write (MB/s)**	**Read (MB/s)**	**Write (MB/s)**	**Read (MB/s)**	**Write (MB/s)**	**Read (MB/s)**
8GB	60	300	60	170	60	90

Table 3-8. Random Performance[4,5]

	HS400			HS200			DDR52		
	Write (IOPs)	**Read (IOPs)**		**Write (IOPs)**	**Read (IOPs)**		**Write (IOPs)**	**Read (IOPs)**	
Capacity	**Cache ON**	**QD=8**	**QD=1**	**Cache ON**	**QD=8**	**QD=1**	**Cache ON**	**QD=8**	**QD=1**
8GB	8k	17k	7.8k	6k	10k	4.5k	5.5k	10k	3.5k

1 All performance is measured using Western Digital proprietary test environment, without file system overhead and host turn-around time (HTAT).
2 Sequential Read/Write performance is measured under HS400 mode with a bus width of 8 bit at 200 MHz DDR mode, chunk size of 512KB, and data transfer of 1GB.
3 Sequential Write performance is measured for 100MB host payloads.
4 Random performance is measured with a chunk size of 4KB and address range of 1GB.
5 Random Write IOPs shown are with cache on.

4.0 PHYSICAL SPECIFICATIONS

The device package consists of a 153-pin, thin fine-pitched ball grid array (BGA). See Figure 4-1, Figure 4-2, Figure 4-3, and Table 4-1 on page 21 for physical specifications and dimensions.

Figure 4-1. 153-Ball Package Dimensions – Top and Side View

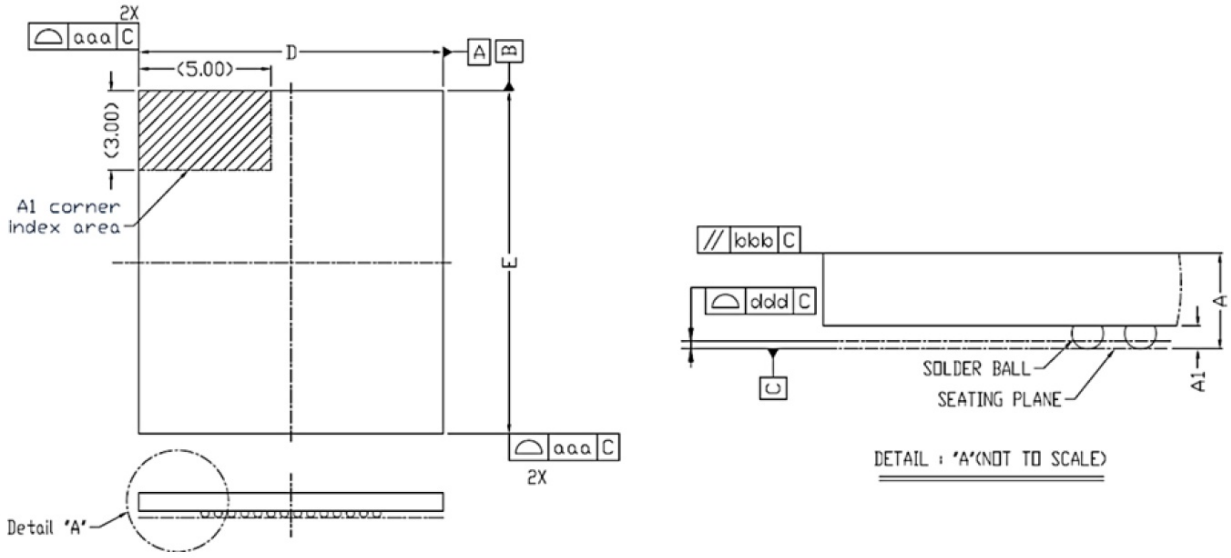


Figure 4-2. 153-Ball Package Dimensions – Bottom View

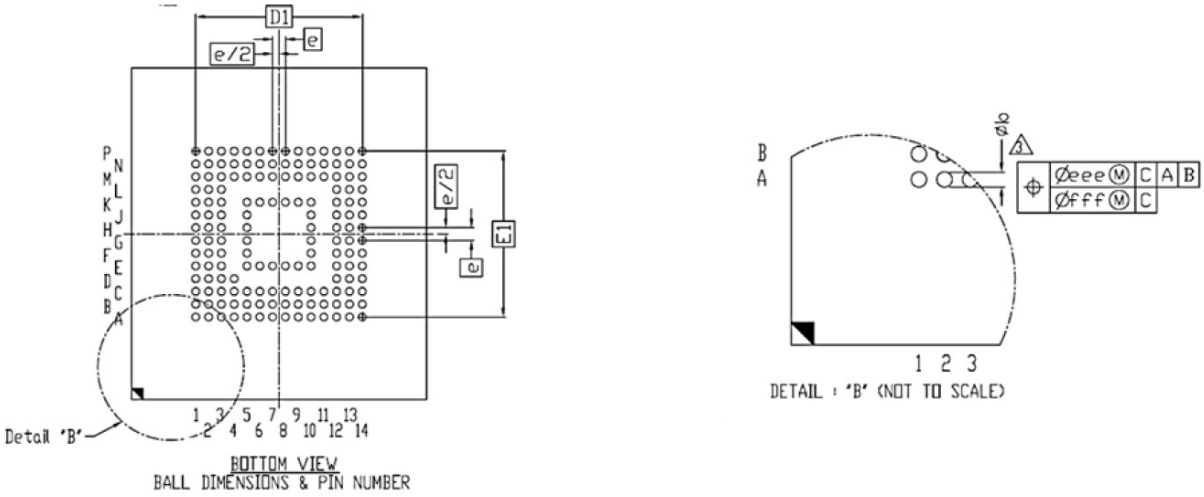


Figure 4-3. 153-Ball BGA Pad Details

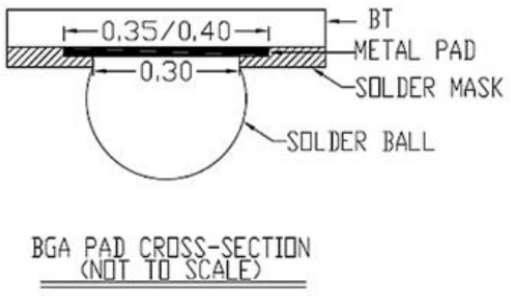


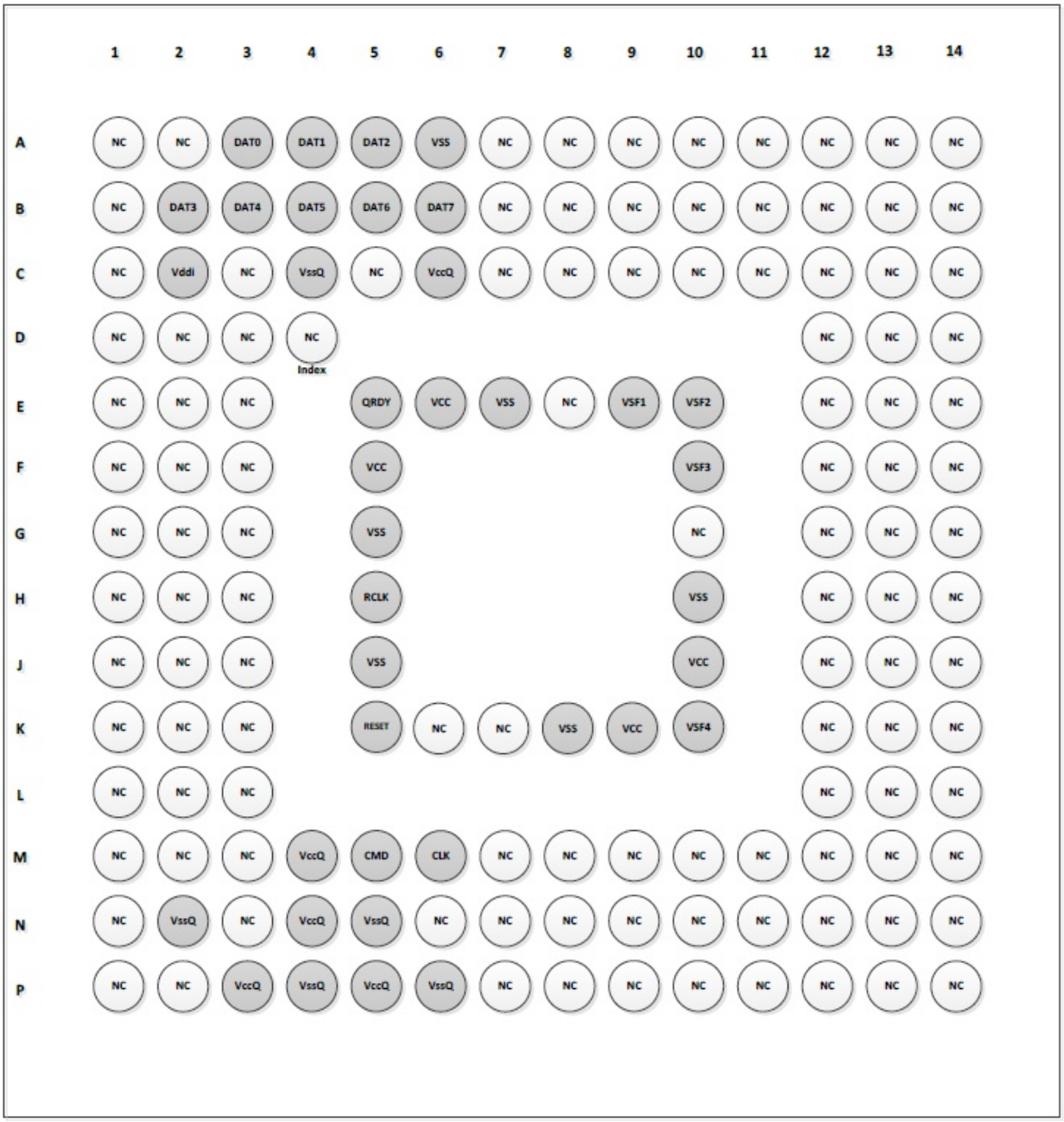
Table 4-1. Package Specification

	8GB		
Symbol	**Min (mm)**	**Nom (mm)**	**Max (mm)**
A	0.6	0.7	0.8
A1	0.17	0.22	0.27
D	11.4	11.5	11.6
E	12.9	13	13.1
D1	—	6.5	—
E1	—	6.5	—
e	—	0.5	—
b	0.25	0.3	0.35
aaa	0.1		
bbb	0.1		
ddd	0.08		
eee	0.15		
fff	0.05		
MD/ME	14/14		

4.1 Interface Description

4.1.1 MMC I/F Ball Array

Figure 4-4. 153 balls - Ball Array (Top View)



4.2 Pins and Signal Description

Table 4-2 lists the functional pin assignments of the iNAND 153-ball package.

Table 4-2. Functional Pin Assignment – 153-Balls with MMC Interface

Pin	Signal	Type	Description
A3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer.
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
E5	QRDY	O	An optional pin, disabled by default, toggled by the device when the value of QSR changes.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
K5	RST_n		Hardware Reset
H5	RCLK	Output	Data Strobe
E6	VCC	Supply	Flash I/O and memory power supply.
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply.
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
E7	VSS	Supply	Flash I/O and memory ground connection.
G5	VSS		
H10	VSS		
K8	VSS		
A6	VSS		
J5	VSS		
C4	VSSQ	Supply	Memory controller core and MMC I/F ground connection.
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
C2	VDDi		Internal power node. A 0.1µF capacitor must be connected from VDDi to GND (Ground).
E9	VSF1	VSF	Vendor Specific Function balls for test/debug. VSF balls should be floating and be brought out to test pads.
E10	VSF2		
F10	VSF3		
K10	VSF4		

NOTE: All other pins are N/C (Not Connected) and can be connected to GND or remain floating.

4.3 Registers Values

4.3.1 OCR Register

Table 4-3. OCR Register Values

Parameter	DSR Slice	Description	Value	Width
Access Mode	[30:29]	Access mode	2h	2
	[23:15]	VDD: 2.7 - 3.6 range	1FFh	9
	[14:8]	VDD: 2.0 - 2.6 range	00h	7
	[7]	VDD: 1.7 - 1.95 range	1h	1

NOTE: Bit 30 is set because the device is High Capacity and Bit 31 will be set only when the device is ready.

4.3.2 CID Register

Table 4-4. CID Register Values

Parameter	DSR Slice	Description	Value	Width
MMC MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Card BGA	01h	2
OID	[111:104]	OEM/Application ID	00h	8
PNM	[103:56]	Product Name	8GB – DG4008	48
PRV	[55:48]	Product Revision	01h	8
PSN	[47:16]	Product Serial Number	Random by Production	32
MDT	[15:8]	Manufacturing Date	Month, Year	8
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

NOTE: Refer to the definition of the MDT field as defined in e.MMC Specification, Version 5.0.

4.3.3 DSR Register

Table 4-5. DSR Register Values

Parameter	DSR Slice	Description	Value	Width
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

Note: DSR is not implemented; in case of read, a value of 0x0404 will be returned.

4.3.4 CSD Register

Table 4-6. CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD Structure	3h	3
SPEC_VERS	[125:122]	System Specification Version	4h	4
TAAC	[119:112]	Data Read Access-Time 1	0Fh	8
NSAC	[111:104]	Data Read Access-Time 2 in CLK Cycles (NSAC*100)	00h	8
TRAN_SPEED	[103:96]	Max. Bus Clock Frequency	32h	8
CCC	[95:84]	Card Command Classes	8F5h	12
READ_BL_LEN	[83:80]	Max. Read Data Block Length	9h	4
READ_BL_PARTIAL	[79:79]	Partial Blocks for Read Allowed	0h	1
WRITE_BLK_MISALIGN	[78:78]	Write Block Misalignment	0h	1
READ_BLK_MISALIGN	[77:77]	Read Block Misalignment	0h	1
DSR_IMP	[76:76]	DSR Implemented	0h	1
C_SIZE	[73:62]	Device Size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. Read Current @ VDD Min	7h	3
VDD_R_CURR_MAX	[58:56]	Max. Read Current @ VDD Max	7h	3
VDD_W_CURR_MIN	[55:53]	Max. Write Current @ VDD Min	7h	3
VDD_W_CURR_MAX	[52:50]	Max. Write Current @ VDD Max	7h	3
C_SIZE_MULT	[49:47]	Device Size Multiplier	7h	3
ERASE_GRP_SIZE	[46:42]	Erase Group Size	1Fh	5
ERASE_GRP_MULT	[41:37]	Erase Group Size Multiplier	1Fh	5
WP_GRP_SIZE	[36:32]	Write Protect Group Size	0Fh	5
WP_GRP_ENABLE	[31:31]	Write Protect Group Enable	1h	1
DEFAULT_ECC	[30:29]	Manufacturer Default	0h	2
R2W_FACTOR	[28:26]	Write Speed Factor	2h	3
WRITE_BL_LEN	[25:22]	Max. Write Data Block Length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial Blocks for Write Allowed	0h	1

Table 4-6. CSD Register (Continued)

Parameter	CSD Slice	Description	Value	Width
CONTENT_PROT_APP	[16:16]	Content Protection Application	0h	1
FILE_FORMAT_GRP	[15:15]	File Format Group	0h	1
COPY	[14:14]	Copy Flag (OTP)	1h	1
PERM_WRITE_PROTECT	[13:13]	Permanent Write Protection	0h	1
TMP_WRITE_PROTECT	[12:12]	Temporary Write Protection	0h	1
FILE_FORMAT	[11:10]	File Format	0h	2
ECC	[9:8]	ECC Code	0h	2
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

4.3.5 EXT_CSD Register

Table 4-7. EXT_CSD Register

Parameter	ECSD Slice	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background Operations Support	1h
MAX_PACKED_READS	[501]	Max. Packed Read Commands	3Fh
MAX_PACKED_WRITES	[500]	Max. Packed Write Commands	3Fh
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h
TAG_UNIT_SIZE	[498]	Tag Unit Size	3h
TAG_RES_SIZE	[497]	Tag Resources Size	3h
CONTEXT_CAPABILITIES	[496]	Context Management Capabilities	5h
LARGE_UNIT_SIZE_M1	[495]	Large Unit Size	0h
EXT_SUPPORT	[494]	Extended Partitions Attribute Support	3h
SUPPORTED_MODES	[493]	FFU Supported Modes	3h
FFU_FEATURES	[492]	FFU Features	0h
OPERATION_CODES_TIMEOUT	[491]	Operation Codes Timeout	10h
FFU_ARG	[490:487]	FFU Argument	0h
BARRIER_SUPPORT	[486]	Cache Barrier Support	1h
CMDQ_SUPPORT	[308]	Command Queue Support	1h
CMDQ_DEPTH	[307]	Command Queue Depth	1Fh
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	Number of FW Sectors Correctly Programmed	0h
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	Vendor Proprietary Health Report	0h

Table 4-7. EXT_CSD Register (Continued)

Parameter	ECSD Slice	Description	Value
DEVICE_LIFE_TIME_EST_TYP_B	[269]	Device Life Time Estimation Type B (MLC)	1h
DEVICE_LIFE_TIME_EST_TYP_A	[268]	Device Life Time Estimation Type A (SLC)	1h
PRE_EOL_INFO	[267]	Pre-EOL Information	1h
OPTIMAL_READ_SIZE	[266]	Optimal Read Size	8h
OPTIMAL_WRITE_SIZE	[265]	Optimal Write Size	8h
OPTIMAL_TRIM_UNIT_SIZE	[264]	Optimal Trim Unit Size	8h
DEVICE_VERSION	[263:262]	Device Version	5025h
FIRMWARE_VERSION	[261:254]	Firmware Version	FW Version
PWR_CL_DDR_200_360	[253]	Power Class for 200MHz; DDR at VCC= 3.6V	DDh
CACHE_SIZE	[252:249]	Cache Size	1000h
GENERIC_CMD6_TIME	[248]	Generic CMD6 Timeout	19h
POWER_OFF_LONG_TIME	[247]	Power-off Notification (long) Timeout	19h
BKOPS_STATUS	[246]	Background Operations Status	Default = 0h
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of Correctly Programmed Sectors	Default = 0h
INI_TIMEOUT_AP	[241]	First Initialization Time After Partitioning	5Ah
CACHE_FLUSH_POLICY	[240]	Cache Flush Policy	1h
PWR_CL_DDR_52_360	[239]	Power Class for 52MHz, DDR at VCC = 3.6V	0h
PWR_CL_DDR_52_195	[238]	Power Class for 52MHz, DDR at VCC = 1.95V	DDh
PWR_CL_200_195	[237]	Power Class for 200MHz at VCCQ=1.95V, VCC = 3.6V	DDh
PWR_CL_200_130	[236]	Power Class for 200MHz, at VCCQ=1.3V, VCC = 3.6V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR Mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at 52MHz in DDR Mode	0h
TRIM _MULT	[232]	TRIM Multiplier	3h
SEC_FEATURE_SUPPORT	[231]	Secure Feature Support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	A6h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	A6h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot Partition Size	20h
ACCESS_SIZE	[225]	Access Size	8h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase Unit Size	1h (see Table 4-9 on page 31).

Table 4-7. EXT_CSD Register (Continued)

Parameter	ECSD Slice	Description	Value
ERASE_TIMEOUT_MULT	[223]	High Capacity Erase Timeout	3h
REL_WR_SEC_C	[222]	Reliable Write Sector Count	1h
HC_WP_GRP_SIZE	[221]	High Capacity Write Protect Group Size	10h (see Table 4-9 on page 31).
S_C_VCC	[220]	Sleep Current [VCC]	8GB – 5h
S_C_VCCQ_	[219]	Sleep Current [VCCQ_]	7h
PRODUCTION_STATE_AWARE-NESS_TIMEOUT	[218]	Production State Awareness Timeout	17h
S_A_TIMEOUT	[217]	Sleep/Awake Timeout	12h
SLEEP_NOTIFICATION_TIME	[216]	Sleep Notification Timeout	17h
SEC_COUNT	[215:212]	Sector Count	See Table 4-8 on page 31.
SECURE_WP_INFO	[211]	Secure Write Protect Info	1h
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	Ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	Ah
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	Ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	Ah
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	0h
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	0h
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	DDh
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	DDh
PARTITION_SWITCH_TIME	[199]	Partition Switching Timing	3h
OUT_OF_INTERRUPT_TIME	[198]	Out-of-Interrupt Busy Timing	19h
DRIVER_STRENGTH	[197]	I/O Driver Strength	1Fh (Reporting four strengths, but sup-porting only one)
CARD_TYPE	[196:195]	Card Type	57h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	8h
CMD_SET	[191]	Command Set	Default = 0h
CMD_SET_REV	[189]	Command Set Revision	0h Updated in runtime.
POWER_CLASS	[187]	Power Class	Dh

Table 4-7. EXT_CSD Register (Continued)

Parameter	ECSD Slice	Description	Value
HS_TIMING	[185]	High Speed Interface Timing	Default = 0h Updated in runtime by the host.
DATA_STRB_MODE_SUPPORT	[184]	Data Strobe Mode Support	1h
BUS_WIDTH	[183]	Bus Width Mode	Default = 0h Updated in runtime by the host.
ERASE_MEM_CONT	[181]	Content of Explicit Erased Memory Range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default = 0h Updated in runtime by the host.
BOOT_CONFIG_PROT	[178]	Boot Config Protection	Default = 0h Updated in runtime by the host.
BOOT_BUS_CONDITIONS	[177]	Boot Bus Width	Default = 0h Updated in runtime by the host.
ERASE_GROUP_DEF	[175]	High-Density Erase Group Definition	Default = 0h Updated in runtime by the host.
BOOT_WP_STATUS	[174]	Boot Write Protection Status Registers	Default = 0h Updated in runtime.
BOOT_WP	[173]	Boot Area Write Protect Register	0h
USER_WP	[171]	User Area Write Protect Register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	20h
WR_REL_SET	[167]	Write Reliability Setting Register	1Fh
WR_REL_PARAM	[166]	Write Reliability Parameter Register	15h
SANITIZE_START	[165]	Start Sanitize Operation	Default = 0h Updated in runtime by the host.
BKOPS_START	[164]	Manually Start Background Operations	Default = 0h Updated in runtime by the host.
BKOPS_EN	[163]	Enable Background Operations Handshake	2h
RST_n_FUNCTION	[162]	H/W Reset Function	Default = 0h Updated by the host.
HPI_MGMT	[161]	HPI Management	Default = 0h Updated by the host.
PARTITIONING SUPPORT	[160]	Partitioning Support	7h
MAX_ENH_SIZE_MULT	[159:157]	Max. Enhanced Area Size	8GB – 1B5h
PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	Default = 0h Updated by the host.

Table 4-7. EXT_CSD Register (Continued)

Parameter	ECSD Slice	Description	Value
PARTITION_SETTING_COMPLETED	[155]	Partitioning Setting	Default = 0h Updated by the host.
GP_SIZE_MULT	[154:143]	General Purpose Partition Size (GP4)	0h
GP_SIZE_MULT	[151:149]	General Purpose Partition Size (GP3)	0h
GP_SIZE_MULT	[148:146]	General Purpose Partition Size (GP2)	0h
GP_SIZE_MULT	[145:143]	General Purpose Partition Size (GP1)	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management Mode	0h
PRODUCTION_STATE_AWARENESS	[133]	Production State Awareness	0h
TCASE_SUPPORT	[132]	Package Case Temperature is Controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h
PROGRAM_CID_CSD_DDR_SUPPORT	[130]	Program CID/CSD in DDR Mode Support	1h
VENDOR_SPECIFIC_FIELD	[127:87]	Vendor Specific Fields	Reserved
PWR_CL_DDR_266	[86]	Maximum Power Class for HS533	0h
CARD_TYPE_2ND_INDEX	[84]	Device HS533 Support	0h
SKU_FEATURES_ID	[80]	7250-B SKU Identification	0h
VENDOR_SPECIFIC_FIELD	[82:64]	Vendor Specific Fields	Reserved
NATIVE_SECTOR_SIZE	[63]	Native Sector Size	0h
USE_NATIVE_SECTOR	[62]	Sector Size Emulation	0h
DATA_SECTOR_SIZE	[61]	Sector Size	0h
INI_TIMEOUT_EMU	[60]	First Initialization After Disabling Sector Size Emulation	Ah
CLASS_6_CTRL	[59]	Class 6 Commands Control	0h
DYNCAP_NEEDED	[58]	Number of Addressed Group to be Released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception Events Control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception Events Status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context Configuration	Default = 0h
PACKED_COMMAND_STATUS	[36]	Packed Command Status	Default = 0h Updated in runtime.
PACKED_FAILURE_INDEX	[35]	Packed Command Failure Index	Default = 0h Updated in runtime.

Table 4-7. EXT_CSD Register (Continued)

Parameter	ECSD Slice	Description	Value
POWER_OFF_NOTIFICATION	[34]	Power-off Notification	Default = 0h Updated in runtime by the host.
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF.	0h
FLUSH_CACHE	[32]	Flushing of the Cache	0h
BARRIER_CTRL	[31]	Cache Barrier	0h
MODE_CONFIG	[30]	Mode Config	0h
MODE_OPERATION_CODES	[29]	Mode Operation Codes	0h
FFU_STATUS	[26]	FFU Status	0h
PRE_LOADING_DATA_SIZE	[25:22]	Preloading Data Size	0h
MAX_PRE_LOADING_DATA_SIZE	[21:18]	Max. Preloading Data Size	See Table 4-10 on page 31.
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17]	Product State Awareness Enablement	3h AUTO_PRE_SOLDERING
SECURE_REMOVAL_TYPE	[16]	Secure Removal Type	8h
CMDQ_MODE_EN	[15]	Command Queue	0h

4.4 User Density

Table 4-8 shows the available capacity for user data according to the device size.

Table 4-8. Exported Capacity for User Data

Capacity	LBA [Hex]
8GB	0xE90E80

Table 4-9. Write Protect Group Size

Capacity	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
8GB	0x1	0x10	0.5MB	8MB

The maximum preloading image for the device is reflected in the exported capacity as shown in Table 4-10 below.

Table 4-10. Maximum Preloading Data Size

Capacity	Maximum Preloading Image Size (in LBA HEX)
8GB	0xE90E80

5.0 Hardware Application Guidelines

5.1 Design Guidelines

1. The e.MMC specification enforces single device per host channel; a multi-device configuration per a single host channel is not supported.
2. CLK, RCLK(DS), CMD and DATx lines should be connected to respected host signals. The e.MMC specification requires that all signals will be connected point-to-point, e.g., a single e.MMC device per host channel.
3. The e.MMC hardware reset signal (RST_n) is not mandatory and can be connected to the host reset signal or remain unconnected (floating) if not used.
4. All power supply and ground pads must be connected.
5. Make sure any external pull-up resistors are placed on the schematic. Refer to Table 5-2 on page 35 for details.
6. Bypass capacitors shall be placed as close to the e.MMC device as possible; it is recommended to have 0.1µF and 4.7µF capacitors per power supply rail, although specific designs may include a different configuration in which there are more than two capacitors:
    a. VCC and VCCQ slew rates shall be minimally affected by any bypass capacitors configuration.
    b. It is recommended to verify the bypass capacitors requirement in the product data sheet.
7. The VDDi bypass capacitor shall be placed on the PCB. The VDDi is an internal power node for the controller and requires capacitor in the range of 0.1µF-2.2µF connected between the VDDi pad and ground.
8. Vendor-Specific Function (VSF) pins should be connected to accessible test points on the PCB (TP on the following schematic). It is recommended to have accessible ground (GND) pads near each TP on PCB.
9. It is recommended to layout e.MMC signals with a controlled impedance of 45-55 Ohm, referencing to the adjusted ground plane.

5.2 Capacitor Selection and Layout Guidelines

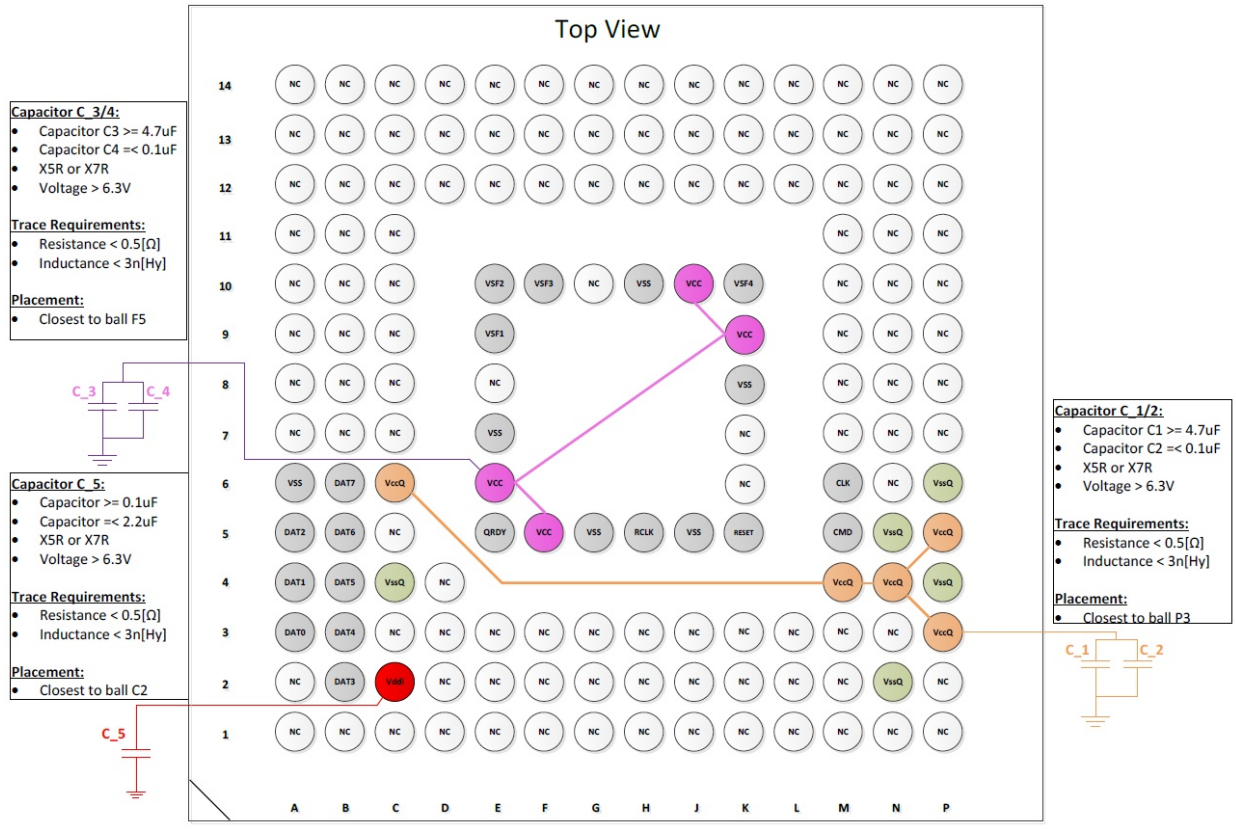
The device has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 5-1.

Table 5-1. Power Domains

Pin	Power Domain	Comments
VCCQ	Host Interface	Supported voltage ranges: Low Voltage Region: 1.8V (nominal)
VCC	Memory	Supported voltage range: High Voltage Region: 3.3V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

It is recommended that the power domains connectivity will follow Figure 5-1.

Figure 5-1. Recommended Power Domain Connectivity



NOTES:

- Signal routing in the diagram is for illustration purposes only and the final routing depends on the final PCB layout. For clarity, the diagram does not include the VSS connection. All balls marked VSS shall be connected to a ground (GND) plane.

5.3 Capacitor Recommendations

5.3.1 General Recommendations

1. It is recommended to use X5R/X7R SMT-Ceramic capacitors rated for 6.3V/10V with a footprint of 0402 or greater.
2. When using ceramic capacitors, the capacitors should be located as close to the supply ball as possible. This will eliminate mounting inductance effects and result in a cleaner voltage supply for the internal IC rail.
3. Make all the power (high current) traces as short, direct and thick as possible. The capacitors should be as close to each other as possible, as it reduces EMI radiated by the power traces due to the high switching currents; it will also reduce mounting inductance and resistance, which will reduce noise spikes, ringing and IR drop that produce voltage errors.
4. The grounds of the IC capacitors should be connected as close together directly to a ground plane. It is also recommended to have a ground plane on both sides of the PCB, as it reduces noise by reducing ground loop.
5. The loop inductance per capacitor shall not exceed 3nH (both on VCC/VCCQ and VSS/VSSQ loops).
6. Cin2 shall be placed closer (from both a distance and inductance POV) to the iNAND power and ground balls.
7. Multiple via connections are recommended per each capacitor pad. It is recommended to place the power and ground vias of the capacitor as close to each other as possible.
8. On test platforms, where the iNAND socket is in use, the loop inductance per capacitor shall not exceed 5nH (both on VCC/VCCQ and VSS/VSSQ loop).
9. No passives should be placed below the iNAND device (between iNAND & PCB).
10. VSF balls (VSF1/4) should have exposed and floated test pads on the PCB, with near exposed GND for better measurement.

5.3.2 Signal Traces

1. Data, CMD, CLK and RCLK bus trace length mismatch should be minimal (up to ±1mm).
2. Traces should be 45-55 Ohm controlled impedance.

5.4 Reference Schematics

Figure 5-2. e.MMC Reference Schematics

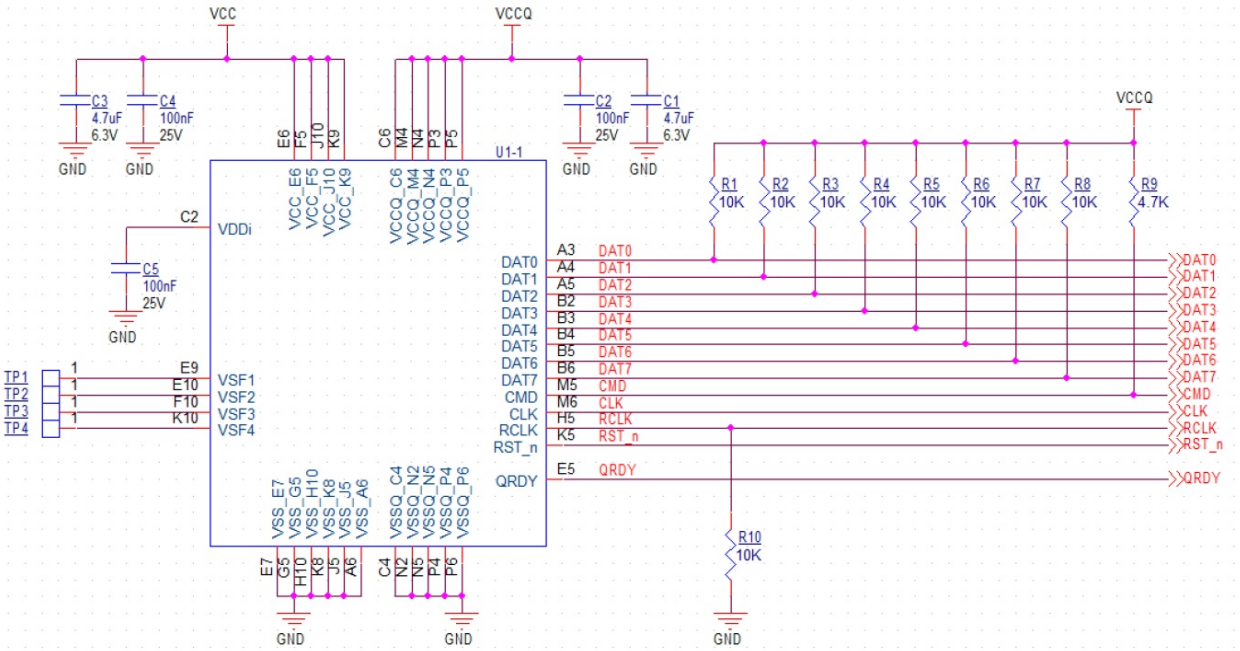


Table 5-2. Pull-up Resistor Definitions

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for DAT0–7	R_{DAT}	10	—	100[1]	Kohm	To prevent bus floating.
Pull-up resistance for CMD	R_{CMD}	4.7	—	100	Kohm	To prevent bus floating.
Pull-down resistance for Data Strobe (RCLK)	R_{PD}	10	—	47	Kohm	At HS400 mode

[1] *Recommended maximum pull-up is 50Kohm for 1.8V interface supply voltages. A 3V part may use the whole range up to 100 Kohms.*

5.5 Recommended Capacitors

Table 5-3. Recommended Capacitors

Capacitor Value	Manufacturer	Manufacturer Part Number
4.7µF	MURATA	GRM185R60J475ME15D
	TAIYO YUDEN	JMK107BJ475MK-T
0.1µF	MURATA	GRM155R71A104KA01D
	KYOCERA	CM05X5R104K06AH
2.2µF	PANASONIC	ECJ0EB0J225M
	SAMSUNG	CL05A225MQ5NSNC

6.0 Propriety iNAND Feature Overview

6.1 Device Report

The Device Report feature indicates the firmware and device status.

- Enabling Device Report Mode: Send CMD62 with argument of 0x96C9D71C - R1b Response will be returned.
- Reading Device Report Data: Once the host enters Device Report mode, CMD63 with argument 0x00000000 will retrieve the report - 512 Bytes will be returned to the host (*Note*: CMD63 behaves similarly to CMD17).
- Resume Normal Operation Mode: Once the Device Report read command (CMD63) is completed, the device automatically exits Device Report mode, and resumes normal operation mode.

6.1.1 Device Report Fields

Table 6-1. Device Report Fields

Byte Offset	Size (Bytes)	Field	Comments
[3:0]	4	Avg Erase Count System	Average erase value across all system blocks.
[7:4]	4	Avg Erase Count SLC	Average erase value across all SLC blocks.
[11:8]	4	Avg Erase Count MLC	Average erase value across all MLC blocks.
[15:12]	4	Read Reclaim Count System	Number of reads of system data which passed read-scrub thresholds and require reclaim.
[19:16]	4	Reserved	
[23:20]	4	Read Reclaim Count MLC	Number of MLC reads which passed read-scrub thresholds and require reclaim.
[27:24]	4	Bad Block Manufacturer	Total bad blocks detected during manufacturing process.
[31:28]	4	Bad Block Runtime System	Total bad blocks in system partitions detected during run-time.
[35:32]	4	Reserved	
[39:36]	4	Bad Block Runtime MLC	Total bad blocks in MLC partition detected during run-time.
[43:40]	4	Patch Trial Count	Number of secure field firmware updates (sFFU) done from the beginning of the device life.
[55:44]	12	Patch Release Date	Current sFFU Release Date
[63:56]	8	Patch Release Time	Current sFFU Release Hour
[67:64]	4	Cumulative Write Data Size In 100MB	Total bytes written from the host in multiples of 100MB.

Table 6-1. Device Report Fields (Continued)

Byte Offset	Size (Bytes)	Field	Comments
[71:68]	4	VCC Voltage Drop Occurrences	Number of ungraceful power downs to the device. The counter may be inaccurate due to uncommitted counter updates during repeated voltage drops.
[75:72]	4	VCC Voltage Droop Occurrences	Number of power-droops (slight power-droop below a threshold and for a very short time).
[79:76]	4	Failures to Recover New Host Data After Power Loss	Counts times the new host data is discarded due to power loss.
[83:80]	4	Recovery Operations After Voltage Droop	Number of recovery operations done by the device while power-droop detected.
[511:84]	428	Reserved	

6.1.2 Power-Loss Indications

The device will notify the host of any power-loss events and of the internal management of those events. A dedicated field in the EXT_CSD register is allocated to indicate the occurrence of Power Loss/Write Abort during the last power down. This field reports if a power loss was detected and recovered during the last power-up.

To retrieve this field, the host should issue the CMD8 command of SEND_EXT_CSD. This command returns full EXT_CSD structure: 512 bytes as block of data. The details of the EXT_CSD are shown in Table 6-2:

Table 6-2. Power-Loss Indications

Name	Field	Size (Bytes)	Cell Type	Hexadecimal Offset	Decimal Offset
Power Loss Indication	POWER_LOSS_REPORT	1	R	0x79	121

POWER_LOSS_REPORT[121] details:

- Bit[2]: RECOVERY_SUCCESS
  0x1: Recovery passed successfully
  0x0: Recovery failed
- Bit[1]: RECOVER_OLD_DATA
  0x1: Recovery to old copy of data
  0x0: No data recovery required
- Bit[0]: POWER_LOSS_DETECTED
  0x1: Unexpected Power Loss was detected - Detection is done during initialization, immediately after Power-Up

Note: In case Power Loss did not occur on last shut down, this register will show 0x00.

6.1.3 Unstable Power-Supply Indications

In the event of a flash voltage drop, the device may not be able to recover the data that was already transferred to the device, but was not yet committed in the flash; the device will "abort" the current host write and return an error indication to the host.

The device uses BIT19 and BIT20 (cc_error) in the command response to indicate a VDET error status to the host. The VDET error indication can only be returned if CMD13 was issued, or in the next command response.

Examples:

- Open Mode (CMD25+CMD12+CMD13):

  In both cases, where the voltage droop occurs before or after CMD12:
  - CMD12 response will not have BIT19 and BIT20 set.
  - CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response.

  Note: The host may send multiple CMD13 and the BIT19 will be set only in first CMD13 after releasing the busy.

- Close Mode (CMD23+CMD25+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response.
- Single Block Mode (CMD24+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response.

The host shall retry latest command provided that the VDET error indication on CMD13 response (or next command response (BIT19 and BIT20 are set) is still set.

7.0 Unified Boot

Unified Boot is a proprietary feature that allows the host to boot from a secondary boot partition without the need to explicitly switch to the secondary partition. When this feature is enabled, the device will transfer the data from both boot partitions to the host, first from the enabled boot partition followed by the other partition.

A typical use case is to guarantee a version of the boot will always be valid in case of Over The Air (OTA) boot update. The host can set one boot partition as permanent write protect (never to be changed) and the other as temporary write protect. The second boot will be used for update. In case OTA is corrupted or fail, host will always be able to boot based on the previous version saved in boot one.

Note: This feature is only supported on FW version CS2.2.

7.1 Unified Boot Support Indication

Table 7-1. Unified Boot Support Indication

EXT_CSD Field Name	Bit(s)	Value	Description
UNI_BOOT_PROC_SUPPORT[93]	[0] Read Only	0x0	Device does not support Unified Boot.
		0x1	Device supports Unified Boot.

7.2 Enable Unified Boot

Table 7-2. Enable Unified Boot

EXT_CSD Field Name	Bit(s)	Value	Description
UNI_BOOT_PROC_ENABLE[92]	[0-7] R/W	0x0	Unified Boot is disabled.
		0x1	Unified Boot is enabled.

7.3 Important Considerations

The configuration of Unified Boot can only be performed once at the beginning of life of a device, before any data is transferred to it. After all the parameters have been specified and committed to the device, it cannot be changed.

NOTE:

- This functionality is disabled if either of the boot partitions have ever been write protected.
- The amount of data transferred for each partition is equal to the partition size, regardless of the size of the programmed image.

7.4 Hardware Pin Secure Boot

Hardware Pin Secure Boot is a physical authentication procedure requiring the use of VSF Pin #4 as a verification of the device controller to authorize the writing to a boot partition.

As per the JEDEC e.MMC 5.1 specification, e.MMC boot partitions have three write protection methods:

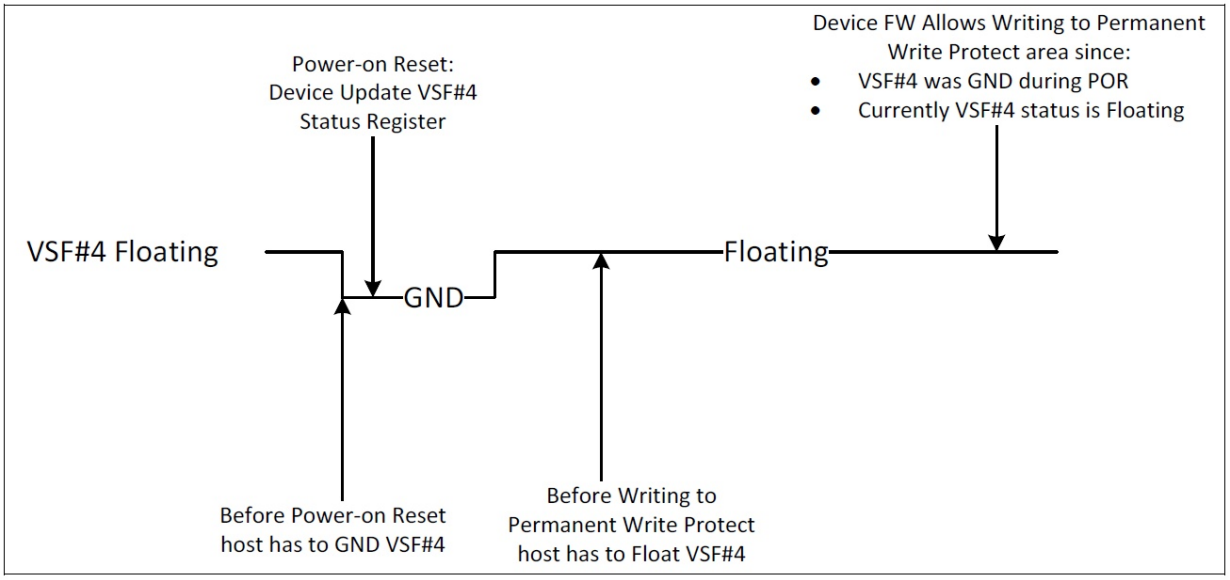
1. Permanent Write Protection: once set, boot data cannot be written.
2. Power-on Write Protection: once set, boot data cannot be written until a device reset.
3. Secure Write Protection: host may set/clear write protection using a secure key.

The Hardware Pin Secure Boot option implements a fourth method that works with a permanently write protected boot partition.

The physical authentication requires the host to keep VSF Pin #4 at ground voltage level and restore it to floating state after the device power-up sequence is complete. This procedure would authorize the user to write to the permanently protected boot partition. Upon reset of the device, the authorization to update the boot partition would be aborted and permanent write protection is restored upon reset of the device.

The host can implement this feature by enabling a push button switch on the platform that would generate the signal as shown in Figure 7-1.

Figure 7-1. Power-on Sequence



Note: This feature is only supported on FW version CS2.2.

7.4.1 Requirements

This feature is designed only for the boot partitions. It works only in addition to boot partition permanent write protection. It will not work with power-on write protection of the boot partitions nor will it work with whole device permanent or temporary write protection.

7.4.2 Physical Proof Protocol Support Indication

Table 7-3. Physical Proof Protocol Support Indication

EXT_CSD Field Name	Bit(s)	Value	Description
PPP_FEATURES_SUPPORT[123]	[0] Read Only	0x0	Device does not support HW pin.
		0x1	Device supports HW pin.

7.4.3 Enable Physical Proof Protocol

Table 7-4. Enable Physical Proof Protocol

EXT_CSD Field Name	Bit(s)	Value	Description
PPP_FEATURES_ENABLE[122]	[0] R/W	0x0	PPP features are disabled.
		0x1	PPP features are enabled.

7.4.4 Configuration Process

NOTE: This feature must be enabled BEFORE setting permanent write protection on the boot partitions.

Use the following steps:

1. Check PPP_FEATURES_SUPPORT bit 0 to determine that this feature is supported.
2. Set PPP_FEATURES_ENABLE bit 0 to 1 to indicate PPP features will be used.
3. Set permanent write protection of the boot partitions (BOOT_WP[173] = 0x04).

7.4.5 Authentication Process

NOTE: Once authenticated, the boot partitions are write enabled until the next POR.

The following must occur during the authentication process:

1. The host must set VSF #4 to GND before, during and for at least two (2) seconds after POR.
2. The host must return VSF #4 to floating state.
3. If the device has determined that all the proper authentication criteria have been met, the host may now write to the protected boot partitions.

8.0 Automatic Refresh

The device has an automatic background scan feature that recognizes early signs of degradation and refreshes the block before any chance of failure. Physical phenomena exist in the NAND that over time can cause read errors. There are three phenomena that need to be addressed:

- **Read Disturb**: This error occurs when reading from NAND flash memory affects nearby cells in the same block.
- **Hot Spot**: Each cell has a useful read life known as its endurance. Repeatedly reading from the same cell can eventually result in errors.
- **Cold Spot**: If a cell is not accessed for a very long time, the data in it could eventually degrade. This amount of time for which a cell can reliably maintain the correct information is referred to as its retention period.

8.1 Mechanism

The automatic read refresh algorithms include three types of scans: Passive, Active and Random, which identify pages affected by a high BER (Bit Error Rate). The algorithms are designed to maximize data integrity with minimal impact on performance.

The BER threshold is much lower than the ECC (Error Correction Capabilities) of the device, guaranteeing the reliability of the metadata before it can become an UECC (Uncorrectable Error Correction Capabilities) condition.

8.1.1 Passive Scan

The Passive Scan protects against read endurance errors. It checks the BER at the time of every read, identifying blocks that have exceeded the BER threshold.

8.1.2 Active Scan

The Active Scan protects against data retention errors. It scans blocks across the entire device during background operations, and in some cases, during writes, checking the BER on each block, identifying those that have exceeded the threshold.

8.1.3 Random Scan

The Random Scan protects against read disturb errors. It scans blocks in nearby pages during background operations (and in some cases during writes), checking the BER on each block and flagging those blocks that have exceeded the threshold.

8.2 Registration

When any type of scan finds a block that violates the BER threshold, it is added to the relocation list with a high priority, indicating that it is critical to relocate the block, as opposed to a block that needs relocation due to standard activities such as wear-leveling.

8.3 Correction

At appropriate times determined by the system to avoid any impact on performance, all blocks marked as high priority for relocation, followed by any standard priority blocks are reclaimed.

8.4 BKOPs and PON

For any refresh activity to occur (automatic or manual):

- Background operations must be enabled
- Power-off notification (EXT_CSD POWER_OFF_NOTIFICATION[34]) must be used.

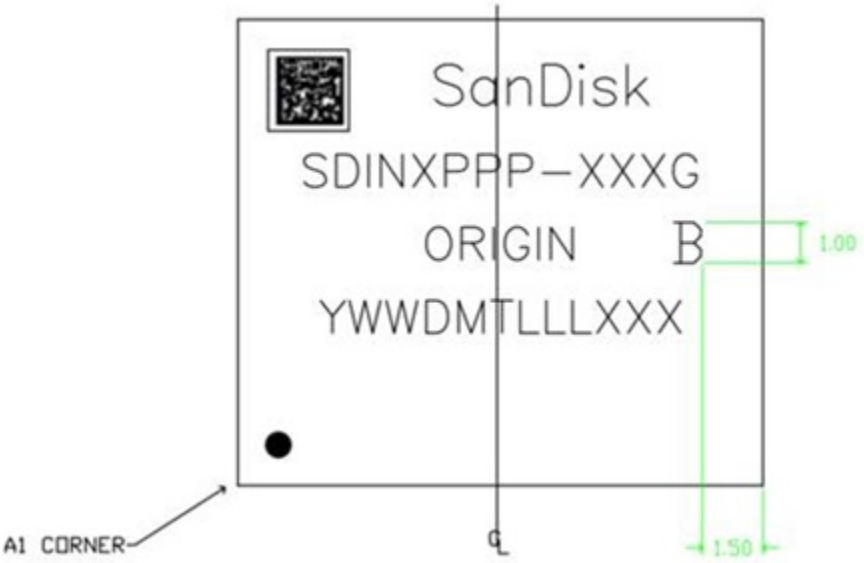
9.0 Product Marking

Table 9-1 lists the position of each element that appears on the label, and Figure 9-1 shows the relative position of each element.

Table 9-1. Product Marking Elements

Row	Description
1	Simplified Logo 2D Barcode: A 12-digit unique ID that reflects the "Sales Item Part Number".
2	Sales Item Part Number
3	Country of Origin, e.g., "TAIWAN" or "CHINA" *No ES marking for product in mass production.
4	■ Y - Last digit of year ■ WW - Work Week ■ D - A day within the week. ■ MTLLLXXX - Internal Use

Figure 9-1. Product Marking 8GB



10.0 Ordering Information

Table 10-1. Ordering Information (-25°C to +85°C Ambient)

Capacity	Technology	Part Number	Samples Part Number	Package	e.MMC
8GB	15nm X2 eMLC	SDINBDG4-8G-B	SDINBDG4-8G-B	11.5x13x0.8mm	5.1

11.0 Product Name Change

This section describes the product name change from SanDisk to Western Digital.

Description of Change

- Update company logo to Western Digital in collateral and marketing materials. No impact on product marking.
- Retain iNAND as the product brand for embedded flash drives.
- Assign each letter of the new taxonomy with its unique identification.

Figure 11-1. SanDisk to Western Digital

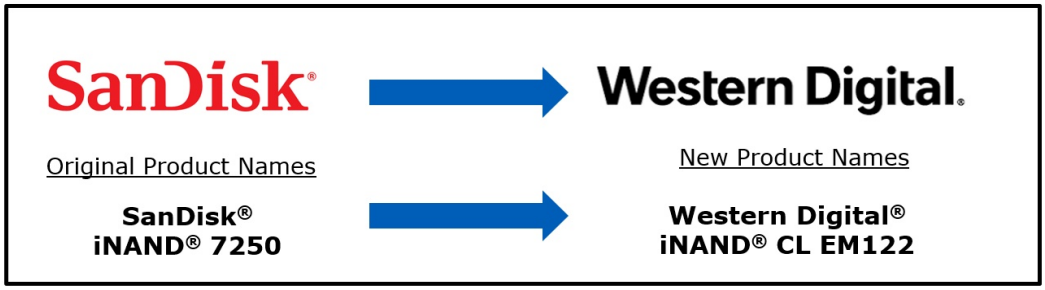
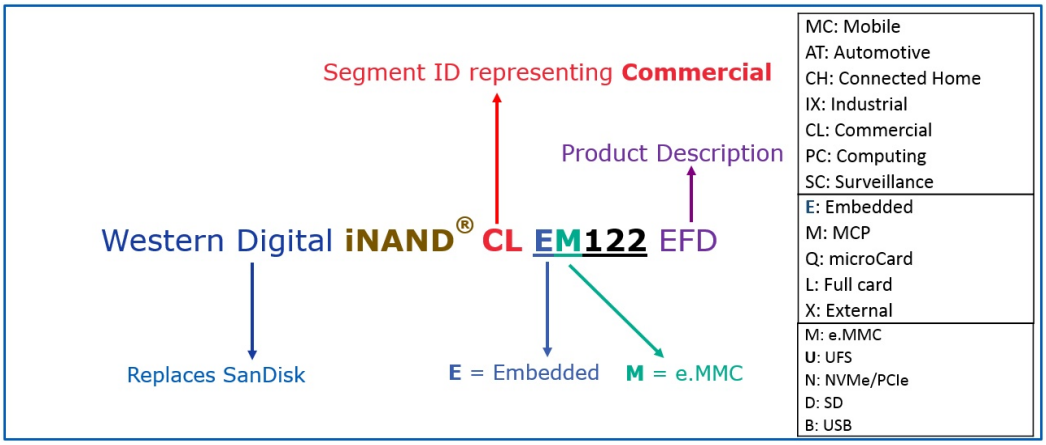


Figure 11-2. Decoding New Naming Structure



Important Exceptions

- No impact on currently shipping or qualified products
- No change to part number/SKU systems
- SanDisk, WD, and HGST part numbers and ordering system are unchanged

If you have any questions or require further assistance, contact oemproducts@wdc.com for support.

12.0 Contact Information

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