DATA SHEET

AL7230 2.4/5GHz RF Transceiver

Single Chip Transceiver for 802.11abg Applications

Datasheet

Airoha Technology Corp.

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1 Features

- Fully integrated, 2.4/5 GHz dual-band transceiver
- Receiver with 37/32dB RF selectable gain range and 60dB baseband variable gain range
- Analog RSSI output with 60dB dynamic range
- Integrated baseband filters with programmable bandwidth for Transmit and Receive
- Three-wire interface for transceiver control
- Integrate PA with 20dBm output power for 11b, 17dBm for 11g, and 15dBm for 11a
- Integrate RF detector and temperature sensor for APC
- Integrated PLL with on-chip loop filter
- Single-ended LNA input without the need of external balun
- On-chip DC offset correction
- Embedded IQ mismatch calibration
- Small QFPN-56 package (8mm×8mm)

2 Description

AL7230 is a highly integrated RF transceiver IC for 2.4 GHz and 5 GHz dual-band 802.11a/b/g applications, and combines all functions of the transceiver in a single chip. AL7230 also integrates on-chip PA and PLL with embedded loop filter to help you to minimize the use of external components to design an RF subsystem.

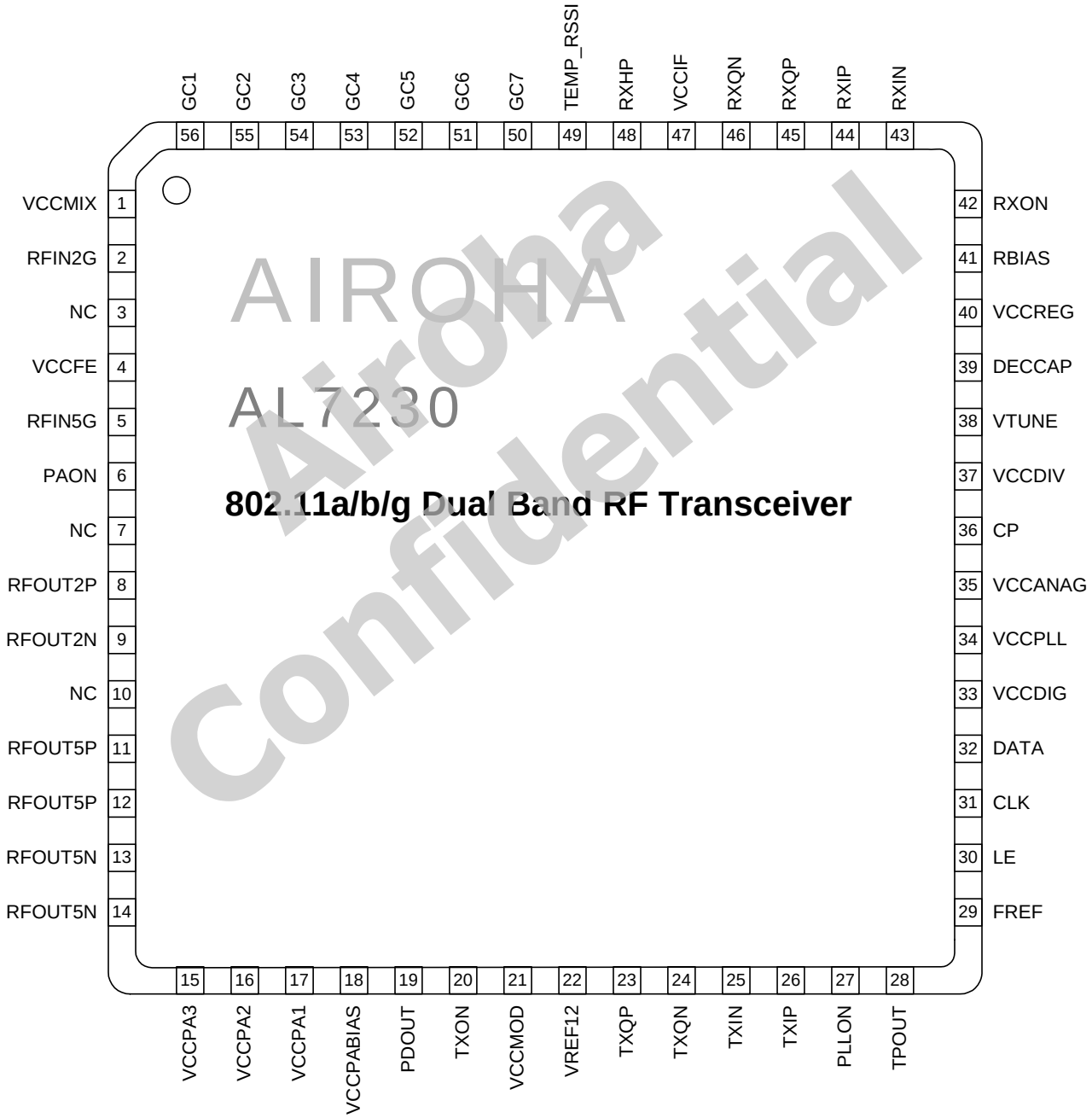
The receive path includes two single-ended input Low Noise Amplifiers (LNA) and down-conversion mixers with DC-offset cancellation for both 2.4GHz and 5GHz band, and a variable gain amplifier with a baseband low-pass filter without the need of external SAW filters.

The transmitter consists of a up-conversion quadrature modulator with a baseband low pass filter, a variable gain amplifier, and two power amplifiers with power detector and temperature sensor to complete the whole transmit path function for both 2.4GHz and 5GHz band.

A power-on calibration procedure is established to correct the TX DC offset, filters mismatch and phase imbalance.

These functions are housed in a 56-pin QFPN package.

3 Pin Assignment



4 Block Description

4.1 General Description

The AL7230 is a 2.4/5GHz dual-band transceiver for 802.11a/b/g applications. There are five main blocks – power amplifier, transmitter, receiver, synthesizer and three-wire interface.

The control pins: PLLON, TXON, RXON and PAON are responsible for the power control of the chip. The whole chip is powered up when PLLON is set to High, and the synthesizer is enabled at the same time. After the chip powered-up, the transmitter or receiver block is enabled when TXON or RXON set to High, respectively. The PA block is controlled by the PAON independently, irrelative to the state of PLLON.

4.2 Receiver

The receiver is composed with two parts: RF front-end and baseband. The RF front-end part comprises two independent sets, one for 2.4GHz and the other for 5GHz. The baseband part comprises a low-pass filter (LPF) for channel filtering, a variable gain amplifier (VGA) and a RSSI log amplifier for RSSI output.

At the RF front-end part, the LNA inputs for both 2.4GHz and 5GHz are single-ended without the need of external balun. The front-end gain could be adjusted through control pins or 3-wire interface, and thus reduce the probability of bit errors caused by poor signal-to-noise ratio.

At the baseband part, the down-converted baseband signal is first low-pass filtered by the LPF, and then amplified by the VGA. The 3dB bandwidth of the LPF could be set from 7.5MHz to 20MHz through 3-wire interface. No external SAW filter is needed.

The VGA provides variable gain with 60dB dynamic range, and could be controlled through control pins or 3-wire interface.

The RSSI log amplifier measures the received signal strength and converts to a voltage signal RSSI output. The dynamic range of RSSI is 60dB. The output range is selectable for

HIGH range (max. output voltage 2.0V) and LOW range (max. output voltage 1.5V).

The Rx I/Q output are designed to be directly connected (DC-coupled) to I/Q ADC inputs of the baseband IC. The common voltage of RX I/Q outputs is 1.2V.

4.3 Transmitter

The transmitter comprises a LPF, a modulator and a VGA stage. The Tx baseband I/Q interface is designed as differential analog inputs directly connected (DC-coupled) to the I/Q DAC outputs of the baseband IC.

A LPF is implemented to attenuate the second sidelobe of signal spectrum and unwanted oversampling clock or spurious signals. The 3dB bandwidth of the LPF could be set from 12MHz to 30MHz through 3-wire interface.

The VGA provides variable gain with 30dB dynamic range, and could be controlled through control pins or 3-wire interface.

4.4 PA

There are two internal PA for 2.4GHz and 5GHz operation modes, respectively. The gain of the power amplifier can be adjusted via bias current, which is controlled through 3-wire interface. Output power is 20dBm for 11b CCK, 17dBm for 11g OFDM and 15dBm for 11a OFDM.

An on-chip power detector is integrated to measure the output power strength. Power detector samples the peak voltage of the output power and generates a voltage proportional to the output power. An on-chip temperature sensor is also integrated to measure the temperature of the chip.

4.5 Synthesizer

The AL7230 includes a fractional-N synthesizer with an embedded loop filter. The reference frequency is fed from an external 20/40MHz oscillator.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

AL7230 could be damaged by any stress in excess of the absolute maximum ratings listed below.

ITEM	MIN.	MAX.
Power supply voltage (Vcc)	-0.3V	3.6V
Pin voltage	-0.3V	3.6V
Maximum power dissipation	-	2W
Operating temperature	-40°C	+85°C
Storage temperature	-65°C	+150°C
LNA input level	-	+10 dBm
PA output load mismatch	-	10:1

5.2 DC Electrical Specifications

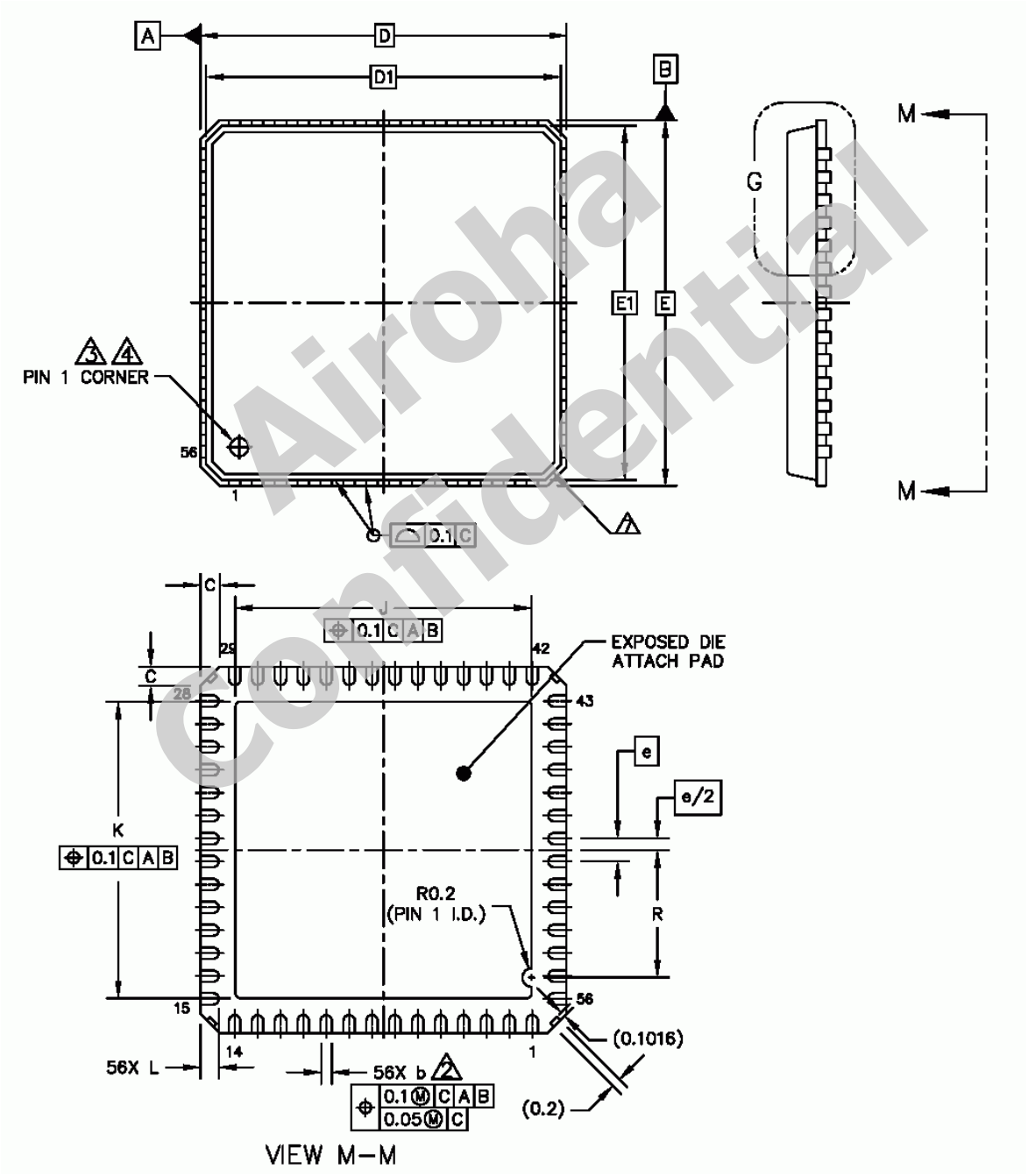
Typical values are at VCC=3.3V(PA)/ 2.8V(TRX), Ta=25°C unless otherwise specified

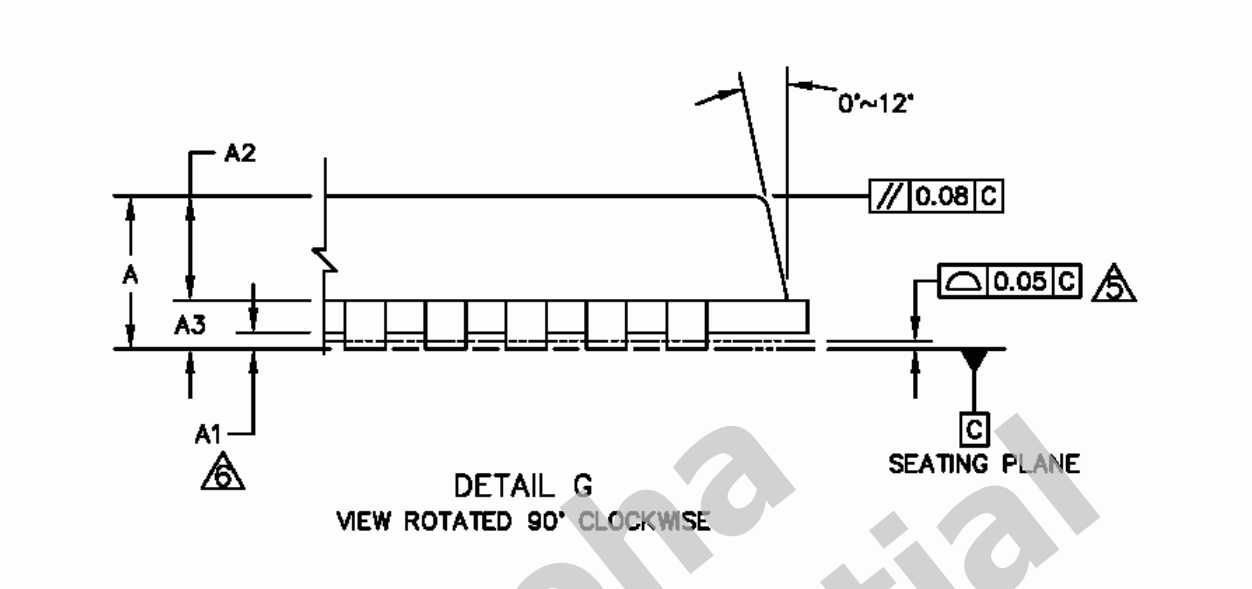
Item	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Power Amplifier	3	3.3	3.6	V
	Transceiver (V_{DD})		2.8		
Digital input voltage	Logic High (V_{IH})	$0.7V_{DD}$			V
	Logic Low (V_{IL})	-		$0.3V_{DD}$	
Shut down current	PLLON=L, PD =1		5*		μA
	PLLON=L, PD =0		500		
Standby current	Low band, PLLON=H		56		mA
	High band, PLLON=H		83		
Rx current	Low band, PLLON=RXON=H		92		mA
	High band, PLLON=RXON=H		140		
Tx current	Low band, PLLON=TXON=H		103		mA
	High band, PLLON=TXON=H		168		
	Low band, PLLON=TXON=PAON=H		267/291**		
	High band, PLLON=TXON=PAON=H		315***		

Note*: About 1ms recovery time is required when PD is set from 1 back to 0.
Note**: 267mA under Pout 17dBm OFDM mode, 291mA under Pout 20dBm CCK mode at Balun out.
Note***: 315mA under Pout 15dBm OFDM mode at Balun out.

6 Package Dimensions

PUNCH QFN 56LD
8x8x0.9 PKG 0.5 PITCH POD





DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		8 BSC	
D1		7.75 BSC	
E		8 BSC	
E1		7.75 BSC	
e		0.5 BSC	
J	6.37	6.47	6.57
K	6.37	6.47	6.57
L	0.3	0.4	0.5
R	2.685	2.785	2.885

NOTES

1. DIE THICKNESS ALLLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
6. APPLIED ONLY TO TERMINALS.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.