

General Description

The WST2319 is the highest performance trench P-ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WST2319 meet the RoHS and Green Product requirement,100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

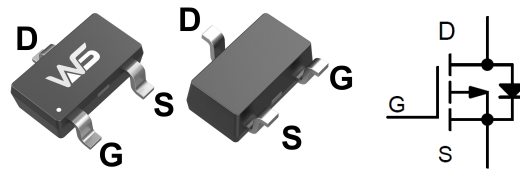
Product Summary

BVDSS	RDSON	ID
-40V	35mΩ	-6A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter.
- Networking DC-DC Power System
- Load Switch

SOT-23-3L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-6.0	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-4.5	A
I_{DM}	Pulsed Drain Current ²	-24	A
EAS	Single Pulse Avalanche Energy ³	12	mJ
I_{AS}	Avalanche Current	-7	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	1.4	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	125	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	36	$^\circ C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-40	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.03	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-3A	---	35	40	mΩ
		V _{GS} =-4.5V, I _D =-1A	---	40	58	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-0.8	-1.2	-2.2	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.56	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-28V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-28V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	15	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	3.8	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-18V, V _{GS} =-10V, I _D =-4A	---	9.5	---	nC
Q _{gs}	Gate-Source Charge		---	1.7	---	
Q _{gd}	Gate-Drain Charge		---	2.0	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =6Ω, I _D =-1A, R _L =15Ω	---	8	---	ns
T _r	Rise Time		---	10	---	
T _{d(off)}	Turn-Off Delay Time		---	18	---	
T _f	Fall Time		---	8	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	420	---	pF
C _{oss}	Output Capacitance		---	77	---	
C _{rss}	Reverse Transfer Capacitance		---	55	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =-25V, L=0.1mH, I _{AS} =-8A	10	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V, Force Current	---	---	-1.0	A
I _{SM}	Pulsed Source Current ^{2,6}		---	---	-16	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
3. The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-8A
4. The power dissipation is limited by 150°C junction temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

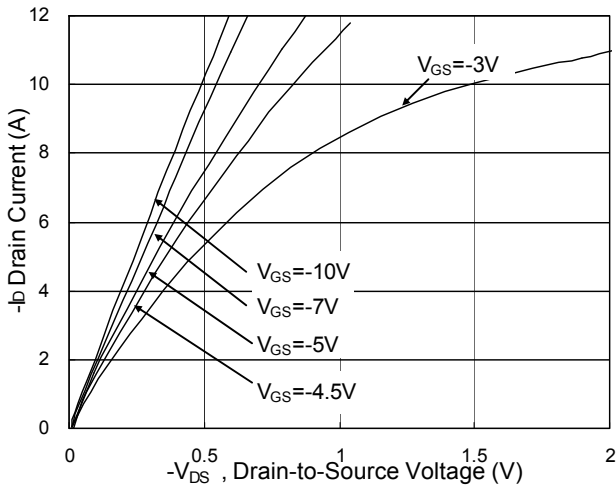


Fig.1 Typical Output Characteristics

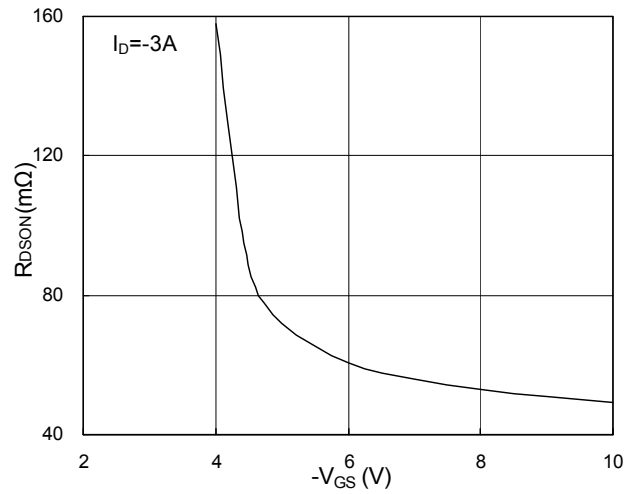


Fig.2 On-Resistance v.s Gate-Source

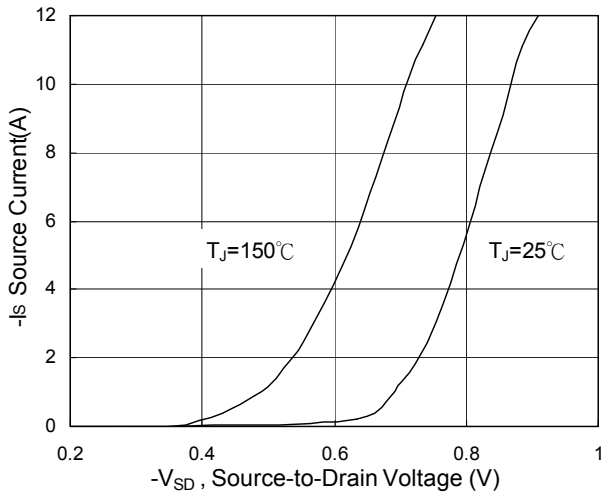


Fig.3 Forward Characteristics of Reverse

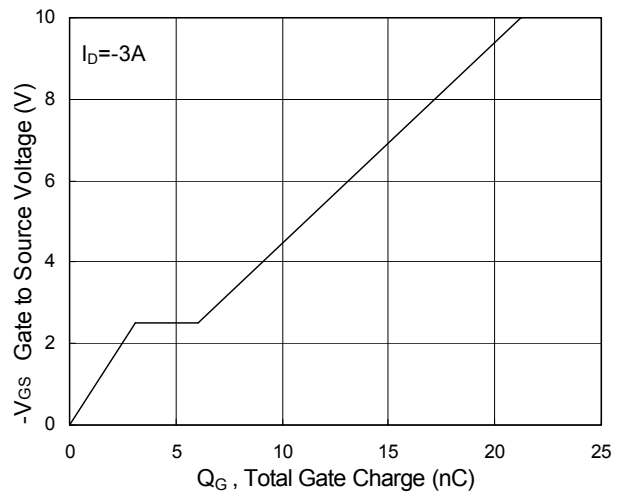


Fig.4 Gate-Charge Characteristics

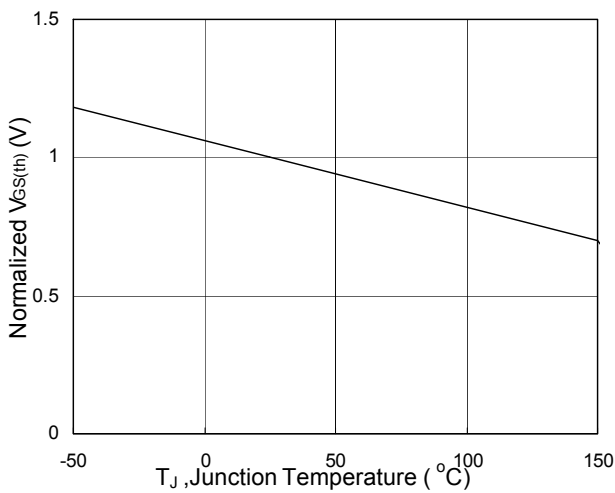


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

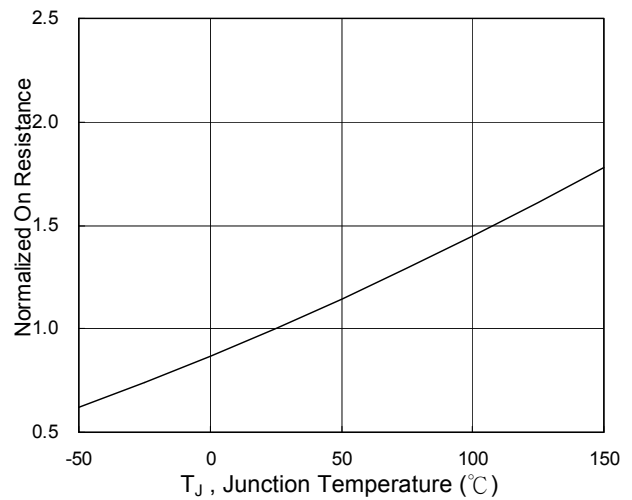


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

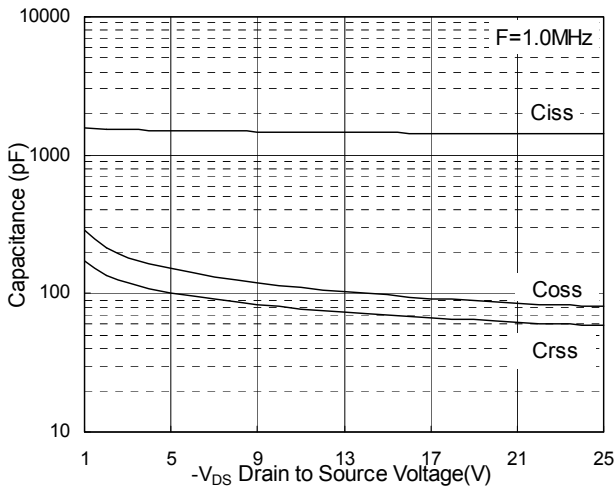


Fig.7 Capacitance

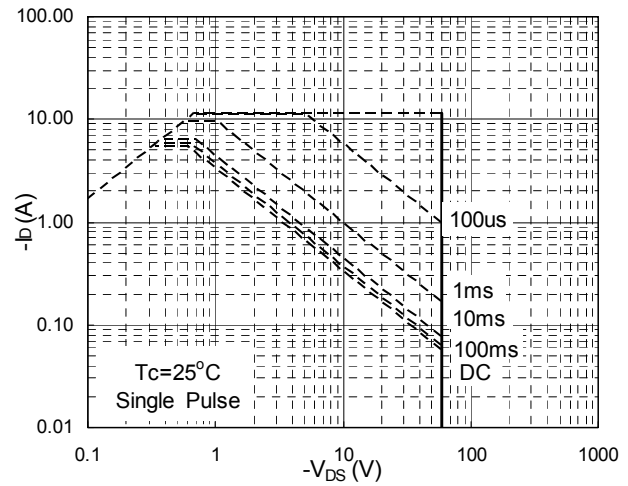


Fig.8 Safe Operating Area

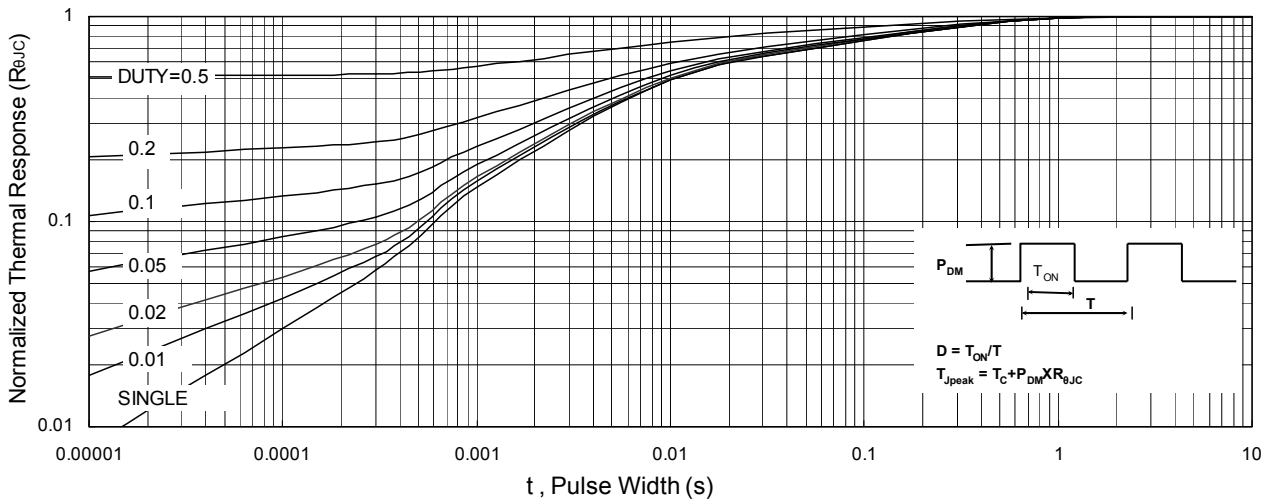


Fig.9 Normalized Maximum Transient Thermal Impedance

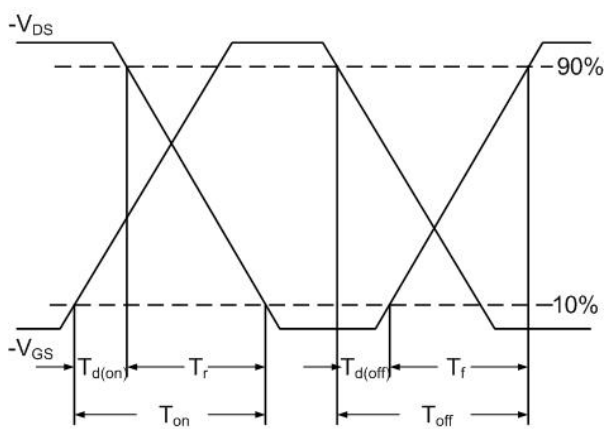


Fig.10 Switching Time Waveform

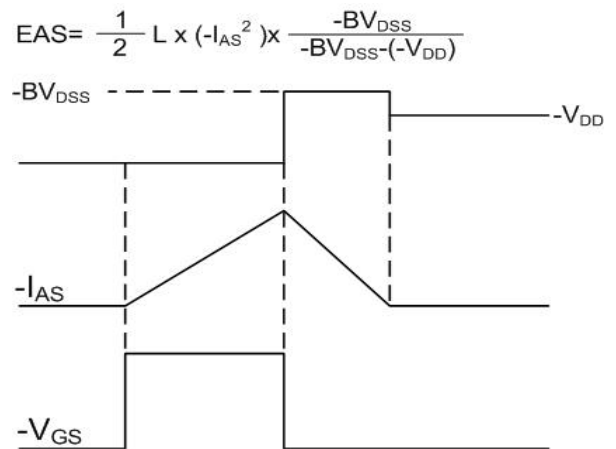


Fig.11 Unclamped Inductive Waveform



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