NSiP8940/ NSiP8941/ NSiP8942/ NSiP8943/ NSiP8944: Quad-Channel Digital Isolators with Integrated DC to DC Converter

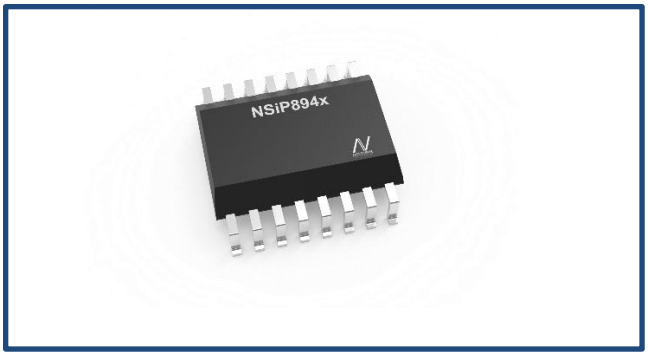
Datasheet (EN) 1.0

Product Overview

The NSiP894x devices are quad-channel digital isolators with integrated isolated DC-DC converter. The isolated DC-DC converter provide up to 500mW output power use on chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSiP894x device are safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSiP894x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The NSiP894x devices provide 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion mode, the output voltage can be set by SEL pin. The device can go into standby mode when the PDIS pin set to high, and there is no output voltage at VISO pin.

Key Features

- Up to 5000V$_{rms}$ Insulation voltage
- Power supply voltage: 3.3V to 5.5V
- 5V to 5V, 5V to 3.3V, support 100mA load current
- 3.3V to 3.3V, support 60mA load current
- Over current and over temperature protection
- Date rate: DC to 150Mbps
- High CMTI: 100kV/us
- Propagation delay: <15ns
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  SOIC-16 wide body



Safety Regulatory Approvals

- UL recognition: up to 5000V$_{rms}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation

Functional Block Diagrams

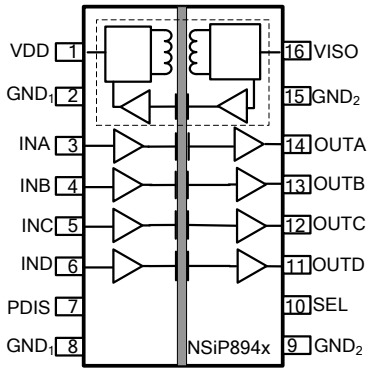


Figure 1. NSiP894x Block Diagram[1]

[1] The isolation channel direction can be either depend on different part number.

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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD	-0.5		6.5	V	
Maximum Input Voltage	V_{INA}, V_{INB} V_{INC}, V_{IND}	-0.4		VDD+0.4 V_{ISO}+0.4	V	
Maximum Output Voltage	V_{OUTA}, V_{OUTB} V_{OUTC}, V_{OUTD}	-0.4		VDD+0.4 V_{ISO}+0.4	V	
Common-Mode Transients	CMTI	±100		±150	kV/us	
Output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{STEST}			10	kV	
Operating Temperature	Topr	-40		125	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

2.0 SPECIFICATIONS

2.1. ISOLATED DC/DC CONVERTER STATIC SPECIFICATIONS

(VDD=4.5V~5.5V, VISO=5V, Ta=-40℃ to 125℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Isolated Supply Voltage	V_{ISO}	4.75	5	5.25	V	
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	
Load Regulation	$V_{ISO(LOAD)}$		0.2	0.5	%	
Output Ripple	$V_{ISO(RIP)}$		35		mVpp	
Output Noise	$V_{ISO(NOISE)}$		230		mVpp	
Efficiency at maximum load current	EFF	45			%	
Output supply current	I_{ISO}	100			mA	
VDD supply current without digital isolator	I_{VDD_POWER}		10		mA	No VISO Load
				215	mA	Full VISO Load (I_{ISO}=100mA)
Thermal Shutdown Temperature			165		℃	

(VDD=4.5V~5.5V, VISO=3.3V, Ta=-40℃ to 125℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*

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Isolated Supply Voltage	V_{ISO}	3.135	3.3	3.465	V	
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	
Load Regulation	$V_{ISO(LOAD)}$		0.2	0.5	%	
Output Ripple	$V_{ISO(RIP)}$		35		mVpp	
Output Noise	$V_{ISO(NOISE)}$		150		mVpp	
Efficiency at maximum load current	EFF	40			%	
Output supply current	I_{ISO}	100			mA	
VDD supply current without digital isolator	I_{VDD_POWER}		8		mA	No VISO Load
				93	mA	Full VISO Load (I_{ISO}=100mA)
Thermal Shutdown Temperature			165		℃	

(VDD=3V~3.6V, VISO=3.3V, Ta=-40℃ to 125℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Isolated Supply Voltage	V_{ISO}	3.135	3.3	3.465	V	
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	
Load Regulation	$V_{ISO(LOAD)}$		0.1	0.5	%	
Output Ripple	$V_{ISO(RIP)}$		25		mVpp	
Output Noise	$V_{ISO(NOISE)}$		130		mVpp	
Efficiency at maximum load current	EFF	45			%	
Output supply current	I_{ISO}	60			mA	
VDD supply current without digital isolator	I_{VDD_POWER}		10		mA	No VISO Load
				132	mA	Full VISO Load (I_{ISO}=60mA)
Thermal Shutdown Temperature			165		℃	

2.2 DIGITAL ISOLATOR ELECTRICAL CHARACTERISTICS

(VDD=4.5V~5.5V, VISO=5V, Ta=-40℃ to 125℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDDPOR		2.5		V	POR threshold as during power-up
	VDD HYS		0.2		V	POR threshold Hysteresis
High Level Input Voltage	VIH	0.7*VDD			V	

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Low Level Input Voltage	VIL			0.3*VDD	V	
High Level Output Voltage	VOH	VDD-0.4			V	IOH ≤ 4mA
Low Level Output Voltage	VOL			0.4	V	IOL ≤ 4mA
Output Impedance	Rout		50		ohm	
Input Pull high or low Current	Ipull		8	15	uA	
Common Mode Transient Immunity	CMTI	100	150		kV/us	

(VDD=4.5V~5.5V, VISO=5V, Ta=-40℃ to 125℃.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSiP8940					
	I_{DD}(Q0)		11.42		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(Q1)		13.77		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(1M)		13.28		mA	All Input with 1Mbps, C_L=15pF
	NSiP8941					
	I_{DD}(Q0)		10.56		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(Q1)		14.61		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(1M)		13.15		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	NSiP8942					
	I_{DD}(Q0)		9.69		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(Q1)		15.45		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(1M)		13.02		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	NSiP8943					
	I_{DD}(Q0)		8.83		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(Q1)		16.29		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1

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	I_{DD}(1M)		12.9		mA	All Input with 1Mbps, C_L=15pF
	NSiP8944					
	I_{DD}(Q0)		7.97		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(Q1)		17.13		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(1M)		12.77		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	5	9.0	15	ns	
	t_{PHL}	5	9.0	15	ns	
Pulse Width Distortion	PWD			5.0	ns	|t PHL – t PLH |
Rising Time	tr			5.0	ns	CL = 15pF
Falling Time	tf			5.0	ns	CL = 15pF
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

(VDD=4.5V~5.5V, VISO=3.3V, Ta=-40℃ to 125℃.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSiP8940					
	I_{DD}(Q0)		8.75		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(Q1)		11.06		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(1M)		10.22		mA	All Input with 1Mbps, C_L=15pF
	NSiP8941					
	I_{DD}(Q0)		8.22		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(Q1)		11.65		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(1M)		10.21		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	NSiP8942					

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	I_{DD}(Q0)		7.69		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(Q1)		12.25		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(1M)		10.20		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	NSiP8943					
	I_{DD}(Q0)		7.17		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(Q1)		12.84		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(1M)		10.19		mA	All Input with 1Mbps, C_L=15pF
	NSiP8944					
	I_{DD}(Q0)		6.64		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(Q1)		13.44		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(1M)		10.18		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	5	9.0	15	ns	
	t_{PHL}	5	9.0	15	ns	
Pulse Width Distortion	PWD			5.0	ns	|t PHL – t PLH |
Rising Time	tr			5.0	ns	CL = 15pF
Falling Time	tf			5.0	ns	CL = 15pF
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

(VDD=3V~3.6V, VISO=3.3V, Ta=-40℃ to 125℃.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSiP8940					
	I_{DD}(Q0)		10.64		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(Q1)		12.97		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1

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	I_{DD}(1M)		12.22		mA	All Input with 1Mbps, C_L=15pF
	NSiP8941					
	I_{DD}(Q0)		9.87		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(Q1)		13.73		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(1M)		12.16		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	NSiP8942					
	I_{DD}(Q0)		9.10		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(Q1)		14.48		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(1M)		12.11		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	NSiP8943					
	I_{DD}(Q0)		8.33		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
	I_{DD}(Q1)		15.24		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(1M)		12.05		mA	All Input with 1Mbps, C_L=15pF
	NSiP8944					
	I_{DD}(Q0)		7.56		mA	All Input at supply for NSiP8941x0 or All Input 0V for NSiP8941x1
	I_{DD}(Q1)		15.99		mA	All Input with 1Mbps, C_L=15pF
	I_{DD}(1M)		11.99		mA	All Input 0V for NSiP8941x0 or All Input at supply for NSiP8941x1
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	5	9.0	15	ns	
	t_{PHL}	5	9.0	15	ns	
Pulse Width Distortion	PWD			5.0	ns	|t PHL – t PLH |
Rising Time	tr			5.0	ns	CL = 15pF
Falling Time	tf			5.0	ns	CL = 15pF
Channel-to-Channel	t_{SK}(c2c)			2.5	ns	

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Delay Skew						
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

2.2. TYPICAL PERFORMANCE CHARACTERISTICS

2.3. PARAMETER MEASUREMENT INFORMATION

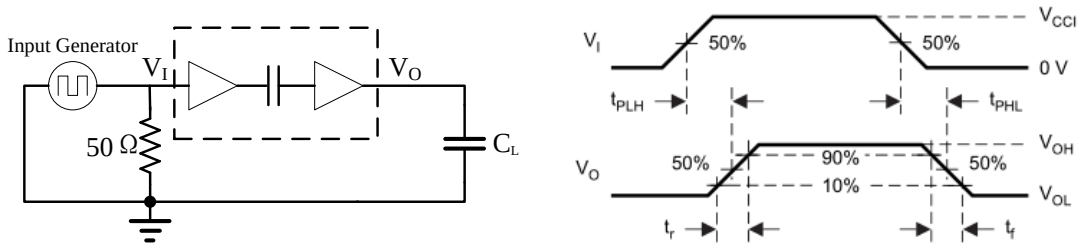

Figure 2.7 Switching Characteristics Test Circuit and Waveform

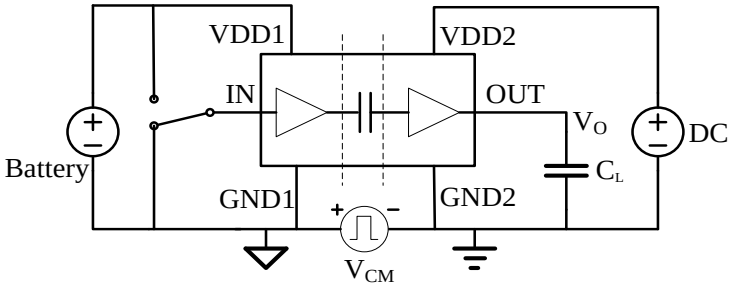

Figure 2.8 Common-Mode Transient Immunity Test Circuit

3.0 HIGH VOLTAGE FEATURE DESCRIPTION

3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	*Symbol*	*Value* *SOIC-16*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	L(I01)	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400	**V**	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		II		

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3.2. DIN VDE V 0884-11（VDE V 0884-11）:2017-01 INSULATION CHARATERISTICS

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
			SOIC-16	
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150V_{rms}			Ito IV	
For Rated Mains Voltage ≤ 300V_{rms}			Ito III	
For Rated Mains Voltage ≤ 400V_{rms}			Ito III	
Climatic Classification			10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage		VIORM	849	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1274	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1019	Vpeak
Maximum transient isolation voltage	t = 60 sec	VIOTM	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.3	VIOSM	6000	Vpeak
Isolation resistance	VIO =500V	RIO	$>10^9$	Ω
Isolation capacitance	f = 1MHz	CIO	0.8	pF
Input capacitance		CI	2	pF
Total Power Dissipation at 25℃		Ps	1.5	W
Safety input, output, or supply current	θJA = 84 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is	237	mA
Case Temperature		Ts	150	℃

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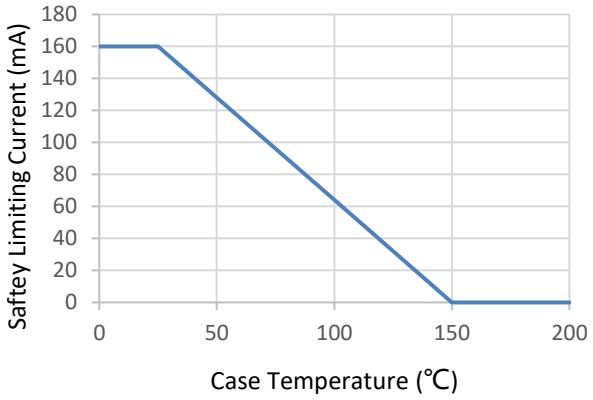

Figure 3.1 NSiP894x Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

3.3. REGULATORY INFORMATION

The NSiP894x are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Basic Insulation 849Vpeak, V_{IOSM}=5384Vpeak	Basic insulation at 780V_{rms} (1103Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

[1] In accordance with UL 1577, each NSiP894x is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 sec.

[2] In accordance with DIN VDE V 0884-11, each NSiP894x is proof tested by applying an insulation test voltage ≥ 1273 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

4.0 FUNCTION DESCRIPTION

The NSiP894x devices are quad-channel digital isolators with integrated isolated DC-DC converter. The digital isolators are based on Novosense capacity isolation barrier technique. The isolated DC-DC converter provide up to 500mW output power use on chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on capacity isolation technology. The NSiP894x device are safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSiP894x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The device can go into standby mode when the PDIS pin set to high, and there is no output voltage at VISO pin.

The high integrated solution can help to simplify system design and improve reliability. The NSiP894x devices are suitable for the limited PCB space applications. The devices are also suitable for wide temperature application which the most the power module can not support.

4.1. DEVICE FUNCTIONAL MODES

The NSiP894x devices provide 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion mode, the output voltage can be set by

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SEL pin. Supply configuration table showed below.

PDIS PIN	*SEL PIN*	*VDD*	*VISO*
Shorted to GND1 or floating	Shorted to VISO	5V	5V
Shorted to GND1 or floating	Shorted to GND2 or floating	5V	3.3V
Shorted to GND1 or floating	Shorted to GND2 or floating	3.3V	3.3V
Shorted to VDD1	X	3.3V/5V	0V

The NSiP894x devices provide four channel digital isolators. The digital isolators have default output status when VDDIN is unready and VDDOUT is ready as shown in below table.

Input	*VDDIN status*	*VDDOUT status*	*Output*	*Comment*
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSiP894xW0) H(NSiP894xW1)	The output follows the same status with the input within 60us after input side VDDIN is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDDOUT is powered on.

4.2. EMI CONSIDERATIONS

The NSiP894x devices are using on chip transformer, so the power transfer must operate at high frequency allow higher efficiency transfer using the small transformer. This will cause emissions which need to pay attention to PCB layout if the application allow low emission. Please see the application note if needed.

4.3. OUTPUT SHORT AND OVER TEMPERATURE PROTECTION

The NSiP894x devices are protected against output short. When the devices detect the output is short, the device will be in Hiccup mode and the transfer power will be limited. So the temperature of the device will be low, and the device is protected.

The NSiP894x devices are also protected against over temperature. When the devices detect the chip is over 165℃, the device will be shut down until the temperature of the device is below 145℃.

5.0 APPLICATION NOTE

5.1. TYPICAL APPLICATION

The NSiP894x requires a 0.1 μF and 10uF bypass capacitors between VDD and GND1, VISO and GND2. The capacitor should be placed as close as possible to the package. This is very important for the performance of the device. The figure5.1 is the basic schematic of NSiP894x and the figure5.2 is the typical isolated RS485 schematic using NSiP894x.

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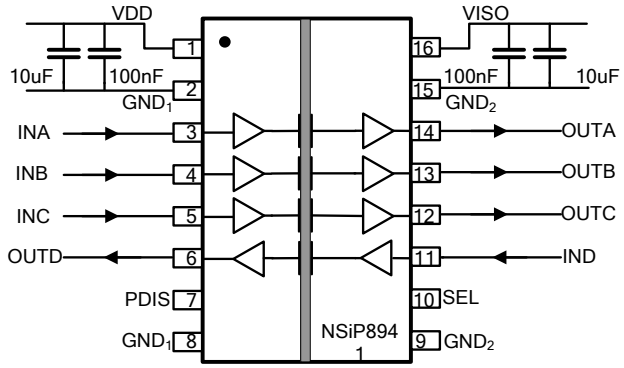

Figure5.1 Basic schematic of NSiP894x

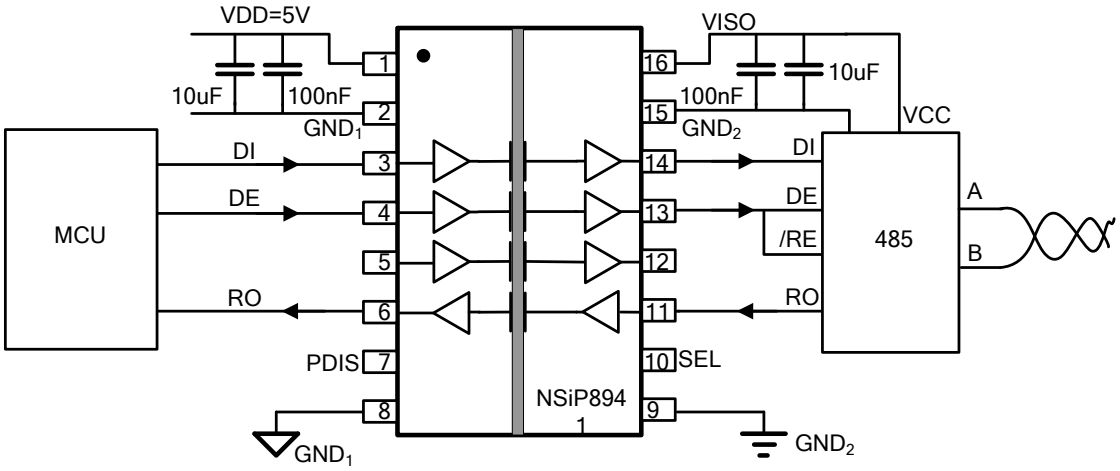

Figure5.2 Isolated RS485 schematic using NSiP894x

5.2. PCB LAYOUT

The recommended PCB layout shown below. The low ESR capacitor C1 should be closed to PIN1 and PIN2, the distance should be less than 1mm. The low ESR capacitor C3 should be closed to PIN15 and PIN16, the distance should be less than 1mm.

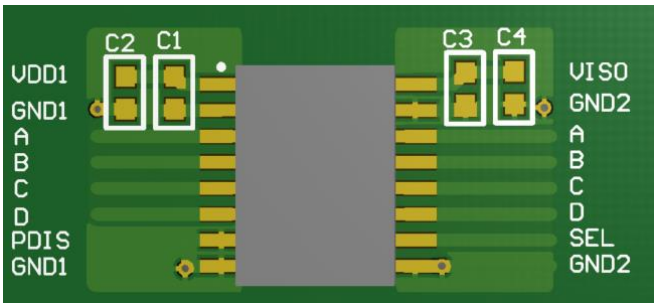

Figure5.1 Recommended PCB Layout — Top Layer

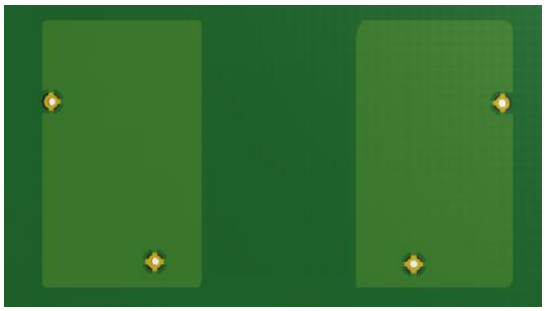

Figure5.2 Recommended PCB Layout — Bottom Layer

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6.0 PACKAGE INFORMATION

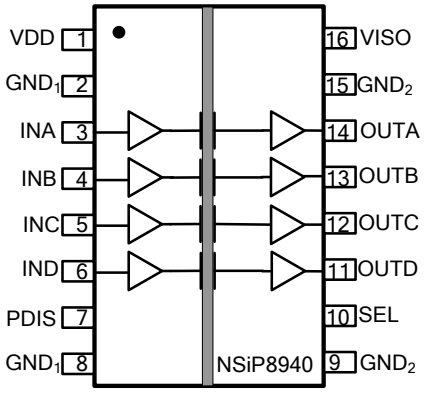

Figure 6.1 NSiP8940 Package

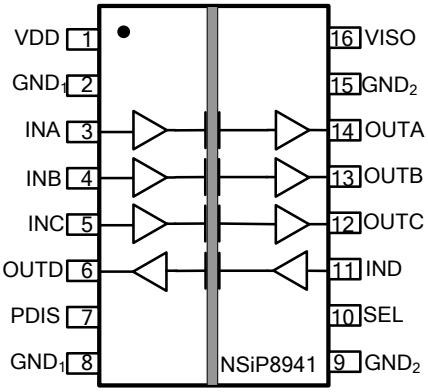

Figure 6.2 NSiP8941 Package

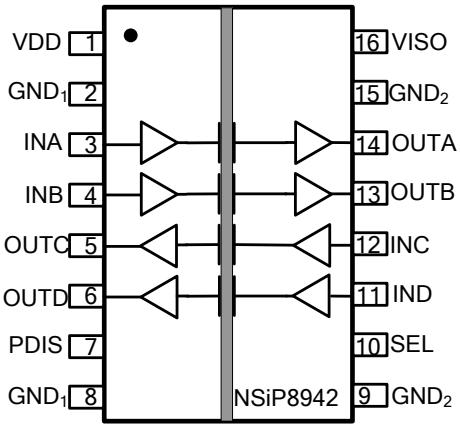

Figure 6.3 NSiP8942 Package

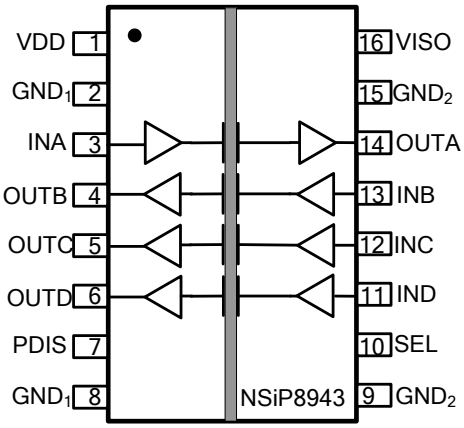

Figure 6.4 NSiP8943 Package

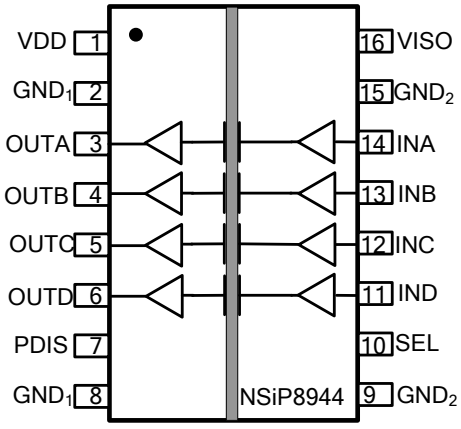

Figure 6.5 NSiP8944 Package

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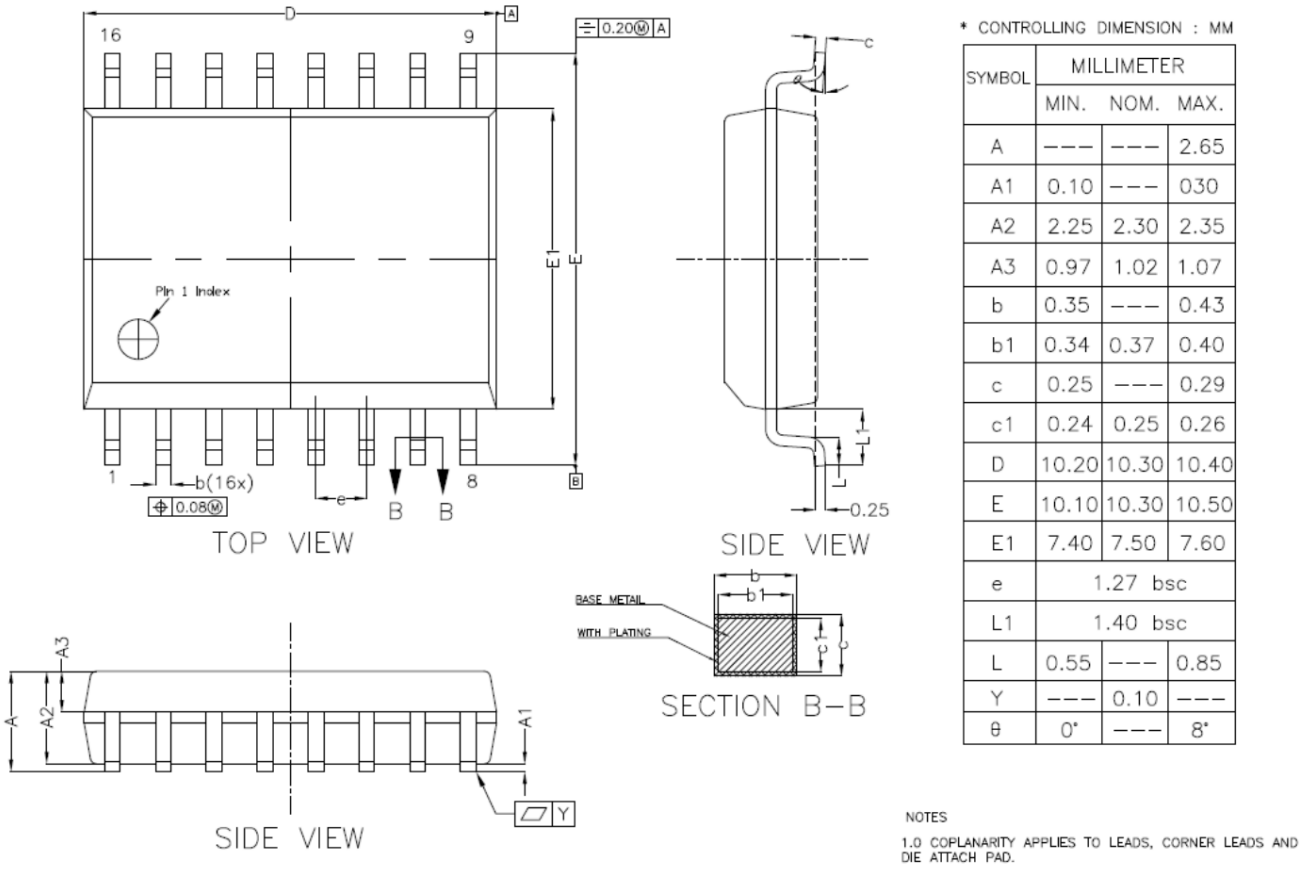

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
b1	0.34	0.37	0.40
c	0.25	---	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 6.6 SOIC16 Package Shape and Dimension in millimeters (inches)

Table6.1 NSiP8940/ NSiP8941/ NSiP8942/ NSiP8943/NSiP8944 Pin Configuration and Description

NSiP8940 PIN NO.	NSiP8941 PIN NO.	NSiP8942 PIN NO.	NSiP8943 PIN NO.	NSiP8944 PIN NO.	SYMBOL	FUNCTION
1	1	1	1	1	VDD	Power Supply for Isolator Side 1
2	2	2	2	2	GND1	Ground 1, the ground reference for Isolator Side 1
3	3	3	3	14	INA	Logic Input A
4	4	4	13	13	INB	Logic Input B
5	5	12	12	12	INC	Logic Input C
6	11	11	11	11	IND	Logic Input D
7	7	7	7	7	PDIS	Power Disable. When tied to any GND1 pin, the VISO output voltage is active. When a logic high voltage is applied, the VISO output voltage is shut down. Do not leave this pin floating.
8	8	8	8	8	GND1	Ground 1, the ground reference for Isolator Side 1
9	9	9	9	9	GND2	Ground 2, the ground reference for Isolator Side 2
10	10	10	10	10	SEL	VISO output voltage select, VISO=5V when SEL

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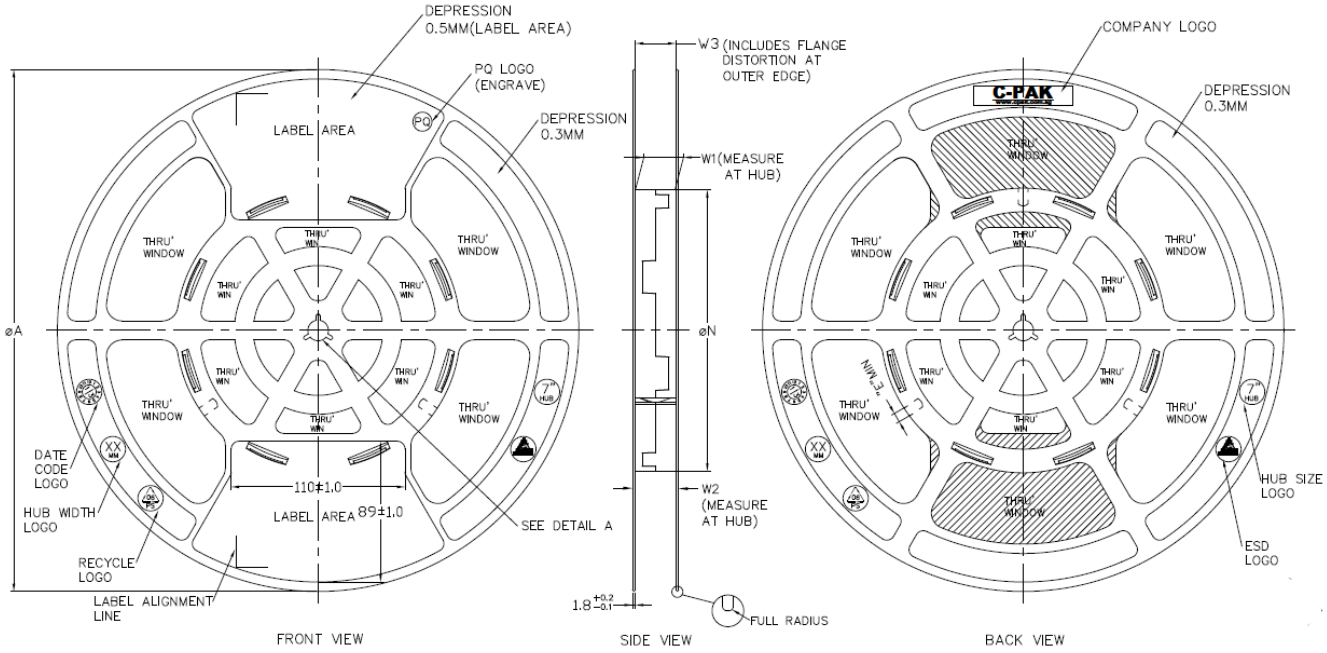
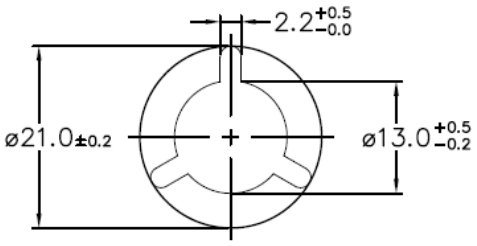
						pull high, VISO=3.3V when SEL pull low.
11	6	6	6	6	OUTD	Logic Output D
12	12	5	5	5	OUTC	Logic Output C
13	13	13	4	4	OUTB	Logic Output B
14	14	14	14	3	OUTA	Logic Output A
15	15	15	15	15	GND2	Ground 2, the ground reference for Isolator Side 2
16	16	16	16	16	VISO	Secondary Supply Voltage Output for External Load.

7.0 TAPE AND REEL INFORMATION





ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

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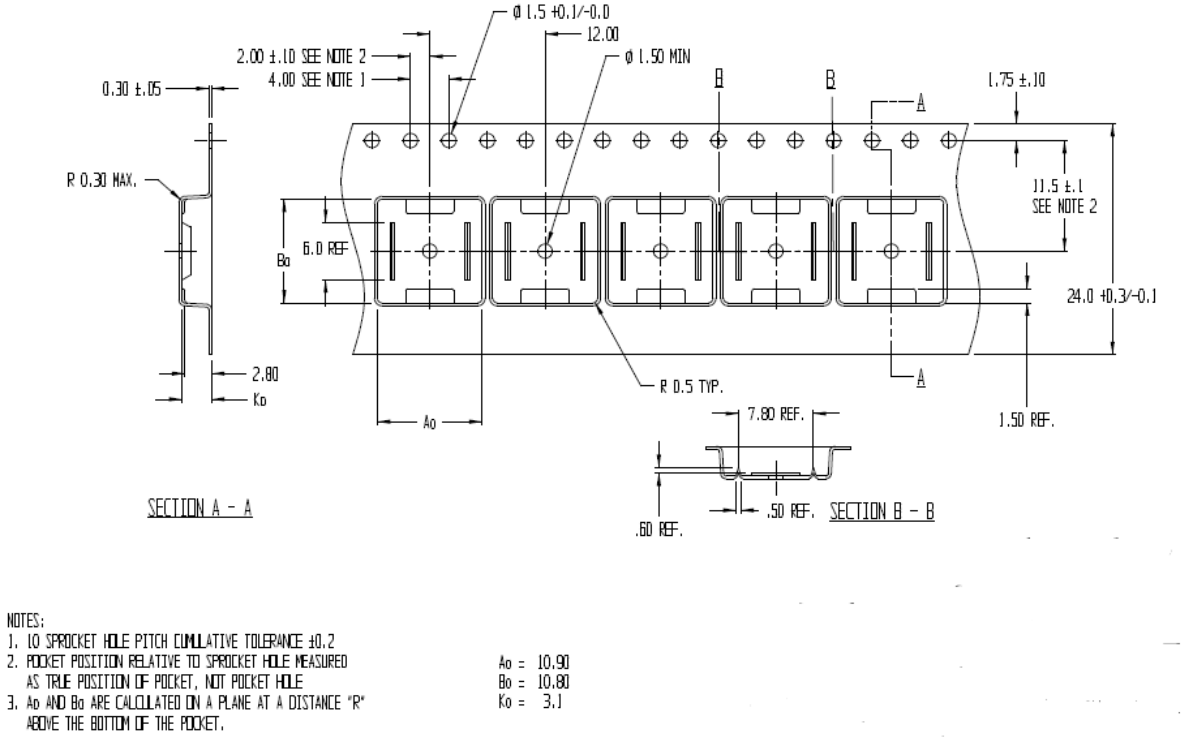

Figure 7.1 Tape and Reel Information of WB SOIC16

8.0 ORDER INFORMATION

Part No.	*Isolation Rating(kV)*	*Number of side 1 inputs*	*Number of side 2 inputs*	*Max Data Rate (Mbps)*	*Default Output State*	*Temperature*	*Automotive*	*Package*
NSIP8940W0-DSWR	5	4	0	150	Low	-40 to 125°C	NO	SOIC16W
NSIP8940W1-DSWR	5	4	0	150	High	-40 to 125°C	NO	SOIC16W
NSIP8941W0-DSWR	5	3	1	150	Low	-40 to 125°C	NO	SOIC16W
NSIP8941W1-DSWR	5	3	1	150	High	-40 to 125°C	NO	SOIC16W
NSIP8942W0-DSWR	5	2	2	150	Low	-40 to 125°C	NO	SOIC16W
NSIP8942W1-DSWR	5	2	2	150	High	-40 to 125°C	NO	SOIC16W
NSIP8943W0-DSWR	5	1	3	150	Low	-40 to 125°C	NO	SOIC16W
NSIP8943W1-DSWR	5	1	3	150	High	-40 to 125°C	NO	SOIC16W

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NSIP8944W0-DSWR	5	0	4	150	Low	-40 to 125℃	NO	SOIC16W
NSIP8944W1-DSWR	5	0	4	150	High	-40 to 125℃	NO	SOIC16W
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.								

9.0 REVISION HISTORY

Revision	Description	Date
1.0	Original	2019/11/15

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