YC5X NFC IC

Product Brief

Yichip Microelectronics

Revision History

Version	Date	Author	Description
V1.0	2019-6-6	Team	Initial version datasheet V2.8

Contents

1 General Description

1.1 Product Selection

NFC IC					
No.	**Part Number**	**Package**	**Spec**	**Pin-to-pin Compatibility**	**Recommended Voltage (V)**
1	YC5018	QFN5X5 32pin	EMV2.6	FM17550、NXP RC523	3.3
2	YC5118	QFN5X5 32pin	EMV3.0	FM17550、NXP RC523	3.3
3	YC5016	SOP16	EMV2.6		3.3
4	YC5116	SOP16	EMV3.0		3.3
5	YC5020	QFN3X3 20pin	EMV2.6		3.3

1.2 Product Introduction

YC5X is a serial of highly integrated ultra-low power NFC ICs. In accordance with EMV2.6 and EMV3.0 respectively, YC50XX and YC51XX support all layer applications for ISO/IEC14443 Type A/MIFARE and Type B. With extremely simplified peripheral circuits, YC5X serials can provide flexible implementations of all kinds of NFC applications.

1.3 Key Features

- YC50XX follows EMV2.6 standard while YC51XX follows EMV3.0 standard;
- Supporting ISO/IEC 14443 TypeA/MIFARE communication protocol;
- Supporting ISO/IEC 14443 TypeB communication protocol;
- Supporting ISO 14443 A/B high speed transport communication at 106kbps / 212kbps / 424kbps / 848kbps;
- Supporting external clock input (27.12M/12MHz selectable) without external crystal;
- Supporting software AGC with high RX sensitivity and effective communication distance up to 12cm;
- Supporting TX waveform self-shaping in order to effectively suppress TX overshoots;

- Supporting self-calibration for modulation depth so that the modulation depth is complied with EMV3.0 test requirements under different heights and loadings;
- Supporting hardware EMD detection to pass all EMV3.0 EMD cases in order to simplify the design of master program;
- Supporting low power card detection (LPCD) function;
- Package format: QFN32, SOP16 and QFN20;
- IO operating voltage range: 1.65V ~ 5V;
- Maximum TX power: 1.4W;
- Supporting host interface: 10Mbps SPI, or I2C speed mode up to 400Kbps & speed plus mode up to 1MKbps;
- Low power mode: Standby mode and RF off mode
- Equipped with CRC and Parity functions, embedded with CRC co-processor, complied with ISO/1EC14443 & CCITT protocol;
- Programmable timer and flexible interrupt modes.

1.4 Block Diagram

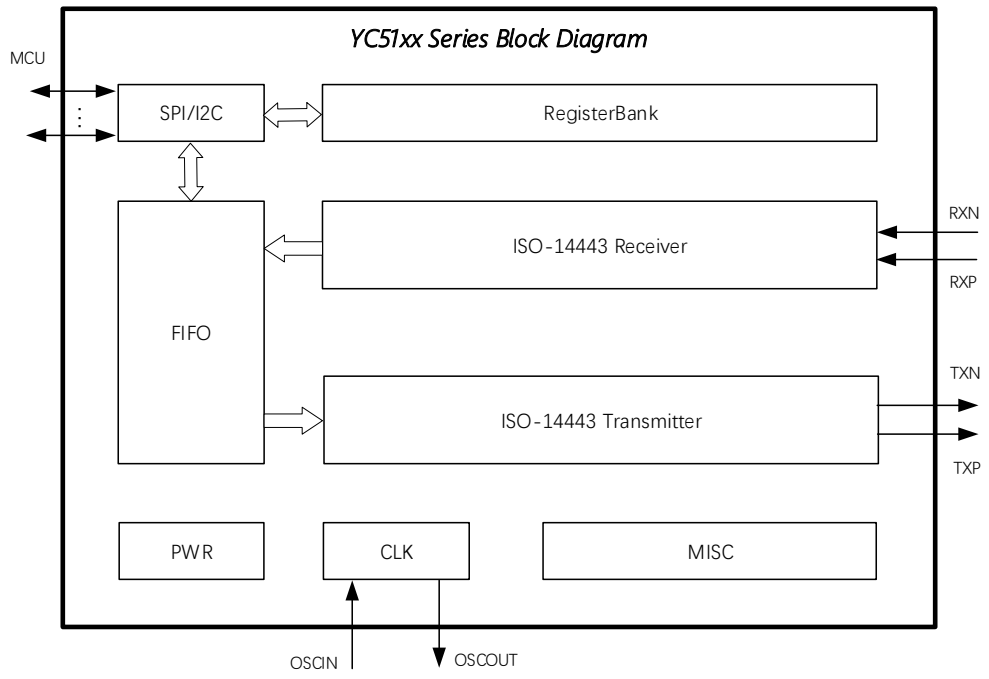

图 1. YC5X NFC 芯片系列框图

1.5 Pin Assignment

1.5.1 QFN32 — YC5118 / YC5018(G)

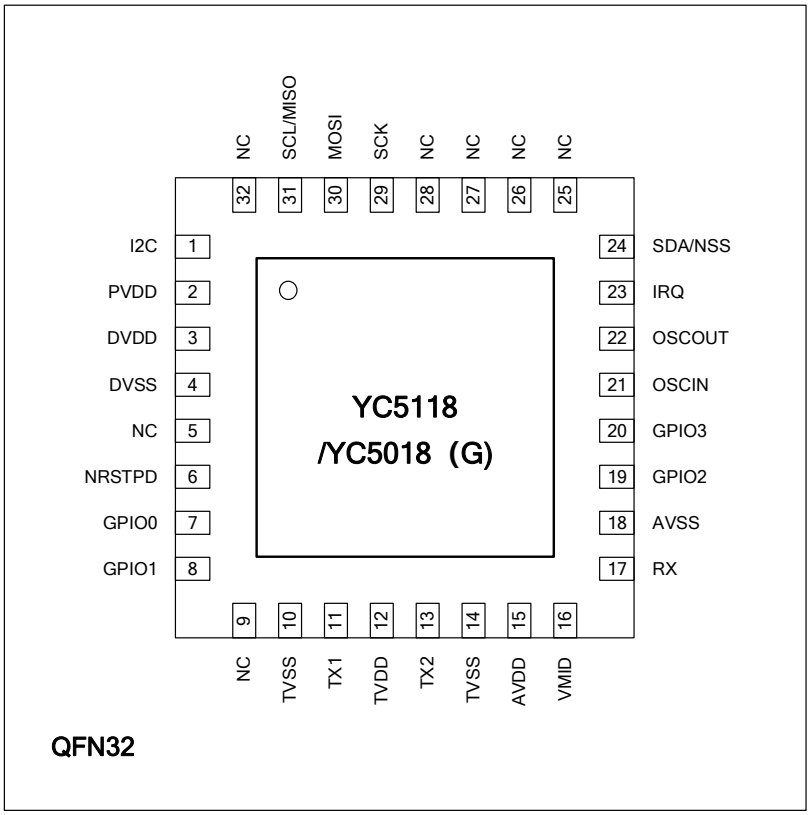

Figure 2. YC5118 / YC5018(G) package pin Assignment

Table 1. QFN32 Pin Assignment —— YC5118 / YC5018(G)

序号	符号	类型	描述
1	I2C	I	Low level: SPI, High Level: I2C
2	PVDD	PWR	IO Power supply
3	DVDD	PWR	Digital Power supply
4	DVSS	PWR	Digital Ground
5	NC	—	—
6	NRSTPD	I	Low enable: Reset or lost power, High for normal operation
7	GPIO0	O	GPIO0 control pin 0: low level & 1: Hi-Z
8	GPIO1	O	GPIO1 control pin 0: low level & 1: Hi-Z
9	NC	—	—
10	TVSS	PWR	TX Ground
11	TX1	O	TX output for 13.56MHz modulation on Energy carrier signal
12	TVDD	PWR	TX Power supply
13	TX2	O	TX output for 13.56MHz modulation on Energy carrier signal
14	TVSS	PWR	TX Ground
15	AVDD	PWR	Analog Power supply

16	VMID	PWR	Internal reference voltage
17	RX	I	RX input
18	AVSS	PWR	Analog Ground
19	GPIO2	O	GPIO2 control pin 0: low level & 1: Hi-Z
20	GPIO3	O	GPIO3 control pin 0: low level & 1: Hi-Z
21	OSCIN	I	Connect to external 27.12MHz Crystal, and optionally to external 27.12MHz or 12MHz clock signal
22	OSCOUT	O	Connect to external 27.12MHz Crystal
23	IRQ	O	Output interrupt signal
24	NSS/ SDA/	I/O	SPI CS / I2C SDA
25	NC	—	—
26	NC	—	—
27	NC	—	—
28	NC	—	—
29	SCK	I/O	SPI SCK
30	MOSI	I/O	SPI MOSI
31	MISO/SCL	I/O	SPI MISO / I2C SCL
32	NC	—	—

1.5.2 QFN32 — YC5018(H)

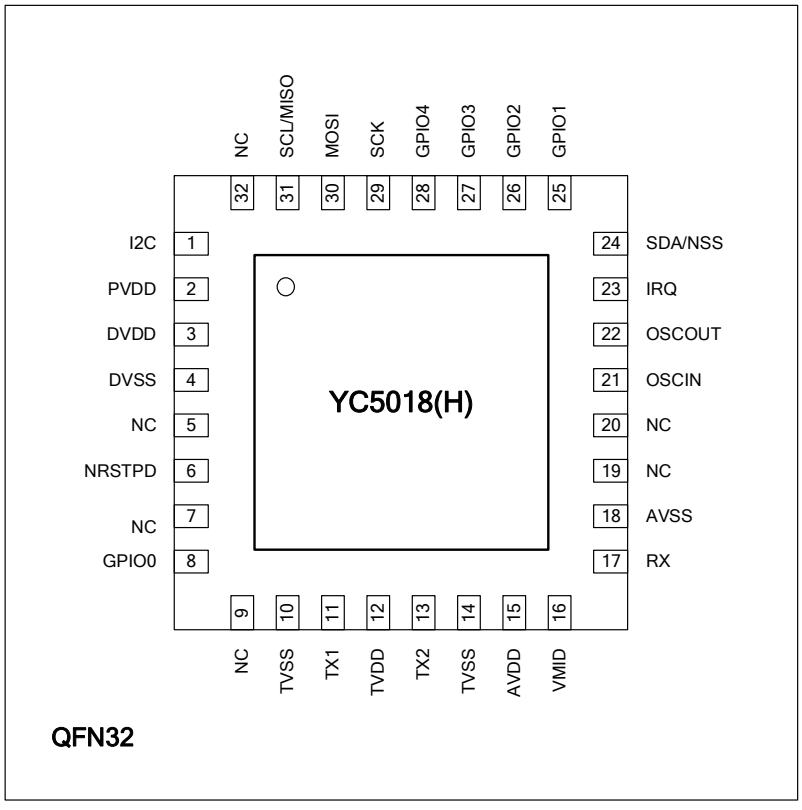

Figure 3. YC5018(H) Package Pin Assignment

Table 2. QFN32 Pin Assignment —— YC5018（H）

序号	符号	类型	描述
1	I2C	I	Low level: SPI, High Level: I2C
2	PVDD	PWR	IO Power supply
3	DVDD	PWR	Digital Power supply
4	DVSS	PWR	Digital Ground
5	NC	—	—
6	NRSTPD	I	Low enable: Reset or lost power, High for normal operation
7	NC	—	—
8	GPIO0	O	GPIO0 control pin 0: low level & 1: Hi-Z
9	NC	—	—
10	TVSS	PWR	TX Ground
11	TX1	O	TX output for 13.56MHz modulation on Energy carrier signal
12	TVDD	PWR	TX Power supply
13	TX2	O	TX output for 13.56MHz modulation on Energy carrier signal
14	TVSS	PWR	TX Ground
15	AVDD	PWR	Analog Power supply
16	VMID	PWR	Internal reference voltage
17	RX	I	RX input
18	AVSS	PWR	Analog Ground
19	NC	—	—
20	NC	—	—
21	OSCIN	I	Connect to external 27.12MHz Crystal, and optionally to external 27.12MHz or 12MHz clock signal
22	OSCOUT	O	Connect to external 27.12MHz Crystal
23	IRQ	O	Output interrupt signal
24	NSS/ SDA/	I/O	SPI CS / I2C SDA
25	GPIO1	O	GPIO1 control pin 0: low level & 1: Hi-Z
26	GPIO2	O	GPIO2 control pin 0: low level & 1: Hi-Z
27	GPIO3	O	GPIO3 control pin 0: low level & 1: Hi-Z
28	GPIO4	O	GPIO4 control pin 0: low level & 1: Hi-Z
29	SCK	I/O	SPI SCK
30	MOSI	I/O	SPI MOSI
31	MISO/SCL	I/O	SPI MISO / I2C SCL
32	NC	—	—

1.5.3 SOP16 — YC5016 / YC5116

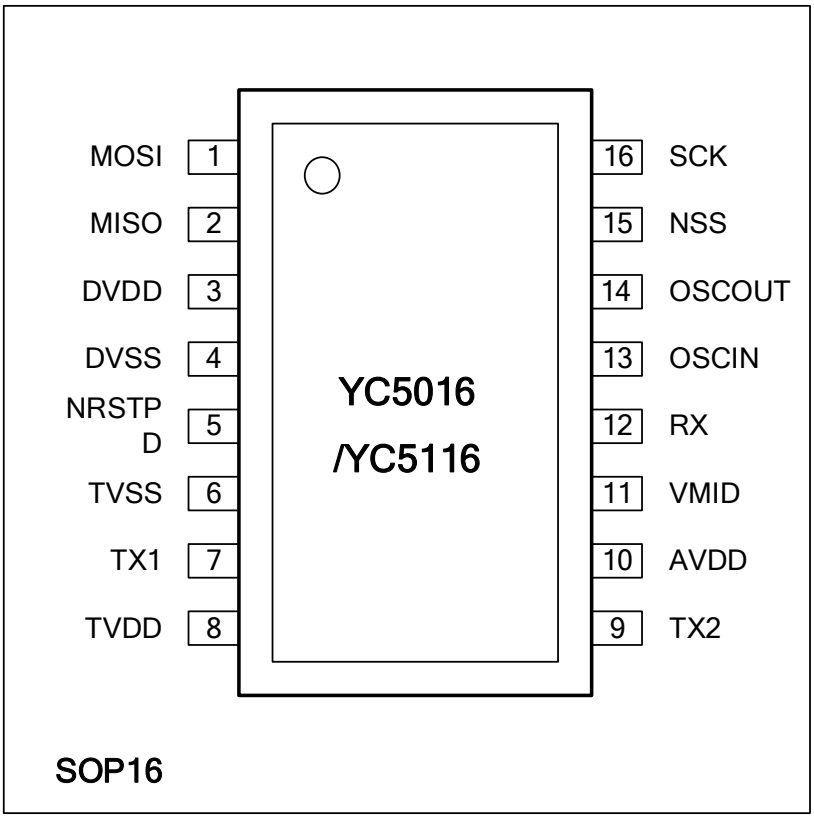

Figure 4. YC5016/YC5116 Package Pin Assignment

Table 3. SOP16 Pin Assignment —— YC5016 / YC5116

序号	符号	类型	描述
1	MOSI	I	SPI MOSI
2	MISO	O	SPI MISO
3	DVDD	PWR	Digital Power supply
4	DVSS	PWR	Digital Ground
5	NRSTPD	I	Low enable: Reset or lost power, High for normal operation
6	TVSS	PWR	TX Ground
7	TX1	O	TX output for 13.56MHz modulation on Energy carrier signal
8	TVDD	PWR	TX Power supply
9	TX2	O	TX output for 13.56MHz modulation on Energy carrier signal
10	AVDD	PWR	Analog Power supply
11	VMID	PWR	Internal reference voltage
12	RX	I	RX input
13	OSCIN	I	Connect to external 27.12MHz Crystal, and optionally to external 27.12MHz or 12MHz clock signal
14	OSCOUT	O	Connect to external 27.12MHz Crystal
15	NSS	I	SPI NSS
16	SCK	I	SPI SCK

1.5.4 QFN20—YC5020

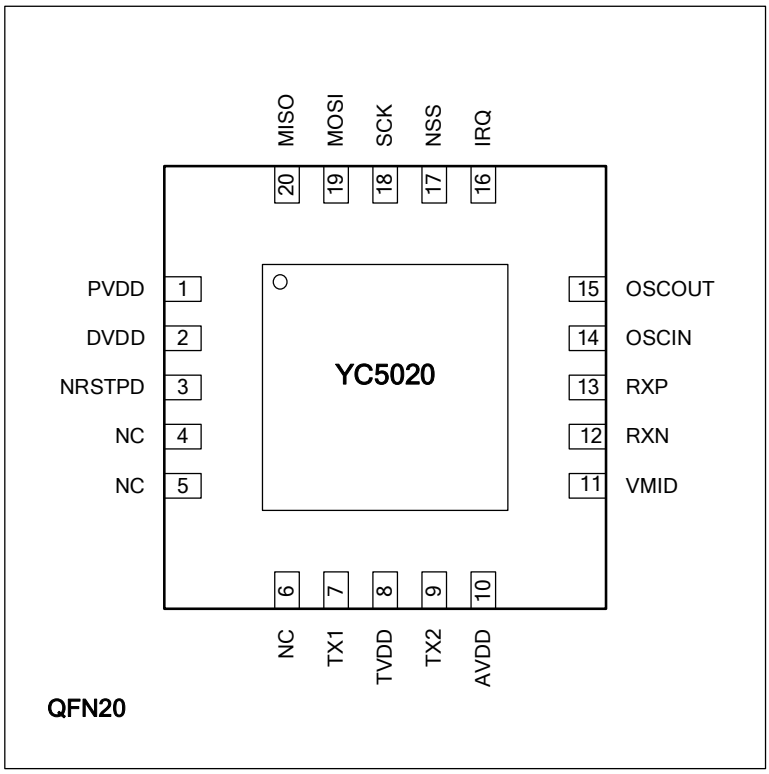

Figure 5. YC5020 Package Pin Assignment

Table 4. QFN20 Pin Assignment —— YC5020

序号	符号	类型	描述
1	VIO	PWR	IO Power supply
2	DVDD	PWR	Digital Power supply
3	NRSTPD	I	Low enable: Reset or lost power, High for normal operation
4	NC	—	—
5	NC	—	—
6	NC	—	—
7	TX1	O	TX output for 13.56MHz modulation on Energy carrier signal
8	TVDD	PWR	TX Power supply
9	TX2	O	TX output for 13.56MHz modulation on Energy carrier signal
10	AVDD	PWR	Analog Power supply
11	VMID	PWR	Internal reference voltage
12	RXN	I	RX- input
13	RXP	I	RX+ input
14	OSCIN	I	Connect to external 27.12MHz Crystal, and optionally to external 27.12MHz or 12MHz clock signal
15	OSCOUT	O	Connect to external 27.12MHz Crystal

16	IRQ	O	Output interrupt signal
17	NSS	I/O	SPI NSS
18	SCK	I/O	SPI SCK
19	MOSI	I/O	SPI MOSI
20	MISO	I/O	SPI MISO
21	GND	PWR	Soldering pad ground

2 Functional Description

2.1 ISO/IEC14443A Function Support

Table 5. YC5X ISO/IEC A Communication Overview

Communication Direction	Signal Type	Transmission Rate			
		106kBd	212kBd	424kBd	848kBd
PCD→PICC	PCD Modulation	100%ASK	100%ASK	100%ASK	100%ASK
	Bit Coding	Modified Miller	Modified Miller	Modified Miller	Modified Miller
	Bit Length	(128/13.56)us	(64/13.56)us	(32/13.56)us	(16/13.56)us
PICC→PCD	PICC Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier Frequency	13.56MHz/16	13.56MHz/16	13.56MHz/16	13.56MHz/16
	Bit Coding	Manchester	BPSK	BPSK	BPSK

The communication between YC5X and RFID card follows ISO14443 Type A protocol. Figure 3 provides the frame format correlated between PCD and PICC. Figure 4 provides the PICC Standard frame format.

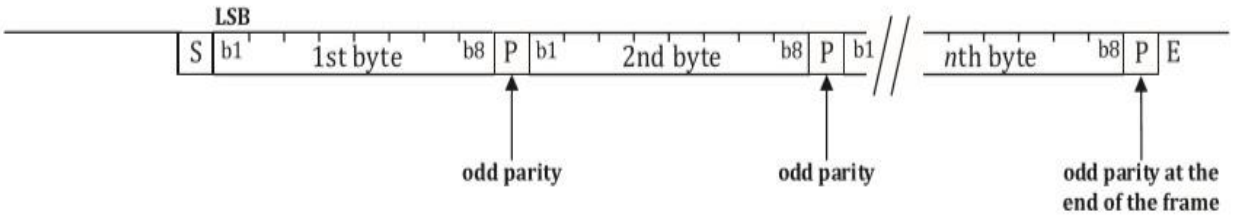

Figure 3. Type A PCD → PICC Standard Frame Format

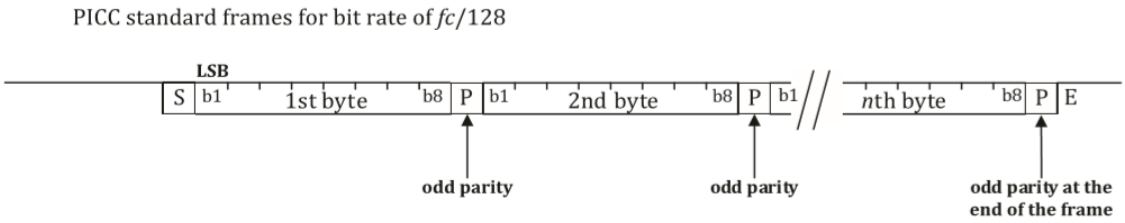

Figure 4. Type A PICC Standard Frame Format 106Kbps

According to Section 3 of ISO/IEC14443A, CRC co-processor calculates CRC value and controls the generation of internal verification per transmission rate.

2.2 ISO/IEC14443B Function Support

YC5Xsupports ISO/IEC14443 Type B protocol. Figure 5 provides the Type B Standard frame format.

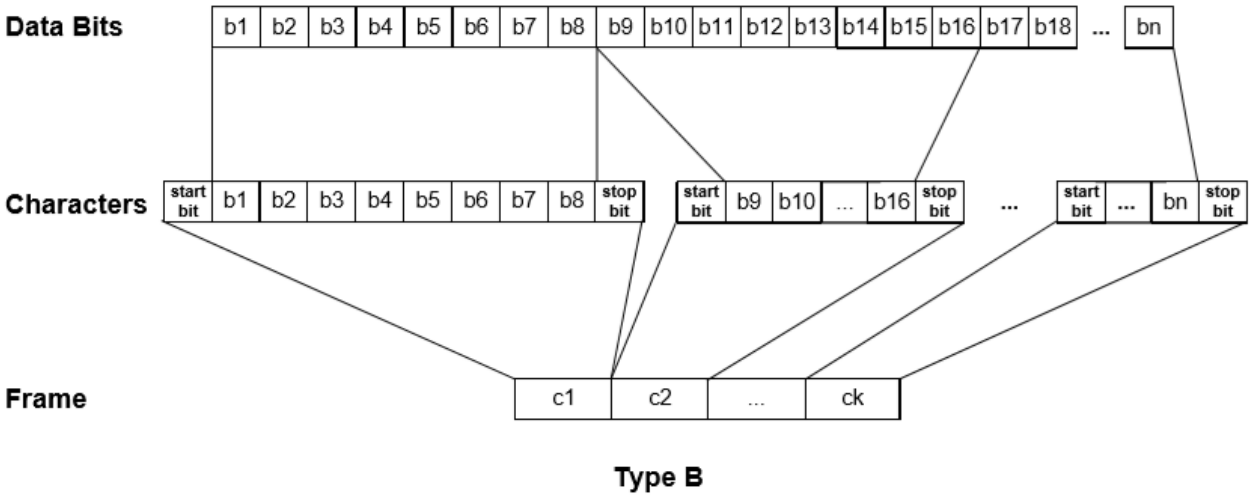

Figure 5. Type B Standard Frame Format

3 Reset and Clock

3.1 Reset

YC5X works normally when reset pin RST at high level, while is under reset status when RST at low level. The reset and startup procedure needs RST low for at least 5ms and then high for at least 20ms. In some application,

if the startup time is sensitive, after RST is pull high from low, powerup_irq or pmu_state register can be periodically visited to judge whether the chip is started up by checking internal interrupt or state machine.

3.2 Clock

YC5X supports clock operation mode with or without external crystal. Mode with crystal supports frequency of 27.12MHz or 13.56MHz. Mode without crystal can reduce BOM cost, but needs external clock with frequency of 27.12Mhz or 12MHz. In this mode, before the chip is powered up, make sure external clock to start up for recommended over 200us. The routine for external clock should be as short as possible and wrapped by ground isolation during PCB layout.

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4 Application Block Diagram

MCU connects YC5X through bus and SPI or I2C to implement 14443 contactless communication. Also through GPIO, MCU can provide reset to YC5X receive interrupt from YC5X. Therefore, all kinds of contactless applications can be developed flexibly. YC5X implements 14443 Type A/MIFARE/Type B protocol for physical and link layers, including modulation/demodulation, framing/Un-framing, CRC verification and etc. YC5X provides AGC adjust for receiving software, detection for low power card and other abundant contactless applications.

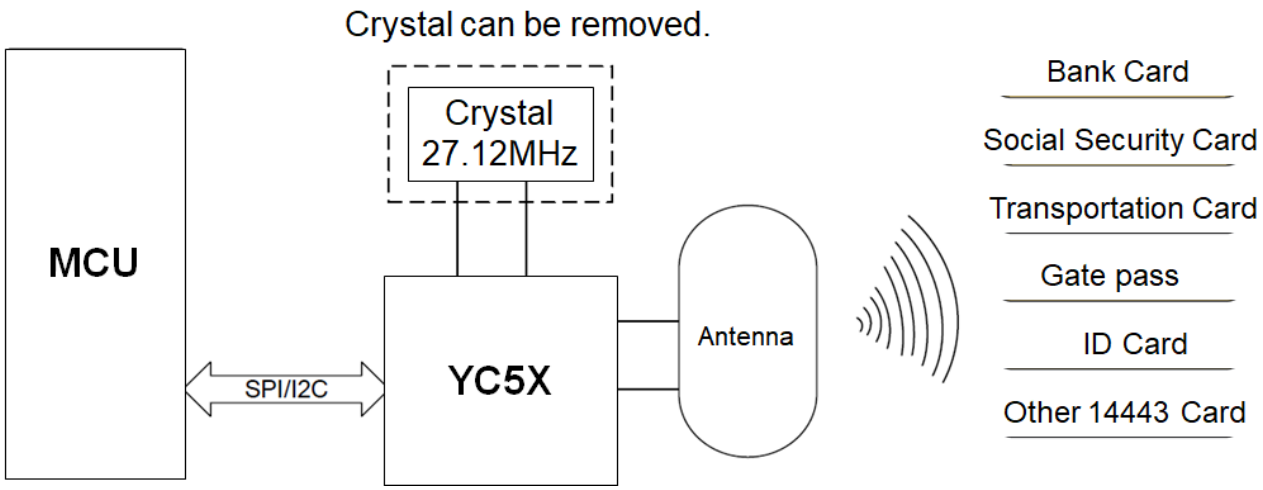


Figure 6. YC5X Application Block Diagram Example

4.1 Typical Circuit

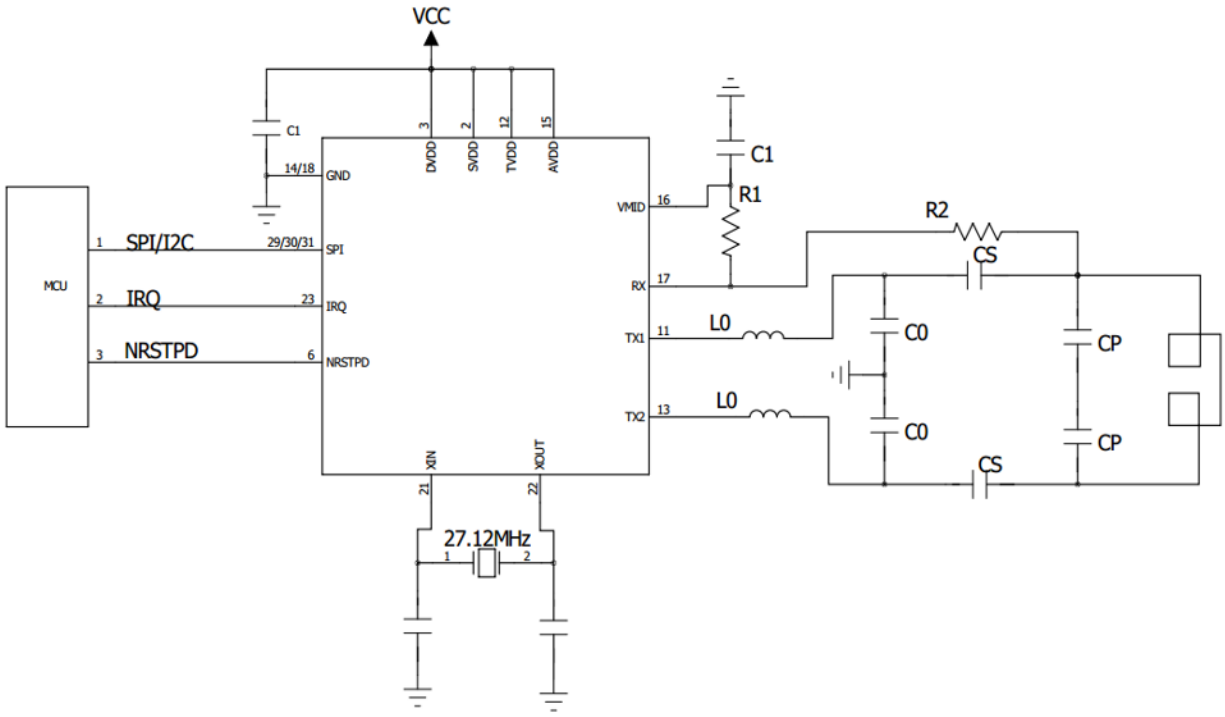


Figure 7. YC5X Typical Circuit

5 Electrical Specifications

5.1 Voltage Parameters

Table 12. Voltage Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVDD	Digital Power Supply Voltage	PVSS=DVSS=AVSS=TVSS=0V PVDD<=DVDD=AVDD=TVDD	2.1	3.3	5.0	V
AVDD	Analog Power Supply Voltage		2.1	3.3	5.0	V
TVDD	TX Power Supply Voltage		2.5	3.3	5.0	V
PVDD	IO Power Supply Voltage		1.65	3.3	5.0	V

5.2 Current Parameters

Table 13. Current Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{HPD}	Shutdown	AVDD=DVDD=TVDD=PVDD=3.3V	—	0.06	—	uA

	Current	NRSTPD=LOW				
I_{STDB}	Standby Current	AVDD=DVDD=TVDD=PVDD=3.3V STANDBY	—	0.65	—	uA
I_{IDLE}	Idle Current	AVDD=DVDD=TVDD=PVDD=3.3V IDLE	—	0.85	—	mA
I_{LPCD}	LPCD Average Current	AVDD=DVDD=TVDD=PVDD=3.3V Lpcd period = 100ms	—	4.1	—	uA
I_{TVDD}	TX Power Supply Current	Continuous TX Transmission TVDD=3.3V	—	60	256	mA

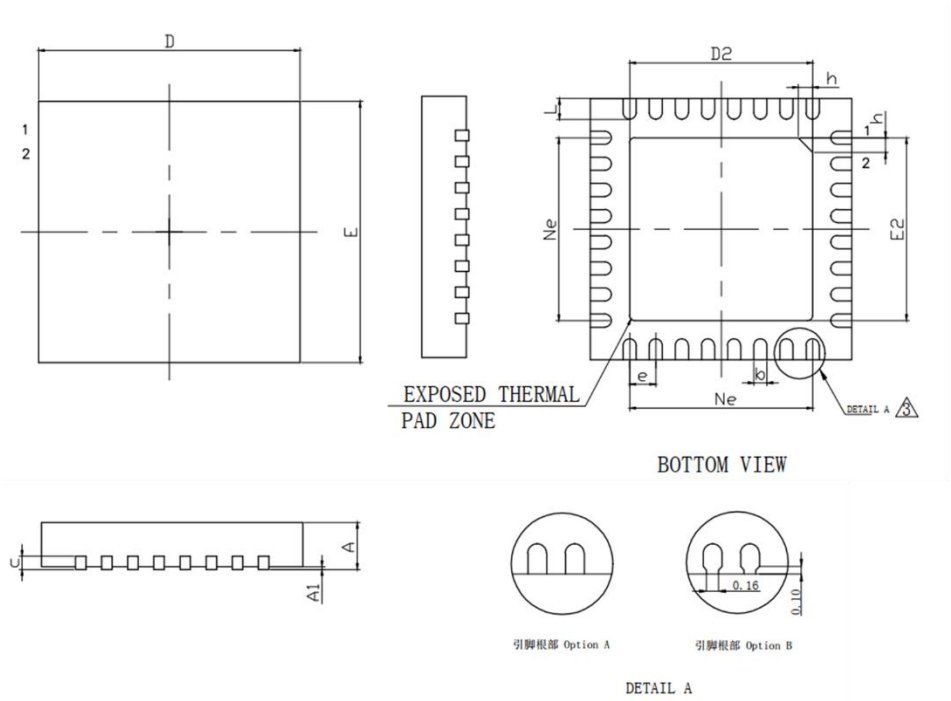
5.3 Environmental Parameters

Table 14. Environmental Parameters

Symbol	Parameter	Conditions	Min
Operating Temperature	-40	+85	℃
ESD (HBM 1500Ω 100pF)	—	2000	V

6 Package Information

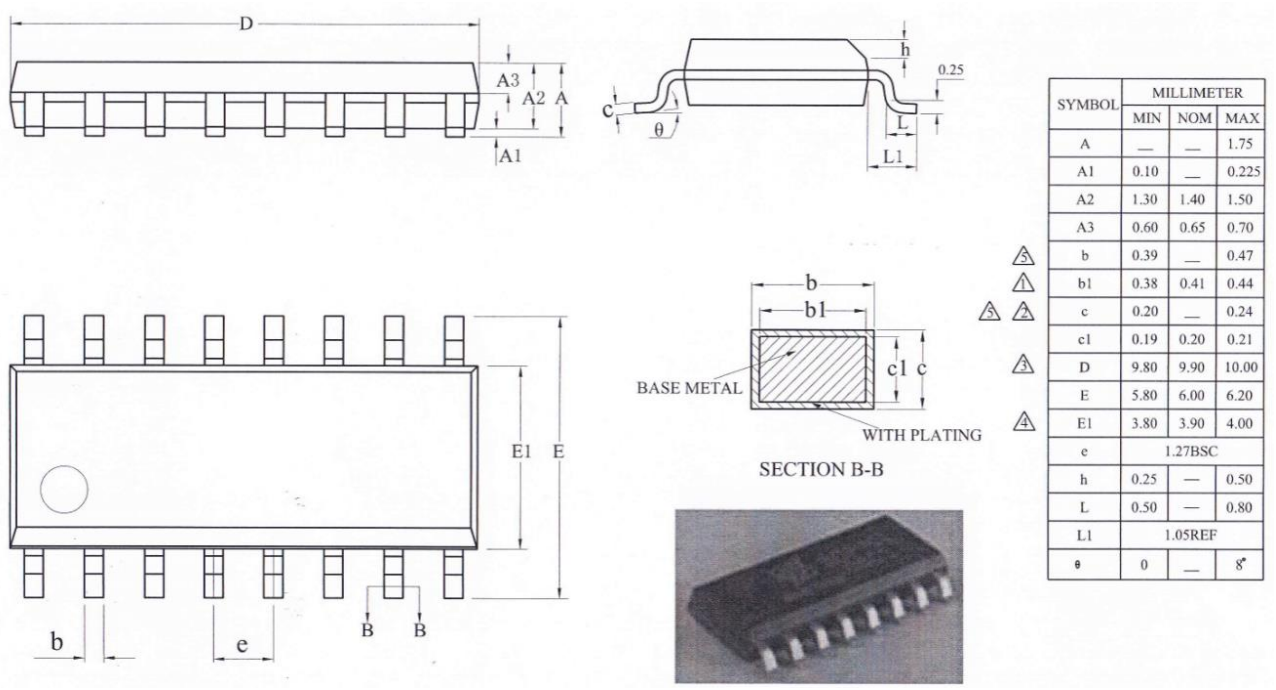
6.1 QFN32 Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸	150x150		130x130

Figure 8. QFN32 Package Dimensions

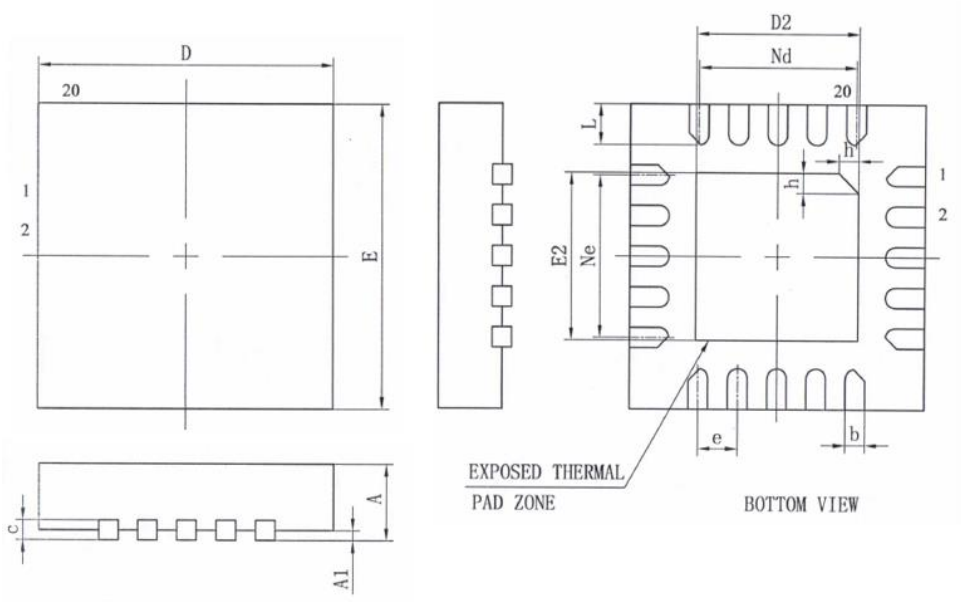
6.2 SOP16 Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 9. SOP16 Package Dimensions

6.3 QFN20 Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (MIL)	75*75		

Figure 10. QFN20 Package Dimensions