Universal High Brightness LED Driver

Features

- Switch mode controller for single switch LED drivers
- Enhanced drop-in replacement to the HT9910
- Open loop peak current controller
- Internal 8.0V to 450V linear regulator
- Constant frequency or constant off-time operation
- Linear and PWM dimming capability
- Requires few external components for operation

Applications

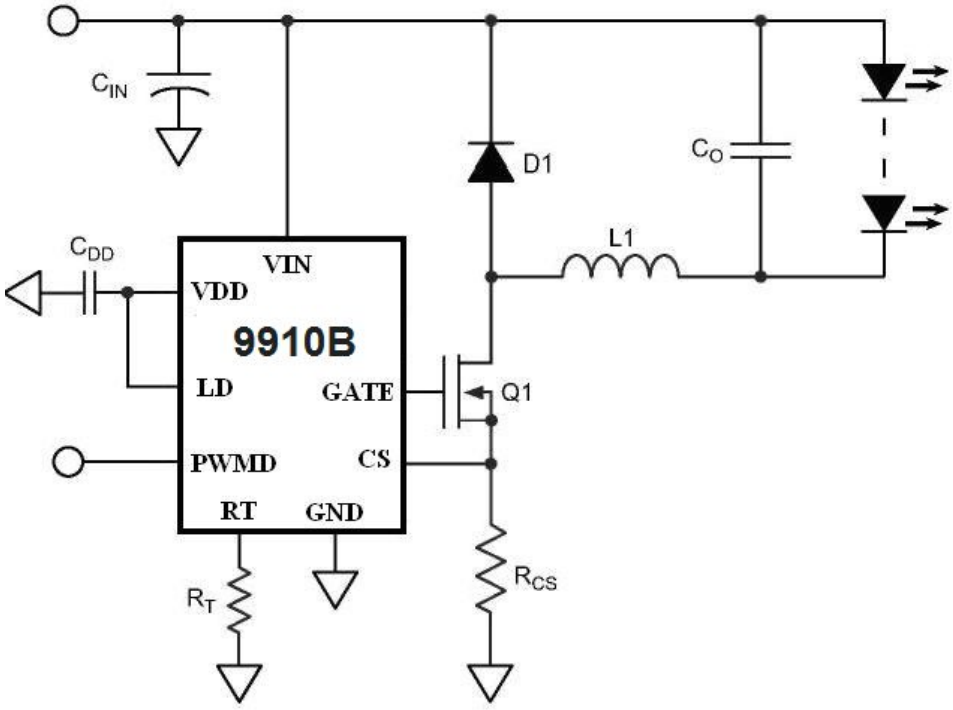
- DC/DC or AC/DC LED Driver applications
- RGB Backlighting LED Driver
- Back Lighting of Flat Panel Displays
- General purpose constant current source
- Signage and Decorative LED Lighting
- Chargers

General Description

The HT9910B is an open loop current mode control LED driver IC. The HT9910B can be programmed to operate in either a constant frequency or constant off-time mode. It includes an 8 – 450V linear regulator which allows it to work from a wide range of input voltages without the need for an external low voltage supply. The HT9910B includes a PWM dimming input that can accept an external control signal with a duty ratio of 0 – 100% and a frequency of up to a few kilohertz. It also includes a 0 – 250mV linear dimming input which can be used for linear dimming of the LED current.

The HT9910B is ideally suited for buck LED drivers. Since the HT9910B operates in open loop current mode control, the controller achieves good output current regulation without the need for any loop compensation. PWM dimming response is limited only by the rate of rise and fall of the inductor current, enabling very fast rise and fall times. The HT9910B requires only three external components (apart from the power stage) to produce a controlled LED current making it an ideal solution for low cost LED drivers

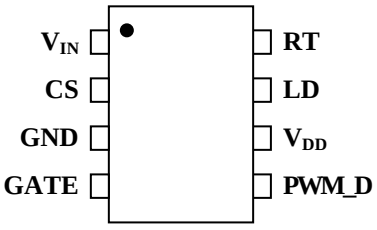
Typical Application Circuit



Pin-out

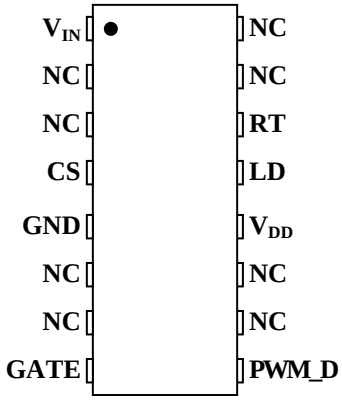
Name	Pad	SOIC-16	SOIC-8 DIP-8	Description
V_{IN}	1	1	1	This pin is the input of an 8V - 450V linear regulator.Input voltage 8V to 450V DC
CS	2	4	2	Senses LED string current
GND	3,4,5	5	3	Device ground
GATE	6	8	4	Drives the gate of the external MOSFET
PWM_D	7	9	5	Low Frequency PWM Dimming pin, also Enable input. Internal 100kΩ pull-down to GND
V_{DD}	8,9,10	12	6	Internally regulated supply voltage. 7.5V nominal. Can supply up to 1mA for external circuitry. A sufficient storage capacitor is used to provide storage when the rectified AC input is near the zero crossings.
LD	11	13	7	Linear Dimming by changing the current limit threshold at current sense comparator
RT	12	14	8	Oscillator control. A resistor connected between this pin and ground sets the PWM frequency.

No Connects (NC) are not internally connected and may be used for pass-thru PCB traces



HT9910BRZ-8
8-Pin SOIC

16-Pin SOIC



HT9910BRZ-16
16-Pin SOIC

Absolute Maximum Ratings

V_{IN} to GND……-0.5V to +470V
CS, LD, PWM_D, GATE, RT to GND……-0.3V to (V_{DD} + 0.3V)
V_{DD} to GND……12V
Maximum duty cycle of the PWM generator cannot be 100%
Continuous Power Dissipation (T_A = +25°C)
8-Lead SOIC…… 630mW
16-Lead SOIC…… 1300mW
Junction Temperature Range..... -40°C to +150°C
Storage Temperature Range .....……..-65°C to +150°C

Stresses beyond those listed under ''Absolute Maximum Ratings'' may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

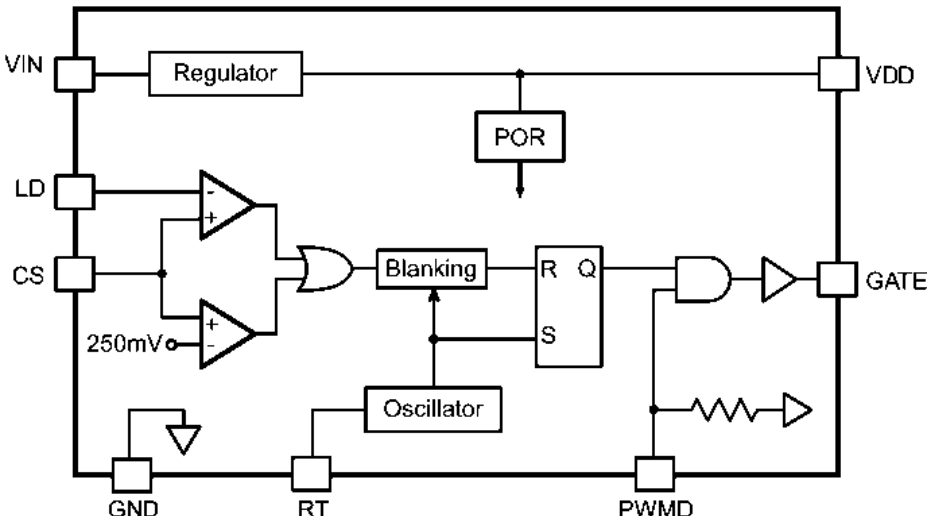
Thermal Resistance ($R_{θja}$)

8- Lead SOIC …… 128°C/W
16- Lead SOIC …… 82°C/W

Electrical Characteristics *(The specifications are at T_A= 25°C. V_{IN} = 12V, unless otherwise noted.)*

Symbol	Description	Min	Typ	Max	Units	Conditions
V_{INDC}	Input DC supply voltage range	8.0		450	V	DC input voltage
I_{INSD}	Shut-Down mode supply current		0.5	1	mA	Pin PWM_D to GND
V_{DD}	Internally regulated voltage	**7.25**	**7.5**	**7.75**	V	V_{IN} = 8V, $I_{DD(ext)}$=0, 500pF at Gate; R_T=226kΩ, PWM_D = V_{DD}
$\Delta V_{DD,line}$	Line Regulation of V_{DD}	0	-	1	V	V_{IN} = 8 - 450V, $I_{DD(ext)}$ = 0, 500pF at GATE; R_T = 226kΩ, PWM_D = V_{DD}
$\Delta V_{DD,load}$	Load Regulation of V_{DD}	0	-	100	mV	$I_{DD(ext)}$ = 0 - 1mA, 500pF at GATE; R_T = 226kΩ, PWMD = V_{DD}
UVLO	V_{DD} undervoltage lockout threshold	6.45	6.7	6.95	V	V_{DD} rising
ΔUVLO	V_{DD} undervoltage lockout hysteresis		500		mV	V_{DD} falling
$I_{IN,MAX}$	Current that the regulator can supply before IC goes into UVLO	5	-	-	mA	V_{IN} = 8V
$V_{EN(lo)}$	Pin PWM_D input low voltage			**0.8**	V	V_{IN} = 8-450V
$V_{EN(hi)}$	Pin PWM_D input high voltage	**2.0**			V	V_{IN} = 8-450V
R_{EN}	Pin PWM_D pull-down resistance at PWM_D	50	100	150	kΩ	V_{EN} = 5V
$V_{CS,TH}$	Current sense pull-in threshold voltage	**225**	**250**	**275**	mV	-40°C < T_A < +85°C
		213	250	287		T_A < +125°C
V_{OFFSET}	Offset voltage for LD comparator	-12	-	12	mV	----
T_{BLANK}	Current sense blanking interval	150	215	280	ns	0< T_A < +85°C, V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}
		145	215	315		-40°C < T_A < +125°C, V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}
t_{DELAY}	Delay to output	-	80	150	ns	V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}
fosc	Oscillator frequency	20	25	30	kHz	R_T = 1.00 MΩ
		80	100	120		R_T = 226 kΩ
I_{SOURCE}	Gate sourcing current	0.165	-	-	A	V_{GATE} = 0V, V_{DD} = 7.5V
I_{SINK}	Gate sinking current	0.165	-	-	A	V_{GATE} = V_{DD}, V_{DD} = 7.5V
t_{RISE}	GATE output rise time	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V
t_{FALL}	GATE output fall time	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V

Block Diagram



Application Information

The 9910B is optimized to drive buck LED drivers using open-loop peak current mode control. This method of control enables fairly accurate LED current control without the need for high side current sensing or the design of any closed loop controllers. The IC uses very few external components and enables both Linear and PWM dimming of the LED current.

A resistor connected to the RT pin programs the frequency of operation (or the off-time). The oscillator produces pulses at regular intervals. These pulses set the SR flip-flop in the 9910B which causes the GATE driver to turn on. The same pulses also start the blanking timer which inhibits the reset input of the SR flip flop and prevent false turn-offs due to the turn-on spike. When the FET turns on, the current through the inductor starts ramping up. This current flows through the external sense resistor RCS and produces a ramp voltage at the CS pin. The comparators are constantly comparing the CS pin voltage to both the voltage at the LD pin and the internal 250mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip flop. When the output of either one of the two comparators goes high, the flip flop is reset and the GATE output goes low. The GATE goes low until the SR flip flop is set by the oscillator. Assuming a 30% ripple in the inductor, the current sense resistor RCS can be set using:

$$R_{CS}= \frac{0.25V \text{ (or } V_{LD})}{1.15*I_{LED}(A)}$$

Constant frequency peak current mode control has an inherent disadvantage – at duty cycles greater than 0.5, the control scheme goes into sub-harmonic oscillations. To prevent this, an artificial slope is typically added to the current sense waveform. This slope compensation scheme will affect the accuracy of the LED current in the present form. However, a constant off-time peak current control scheme does not have this problem and can easily operate at duty cycles greater than 0.5 and also gives inherent input voltage rejection making the LED current almost insensitive to input voltage variations. But, it leads to variable frequency operation and the frequency range depends greatly on the input and output voltage variation. 9910B makes it easy to switch between the two modes of operation by changing one connection (see oscillator section).

Input Voltage Regulator

The 9910B can be powered directly from its VIN pin and can work from 8.0 - 450VDC at its VIN pin. When a voltage is applied at the VIN pin, the 9910B maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The 9910B can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear

regulator of the IC and the 9910B will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 12V.

Although the VIN pin of the 9910B is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an 8-pin SOIC (junction to ambient thermal resistance Rθ,j-a = 128°C/W) 9910B draws about IIN = 2.0mA from the VIN pin, and has a maximum allowable temperature rise of the junction temperature limited to about ΔT = 100°C, the maximum voltage at the VIN pin would be:

$$V_{IN(MAX)} = \frac{\Delta T}{R_{\theta ja}} * \frac{1}{I_{IN}}$$

$$= \frac{100°C}{128°C/W} * \frac{1}{2mA} = 390V$$

In these cases, to operate the 9910B from higher input voltages, a Zener diode can be added in series with the VIN pin to divert some of the power loss from the 9910B to the Zener diode. In the above example, using a 100V zener diode will allow the circuit to easily work up to 450V.

The input current drawn from the VIN pin is a sum of the 1.0mA current drawn by the internal circuit and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the external FET).

$$I_{IN} \approx 1.0mA + Q_G * f_S$$

In the above equation, fS is the switching frequency and QG is the GATE charge of the external FET which can be obtained from the datasheet of the FET

Current Sense

The current sense input of the 9910B goes to the noninverting inputs of two comparators. The inverting terminal of one comparator is tied to an internal 250mV reference whereas the inverting terminal of the other comparator is connected to the LD pin. The outputs of both these comparators are fed into an OR GATE and the output of the OR GATE is fed into the reset pin of the flip-flop. Thus, the comparator which has the lowest voltage at the inverting terminal determines when the GATE output is turned off.

The outputs of the comparators also include a 150-280ns blanking time which prevents spurious turn-offs of the external FET due to the turn-on spike normally present in peak current mode control. In rare cases, this internal blanking might not be enough to filter out the turn-on spike. In these cases, an

external RC filter needs to be added between the external sense resistor (RCS) and the CS pin.

Please note that the comparators are fast (with a typical 80ns response time). Hence these comparators are more susceptible to be triggered by noise than the comparators of the An9910. A proper layout minimizing external inductances will prevent false triggering of these comparators.

Oscillator

The oscillator in the 9910B is controlled by a single resistor connected at the RT pin. The equation governing the oscillator time period tOSC is given by

$$t_{OSC}(\mu s) = \frac{R_T(k\Omega) + 22}{25}$$

If the resistor is connected between RT and GND, 9910B operates in a constant frequency mode and the above equation determines the time-period. If the resistor is connected between RT and GATE, the 9910B operates in a constant off-time mode and the above equation determines the offtime.

GATE Output

The GATE output of the 9910B is used to drive an external FET. It is recommended that the GATE charge of the external FET be less than 25nC for switching frequencies ≤100kHz and less than 15nC for switching frequencies > 100kHz.

Linear Dimming

The Linear Dimming pin is used to control the LED current. There are two cases when it may be necessary to use the Linear Dimming pin.

► In some cases, it may not be possible to find the exact RCS value required to obtain the LED current when the internal 250mV is used. In these cases, an external voltage divider from the VDD pin can be connected to the LD pin to obtain a voltage (less than 250mV) corresponding to the desired voltage across RCS.

► Linear dimming may be desired to adjust the current level to reduce the intensity of the LEDs. In these cases, an external 0-250mV voltage can be connected to the LD pin to adjust the LED current during operation.

To use the internal 250mV, the LD pin can be connected to VDD.

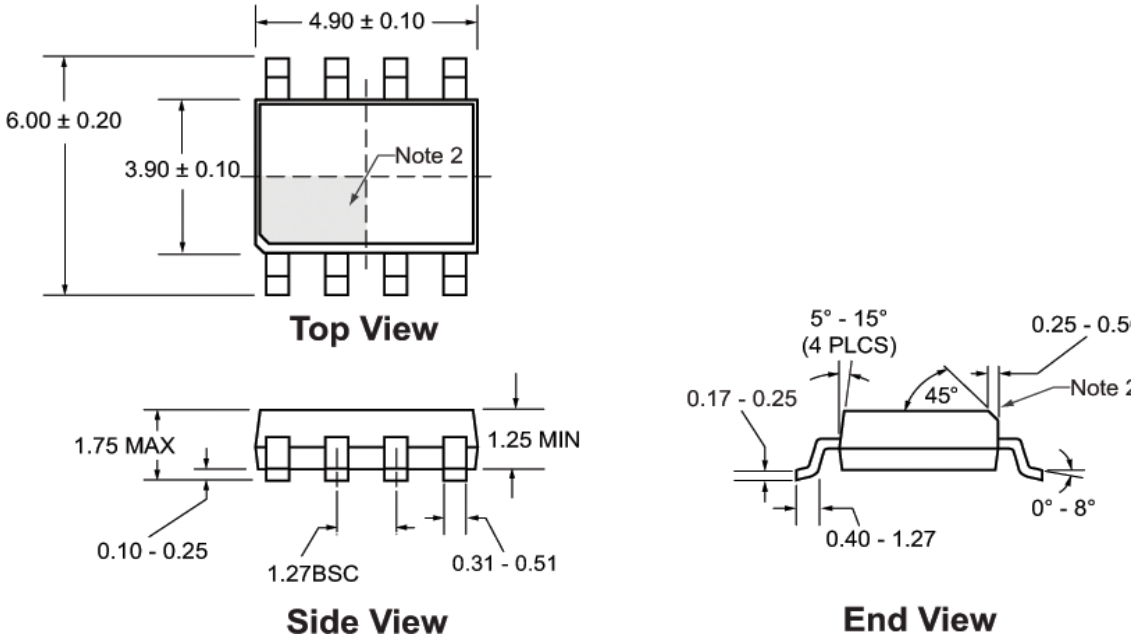
Note:
Although the LD pin can be pulled to GND, the output current will not go to zero. This is due to the presence of a minimum on-time (which is equal to the sum of the blanking time and the delay to output time) which is about 450ns. This will cause the FET to be on for a minimum of 450ns and thus the LED current when LD = GND will not be zero. This current is also dependent on the input voltage, inductance value, forward voltage of the LEDs and circuit parasitics. To get zero LED current, the PWMD pin has to be used.

PWM Dimming

PWM Dimming can be achieved by driving the PWMD pin with a low frequency square wave signal. When the PWM signal is zero, the GATE driver is turned off and when the PWMD signal if high, the GATE driver is enabled. Since the PWMD signal does not turn off the other parts of the IC, the response of the 9910B to the PWMD signal is almost instantaneous. The rate of rise and fall of the LED current is thus determined solely by the rise and fall times of the inductor current.

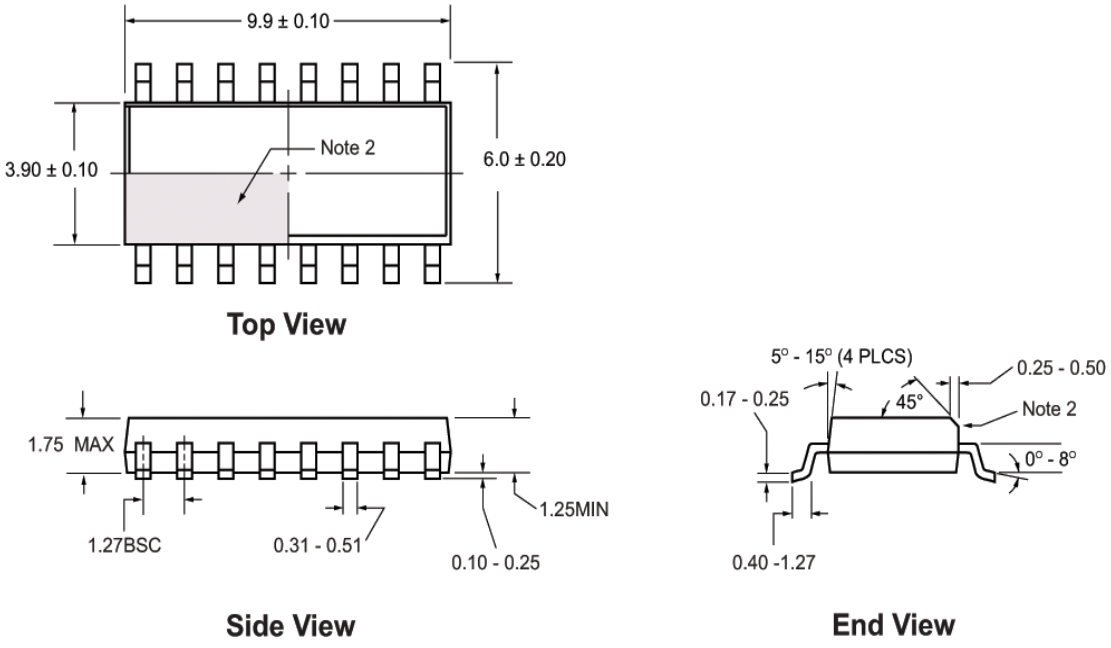
To disable PWM dimming and enable the 9910B permanently, connect the PWMD pin to VDD

8-Lead SO Package



Notes:
1. All dimensions in millimeters. Angles in degrees.
2. If the corner is not chamfered, then a Pin 1 identifier must be located within the area indicated.

16-Lead SO Package



Notes:
1. All dimensions in millimeters; angles in degrees
2. Pin 1 identifier must be located within the indicated area
3. Corner shape may differ from drawing