

## P61089 Series

### Description

P61089 Series has been especially designed to protect 2 new high voltage, as well as classical SLICs, against transient overvoltages. Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to -VBAT through the gate. This component presents a very low gate triggering current in order to reduce the current consumption on printed circuit board the firing phase. This devices are not subject to aging and provide a fail safe mode in short circuit for a better protection. Pic 1 and pic 2 are the device symbol and the package.

### Features and Benefits

- Dual Voltage-Tracking Protectors
- wide negative pressure range
- low dynamic switching voltage:  $V_{FP}$  and  $V_{DGL}$
- low gate triggering current:  $IGT=5mA_{Max}$
- high Holding current:  $I_H \geqslant 150mA$

### Application field

- P61089 Series are designed to protect communication equipment such as SPC exchanger from damaging overvoltage transients in the second level.

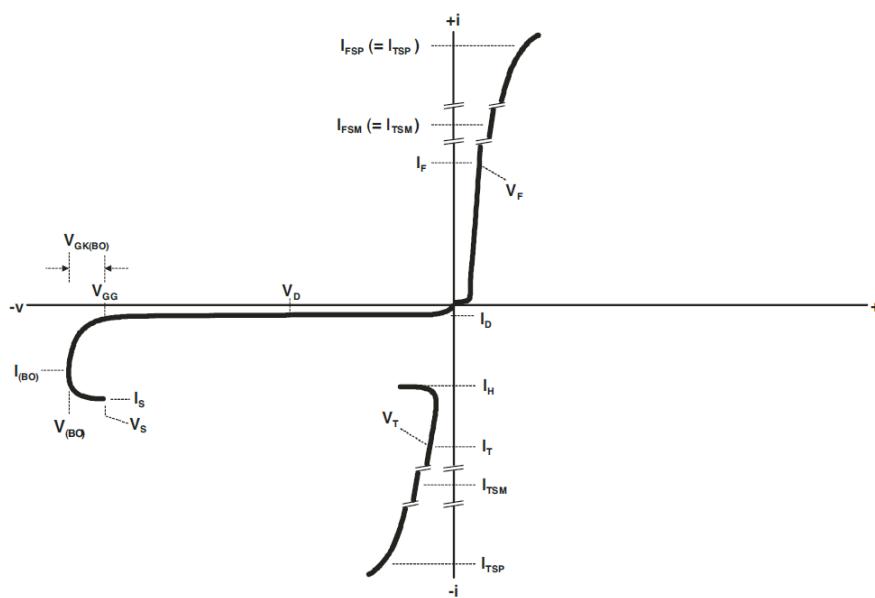
### Characteristic parameters

Part number	VMGL	IPP (10/1000μ s)	IH
P61089A	-170V	30A	150mA
P61089B	-167V	40A	
P61089C	-167V	100A	

### Electrical Characteristics (TA = 25 °C unless otherwise noted)

symbol	parameters	value			unit
		P61089A	P61089B	P61089C	
$I_{TSM}$	Non repetitive peak pulse Current (F=60Hz)	$t_p=500ms$	8	6.5	A
		$T=1s$	3.5	4.6	A
$I_{GSM}$	Maximum gate current (half sinusoid $t_p=10ms$ )	2	2	2	A
$V_{MLG}$	Line-ground maximum voltage	-170	-170	-170	V
$V_{MGL}$	Gate-line maximum voltage	-170	-167	-167	V
$T_{stg}$	Storage Temperature Range	-55~150	-55~150	-55~150	°C
$T_j$	maximum temperature	150	150	150	°C
$T_L$	maximum sustainable temperature of solder in 10 seconds	260	260	260	°C

## V-I characteristic curve(Ta= 25°C)



symbol	parameters
I <sub>GT</sub>	Gate trigger current
I <sub>H</sub>	Holding current
I <sub>RM</sub>	Line-ground reverse leakage current
I <sub>RG</sub>	Gate-line reverse leakage current
V <sub>RM</sub>	Line-ground reverse voltage
V <sub>F</sub>	Line-ground voltage
V <sub>GT</sub>	gate trigger voltage
V <sub>FP</sub>	Line-ground peak voltage
V <sub>DGL</sub>	Gate-line dynamic switching voltage
V <sub>GATE</sub>	Gate-ground voltage
V <sub>LG</sub>	Line-ground voltage
C	Line-ground off state capacitance

## Electrical Parameters

Absolute maximum ratings Ta= 25°C unless otherwise noted

### Line-ground diode parameters

symbol	Test conditions	Max.	unit
V <sub>F</sub>	I <sub>F</sub> =5A, t <sub>P</sub> =500μs	3	V
V <sub>FP</sub>	10/700μs 1.5kV R <sub>P</sub> =10Ω (tip. 1)	5	V

tip.1 • VFP refers to test circuit 2, RP is the protective resistance mounted on the card

### thyristor parameters (Ta=25°C)

symbol	Test conditions	Min.	Max.	unit
I <sub>GT</sub>	V <sub>GND</sub> /L <sub>INE</sub> =-100V	0.1	5	mA
I <sub>H</sub>	V <sub>GATE</sub> =-100V	150		mA
V <sub>GT</sub>	Same to I <sub>GT</sub>		2.5	V
I <sub>RG</sub>	T <sub>C</sub> =25°C V <sub>RG</sub> =-75V		5	μA
	T <sub>C</sub> =70°C V <sub>RG</sub> =-75V		50	
V <sub>DGL</sub>	V <sub>GATE</sub> =-100V (TIP.3) 10/700μs 1.5kV R <sub>P</sub> =10Ω		10	V

Tip.2:see holding current (IH)at test circuit 2;

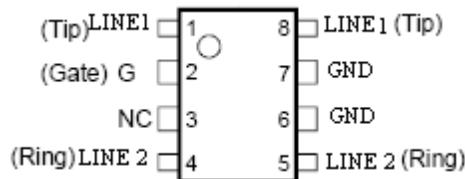
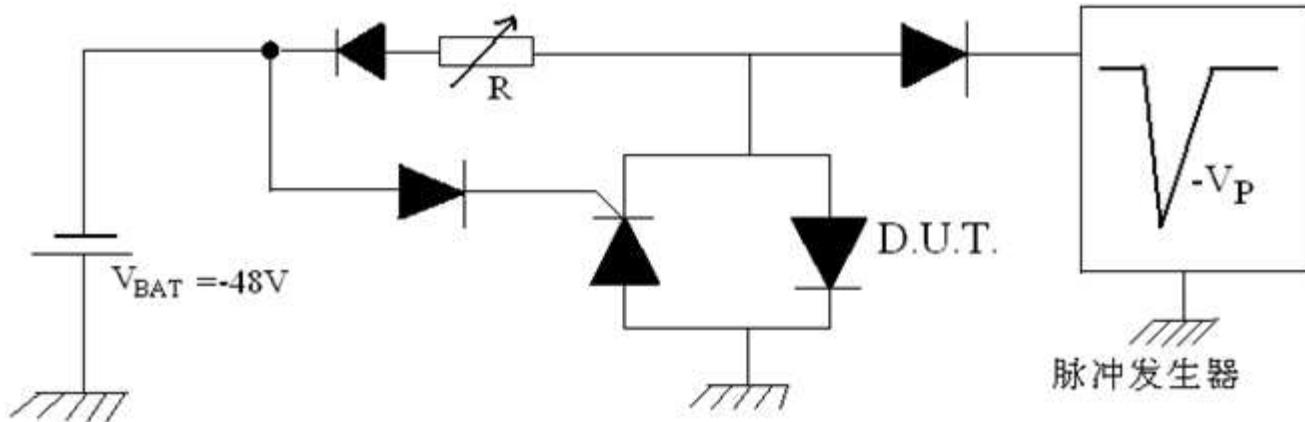
Tip.3:see VDGL at test circuit 1, Don't make records if fluctuation time is less than 50ns.

**thyristor and diode parameters**

Symbol	Test conditions	Max.	unit
I <sub>RM</sub>	T <sub>C</sub> =25°C V <sub>GATE</sub> /L <sub>INE</sub> =-1V V <sub>RM</sub> =-75	5	μA
	T <sub>C</sub> =70°C V <sub>GATE</sub> /L <sub>INE</sub> =-1V V <sub>RM</sub> = -75	50	μA
C	V <sub>R</sub> =-3V F=150KHZ	100	pF
	V <sub>R</sub> =-48V F=150KHZ	50	pF

**Attention**

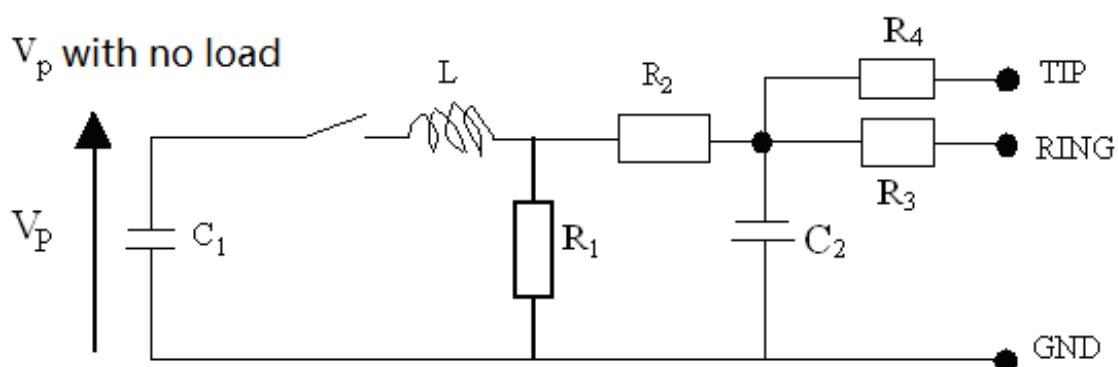
For eliminate the overvoltage from the line Parasitic induction, especially at the high speed and short moment signal, we make TIP and RING across the device.


**Test method and circuit**
**Holding current test circuit (test circuit1)**


This is a “Conducting-cutoff” test. The test circuit can ascertain the size of holding current.

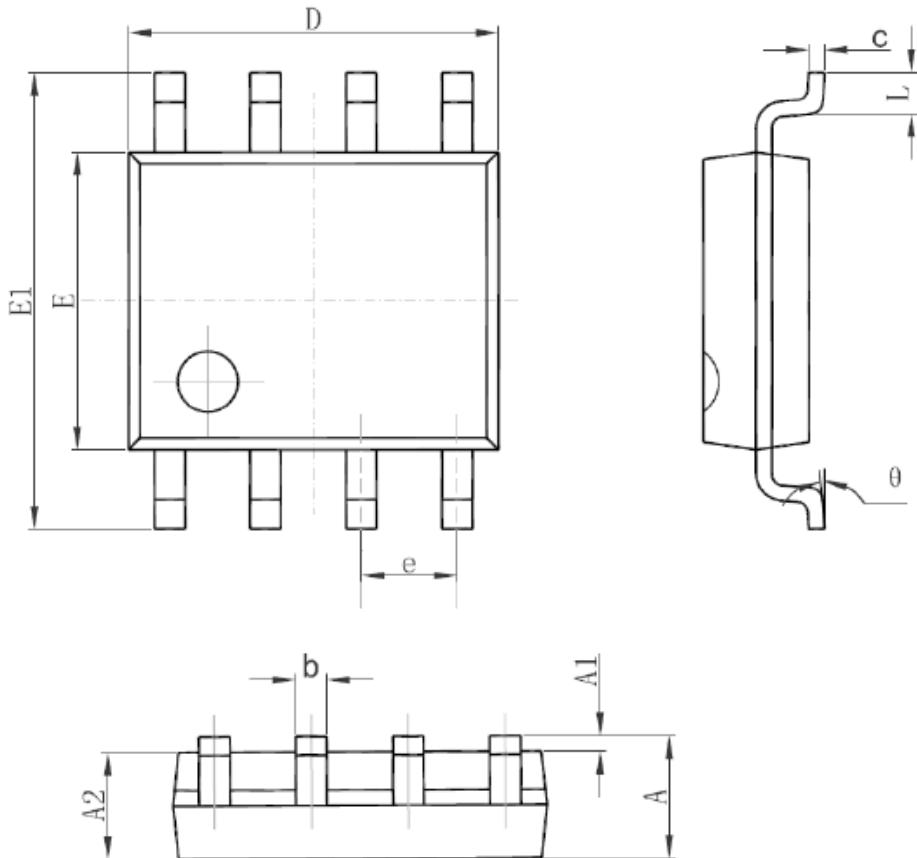
Test method :

- ① short out DUT, regulating current in IH range;
- ② let IPP=10A, 10/1000μs surge current triggers DUT;
- ③ DUT must return to the off-state in 50ms

**VFP and VDGL test circuit2**


Pluse(μs)		VP	C1	C2	L	R1	R2	R3	R4	IPP	RP
t <sub>r</sub>	t <sub>p</sub>	V	μF	nF	μH	Ω	Ω	Ω	Ω	A	Ω
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62

### Package size(SOP-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°