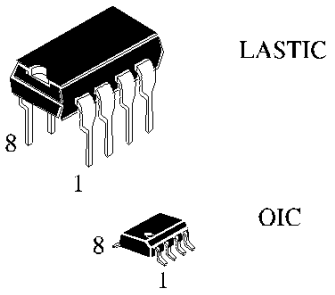
10 bit single channel digital to analog converter

DESCRIPTION

The HT5615A is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the HT5615A is over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The HT5615 is characterized for operation from 0°C to +70°C. The HT5615A is characterized for operation from –40°C to +85°C.

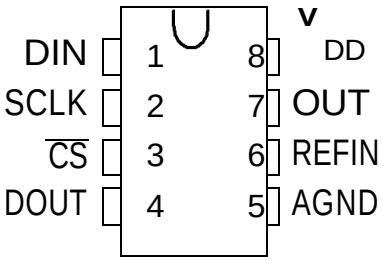


HT5615AN	**DIP8**
HT5615AR	**SOP8**

FEATURES

- **10-Bit CMOS Voltage Output DAC in an 8-Terminal Package**
- **5V Single Supply Operation**
- **3-Wire Serial Interface**
- **High-Impedance Reference Inputs**
- **Voltage Output Range: 2 Times the Reference Input Voltage**
- **Internal Power-On Reset**
- **Low Power Consumption: 1.75mW Max**
- **Update Rate of 1.21MHz**
- **Settling Time to 0.5LSB: 12.5μs Typ**
- **Monotonic Over Temperature**
- **Pin-Compatible With the Maxim MAX515**

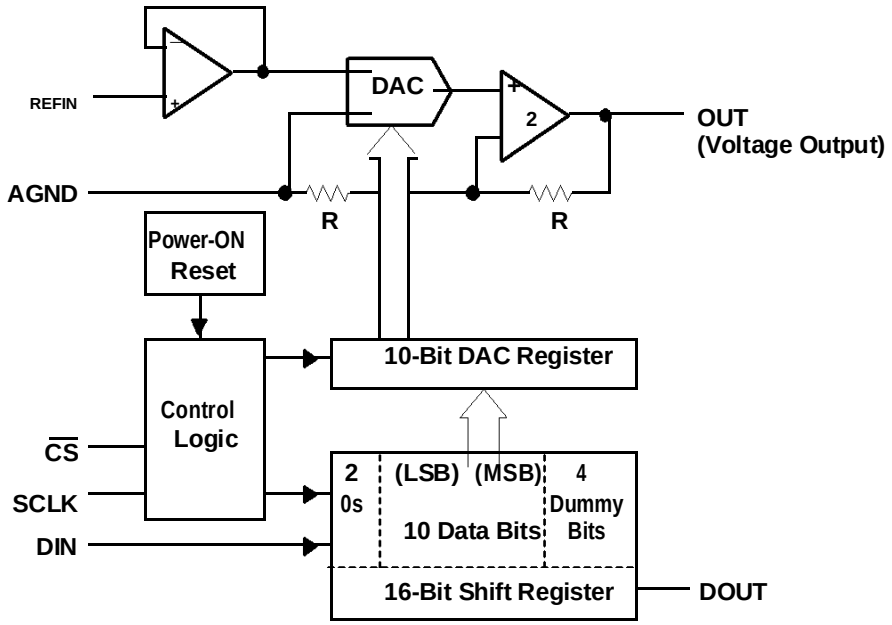
PIN ASSIGNMENT



APPLICATIONS

- **Battery-Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cellular Telephones**

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DIN	1	I	Serialdata input
SCLK	2	I	Serialclockinput
$\overline{CS}$	3	I	Chipselect,activelow
DOUT	4	O	Serialdata outputfordaisychaining
AGND	5		Analogground
REFIN	6	I	Referenceinput
OUT	7	O	DAC analogvoltageoutput
V_{DD}	8		Positivepowersupply

ABSOLUTE MAXIMUM RATINGS overoperatingfree-airtemperaturerange(unlessotherwisenoted)(1)

		UNIT
Supplyvoltage(V_{DD} to AGND)		7V
Digitalinputvoltagerangeto AGND		–0.3V to V_{DD} + 0.3V
Referenceinputvoltagerangeto AGND		–0.3V to V_{DD} + 0.3V
Outputvoltageat OUT fromexternalsource		V_{DD} + 0.3V
Continuouscurrentat any terminal		±20mA
Operatingfree-airtemperaturerange,T_A	HT5615	0°C to +70°C
	HT5615A	–40°C to +85°C
Storagetemperaturerange,T_{stg}		–65°C to +150°C
Lead temperature1,6mm (1/16 inch)fromcase for10 seconds		+260°C

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supplyvoltage,V_{DD}		4.5	5	5.5	V
High-leveldigitalinputvoltage,V_{IH}		2.4			V
Low-leveldigitalinputvoltage,V_{IL}				0.8	V
Referencevoltage,V_{ref} to REFIN terminal		2	2.048	V_{DD}–2	V
Loadresistance,R_L		2			k?
Operatingfree-airtemperature,T_A	HT5615	0		70	°C
	HT5615A	40		85	°C

ELECTRICAL CHARACTERISTICS

overrecommendedoperatingfree-airtemperaturerange,V_{DD} = 5V ± 5%, V_{ref} = 2.048V (unlessotherwisenoted)

STATIC DAC SPECIFICATIONS						
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10			bits
	Integralnonlinearity,end pointadjusted(INL)		V_{ref} = 2.048V, See (1)			±1	LSB
	Differentialnonlinearity(DNL)		V_{ref} = 2.048V, See (2)		±0.1	±0.5	LSB
E_{ZS}	Zero-scaleerror(offseterrorat zero scale)		V_{ref} = 2.048V, See (3)			±3	LSB
	Zero-scale-errortemperaturecoefficient		V_{ref} = 2.048V, See (4)		3		ppm/°C
E_G	Gain error		V_{ref} = 2.048V, See (5)			±3	LSB
	Gain-errortemperaturecoefficient		V_{ref} = 2.048V, See (6)		1		ppm/°C
PSRR	Power-supplyrejectionratio	Zero scale	See (7)(8)	80			dB
		Gain		80			
	AnalogfullscaleOutput		R_L = 100k?		$2V_{ref}$(1023/1024)		V

(1) The relativeaccuracyor integralnonlinearity(INL), sometimesreferredto as linearityerror,is the maximumdeviationof the outputfrom the linebetweenzero and fullscaleexcludingthe effectsof zero codeand full-scaleerrors(see text). Testedfromcode3 to code1024.

(2) The differentialnonlinearity(DNL), sometimesreferredto as differentialerror,is the differencebetweenthe measuredand ideal1LSB amplitudechangeof any twoadjacentcodes.Monotonicmeansthe outputvoltagechangesin the same direction(or remainsconstant) as a changein the digitalinputcode. Testedfromcode3 to code1024.

(3) Zero-scaleerroris the deviationfromzero-voltageoutputwhenthe digitalinputcodeis zero (see text).

(4) Zero-scale-errortemperaturecoefficientis givenby:E_{ZS} TC = [E_{ZS} (T_{max}) – E_{ZS} (T_{min})]/V_{ref} · 10^6/(T_{max}– T_{min}).

(5) Gain erroris the deviationfromthe idealoutput(V_{ref} – 1LSB) withan outputloadof10k? excludingthe effectsof the zero-scaleerror.

(6) Gain temperaturecoefficientis givenby:E_G TC = [E_G(T_{max}) – E_G (T_{min})]/V_{ref} · 10^6/(T_{max}– T_{min}).

(7) Zero-scale-errorrejectionratio(EZS-RR) is measuredby varyingthe V_{DD} from4.5V to 5.5V dc and measuringthe proportionof this signalimposedon the zero-codeoutputvoltage.

(8) Gain-errorrejectionratio(EG-RR) is measuredby varyingthe V_{DD} from4.5V to 5.5V dc and measuringthe proportionof thissignal imposedon the full-scaleoutputvoltageaftersubtractingthe zero-scalechange.

VOLTAGE OUTPUT (OUT)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltageoutputrange	R_L= 10k?		0		V_{DD}–0.4	V
	Outputloadregulationaccuracy	$V_{O(OUT)}$ = 2V,	R_L = 2k?			0.5	LSB
I_{OSC}	Outputshortcircuitcurrent	OUT to V_{DD} or AGND			20		mA
$V_{OL(low)}$	Outputvoltage,low-level	$I_{O(OUT)}$? 5mA				0.25	V
$V_{OH(high)}$	Outputvoltage,high-level	$I_{O(OUT)}$?= 5mA		4.75			V
REFERENCE INPUT (REFIN)							
V_I	Inputvoltage			0		V_{DD}–2	V
r_i	Inputresistance			10			M?
C_i	Inputcapacitance				5		pF
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)							
V_{IH}	High-leveldigitalinputvoltage			2.4			V
V_{IL}	Low-leveldigitalinputvoltage					0.8	V
I_{IH}	High-leveldigitalinputcurrent	$V_I = V_{DD}$				±1	∝A
I_{IL}	Low-leveldigitalinputcurrent	V_I = 0				±1	∝A
C_i	Inputcapacitance				8		pF
DIGITAL OUTPUT (DOUT)							
V_{OH}	Outputvoltage,high-level	I_O = –2mA		V_{DD}–1			V
V_{OL}	Outputvoltage,low-level	I_O = 2mA				0.4	V
POWER SUPPLY							
V_{DD}	Supplyvoltage			4.5	5	5.5	V
I_{DD}	Powersupplycurrent	V_{DD} = 5.5V, No load, Allinputs= 0V or V_{DD}	V_{ref} = 0		150	250	∝A
		V_{DD}= 5.5V, No load, Allinputs= 0V or V_{DD}	V_{ref} = 2.048V		230	350	∝A
ANALOG OUTPUT DYNAMIC PERFORMANCE							
	Signal-to-noise+ distortion,S/(N+D)	V_{ref} = 1V_{PP} at 1kHz + 2.048Vdc, code= 11 1111 1111 (1)		60			dB

(1) The limitingfrequencyvalueat 1V_{PP} is determinedby the output-amplifierslewrate.

DIGITAL INPUT TIMING REQUIREMENTS

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(DS)}$	Setuptime,DIN beforeSCLK high	45			ns
$t_{h(DH)}$	Holdtime,DIN validafterSCLK high	0			ns
$t_{su(CSS)}$	Setuptime,$\overline{CS}$ lowto SCLK high	1			ns
$t_{su(CS1)}$	Setuptime,$\overline{CS}$ highto SCLK high	50			ns
$t_{h(CSH0)}$	Holdtime,SCLK lowto $\overline{CS}$ low	1			ns
$t_{h(CSH1)}$	Holdtime,SCLK lowto $\overline{CS}$ high	0			ns
$t_{w(CS)}$	Pulseduration,minimumchipselectpulsewidthhigh	20			ns
$t_{w(CL)}$	Pulseduration,SCLK low	25			ns
$t_{w(CH)}$	Pulseduration,SCLK high	25			ns

OUTPUT SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{pd(DOUT)}$	Propagationdelaytime,DOUT	C_L = 50pF			50	ns

OPERATING CHARACTERISTICS

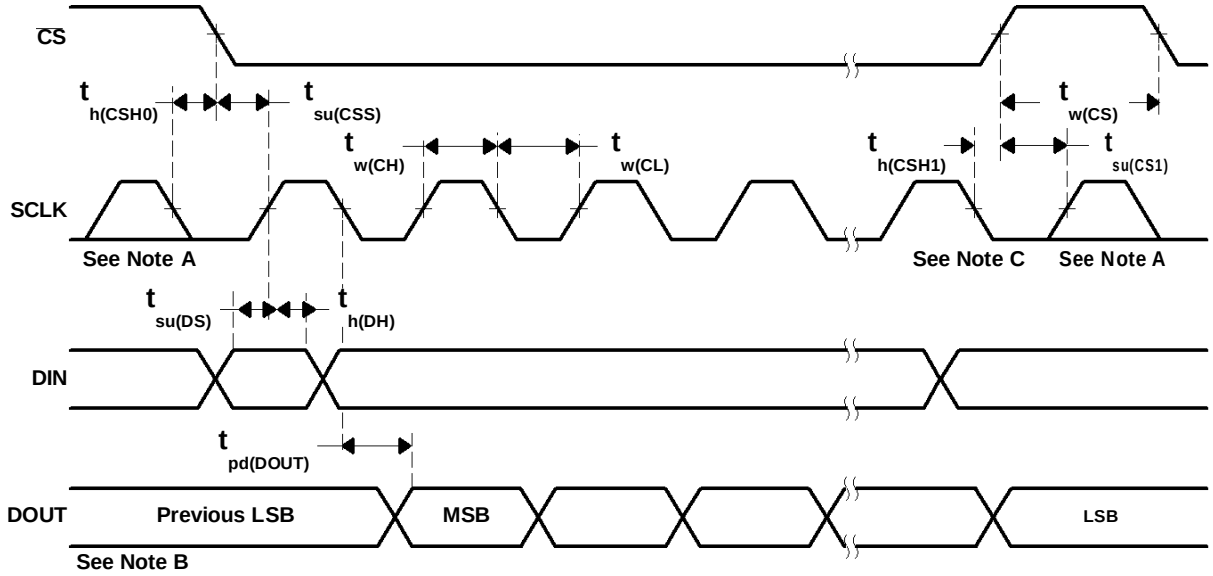
over recommended operating free-air temperature range, V_{DD} = 5V ±5%, V_{ref} = 2.048V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT DYNAMIC PERFORMANCE						
SR	Output slew rate	C_L = 100pF, R_L = 10kΩ, T_A = +25°C	0.3	0.5		V/μs
t_s	Output settling time	To 0.5LSB, R_L = 10kΩ, C_L = 100pF, (1)		12.5		μs
	Glitch energy	DIN = All 0s to all 1s		5		nV-s
REFERENCE INPUT (REFIN)						
	Reference feedthrough	REFIN = 1V_{PP} at 1kHz + 2.048Vdc (2)		–80		dB
	Reference input bandwidth (-3dB)	REFIN = 0.2Vpp + 2.048Vdc		30		kHz

(1) Settling time is the time for the output signal to remain within ±0.5LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex

(2) Reference feedthrough is measured at the DAC output with an input code = 000 hex and a V_{ref} input = 2.048Vdc + 1V_{pp} at 1kHz.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when CS is high to minimize clock feedthrough.

B. Data input from preceeding conversion cycle.

C. Sixteenth SCLK falling edge

Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

OUTPUT SINK CURRENT
vs
OUTPUT PULLDOWN VOLTAGE

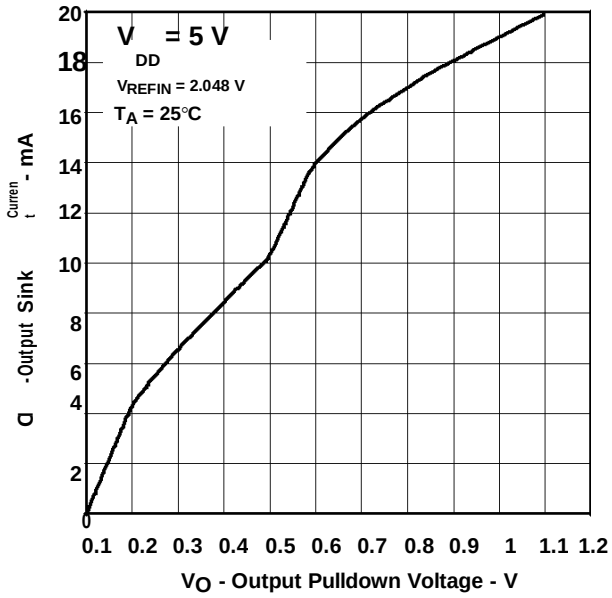


Figure 2.

OUTPUT SOURCE CURRENT
vs
OUTPUT PULLUP VOLTAGE

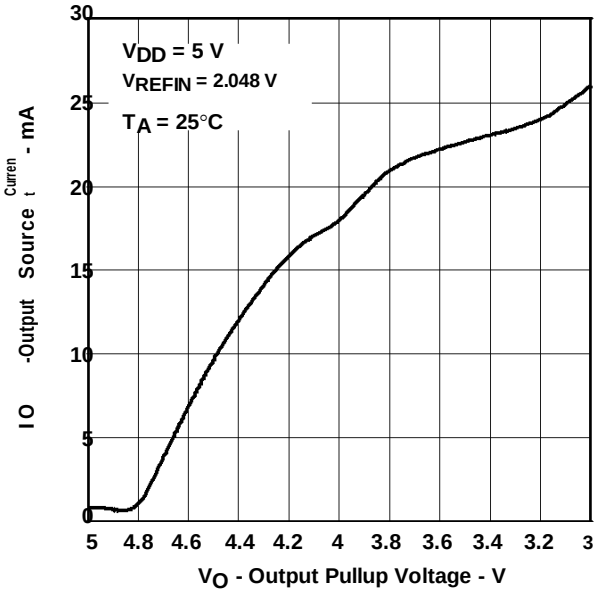


Figure 3.

SUPPLY CURRENT
vs
TEMPERATURE

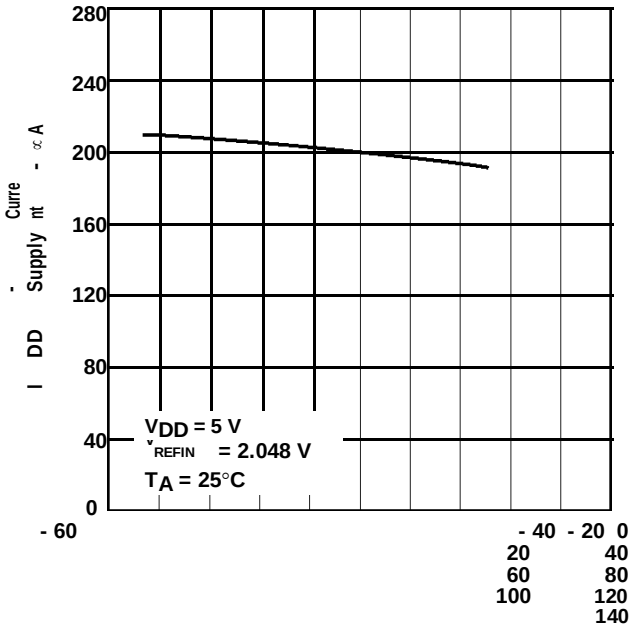


Figure 4.

VREFIN TO V(OUT) RELATIVE GAIN
vs
INPUT FREQUENCY

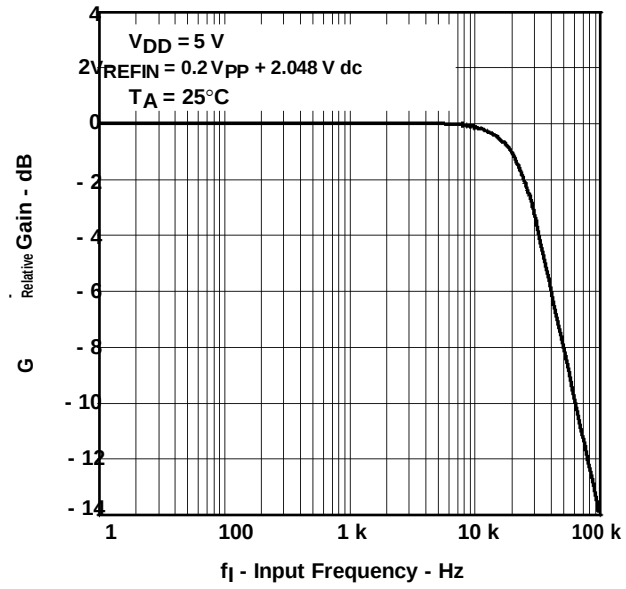


Figure 5.

TYPICAL CHARACTERISTICS (continued)

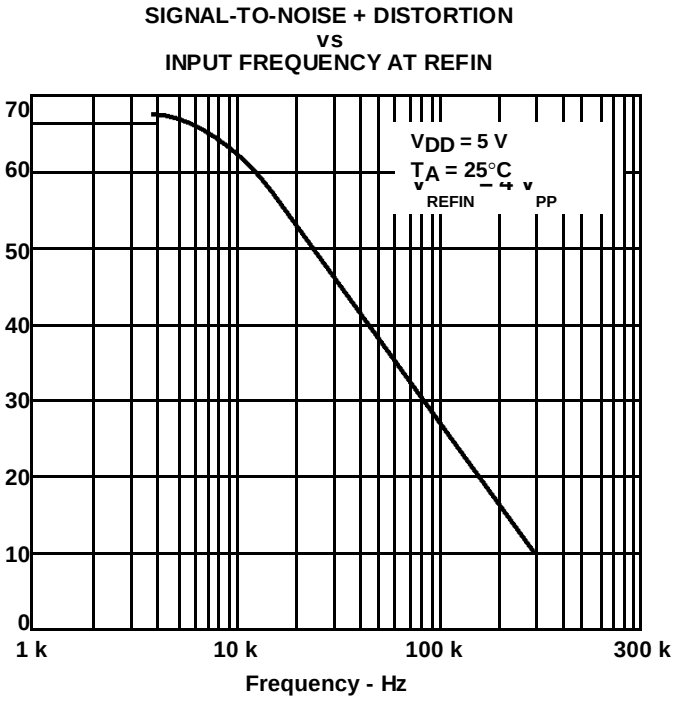


Figure 6.

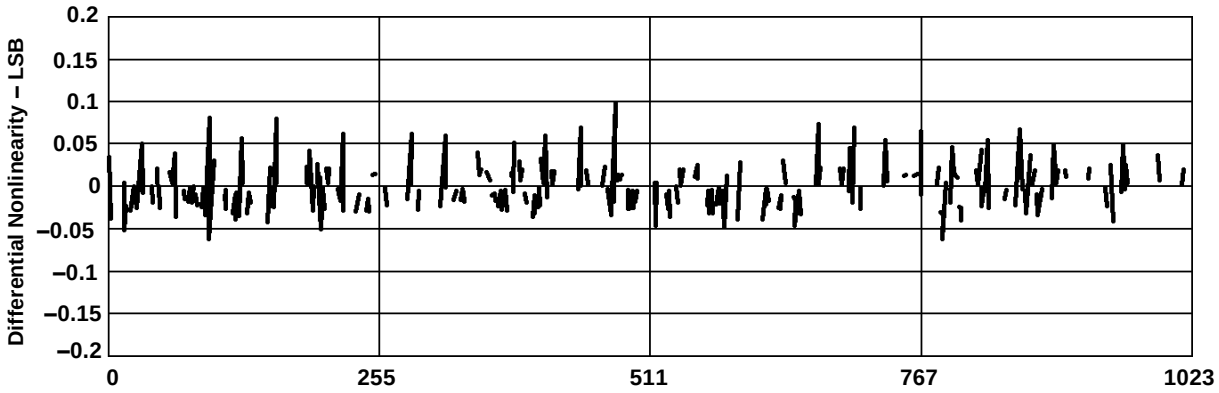


Figure 7. Differential Nonlinearity With Input Code

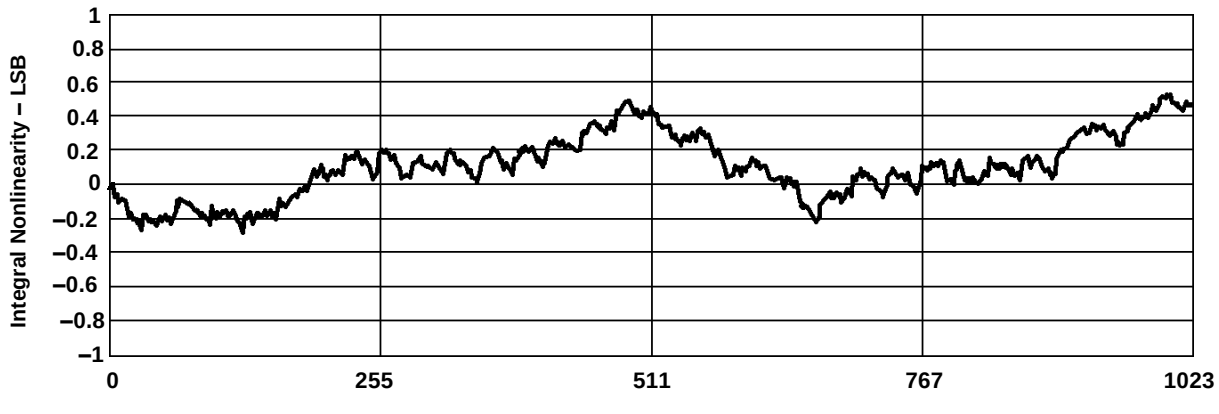


Figure 8. Integral Nonlinearity With Input Code

APPLICATION INFORMATION

GENERAL FUNCTION

The HT5615A uses a resistor string network buffered with an op amp in a fixed gain of 2 to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 9). The output of the HT5615A is the same polarity as the reference input (see Table 1).

An internal circuit resets the DAC register to all zeros on power up.

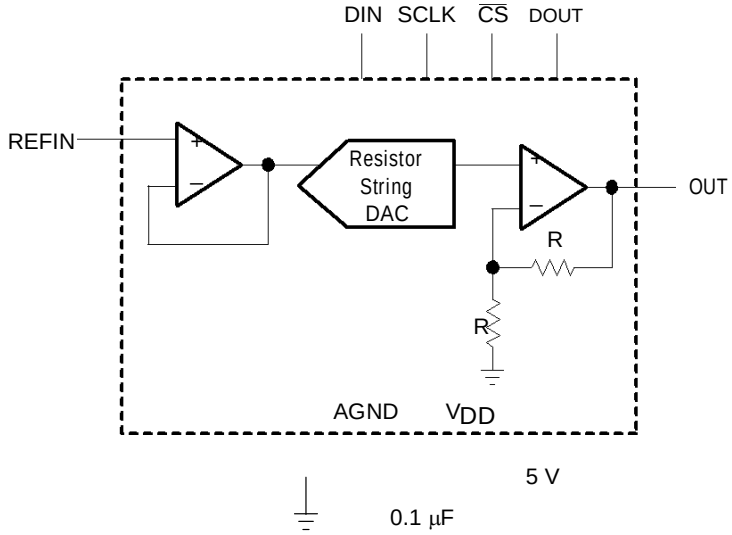


Figure 9. HT5615A Typical Operating Circuit

Table 1. Binary Code Table (0V to 2V $_{REFIN}$ Output) , Gain = 2

INPUT(1)			OUTPUT
1111	1111	11(00)	$2\ V_{REFIN}\ \frac{1023}{1024}$
	:		:
1000	0000	01(00)	$2\ V_{REFIN}\ \frac{513}{1024}$
1000	0000	00(00)	$2\ V_{REFIN}\ \frac{512}{1024} + V_{REFIN}$
0111	1111	11(00)	$2\ V_{REFIN}\ \frac{511}{1024}$
	:		:
0000	0000	01(00)	$2\ V_{REFIN}\ \frac{1}{1024}$
0000	0000	00(00)	0 V

(1) A 10-bit data word with two bits below the LSB bit (sub-LSB) with 0 values must be written since the DAC input latch is 12 bits wide.

BUFFER AMPLIFIER

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2kΩ load with a 100pF load capacitance. Settling time is 12.5μs typical to within 0.5LSB of final value.

EXTERNAL REFERENCE

The reference voltage input is buffered, which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10MΩ and the REFIN input capacitance is typically 5pF independent of input code. The reference voltage determines the DAC full-scale output.

LOGIC INTERFACE

The logic inputs function with either TTL or CMOS logic levels. However, using rail-to-rail CMOS logic achieves the lowest power dissipation. The power requirement increases by approximately 2 times when using TTL logic levels.

SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the HT5615A timing. The maximum serial clock rate is:

$$f_{(SCLK)max} = \frac{1}{t_{w\,CH} + t_{w\,CL}}$$

or approximately 14MHz. The digital update rate is limited by the chip-select period, which is:

$$t_{p(CS)} = 16 \times (t_{w\,CH} + t_{w\,CL}) + t_{w\,CS}$$

and is equal to 820ns which is a 1.21MHz update rate. However, the DAC settling time to 10 bits of 12.5μs limits the update rate to 80kHz for full-scale input step transitions.

SERIAL INTERFACE

When chip select ($\overline{CS}$) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The rising edge of the SLCK input shifts the data into the input register.

The rising edge of $\overline{CS}$ then transfers the data to the DAC register. When $\overline{CS}$ is high, input data cannot be clocked into the input register. All $\overline{CS}$ transitions should occur when the SCLK input is low.

If the daisy chain (cascading) function (see daisy-chaining devices section) is not used, a 12-bit input data sequence with the MSB first can be used as shown in Figure 10:

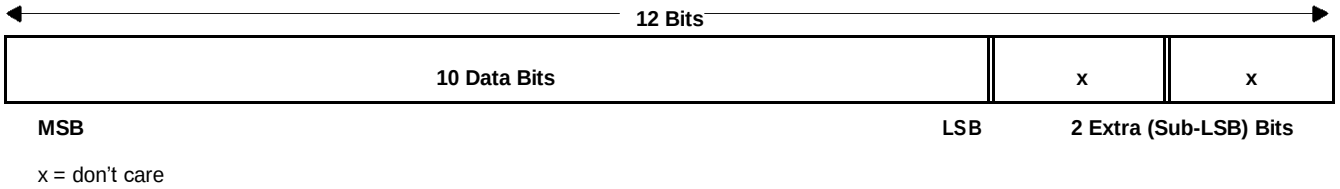


Figure 10. 12-Bit Input Data Sequence

or 16 bits of data can be transferred as shown in Figure 11 with the 4 upper dummy bits first.

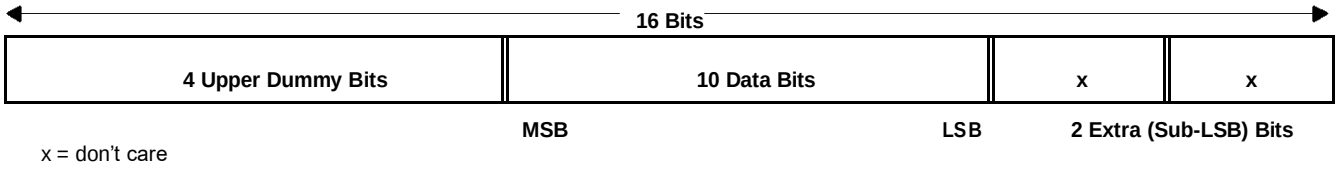


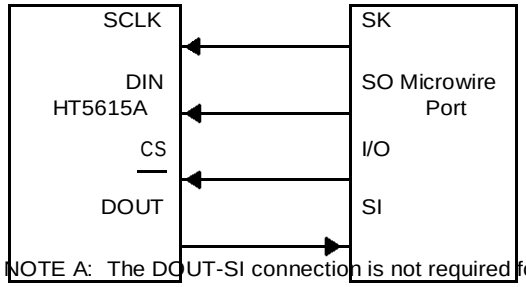
Figure 11. 16-Bit Input Data Sequence

The data from DOUT requires 16 falling edges of the input clock and, therefore, requires an extra clock width. When daisy chaining multiple HT5615A devices, the data requires 4 upper dummy bits because the data transfer requires 16 input-clock cycles plus one additional input-clock falling edge to clock out the data at the DOUT terminal (see Figure 1).

The two extra (sub-LSB) bits are always required to provide hardware and software compatibility with 12-bit data converter transfers.

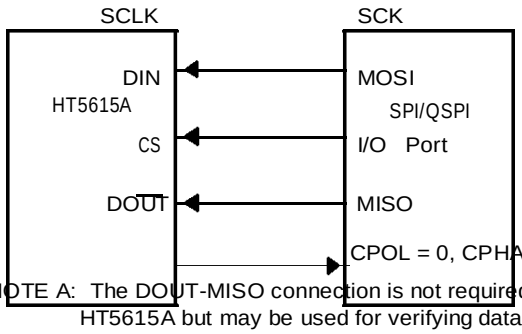
The HT5615A three-wire interface is compatible with the SPI, QSPI, and Microwire serial standards. The hardware connections are shown in Figure 12 and Figure 13.

The SPI and Microwire interfaces transfer data in 8-bit bytes; therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.



NOTE A: The DOUT-SI connection is not required for writing to the HT5615A but may be used for verifying data transfer if desired.

Figure 12. Microwire Connection



NOTE A: The DOUT-MISO connection is not required for writing to the HT5615A but may be used for verifying data transfer.

Figure 13. SPI/QSPI Connection

DAISY-CHAINING DEVICES

DACs can be daisy-chained by connecting the DOUT terminal of one device to the DIN of the next device in the chain, providing that the setup time, $t_{su(CSS)}$ (CS low to SCLK high), is greater than the sum of the setup time, $t_{su(DS)}$, plus the propagation delay time, $t_{pd(DOUT)}$, for proper timing (see digital input timing requirements section). The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. DOUT is a totem-poled output for low power. DOUT changes on the SCLK falling edge when CS is low. When CS is high, DOUT remains at the value of the last data bit and does not go into a high-impedance state.

LINEARITY, OFFSET, AND GAIN ERROR USING SINGLE -ENDED SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.

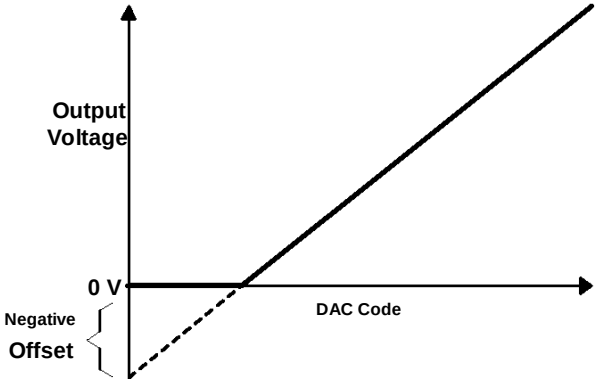


Figure 14. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs '0')and full-scale code (all inputs '1')after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. For the HT5615A, the zero-scale (offset) error is ±3LSB maximum. The code is calculated from the maximum specification for the negative offset.

POWER-SUPPLY BYPASSING AND GROUND MANAGEMENT

Printed circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 15 shows the ground plane layout and bypassing technique.

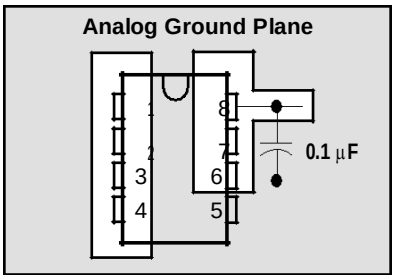


Figure 15. Power-Supply Bypassing

SAVING POWER

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

AC CONSIDERATIONS

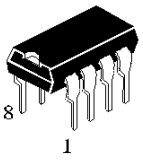
Digital Feedthrough

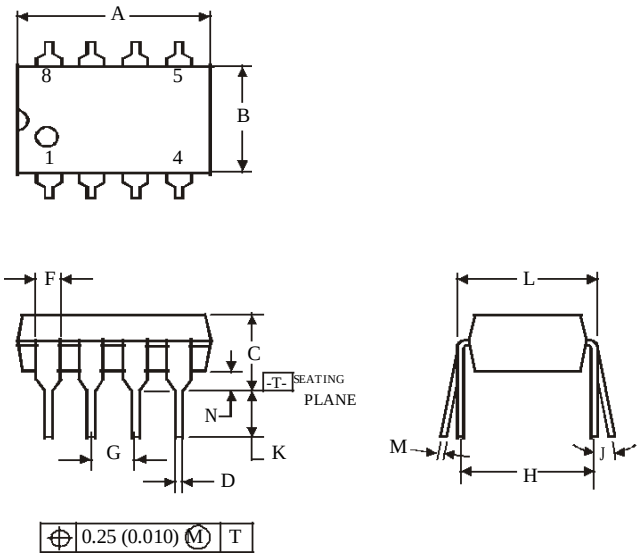
Even with $\overline{CS}$ high, high-speed serial data at any of the digital input or output terminals may couple through the DAC package internal stray capacitance and appear at the DAC analog output as digital feedthrough. Digital feedthrough is tested by holding CS high and transmitting 0101010101 from DIN to DOUT.

Analog Feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding CS high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.

(DIP8)





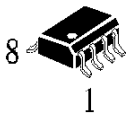
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0 °	10 °
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

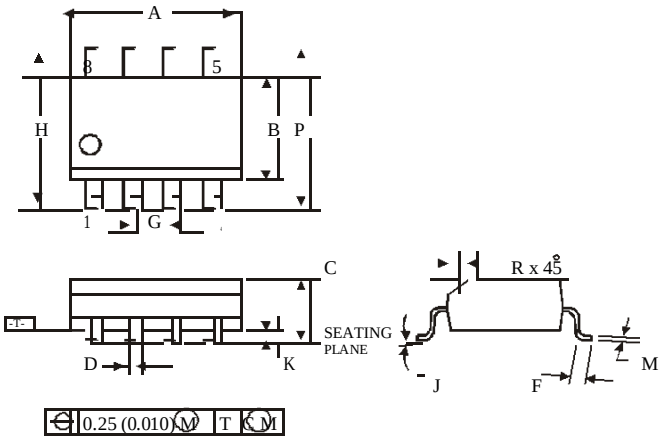
NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

(SOP8)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	4.8	5
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0 °	8 °
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.