# RX65N Group, RX651 Group
Renesas MCUs

R01DS0276EJ0230
Rev.2.30
Jun 20, 2019

120-MHz 32-bit RX MCU, on-chip FPU, 240 DMIPS, up to 2-MB flash memory (supportive of the dual bank function), 640-KB SRAM, various communications interfaces including Ethernet MAC, SD host interface (optional), SD slave interface (optional), quad SPI, and CAN, 12-bit A/D converter, RTC, Encryption functions (optional), CMOS camera interface, Graphic-LCD controller, 2D drawing engine

## Features

### ■ 32-bit RXv2 CPU core
- Max. operating frequency: 120 MHz
  Capable of 240 DMIPS in operation at 120 MHz
- Single precision 32-bit IEEE-754 floating point
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

### ■ Low-power design and architecture
- Operation from a single 2.7- to 3.6-V supply
- Low power consumption: A product that supports all peripheral functions draws only 0.19 mA/MHz (Typ.).
- RTC is capable of operation from a dedicated power supply.
- Four low-power modes

### ■ On-chip code flash memory
- Supports versions with up to 2 Mbytes of ROM
- No wait cycles at up to 50 MHz or when the ROM cache is hit, one-wait state at up to 100 MHz, two-wait state at above 100 MHz
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

### ■ On-chip data flash memory
- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

### ■ On-chip SRAM, no wait states
- 256K/640 Kbytes of SRAM (no wait states)
- 8 Kbytes of standby RAM (backup on deep software standby)

### ■ Data transfer
- DMACAa: 8 channels
- DTCb: 1 channel
- EXDMAC: 2 channels
- DMAC for the Ethernet controller: 1 channel

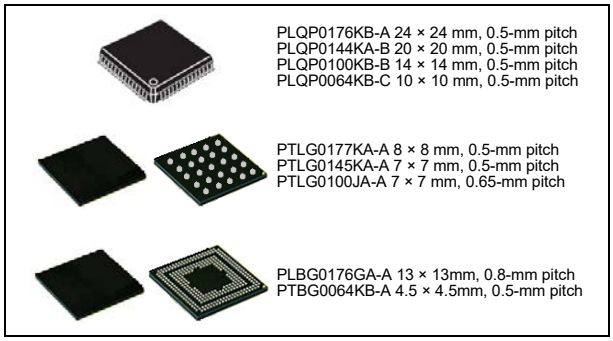
### ■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

### ■ Clock functions
- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

### ■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture function
  (for capturing times in response to event-signal input)

### ■ Independent watchdog timer
- 120-kHz (1/2 LOCO frequency) clock operation

### ■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, frequency measurement, CRCA, IWDTa, self-diagnostic function for the A/D converter, etc.
- Register write protection function can protect values in important registers against overwriting.




### ■ Various communications interfaces
- Ethernet MAC (1 channel)
- PHY layer (1 channel) for host/function or OTG controller (1 channel) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (up to 2 channels)
- SCIg and SCIh with multiple functionalities (up to 11 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I²C, and extended serial mode.
- SCIi with 16-byte transmission and reception FIFOs (up to 2 channels)
- I²C bus interface for transfer at up to 1 Mbps (up to 3 channels)
- Four-wire QSPI (1 channel) in addition to RSPIc (3 channels)
- Parallel data capture unit (PDC) for the CMOS camera interface
- Graphic-LCD controller (GLCDC)
- 2D drawing engine (DRW2D)
- SD host interface (optional: 1 channel) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- SD slave interface (optional: 1 channel) with a 1- or 4-bit SD bus for use with SD host interface
- MMCIF with 1-, 4-, or 8-bit transfer bus width

### ■ External address space
- Buses for full-speed data transfer (max. operating frequency of 60 MHz)
- 8 CS areas
- 8-, 16-, or 32-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

### ■ Up to 25 extended-function timers
- 16-bit TPUa, MTU3a
- 8-bit TMRa (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

### ■ 12-bit A/D converter
- Two 12-bit units (8 channels for unit 0; 21 channels for unit 1)
- Self diagnosis, detection of analog input disconnection

### ■ 12-bit D/A converter: 2 channels

### ■ Temperature sensor for measuring temperature within the chip

### ■ Encryption functions (optional)
- AES (key lengths: 128, 192, and 256 bits)
- Trusted Secure IP (TSIP)

### ■ Up to 136 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

### ■ Operating temp. range
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C

# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.

Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package and the capacity of the code flash memory. For details, see Table 1.2, Code Flash Memory Capacity and Comparison of Functions for Different Packages.

**Table 1.1 Outline of Specifications (1/10)**

| Classification | Module/Function | Description |
|---|---|---|
| CPU | CPU | • Maximum operating frequency: 120 MHz<br>• 32-bit RX CPU (RXv2)<br>• Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>• Address space: 4-Gbyte linear<br>• Register set of the CPU<br>General purpose: Sixteen 32-bit registers<br>Control: Ten 32-bit registers<br>Accumulator: Two 72-bit registers<br>• Basic instructions: 75<br>• Floating-point instructions: 11<br>• DSP instructions: 23<br>• Addressing modes: 11<br>• Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>• On-chip 32-bit multiplier: 32 × 32 → 64 bits<br>• On-chip divider: 32 / 32 → 32 bits<br>• Barrel shifter: 32 bits |
| | FPU | • Single precision (32-bit) floating point<br>• Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | Code flash memory | • Capacity: 512 Kbytes/768 Kbytes/1 Mbyte/1.5 Mbytes/2 Mbytes<br>• 50 MHz ≤ No-wait cycle access<br>100 MHz ≤ 1-wait cycle access<br>100 MHz > 2-wait cycle access<br>• Instructions hitting the ROM cache or operand = 120 MHz: No-wait access<br>• On-board programming: Four types<br>• Off-board programming (parallel programmer mode)<br>• Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized.<br>• A dual-bank structure allows programming during reading or exchanging the start-up areas |
| | Data flash memory | • Capacity: 32 Kbytes<br>• Programming/erasing: 100,000 times |
| | Unique ID | • 16-byte unique ID for the device |
| | RAM | • Capacity: 256 Kbytes (Products with 1 Mbyte of code flash memory or less)<br>RAM: 256 Kbytes<br>• Capacity: 640 Kbytes (Products with at least 1.5 Mbytes of code flash memory)<br>RAM: 256 Kbytes<br>Expansion RAM: 384 Kbytes<br>• 120 MHz, no-wait access |
| | Standby RAM | • Capacity: 8 Kbytes<br>• Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access |

**Table 1.1 Outline of Specifications (2/10)**

| Classification | Module/Function | Description |
|---|---|---|
| Operating modes | | • Operating modes by the mode-setting pins at the time of release from the reset state<br>Single-chip mode<br>Boot mode (for the SCI interface)<br>Boot mode (for the USB interface)<br>Boot mode (for the FINE interface)<br>• Selection of operating mode by register setting<br>Single-chip mode<br>On-chip ROM disabled extended mode<br>On-chip ROM enabled extended mode<br>• Endian selectable |
| Clock | Clock generation circuit | • Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator<br>• The peripheral module clocks can be set to frequencies above that of the system clock.<br>• Main-clock oscillation stoppage detection<br>• Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK)<br>The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz<br>Peripheral modules of MTU3, RSPI, SCIi, ETHERC, EDMAC, AES, GLCDC, and DRW2D run in synchronization with PCLKA, which operates at up to 120 MHz.<br>Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz<br>ADCLK in the S12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz<br>ADCLK in the S12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz<br>Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz<br>Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz<br>• Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit |
| Reset | | Nine types of reset<br>• RES# pin reset: Generated when the RES# pin is driven low.<br>• Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises.<br>• Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby.<br>• Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs.<br>• Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs.<br>• Software reset: Generated by register setting. |
| Power-on reset | | If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled. |
| Voltage detection circuit (LVDA) | | Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or interrupt.<br>• Voltage detection circuit 0<br>Capable of generating an internal reset<br>The option-setting memory can be used to select enabling or disabling of the reset.<br>Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, 2.80 V)<br>• Voltage detection circuits 1 and 2<br>Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, 2.85 V)<br>Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency)<br>Capable of generating an internal reset<br>• Two types of timing are selectable for release from reset<br>An internal interrupt can be requested.<br>• Detection of voltage rising above and falling below thresholds is selectable.<br>• Maskable or non-maskable interrupt is selectable<br>Voltage detection monitoring<br>Event linking |

**Table 1.1 Outline of Specifications (3/10)**

| Classification | Module/Function | Description |
|---|---|---|
| Low power consumption | Low power consumption function | • Module stop function<br>• Four low power consumption modes<br>Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |
| | Battery backup function | • When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating. |
| Interrupt | Interrupt controller (ICUB) | • Peripheral function interrupts: 262 sources<br>• External interrupts: 16 (pins IRQ0 to IRQ15)<br>• Software interrupts: 2 sources<br>• Non-maskable interrupts: 7 sources<br>• Sixteen levels specifiable for the order of priority<br>• Method of interrupt source selection:<br>The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 128 vectors are selected from among the other 123 sources.) |
| External bus extension | | • The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings.<br>Capacity of each area: 16 Mbytes (CS0 to CS7)<br>A chip-select signal (CS0# to CS7#) can be output for each area.<br>Each area is specifiable as an 8-, 16-, or 32-bit bus space.<br>The data arrangement in each area is selectable as little or big endian (only for data).<br>• SDRAM interface connectable<br>• Bus format: Separate bus, multiplex bus<br>• Wait control<br>• Write buffer facility |
| DMA | DMA controller (DMACAa) | • 8 channels<br>• Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| | EXDMA controller (EXDMACa) | • 2 channels<br>Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer<br>• Single-address transfer enabled with the EDACKn signal<br>• Request sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions |
| | Data transfer controller (DTCb) | • Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Request sources: External interrupts and interrupt requests from peripheral functions<br>• Sequence transfer |

**Table 1.1 Outline of Specifications (4/10)**

| Classification | Module/Function | Description |
|---|---|---|
| I/O ports | Programmable I/O ports | • I/O ports for the 177-pin TFLGA, 176-pin LFBGA, and 176-pin LFQFP<br>I/O pins: 136<br>Input pin: 1<br>Pull-up resistors: 136<br>Open-drain outputs: 136<br>5-V tolerance: 19<br>• I/O ports for the 145-pin TFLGA and 144-pin LFQFP<br>I/O pins: 111<br>Input pin: 1<br>Pull-up resistors: 111<br>Open-drain outputs: 111<br>5-V tolerance: 18<br>• I/O ports for the 100-pin TFLGA and 100-pin LFQFP<br>I/O pins: 78<br>Input pin: 1<br>Pull-up resistors: 78<br>Open-drain outputs: 78<br>5-V tolerance: 17<br>• I/O ports for the 64-pin TFBGA<br>I/O pins: 41<br>Input pin: 1<br>Pull-up resistors: 41<br>Open-drain outputs: 41<br>5-V tolerance: 8<br>• I/O ports for the 64-pin LFQFP<br>I/O pins: 42<br>Input pin: 1<br>Pull-up resistors: 42<br>Open-drain outputs: 42<br>5-V tolerance: 8 |
| Event link controller (ELC) | | • Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions.<br>• 83 internal event signals can be freely combined for interlinked operation with connected functions.<br>• Event signals from peripheral modules can be used to change the states of output pins (of ports B and E).<br>• Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules. |

**Table 1.1 Outline of Specifications (5/10)**

| Classification | Module/Function | Description |
|---|---|---|
| Timers | 16-bit timer pulse unit (TPUa) | • (16 bits × 6 channels) × 1 unit<br>• Maximum of 16 pulse-input/output possible<br>• Select from among seven or eight counter-input clock signals for each channel<br>• Input capture/output compare function<br>• Output of PWM waveforms in up to 15 phases in PWM mode<br>• Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel.<br>• PPG output trigger can be generated<br>• Capable of generating conversion start triggers for the A/D converters<br>• Digital filtering of signals from the input capture pins<br>• Event linking by the ELC |
| | Multifunction timer pulse unit (MTU3a) | • 9 channels (16 bits × 8 channels, 32 bits × 1 channel)<br>• Maximum of 28 pulse-input/output and 3 pulse-input possible<br>• Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLK/A32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A)<br>14 of the signals are available for channel 0, 11 are available for channels 1, 3, 4, 6 to 8, 12 are available for channel 2, and 10 are available for channel 5.<br>• Input capture function<br>• 39 output compare/input capture registers<br>• Counter clear operation (synchronous clearing by compare match/input capture)<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Simultaneous register input/output by synchronous counter operation<br>• Buffered operation<br>• Support for cascade-connected operation<br>• 43 interrupt sources<br>• Automatic transfer of register data<br>• Pulse output mode<br>Toggle/PWM/complementary PWM/reset-synchronized PWM<br>• Complementary PWM output mode<br>Outputs non-overlapping waveforms for controlling 3-phase inverters<br>Automatic specification of dead times<br>PWM duty cycle: Selectable as any value from 0% to 100%<br>Delay can be applied to requests for A/D conversion.<br>Non-generation of interrupt requests at peak or trough values of counters can be selected.<br>Double buffer configuration<br>• Reset synchronous PWM mode<br>Three phases of positive and negative PWM waveforms can be output with desired duty cycles.<br>• Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2)<br>• Counter functionality for dead-time compensation<br>• Generation of triggers for A/D converter conversion<br>• A/D converter start triggers can be skipped<br>• Digital filter function for signals on the input capture and external counter clock pins<br>• PPG output trigger can be generated<br>• Event linking by the ELC |
| | Port output enable 3 (POE3a) | • Control of the high-impedance state of the MTU3 waveform output pins<br>• 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11#<br>• Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level)<br>• Initiation by oscillation-stoppage detection or software<br>• Additional programming of output control target pins is enabled |
| | Programmable pulse generator (PPG) | • (4 bits × 4 groups) × 2 units<br>• Pulse output with the MTU3 or TPU output as a trigger<br>• Maximum of 32 pulse-output possible |

**Table 1.1 Outline of Specifications (6/10)**

| Classification | Module/Function | Description |
|---|---|---|
| Timers | 8-bit timers (TMRb) | • (8 bits × 2 channels) × 2 units<br>• Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal<br>• Capable of output of pulse trains with desired duty cycles or of PWM signals<br>• The 2 channels of each unit can be cascaded to create a 16-bit timer<br>• Generation of triggers for A/D converter conversion<br>• Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12<br>• Event linking by the ELC |
| | Compare match timer (CMT) | • (16 bits × 2 channels) × 2 units<br>• Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512)<br>• Event linking by the ELC |
| | Compare match timer W (CMTW) | • (32 bits × 1 channel) × 2 units<br>• Compare-match, input-capture input, and output-comparison output are available.<br>• Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512)<br>• Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.<br>• Event linking by the ELC |
| | Realtime clock (RTCd)*4 | • Clock sources: Main clock, sub clock<br>• Selection of the 32-bit binary count in time count/second unit possible<br>• Clock and calendar functions<br>• Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt<br>• Battery backup operation<br>• Time-capture facility for three values<br>• Event linking by the ELC |
| | Watchdog timer (WDTA) | • 14 bits × 1 channel<br>• Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192) |
| | Independent watchdog timer (IWDTa) | • 14 bits × 1 channel<br>• Counter-input clock: IWDT-dedicated on-chip oscillator<br>• Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256<br>• Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled).<br>• Event linking by the ELC |
| Communication function | Ethernet controller (ETHERC) | • Input and output of Ethernet/IEEE 802.3 frames<br>• Transfer at 10 or 100 Mbps<br>• Full- and half-duplex modes<br>• MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u<br>• Detection of Magic Packets™*1 or output of a “wake-on-LAN” signal (WOL)<br>• Compliance with flow control as defined in IEEE 802.3x standards |
| | DMA controller for Ethernet controller (EDMACa) | • Alleviation of CPU load by the descriptor control method<br>• Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes |
| | USB 2.0 FS host/ function module (USBb) | • Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS<br>• One port<br>• Compliance with the USB 2.0 specification<br>• Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only)<br>• Both self-powered mode and bus-powered mode are supported<br>• OTG (On the Go) operation is possible (low-speed is not supported)<br>• Incorporates 2 Kbytes of RAM as a transfer buffer<br>• External pull-up and pull-down resistors are not required |

**Table 1.1 Outline of Specifications (7/10)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication function | Serial communications interfaces (SCIg, SCIh, SCIi) | • 13 channels (SCIg: 10 channels + SCIh: 1 channel + SCIi: 2 channels)<br>• SCIg, SCIh, SCIi<br>Serial communications modes: Asynchronous, clock synchronous, and smart-card interface<br>Multi-processor function<br>On-chip baud rate generator allows selection of the desired bit rate<br>Choice of LSB-first or MSB-first transfer<br>Start-bit detection: Level or edge detection is selectable.<br>Simple $I^2C$<br>Simple SPI<br>9-bit transfer mode<br>Bit rate modulation<br>Double-speed mode<br>• SCIg, SCIh<br>Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12<br>Event linking by the ELC (only on channel 5)<br>• SCIh<br>Supports the serial communications protocol, which contains the start frame and information frame<br>Supports the LIN format<br>• SCIi<br>Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit |
| | $I^2C$ bus interface (RIICa) | • 3 channels (only channel 0 can be used in fast-mode plus)<br>Communication formats<br>$I^2C$ bus format/SMBus format<br>Supports the multi-master<br>Max. transfer rate: 1 Mbps (channel 0)<br>• Event linking by the ELC |
| | CAN module (CAN) | • 2 channels<br>• Compliance with the ISO11898-1 specification (standard frame and extended frame)<br>• 32 mailboxes per channel |
| | Serial peripheral interface (RSPIc) | • 3 channels<br>• RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>• Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>Transit/receive data can be swapped in byte units<br>• Buffered structure<br>Double buffers for both transmission and reception<br>• RSPCK can be stopped with the receive buffer full for master reception.<br>• Event linking by the ELC |
| | Quad serial peripheral interface (QSPI) | • 1 channel<br>• Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation)<br>• Programmable bit length and selectable active sense and phase of the clock signal<br>• Sequential execution of transfer<br>• LSB or MSB first is selectable |

**Table 1.1 Outline of Specifications (8/10)**

| Classification | Module/Function | Description |
|---|---|---|
| SD host interface (SDHI)*3 | | • 1 channel<br>• Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s)<br>• One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses)<br>• SD specifications<br>Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported)<br>Part E1: SDIO Specification Ver. 3.00<br>• Error checking: CRC7 for commands and CRC16 for data<br>• Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt, SD buffer access interrupt<br>• DMA transfer requests: SD_BUF write and SD_BUF read<br>• Support for card detection and write protection |
| SD slave interface (SDSI)*3 | | • 1 channel<br>• Compliant with the SDIO Card Specification Ver.2.00 (CSA is not supported)<br>• 1-bit SD/4-bit SD/SPI mode<br>• SDIO Proprietary command is supported<br>• SD/SPI Mandatory command is supported<br>• Interrupt requests: 6 |
| MMC host interface (MMCIF) | | • 1 channel<br>• Transfer speed: Data transfer mode (30 MB/s), backward compatible mode (25 MB/s)<br>• Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported)<br>• Interface for Multimedia Cards (MMCs)<br>• Device buses: Support for 1-, 4-, and 8-bit MMC buses<br>• Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt, MMCIF buffer access interrupt<br>• DMA transfer requests: CE_DATA write and CE_DATA read<br>• Support for card detection, boot operation, high priority interrupt (HPI) |
| Parallel data capture unit (PDC) | | • 1 channel<br>• Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals<br>• Setting of the image size when clipping of the output for a one-frame image is required |
| Graphic-LCD controller (GLCDC) | | • 1 channel<br>• Various data formats and LCD panels are supported<br>• Superposition of 3 planes (single-color background, graphic 1, graphic 2)<br>• 32- and 16-bpp graphics data and 8-, 4-, and 1-bit CLUT data formats are supported |
| 2D drawing engine (DRW2D) | | • 1 channel<br>• Vector drawing (straight lines, triangles, and circles)<br>• Bit blitting (with support for filling, copying, stretching, and rotation)<br>• Bus master function for input and output of frame buffer data<br>32-, 16-, and 8-bit pixel graphics data are supported<br>• Bus master function for input of texture data<br>Input of texture data (32, 24, 16, 8, 4, 2, or 1 bit) are supported.<br>Run length encoding is supported<br>A CLUT is installed and index data can be converted into color data<br>• Two rendering modes are supported (register mode and display list mode)<br>• Performance counting<br>• Interrupts in response to completion of rendering and processing of the display list |

**Table 1.1 Outline of Specifications (9/10)**

| Classification | Module/Function | Description |
|---|---|---|
| 12-bit A/D converter (S12ADFa) | | • 12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels)<br>• 12-bit resolution (switchable between 8, 10, and 12 bits)<br>• Conversion time<br>0.48 µs per channel (for 12-bit conversion)<br>0.45 µs per channel (for 10-bit conversion)<br>0.42 µs per channel (for 8-bit conversion)<br>• Operating mode<br>Scan mode (single scan mode, continuous scan mode, or 3 group scan mode)<br>Group priority control (only for 3 group scan mode)<br>• Sample-and-hold function<br>Common sample-and-hold circuit included<br>In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included<br>• Sampling variable<br>Sampling time can be set up for each channel.<br>• Digital comparison<br>Method: Comparison to detect voltages above or below thresholds and window comparison<br>Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1)<br>• Double trigger mode (A/D conversion data duplicated)<br>• Detection of analog input disconnection<br>• Three ways to start A/D conversion<br>Software trigger, timer (MTU3, TMR, TPU) trigger, external trigger<br>• Event linking by the ELC |
| 12-bit D/A converter (R12DA) | | • 2 channels<br>• 12-bit resolution<br>• Output voltage: 0.2 V to AVCC1 – 0.2 V (buffered output), 0 V to AVCC1 (unbuffered output)<br>• Buffered output or unbuffered output can be selected.<br>• Event linking by the ELC |
| Temperature sensor | | • 1 channel<br>• Relative precision: ± 1°C<br>• The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1). |
| Safety | Memory protection unit (MPU) | • Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh.<br>• Minimum protection unit: 16 bytes<br>• Reading from, writing to, and enabling the execution access can be specified for each area.<br>• An access exception occurs when the detected access is not in the permitted area. |
| | Trusted Memory (TM) Function | • Programs in the TM target area in the code flash memory are protected against reading<br>• Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled. |
| | Register write protection function | • Protects important registers from being overwritten for in case a program runs out of control. |
| | CRC calculator (CRCA) | • Generation of CRC codes for 8-/32-bit data<br>8-bit data<br>Selectable from the following three polynomials<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$<br>32-bit data<br>Selectable from the following two polynomials<br>$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$,<br>$X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable |
| | Main clock oscillation stop detection | • Main clock oscillation stop detection: Available |

**Table 1.1 Outline of Specifications (10/10)**

| Classification | Module/Function | Description |
|---|---|---|
| Safety | Clock frequency accuracy measurement circuit (CAC) | • Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded. |
| | Data operation circuit (DOC) | • The function to compare, add, or subtract 16-bit data |
| Encryption function | AESa*2 | • Key lengths: 128, 192, and 256 bits<br>• Support for CFB, OFB, and CMAC operating modes<br>• Speed of calculations:<br>128-bit key length in 22 cycles<br>192-bit key length in 26 cycles<br>256-bit key length in 30 cycles<br>• Compliant with FIPS PUB 197 |
| | True random number generator (RNG)*2 | • Length of random numbers: 16 bits<br>• Generation of random-number-generated interrupts after a number is generated<br>• Random number generation time: 1.9 ms (typ) |
| | Trusted Secure IP (TSIP)*2 | • Security algorithm<br>Common key encryption: AES (compliant with NIST FIPS PUB 197), 3DES, ARC4<br>Non-common key encryption: RSA<br>• Other features<br>TRNG (true-random number generator)<br>Hash value generation: SHA1, SHA224, SHA256, GHASH<br>Prevention from illicit copying of a key |
| Operating frequency | | Up to 120 MHz |
| Power supply voltage | | VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,<br>$V_{BATT}$ = 2.0 to 3.6 V |
| Operating temperature | | D-version: –40 to +85°C<br>G-version: –40 to +105°C*5 |
| Package | | 177-pin TFLGA (PTLG0177KA-A)<br>176-pin LFBGA (PLBG0176GA-A)<br>176-pin LFQFP (PLQP0176KB-A)<br>145-pin TFLGA (PTLG0145KA-A)<br>144-pin LFQFP (PLQP0144KA-B)<br>100-pin TFLGA (PTLG0100JA-A)<br>100-pin LFQFP (PLQP0100KB-B)<br>64-pin TFBGA (PTBG0064KB-A)<br>64-pin LFQFP (PLQP0064KB-C) |
| Debugging interface | | JTAG and FINE interfaces |

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 2. The product part number differs according to whether or not the MCU includes the encryption function.
Note 3. The product part number differs according to whether or not the MCU includes an SDHI (SD host interface)/SDSI (SD slave interface) (products with 1 Mbyte of code flash memory or less).
Note 4. When the realtime clock is not used, initialize the registers in the time clock according to description in section 31.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.
Note 5. Please contact us if you are using a G-version product.

**Table 1.2 Code Flash Memory Capacity and Comparison of Functions for Different Packages (1/2)**

| Functions | Products | Products with 1 Mbyte of code flash memory or less | | | Products with at least 1.5 Mbytes of code flash memory | | | |
|---|---|---|---|---|---|---|---|---|
| | Package | 145 Pins, 144 Pins | 100 Pins | 64 Pins | 177 Pins, 176 Pins | 145 Pins, 144 Pins | 100 Pins | 64 Pins |
| Code Flash Memory | Code Flash Memory Capacity | 512 Kbytes/768 Kbytes /1 Mbyte | | | 1.5 Mbytes/2 Mbytes | | | |
| | Dual bank function | Not available | | | Available | | | |
| | BGO function | Not available | | | Available | | | |
| Data Flash Memory | | Not available | | | 32 Kbytes | | | |
| RAM | | 256 Kbytes | | | 640 Kbytes (256 Kbytes + 384 Kbytes of expansion RAM) | | | |
| External bus | External bus width | 16/8 bits | | Not available | 32/16/8 bits | 16/8 bits | | Not available |
| | SDRAM area controller | Available | Not available | | Available | | Not available | |
| DMA | DMA controller | Ch. 0 to 7 | | | | | | |
| | Data transfer controller | Available | | | | | | |
| | EXDMA controller | Ch. 0 and 1 | | Not available | Ch. 0 and 1 | | | Not available |
| Timers | 16-bit timer pulse unit | Ch. 0 to 5 | | | | | | |
| | Multi-function timer pulse unit 3 | Ch. 0 to 8 | | | | | | |
| | Port output enable 3 | Available | | | | | | |
| | Programmable pulse generator | Ch. 0 and 1 | | Not available | Ch. 0 and 1 | | | Not available |
| | 8-bit timers | Ch. 0 to 3 | | | | | | |
| | Compare match timer | Ch. 0 to 3 | | | | | | |
| | Compare match timer W | Ch. 0 and 1 | | | | | | |
| | Realtime clock | Available | | | | | | |
| | Watchdog timer | Available | | | | | | |
| | Independent watchdog timer | Available | | | | | | |
| Communication function | Ethernet controller | Ch. 0 (only for RX65N group) | | Not available | Ch. 0 (only for RX65N group) | | | Not available |
| | DMA Controller for the Ethernet Controller | Ch. 0 (only for RX65N group) | | Not available | Ch. 0 (only for RX65N group) | | | Not available |
| | USB 2.0 FS host/function module | Ch. 0 | | Ch. 0*1 | Ch. 0 | | | Ch. 0*1 |
| | Serial communications interfaces (SCIg) | Ch. 0 to 9 | Ch. 0 to 3, 5, 6, 8 and 9 | Ch. 1 to 3, 5, 8 and 9 | Ch. 0 to 9 | | Ch. 0 to 3, 5, 6, 8 and 9 | Ch. 1 to 3, 5, 8 and 9 |
| | Serial communications interfaces (SCIh) | Ch. 12 | | | | | | |
| | Serial communications interfaces (SCIi) | Ch. 10 and 11 | | | | | | |
| | $I^2C$ bus interfaces | Ch. 0 and 2 | | | Ch. 0 to 2 | | | Ch. 0 and 2 |
| | Serial peripheral interface | Ch. 0 to 2 | | Ch. 0 and 1 | Ch. 0 to 2 | | | Ch. 0 and 1 |
| | CAN module | Ch. 0 and 1 | | Not available | Ch. 0 and 1 | | | Not available |
| | Quad serial peripheral interface | Ch. 0 | | | | | | |
| | SD host interface | Available | | | | | | |
| | SD slave interface | Available | | Not available | Available | | | Not available |

**Table 1.2 Code Flash Memory Capacity and Comparison of Functions for Different Packages (2/2)**

| Functions | Products | Products with 1 Mbyte of code flash memory or less | | | Products with at least 1.5 Mbytes of code flash memory | | | |
|---|---|---|---|---|---|---|---|---|
| | Package | 145 Pins, 144 Pins | 100 Pins | 64 Pins | 177 Pins, 176 Pins | 145 Pins, 144 Pins | 100 Pins | 64 Pins |
| Communication function | MMC host interface | Available | | Not available | Available | | | Not available |
| | Parallel data capture unit | Available | Not available | | Available | | Not available | |
| Graphics | Graphic-LCD controller | Not available | | | Available | | | Not available |
| | 2D drawing engine | Not available | | | Available | | | Not available |
| 12-bit A/D converter | | AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels) | AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels) | AN000 to 003 (unit 0: 4 channels) AN106, 107, 110 to 113 (unit 1: 6 channels) | AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels) | | AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels) | AN000 to 003 (unit 0: 4 channels) AN106, 107, 110 to 113 (unit 1: 6 channels) |
| 12-bit D/A converter | | Ch. 0 and 1 | Ch. 1*2 | | Ch. 0 and 1 | | Ch. 1*2 | |
| Temperature sensor | | Available | | | | | | |
| CRC calculator | | Available | | | | | | |
| Data operation circuit | | Available | | | | | | |
| Clock frequency accuracy measurement circuit | | Available | | | | | | |
| Encryption | AES | Available*3 | | | Incorporated in the Trusted Secure IP | | | |
| | RNG | Available*3 | | | Incorporated in the Trusted Secure IP | | | |
| | Trusted Secure IP | Not available | | | Available | | | |
| Event link controller | | Available | | | | | | |
| Off-board programming (parallel programmer mode) | | Available | | Not available | Available | | | Not available |

Note 1. Only supports the function controller.
Note 2. Not provided on the 64-pin TFBGA.
Note 3. Regarding the public release of this module, an exchange of non-disclosure agreement is necessary. For details, contact your Renesas sales agency.

## 1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

**Table 1.3 List of Products (1/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX65N (D version) | R5F565NEDDFC | PLQP0176KB-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NEHDFC | PLQP0176KB-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NCDDFC | PLQP0176KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NCHDFC | PLQP0176KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NEDDFB | PLQP0144KA-B | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NEHDFB | PLQP0144KA-B | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NCDDFB | PLQP0144KA-B | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NCHDFB | PLQP0144KA-B | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565N9ADFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N9BDFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N9EDFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N9FDFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565N7ADFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N7BDFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N7EDFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N7FDFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565N4ADFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N4BDFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N4EDFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N4FDFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565NEDDFP | PLQP0100KB-B | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NEHDFP | PLQP0100KB-B | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NCDDFP | PLQP0100KB-B | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NCHDFP | PLQP0100KB-B | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565N9ADFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N9BDFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N9EDFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N9FDFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |

**Table 1.3 List of Products (2/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX65N (D version) | R5F565N7ADFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N7BDFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N7EDFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N7FDFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565N4ADFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N4BDFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N4EDFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N4FDFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565NEDDBG | PLBG0176GA-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NEHDBG | PLBG0176GA-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NCDDBG | PLBG0176GA-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NCHDBG | PLBG0176GA-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NEDDLC | PTLG0177KA-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NEHDLC | PTLG0177KA-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NCDDLC | PTLG0177KA-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NCHDLC | PTLG0177KA-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NEDDLK | PTLG0145KA-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NEHDLK | PTLG0145KA-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NCDDLK | PTLG0145KA-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NCHDLK | PTLG0145KA-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565N9ADLK | PTLG0145KA-A | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N9BDLK | PTLG0145KA-A | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N9EDLK | PTLG0145KA-A | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N9FDLK | PTLG0145KA-A | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565N7ADLK | PTLG0145KA-A | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N7BDLK | PTLG0145KA-A | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N7EDLK | PTLG0145KA-A | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N7FDLK | PTLG0145KA-A | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565N4ADLK | PTLG0145KA-A | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N4BDLK | PTLG0145KA-A | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |

**Table 1.3 List of Products (3/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX65N (D version) | R5F565N4EDLK | PTLG0145KA-A | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N4FDLK | PTLG0145KA-A | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565NEDDLJ | PTLG0100JA-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NEHDLJ | PTLG0100JA-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565NCDDLJ | PTLG0100JA-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F565NCHDLJ | PTLG0100JA-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F565N9ADLJ | PTLG0100JA-A | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N9BDLJ | PTLG0100JA-A | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N9EDLJ | PTLG0100JA-A | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N9FDLJ | PTLG0100JA-A | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565N7ADLJ | PTLG0100JA-A | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N7BDLJ | PTLG0100JA-A | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N7EDLJ | PTLG0100JA-A | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N7FDLJ | PTLG0100JA-A | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F565N4ADLJ | PTLG0100JA-A | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F565N4BDLJ | PTLG0100JA-A | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F565N4EDLJ | PTLG0100JA-A | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F565N4FDLJ | PTLG0100JA-A | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| RX65N (G version) | R5F565NEDGFC | PLQP0176KB-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F565NEHGFC | PLQP0176KB-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F565NCDGFC | PLQP0176KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F565NCHGFC | PLQP0176KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F565NEDGFB | PLQP0144KA-B | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F565NEHGFB | PLQP0144KA-B | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F565NCDGFB | PLQP0144KA-B | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F565NCHGFB | PLQP0144KA-B | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F565N9AGFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F565N9BGFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F565N9EGFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F565N9FGFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |

**Table 1.3 List of Products (4/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX65N (G version) | R5F565N7AGFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F565N7BGFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F565N7EGFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F565N7FGFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F565N4AGFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F565N4BGFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F565N4EGFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F565N4FGFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F565NEDGFP | PLQP0100KB-B | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F565NEHGFP | PLQP0100KB-B | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F565NCDGFP | PLQP0100KB-B | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F565NCHGFP | PLQP0100KB-B | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F565N9AGFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F565N9BGFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F565N9EGFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F565N9FGFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F565N7AGFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F565N7BGFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F565N7EGFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F565N7FGFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F565N4AGFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F565N4BGFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F565N4EGFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F565N4FGFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |

**Table 1.3 List of Products (5/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX651 (D version) | R5F5651EDDFC | PLQP0176KB-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651EHDFC | PLQP0176KB-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651CDDFC | PLQP0176KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651CHDFC | PLQP0176KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651EDDFB | PLQP0144KA-B | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651EHDFB | PLQP0144KA-B | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651CDDFB | PLQP0144KA-B | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651CHDFB | PLQP0144KA-B | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F56519ADFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56519BDFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56519EDFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56519FDFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F56517ADFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56517BDFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56517EDFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56517FDFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F56514ADFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56514BDFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56514EDFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56514FDFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F5651EDDFP | PLQP0100KB-B | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651EHDFP | PLQP0100KB-B | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651CDDFP | PLQP0100KB-B | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651CHDFP | PLQP0100KB-B | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F56519ADFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56519BDFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56519EDFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56519FDFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F56517ADFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56517BDFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |

**Table 1.3 List of Products (6/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX651 (D version) | R5F56517EDFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56517FDFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F56514ADFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56514BDFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56514EDFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56514FDFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F5651EDDFM | PLQP0064KB-C | 2 M | 640 K | 32 K | 120 MHz | Not available | Available*1 | Available | –40 to +85 |
| | R5F5651EHDFM | PLQP0064KB-C | 2 M | 640 K | 32 K | 120 MHz | Available | Available*1 | Available | –40 to +85 |
| | R5F5651CDDFM | PLQP0064KB-C | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available*1 | Available | –40 to +85 |
| | R5F5651CHDFM | PLQP0064KB-C | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available*1 | Available | –40 to +85 |
| | R5F56519BDFM | PLQP0064KB-C | 1 M | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +85 |
| | R5F56519FDFM | PLQP0064KB-C | 1 M | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +85 |
| | R5F56517BDFM | PLQP0064KB-C | 768 K | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +85 |
| | R5F56517FDFM | PLQP0064KB-C | 768 K | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +85 |
| | R5F56514BDFM | PLQP0064KB-C | 512 K | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +85 |
| | R5F56514FDFM | PLQP0064KB-C | 512 K | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +85 |
| | R5F5651EDDBG | PLBG0176GA-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651EHDBG | PLBG0176GA-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651CDDBG | PLBG0176GA-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651CHDBG | PLBG0176GA-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651EDDBP | PTBG0064KB-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available*1 | Available | –40 to +85 |
| | R5F5651EHDBP | PTBG0064KB-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available*1 | Available | –40 to +85 |
| | R5F5651CDDBP | PTBG0064KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available*1 | Available | –40 to +85 |
| | R5F5651CHDBP | PTBG0064KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available*1 | Available | –40 to +85 |
| | R5F56519BDBP | PTBG0064KB-A | 1 M | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +85 |
| | R5F56519FDBP | PTBG0064KB-A | 1 M | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +85 |
| | R5F56517BDBP | PTBG0064KB-A | 768 K | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +85 |
| | R5F56517FDBP | PTBG0064KB-A | 768 K | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +85 |
| | R5F56514BDBP | PTBG0064KB-A | 512 K | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +85 |
| | R5F56514FDBP | PTBG0064KB-A | 512 K | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +85 |

**Table 1.3 List of Products (7/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX651 (D version) | R5F5651EDDLC | PTLG0177KA-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651EHDLC | PTLG0177KA-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651CDDLC | PTLG0177KA-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651CHDLC | PTLG0177KA-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651EDDLK | PTLG0145KA-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651EHDLK | PTLG0145KA-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651CDDLK | PTLG0145KA-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651CHDLK | PTLG0145KA-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F56519ADLK | PTLG0145KA-A | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56519BDLK | PTLG0145KA-A | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56519EDLK | PTLG0145KA-A | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56519FDLK | PTLG0145KA-A | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F56517ADLK | PTLG0145KA-A | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56517BDLK | PTLG0145KA-A | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56517EDLK | PTLG0145KA-A | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56517FDLK | PTLG0145KA-A | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F56514ADLK | PTLG0145KA-A | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56514BDLK | PTLG0145KA-A | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56514EDLK | PTLG0145KA-A | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56514FDLK | PTLG0145KA-A | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F5651EDDLJ | PTLG0100JA-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651EHDLJ | PTLG0100JA-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F5651CDDLJ | PTLG0100JA-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +85 |
| | R5F5651CHDLJ | PTLG0100JA-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +85 |
| | R5F56519ADLJ | PTLG0100JA-A | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56519BDLJ | PTLG0100JA-A | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56519EDLJ | PTLG0100JA-A | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56519FDLJ | PTLG0100JA-A | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F56517ADLJ | PTLG0100JA-A | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56517BDLJ | PTLG0100JA-A | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |

**Table 1.3 List of Products (8/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX651 (D version) | R5F56517EDLJ | PTLG0100JA-A | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56517FDLJ | PTLG0100JA-A | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| | R5F56514ADLJ | PTLG0100JA-A | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +85 |
| | R5F56514BDLJ | PTLG0100JA-A | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +85 |
| | R5F56514EDLJ | PTLG0100JA-A | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +85 |
| | R5F56514FDLJ | PTLG0100JA-A | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +85 |
| RX651 (G version) | R5F5651EDGFC | PLQP0176KB-A | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F5651EHGFC | PLQP0176KB-A | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F5651CDGFC | PLQP0176KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F5651CHGFC | PLQP0176KB-A | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F5651EDGFB | PLQP0144KA-B | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F5651EHGFB | PLQP0144KA-B | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F5651CDGFB | PLQP0144KA-B | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F5651CHGFB | PLQP0144KA-B | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F56519AGFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F56519BGFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F56519EGFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F56519FGFB | PLQP0144KA-B | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F56517AGFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F56517BGFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F56517EGFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F56517FGFB | PLQP0144KA-B | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F56514AGFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F56514BGFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F56514EGFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F56514FGFB | PLQP0144KA-B | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F5651EDGFP | PLQP0100KB-B | 2 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F5651EHGFP | PLQP0100KB-B | 2 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |
| | R5F5651CDGFP | PLQP0100KB-B | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available | Available | –40 to +105 |
| | R5F5651CHGFP | PLQP0100KB-B | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available | Available | –40 to +105 |

**Table 1.3 List of Products (9/9)**

| Group | Part No. | Package | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI | Dual bank | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|---|---|
| RX651 (G version) | R5F56519AGFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F56519BGFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F56519EGFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F56519FGFP | PLQP0100KB-B | 1 M | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F56517AGFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F56517BGFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F56517EGFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F56517FGFP | PLQP0100KB-B | 768 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F56514AGFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Not available | Not available | Not available | –40 to +105 |
| | R5F56514BGFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Not available | Available | Not available | –40 to +105 |
| | R5F56514EGFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Available | Not available | Not available | –40 to +105 |
| | R5F56514FGFP | PLQP0100KB-B | 512 K | 256 K | Not included | 120 MHz | Available | Available | Not available | –40 to +105 |
| | R5F5651EDGFM | PLQP0064KB-C | 2 M | 640 K | 32 K | 120 MHz | Not available | Available*1 | Available | –40 to +105 |
| | R5F5651EHGFM | PLQP0064KB-C | 2 M | 640 K | 32 K | 120 MHz | Available | Available*1 | Available | –40 to +105 |
| | R5F5651CDGFM | PLQP0064KB-C | 1.5 M | 640 K | 32 K | 120 MHz | Not available | Available*1 | Available | –40 to +105 |
| | R5F5651CHGFM | PLQP0064KB-C | 1.5 M | 640 K | 32 K | 120 MHz | Available | Available*1 | Available | –40 to +105 |
| | R5F56519BGFM | PLQP0064KB-C | 1 M | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +105 |
| | R5F56519FGFM | PLQP0064KB-C | 1 M | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +105 |
| | R5F56517BGFM | PLQP0064KB-C | 768 K | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +105 |
| | R5F56517FGFM | PLQP0064KB-C | 768 K | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +105 |
| | R5F56514BGFM | PLQP0064KB-C | 512 K | 256 K | Not included | 120 MHz | Not available | Available*1 | Not available | –40 to +105 |
| | R5F56514FGFM | PLQP0064KB-C | 512 K | 256 K | Not included | 120 MHz | Available | Available*1 | Not available | –40 to +105 |

Note 1. Only SDHI is available.

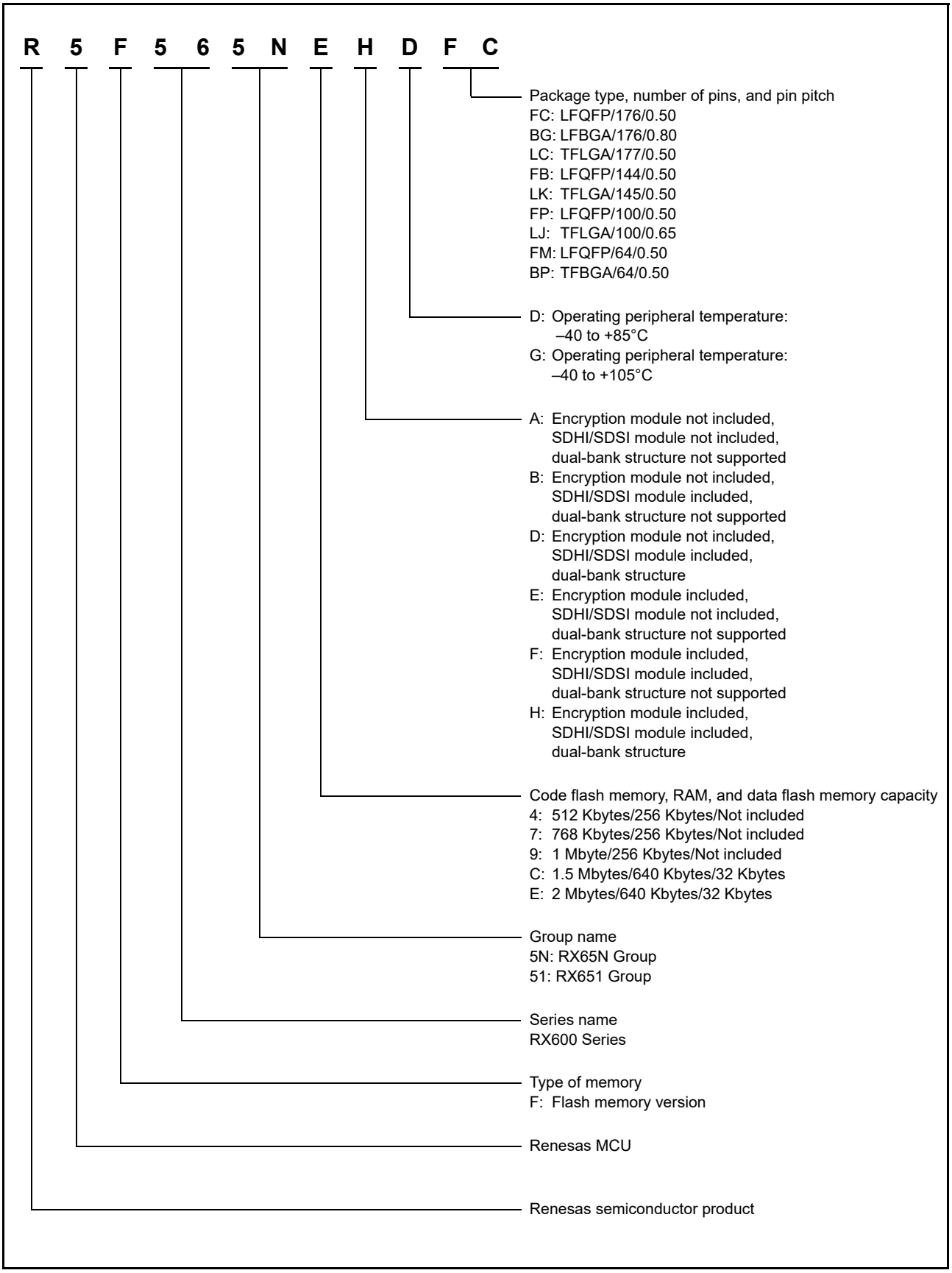
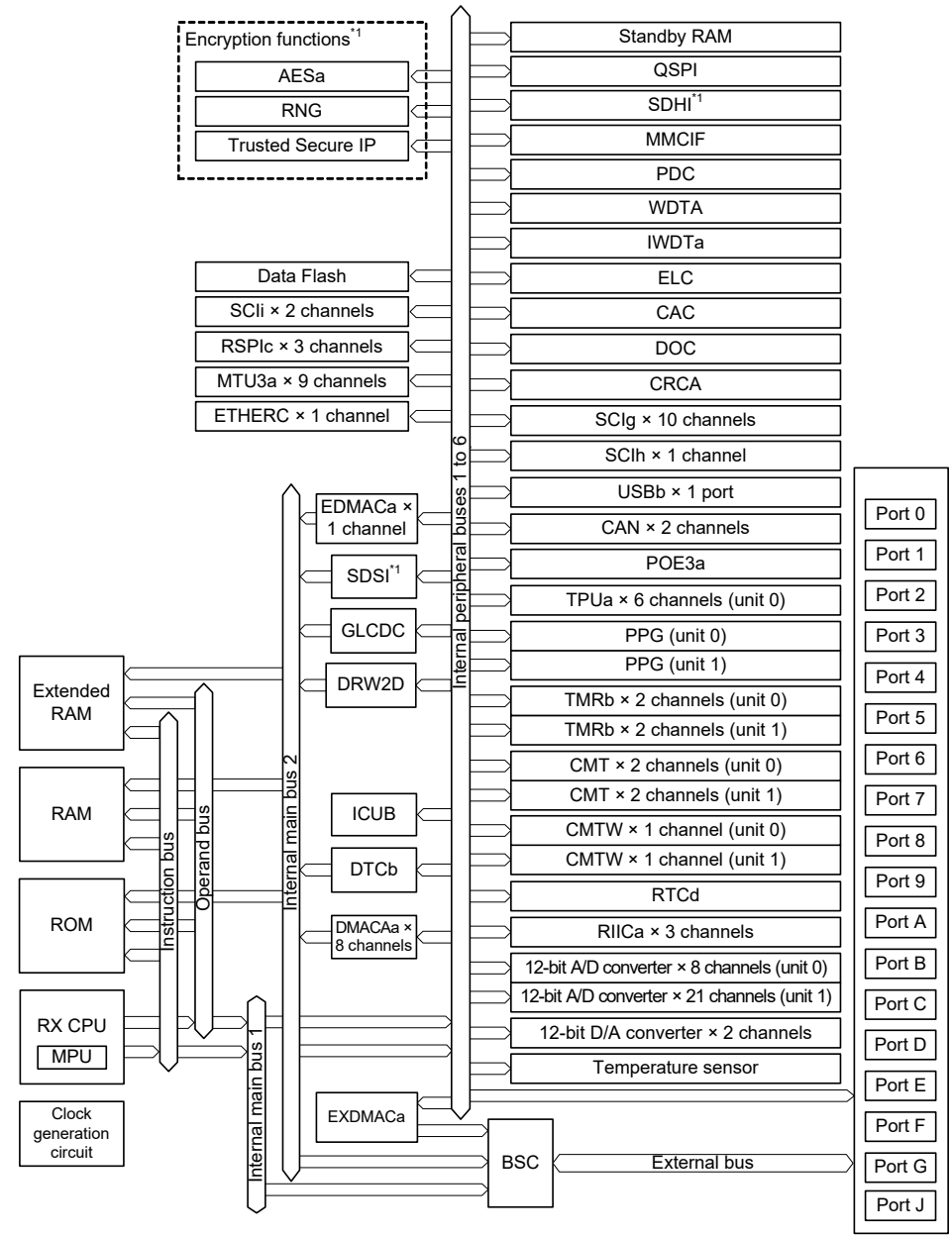



**Figure 1.1 How to Read the Product Part Number**

## 1.3 Block Diagram

Figure 1.2 shows a block diagram.




| | |
|---|---|
| ETHERC: | Ethernet controller |
| EDMACa: | DMA controller for ethernet controller |
| ICUB: | Interrupt controller |
| DTCb | Data transfer controller |
| DMACAa: | DMA controller |
| EXDMACa: | EXDMA controller |
| BSC: | Bus controller |
| WDTA: | Watchdog timer |
| IWDTa: | Independent watchdog timer |
| CRCA: | CRC (cyclic redundancy check) calculator |
| SCIg, SCIh, SCIi: | Serial communications interface |
| USBb: | USB2.0 FS host/function module |
| RSPIc: | Serial peripheral interface |
| MPU: | Memory protection unit |
| QSPI: | Quad serial peripheral interface |
| SDHI: | SD host interface*1 |
| SDSI: | SD slave interface*1 |
| MMCIF: | MMC host interface |

| | |
|---|---|
| PDC: | Parallel data capture unit |
| CAN: | CAN module |
| MTU3a: | Multi-function timer pulse unit 3 |
| POE3a: | Port output enable 3 |
| TPUa: | 16-bit timer pulse unit |
| PPG: | Programmable pulse generator |
| TMRb: | 8-bit timer |
| CMT: | Compare match timer |
| CMTW: | Compare match timer W |
| RTCd: | Realtime clock |
| RIICa: | I²C bus interface |
| DOC: | Data operation circuit |
| CAC: | Clock frequency accuracy measurement circuit |
| AESa: | AES*1 |
| RNG: | True random number generator*1 |
| GLCDC: | Graphic-LCD controller |
| DRW2D: | 2D drawing engine |
| Trusted Secure IP: | Encryption engine*1 |

Note 1. Optional

**Figure 1.2 Block Diagram**

## 1.4 Pin Functions

Table 1.4 lists the pin functions.

**Table 1.4 Pin Functions (1/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Digital power supply | VCC | Input | Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VCL | Input | Connect this pin to VSS via a 0.22-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VBATT | Input | Backup power pin |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | SDCLK | Output | Outputs the SDRAM-dedicated clock. |
| | XCOUT | Output | Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCIN | Input | |
| Clock frequency accuracy measurement | CACREF | Input | Reference clock input pin for the clock frequency accuracy measurement circuit |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal level on this pin must not be changed during operation. |
| | UB | Input | USB boot mode enable pin |
| | UPSEL | Input | Selects the power supply method in USB boot mode.<br>The low level selects self-powered mode and the high level selects bus-powered mode. |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| | BSCANP | Input | Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low. |
| On-chip emulator | FINED | I/O | Fine interface pin |
| | TRST# | Input | On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC<br>TRSYNC1 | Output | These pins indicate that output from the TRDATA0 to TRDATA7 pins is valid. |
| | TRDATA0<br>TRDATA1<br>TRDATA2<br>TRDATA3<br>TRDATA4<br>TRDATA5<br>TRDATA6<br>TRDATA7 | Output | These pins output the trace information. |
| Address bus | A0 to A23 | Output | Output pins for the address |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus |

**Table 1.4 Pin Functions (2/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Multiplexed bus | A0/D0 to A15/D15 | I/O | Address/data multiplexed bus |
| Bus control | RD# | Output | Strobe signal which indicates that reading from the external bus interface space is in progress |
| | WR# | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode |
| | WR0# to WR3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode |
| | BC0# to BC3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected |
| | WAIT# | Input | Input pin for wait request signals in access to the external space |
| | CS0# to CS7# | Output | Select signals for CS areas |
| | CKE | Output | SDRAM clock enable signal |
| | SDCS# | Output | SDRAM chip select signal |
| | RAS# | Output | SDRAM row address strobe signal |
| | CAS# | Output | SDRAM column address strove signal |
| | WE# | Output | SDRAM write enable pin |
| | DQM0 to DQM3 | Output | SDRAM I/O data mask enable signals |
| EXDMA controller | EDREQ0, EDREQ1 | Input | External DMA transfer request pins |
| | EDACK0, EDACK1 | Output | Single address transfer acknowledge signals |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ15, IRQ0-DS to IRQ15-DS | Input | Maskable interrupt request pins |
| Multi-function timer pulse unit 3 | MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins |
| | MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins |
| | MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins |
| | MTIC5U, MTIC5V, MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins |
| | MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D | I/O | The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins |
| | MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D | I/O | The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins |
| | MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D | I/O | The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins |
| | MTCLKA, MTCLKB, MTCLKC, MTCLKD | Input | Input pins for external clock signals or for phase counting mode clock signals |
| Port output enable 3 | POE0#, POE4#, POE8#, POE10#, POE11# | Input | Input pins for request signals to place the MTU in the high impedance state |

**Table 1.4 Pin Functions (3/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| 16-bit timer pulse unit | TIOCA0, TIOCB0, TIOCC0, TIOCD0 | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins |
| | TIOCA1, TIOCB1 | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins |
| | TIOCA2, TIOCB2 | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins |
| | TIOCA3, TIOCB3, TIOCC3, TIOCD3 | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins |
| | TIOCA4, TIOCB4 | I/O | The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins |
| | TIOCA5, TIOCB5 | I/O | The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins |
| | TCLKA, TCLKB, TCLKC, TCLKD | Input | Input pins for external clock signals or for phase counting mode clock signals |
| Programmable pulse generator | PO0 to PO31 | Output | Output pins for the pulse signals |
| 8-bit timer | TMO0 to TMO3 | Output | Compare match output pins |
| | TMCI0 to TMCI3 | Input | Input pins for external clocks to be input to the counter |
| | TMRI0 to TMRI3 | Input | Input pins for the counter reset |
| Compare match timer W | TIC0 to TIC3 | Input | Input pins for CMTW |
| | TOC0 to TOC3 | Output | Output pins for CMTW |
| Serial communications interface (SCIg) | • Asynchronous mode/clock synchronous mode | | |
| | SCK0 to SCK9 | I/O | Input/output pins for the clock |
| | RXD0 to RXD9 | Input | Input pins for received data |
| | TXD0 to TXD9 | Output | Output pins for transmitted data |
| | CTS0# to CTS9# | Input | Input pins for controlling the start of transmission and reception |
| | RTS0# to RTS9# | Output | Output pins for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL0 to SSCL9 | I/O | Input/output pins for the $I^2C$ clock |
| | SSDA0 to SSDA9 | I/O | Input/output pins for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK0 to SCK9 | I/O | Input/output pins for the clock |
| | SMISO0 to SMISO9 | I/O | Input/output pins for slave transmission of data |
| | SMOSI0 to SMOSI9 | I/O | Input/output pins for master transmission of data |
| | SS0# to SS9# | Input | Chip-select input pins |

**Table 1.4 Pin Functions (4/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Serial communications interface (SCIh) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | RXD12 | Input | Input pin for received data |
| | TXD12 | Output | Output pin for transmitted data |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL12 | I/O | Input/output pin for the $I^2C$ clock |
| | SSDA12 | I/O | Input/output pin for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | SMISO12 | I/O | Input/output pin for slave transmission of data |
| | SMOSI12 | I/O | Input/output pin for master transmission of data |
| | SS12# | Input | Chip-select input pin |
| | • Extended serial mode | | |
| | RXDX12 | Input | Input pin for received data |
| | TXDX12 | Output | Output pin for transmitted data |
| | SIOX12 | I/O | Input/output pin for received or transmitted data |
| Serial communications interface (SCIi) | • Asynchronous mode/clock synchronous mode | | |
| | SCK10 and SCK11 | I/O | Input/output pin for the clock |
| | RXD10 and RXD11 | Input | Input pin for received data |
| | TXD10 and TXD11 | Output | Output pin for transmitted data |
| | CTS10# and CTS11# | Input | Input pin for controlling the start of transmission and reception |
| | RTS10# and RTS11# | Output | Output pin for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL10 and SSCL11 | I/O | Input/output pin for the $I^2C$ clock |
| | SSDA10 and SSDA11 | I/O | Input/output pin for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK10 and SCK11 | I/O | Input/output pin for the clock |
| | SMISO10 and SMISO11 | I/O | Input/output pin for slave transmission of data |
| | SMOSI10 and SMOSI11 | I/O | Input/output pin for master transmission of data |
| | SS10# and SS11# | Input | Chip-select input pin |
| $I^2C$ bus interface | SCL0[FM+], SCL1, SCL2, SCL2-DS | I/O | Input/output pins for clocks. Bus can be directly driven by the N-channel open drain |
| | SDA0[FM+], SDA1, SDA2, SDA2-DS | I/O | Input/output pins for data. Bus can be directly driven by the N-channel open drain |

**Table 1.4 Pin Functions (5/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Ethernet controller | REF50CK0 | Input | 50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode. |
| | RMII0_CRS_DV | Input | Indicate that there are carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode. |
| | RMII0_TXD0, RMII0_TXD1 | Output | 2-bit transmit data in RMII mode |
| | RMII0_RXD0, RMII0_RXD1 | Input | 2-bit receive data in RMII mode |
| | RMII0_TXD_EN | Output | Output pins for data transmit enable signals in RMII mode |
| | RMII0_RX_ER | Input | Indicate an error has occurred during reception of data in RMII mode. |
| | ET0_CRS | Input | Carrier detection/data reception enable pins |
| | ET0_RX_DV | Input | Indicate that there are valid receive data on ET0_ERXD3 to ET0_ERXD0. |
| | ET0_EXOUT | Output | General-purpose external output pins |
| | ET0_LINKSTA | Input | Input link status from the PHY-LSI. |
| | ET0_ETXD0 to ET0_ETXD3 | Output | 4 bits of MII transmit data |
| | ET0_ERXD0 to ET0_ERXD3 | Input | 4 bits of MII receive data |
| | ET0_TX_EN | Output | Transmit enable pins. Function as signals indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0. |
| | ET0_TX_ER | Output | Transmit error pins. Function as signals notifying the PHY-LSI of an error during transmission. |
| | ET0_RX_ER | Input | Receive error pins. Function as signals to recognize an error during reception. |
| | ET0_TX_CLK | Input | Transmit clock pins. These pins input reference signals for output timings from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER. |
| | ET0_RX_CLK | Input | Receive clock pins. These pins input reference signals for input timings to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER. |
| | ET0_COL | Input | Input collision detection signals. |
| | ET0_WOL | Output | Receive Magic packets. |
| | ET0_MDC | Output | Output reference clock signals for information transfer via ET0_MDIO. |
| | ET0_MDIO | I/O | Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI. |
| USB 2.0 host/function module | VCC_USB | Input | Power supply pin |
| | VSS_USB | Input | Ground pin |
| | USB0_DP | I/O | Input or output USB transceiver D+ data. |
| | USB0_DM | I/O | Input or output USB transceiver D- data. |
| | USB0_EXICEN | Output | Connect to the OTG power IC. |
| | USB0_ID | Input | Connect to the OTG power IC. |
| | USB0_VBUSEN | Output | USB VBUS power enable pins |
| | USB0_OVRCURA/ USB0_OVRCURB | Input | USB overcurrent pins |
| | USB0_VBUS | Input | USB cable connection/disconnection detection input pin |
| CAN module | CRX0, CRX1, CRX1-DS | Input | Input pins |
| | CTX0, CTX1 | Output | Output pins |

**Table 1.4 Pin Functions (6/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Serial peripheral interface | RSPCKA-A/RSPCKA-B/ RSPCKB-A/RSPCKB-B/ RSPCKC-A/RSPCKC-B | I/O | Clock input/output pins |
| | MOSIA-A/MOSIA-B/ MOSIB-A/MOSIB-B/ MOSIC-A/MOSIC-B | I/O | Input or output data output from the master |
| | MISOA-A/MISOA-B/ MISOB-A/MISOB-B/ MISOC-A/MISOC-B | I/O | Input or output data output from the slave |
| | SSLA0-A/SSLA0-B/ SSLB0-A/SSLB0-B/ SSLC0-A/SSLC0-B | I/O | Input or output pins for slave selection |
| | SSLA1-A/SSLA1-B/ SSLB1-A/SSLB1-B/ SSLC1-A/SSLC1-B, SSLA2-A/SSLA2-B/ SSLB2-A/SSLB2-B/ SSLC2-A/SSLC2-B, SSLA3-A/SSLA3-B/ SSLB3-A/SSLB3-B/ SSLC3-A/SSLC3-B | Output | Output pins for slave selection |
| Quad serial peripheral interface | QSPCLK-A/QSPCLK-B | Output | QSPI clock output pins |
| | QSSL-A/QSSL-B | Output | QSPI slave output pins |
| | QMO-A/QMO-B, QIO0-A/QIO0-B | I/O | Master transmit data/data 0 |
| | QMI-A/QMI-B, QIO1-A/QIO1-B | I/O | Master input data/data 1 |
| | QIO2-A/QIO2-B, QIO3-A/QIO3-B | I/O | Data 2, data 3 |
| MMC host interface | MMC_CLK-A/ MMC_CLK-B | Output | MMC clock pins |
| | MMC_CMD-A/ MMC_CMD-B | I/O | Command/response pins |
| | MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B | I/O | Transmit data/receive data |
| | MMC_CD-A/MMC_CD-B | Input | Card detection pins |
| | MMC_RES#-A/MMC_RES#-B | Output | MMC reset output pins |
| SD host interface | SDHI_CLK-A/SDHI_CLK-B/ SDHI_CLK-C | Output | SD clock output pins |
| | SDHI_CMD-A/SDHI_CMD-B/ SDHI_CMD-C | I/O | SD command output, response input signal pins |
| | SDHI_D3-A/SDHI_D3-B/ SDHI_D3-C to SDHI_D0-A/ SDHI_D0-B/SDHI_D0-C | I/O | SD data bus pins |
| | SDHI_CD | Input | SD card detection pin |
| | SDHI_WP | Input | SD write-protect signal |
| SD slave interface | SDSI_CLK-A/SDSI_CLK-B | Input | SD clock input pins |
| | SDSI_CMD-A/SDSI_CMD-B | I/O | SD command input, response output signal pins |
| | SDSI_D3-A/SDSI_D3-B, SDSI_D2-A/SDSI_D2-B, SDSI_D1-A/SDSI_D1-B, SDSI_D0-A/SDSI_D0-B | I/O | SD data bus pins |

**Table 1.4 Pin Functions (7/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Parallel data capture unit | PIXCLK | Input | Image transfer clock pin |
| | VSYNC | Input | Vertical synchronization signal pin |
| | HSYNC | Input | Horizontal synchronization signal pin |
| | PIXD0 to PIXD7 | Input | 8-bit image data pins |
| | PCKO | Output | Output pin for dot clock |
| Graphic-LCD controller | LCD_CLK-A, LCD_CLK-B | Output | Panel clock output pins |
| | LCD_TCON3-A/ LCD_TCON3-B to LCD_TCON0-A/ LCD_TCON0-B | Output | Control signal output pins |
| | LCD_DATA23-A/ LCD_DATA23-B to LCD_DATA0-A/ LCD_DATA0-B | Output | LCD signal output pins |
| | LCD_EXTCLK-A, LCD_EXTCLK-B | Input | Panel clock source input pins |
| Realtime clock | RTCOUT | Output | Output pin for 1-Hz/64-Hz clock |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pins |
| 12-bit A/D converter | AN000 to AN007, AN100 to AN120 | Input | Input pins for the analog signals to be processed by the A/D converter |
| | ADTRG0#, ADTRG1# | Input | Input pins for the external trigger signals that start the A/D conversion |
| | ANEX0 | Output | Extended analog output pin |
| | ANEX1 | Input | Extended analog input pin |
| 12-bit D/A converter | DA0, DA1 | Output | Output pins for the analog signals to be processed by the D/A converter |
| Analog power supply | AVCC0 | Input | Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | AVSS0 | Input | Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VREFH0 | Input | Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used. |
| | VREFL0 | Input | Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used. |
| | AVCC1 | Input | Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | AVSS1 | Input | Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |

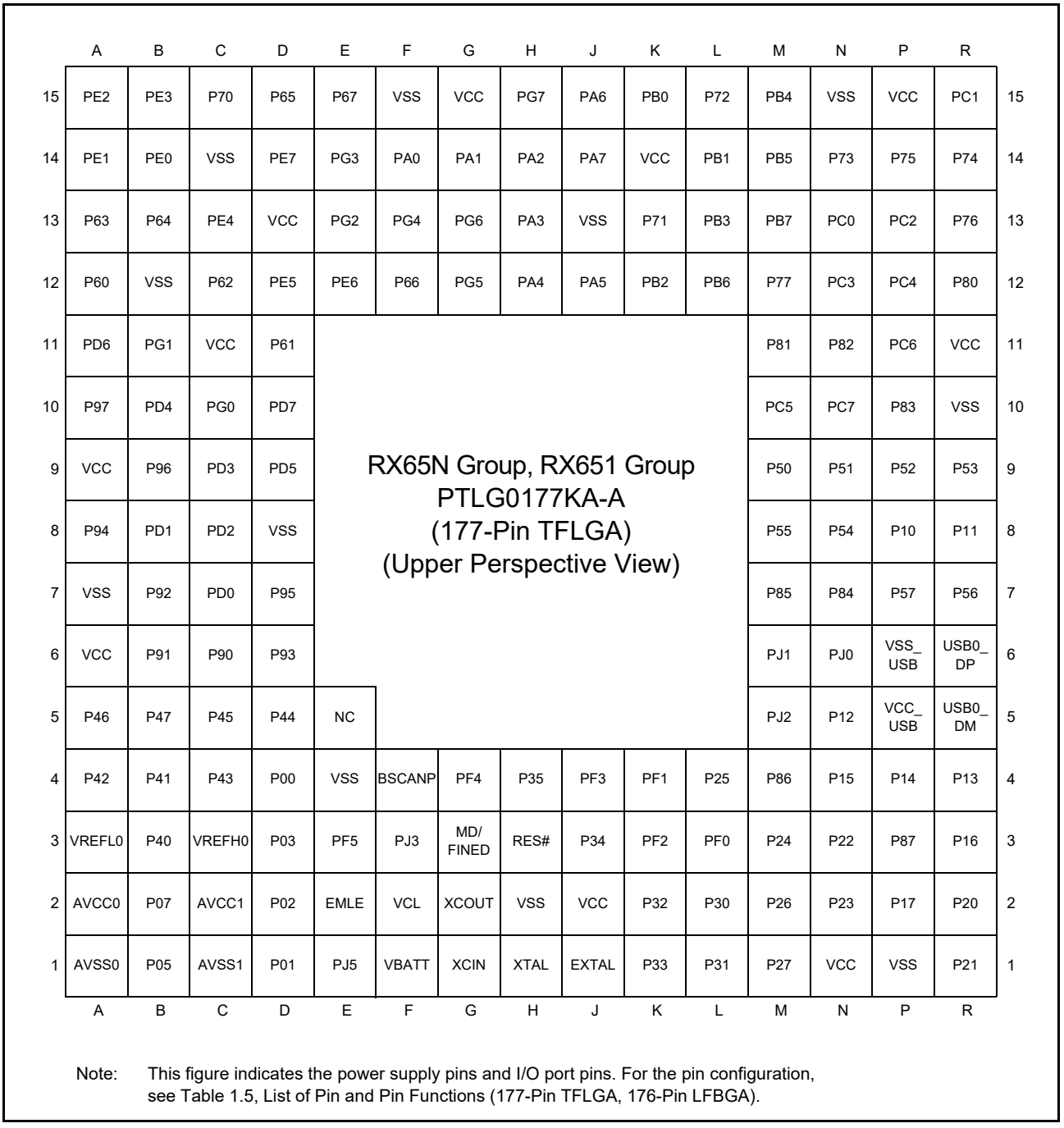
**Table 1.4 Pin Functions (8/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| I/O ports | P00 to P03, P05, P07 | I/O | 6-bit input/output pins |
| | P10 to P17 | I/O | 8-bit input/output pins |
| | P20 to P27 | I/O | 8-bit input/output pins |
| | P30 to P37 | I/O | 8-bit input/output pins (P35: input pin) |
| | P40 to P47 | I/O | 8-bit input/output pins |
| | P50 to P57 | I/O | 8-bit input/output pins |
| | P60 to P67 | I/O | 8-bit input/output pins |
| | P70 to P77 | I/O | 8-bit input/output pins |
| | P80 to P87 | I/O | 8-bit input/output pins |
| | P90 to P97 | I/O | 8-bit input/output pins |
| | PA0 to PA7 | I/O | 8-bit input/output pins |
| | PB0 to PB7 | I/O | 8-bit input/output pins |
| | PC0 to PC7 | I/O | 8-bit input/output pins |
| | PD0 to PD7 | I/O | 8-bit input/output pins |
| | PE0 to PE7 | I/O | 8-bit input/output pins |
| | PF0 to PF5 | I/O | 6-bit input/output pins |
| | PG0 to PG7 | I/O | 8-bit input/output pins |
| | PJ0 to PJ3, PJ5 | I/O | 5-bit input/output pins |

Note: Note the following regarding pin names. For details, see section 1.5, Pin Assignments.
- When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group.
  All RSPI, QSPI, SDHI, MMC, GLCDC AC timings are measured in combination with the pins in the same group.
- When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.
- RIIC pin functions that have [FM+] appended to their names support fast-mode plus.

## 1.5 Pin Assignments

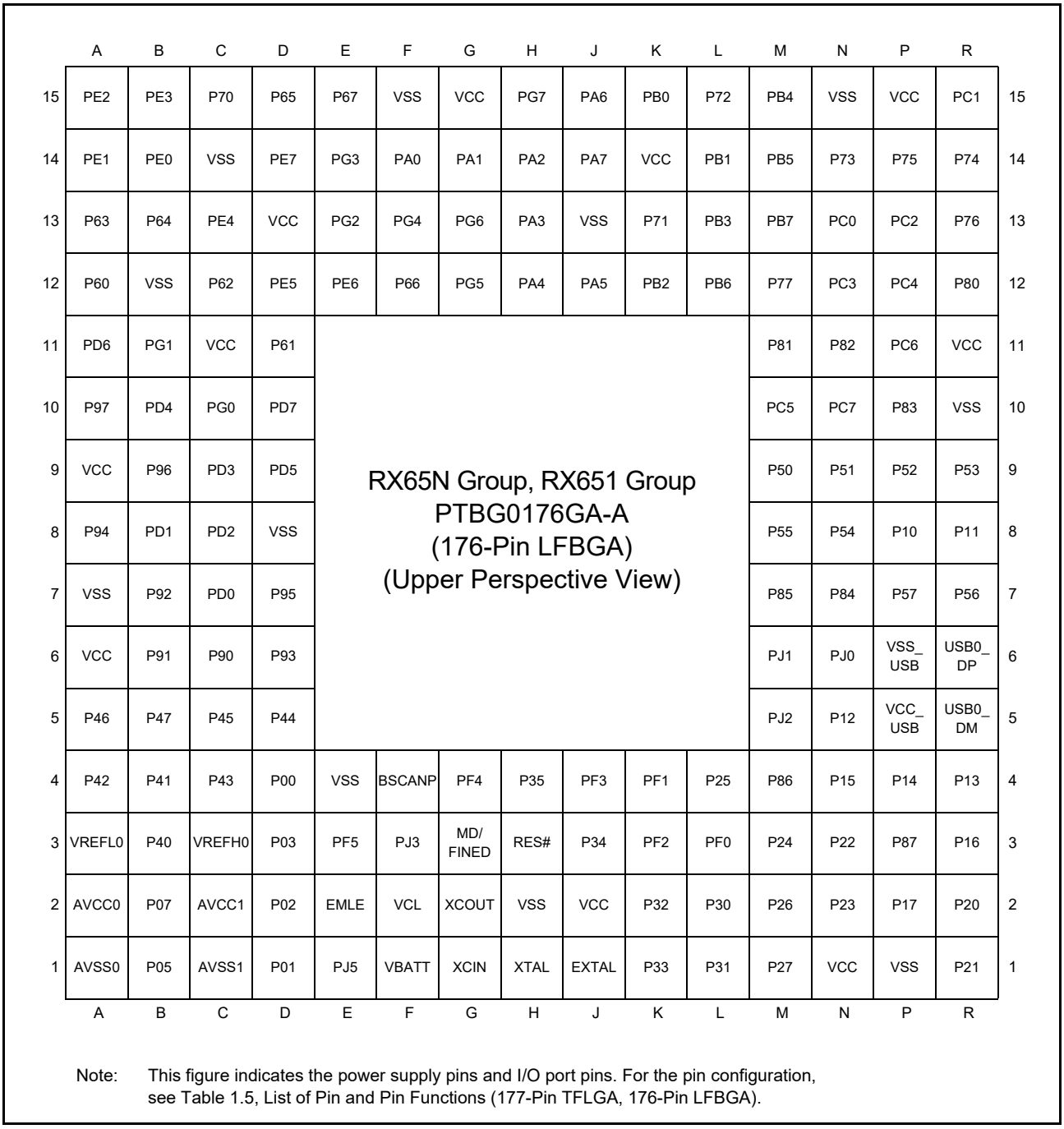
Figure 1.3 to Figure 1.11 show the pin assignments. Table 1.5 to Table 1.12 show the lists of pins and pin functions.




| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | PE2 | PE3 | P70 | P65 | P67 | VSS | VCC | PG7 | PA6 | PB0 | P72 | PB4 | VSS | VCC | PC1 | 15 |
| 14 | PE1 | PE0 | VSS | PE7 | PG3 | PA0 | PA1 | PA2 | PA7 | VCC | PB1 | PB5 | P73 | P75 | P74 | 14 |
| 13 | P63 | P64 | PE4 | VCC | PG2 | PG4 | PG6 | PA3 | VSS | P71 | PB3 | PB7 | PC0 | PC2 | P76 | 13 |
| 12 | P60 | VSS | P62 | PE5 | PE6 | P66 | PG5 | PA4 | PA5 | PB2 | PB6 | P77 | PC3 | PC4 | P80 | 12 |
| 11 | PD6 | PG1 | VCC | P61 | | | | | | | | P81 | P82 | PC6 | VCC | 11 |
| 10 | P97 | PD4 | PG0 | PD7 | | | | | | | | PC5 | PC7 | P83 | VSS | 10 |
| 9 | VCC | P96 | PD3 | PD5 | | | | | | | | P50 | P51 | P52 | P53 | 9 |
| 8 | P94 | PD1 | PD2 | VSS | | | | | | | | P55 | P54 | P10 | P11 | 8 |
| 7 | VSS | P92 | PD0 | P95 | | | | | | | | P85 | P84 | P57 | P56 | 7 |
| 6 | VCC | P91 | P90 | P93 | | | | | | | | PJ1 | PJ0 | VSS_ USB | USB0_ DP | 6 |
| 5 | P46 | P47 | P45 | P44 | NC | | | | | | | PJ2 | P12 | VCC_ USB | USB0_ DM | 5 |
| 4 | P42 | P41 | P43 | P00 | VSS | BSCANP | PF4 | P35 | PF3 | PF1 | P25 | P86 | P15 | P14 | P13 | 4 |
| 3 | VREFL0 | P40 | VREFH0 | P03 | PF5 | PJ3 | MD/ FINED | RES# | P34 | PF2 | PF0 | P24 | P22 | P87 | P16 | 3 |
| 2 | AVCC0 | P07 | AVCC1 | P02 | EMLE | VCL | XCOUT | VSS | VCC | P32 | P30 | P26 | P23 | P17 | P20 | 2 |
| 1 | AVSS0 | P05 | AVSS1 | P01 | PJ5 | VBATT | XCIN | XTAL | EXTAL | P33 | P31 | P27 | VCC | VSS | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

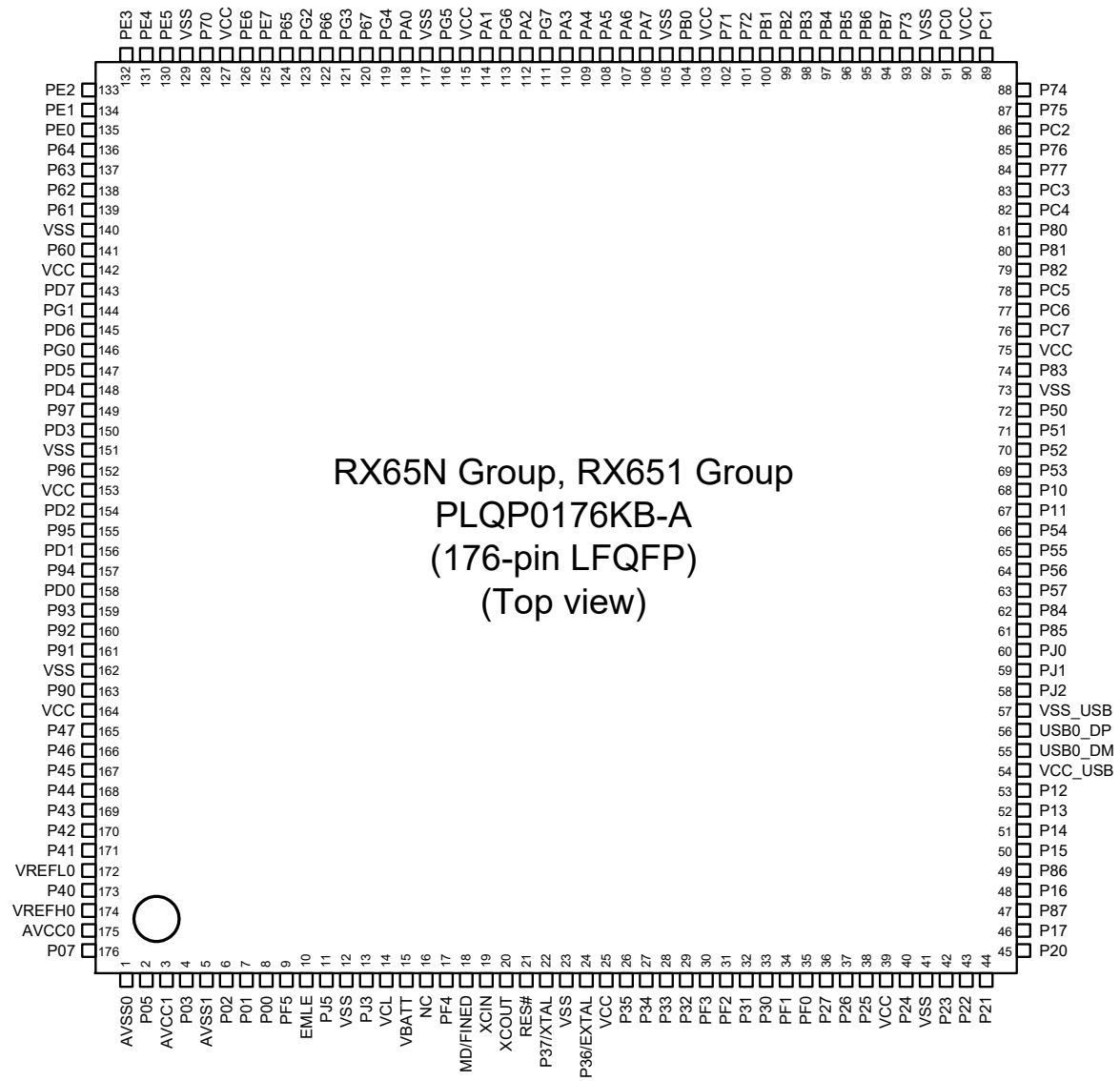
**Figure 1.3 Pin Assignment (177-Pin TFLGA)**




| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | PE2 | PE3 | P70 | P65 | P67 | VSS | VCC | PG7 | PA6 | PB0 | P72 | PB4 | VSS | VCC | PC1 | 15 |
| 14 | PE1 | PE0 | VSS | PE7 | PG3 | PA0 | PA1 | PA2 | PA7 | VCC | PB1 | PB5 | P73 | P75 | P74 | 14 |
| 13 | P63 | P64 | PE4 | VCC | PG2 | PG4 | PG6 | PA3 | VSS | P71 | PB3 | PB7 | PC0 | PC2 | P76 | 13 |
| 12 | P60 | VSS | P62 | PE5 | PE6 | P66 | PG5 | PA4 | PA5 | PB2 | PB6 | P77 | PC3 | PC4 | P80 | 12 |
| 11 | PD6 | PG1 | VCC | P61 | | | | | | | | P81 | P82 | PC6 | VCC | 11 |
| 10 | P97 | PD4 | PG0 | PD7 | | | | | | | | PC5 | PC7 | P83 | VSS | 10 |
| 9 | VCC | P96 | PD3 | PD5 | | | | | | | | P50 | P51 | P52 | P53 | 9 |
| 8 | P94 | PD1 | PD2 | VSS | | | | | | | | P55 | P54 | P10 | P11 | 8 |
| 7 | VSS | P92 | PD0 | P95 | | | | | | | | P85 | P84 | P57 | P56 | 7 |
| 6 | VCC | P91 | P90 | P93 | | | | | | | | PJ1 | PJ0 | VSS_ USB | USB0_ DP | 6 |
| 5 | P46 | P47 | P45 | P44 | | | | | | | | PJ2 | P12 | VCC_ USB | USB0_ DM | 5 |
| 4 | P42 | P41 | P43 | P00 | VSS | BSCANP | PF4 | P35 | PF3 | PF1 | P25 | P86 | P15 | P14 | P13 | 4 |
| 3 | VREFL0 | P40 | VREFH0 | P03 | PF5 | PJ3 | MD/ FINED | RES# | P34 | PF2 | PF0 | P24 | P22 | P87 | P16 | 3 |
| 2 | AVCC0 | P07 | AVCC1 | P02 | EMLE | VCL | XCOUT | VSS | VCC | P32 | P30 | P26 | P23 | P17 | P20 | 2 |
| 1 | AVSS0 | P05 | AVSS1 | P01 | PJ5 | VBATT | XCIN | XTAL | EXTAL | P33 | P31 | P27 | VCC | VSS | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

**Figure 1.4 Pin Assignment (176-Pin LFBGA)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (176-Pin LFQFP).

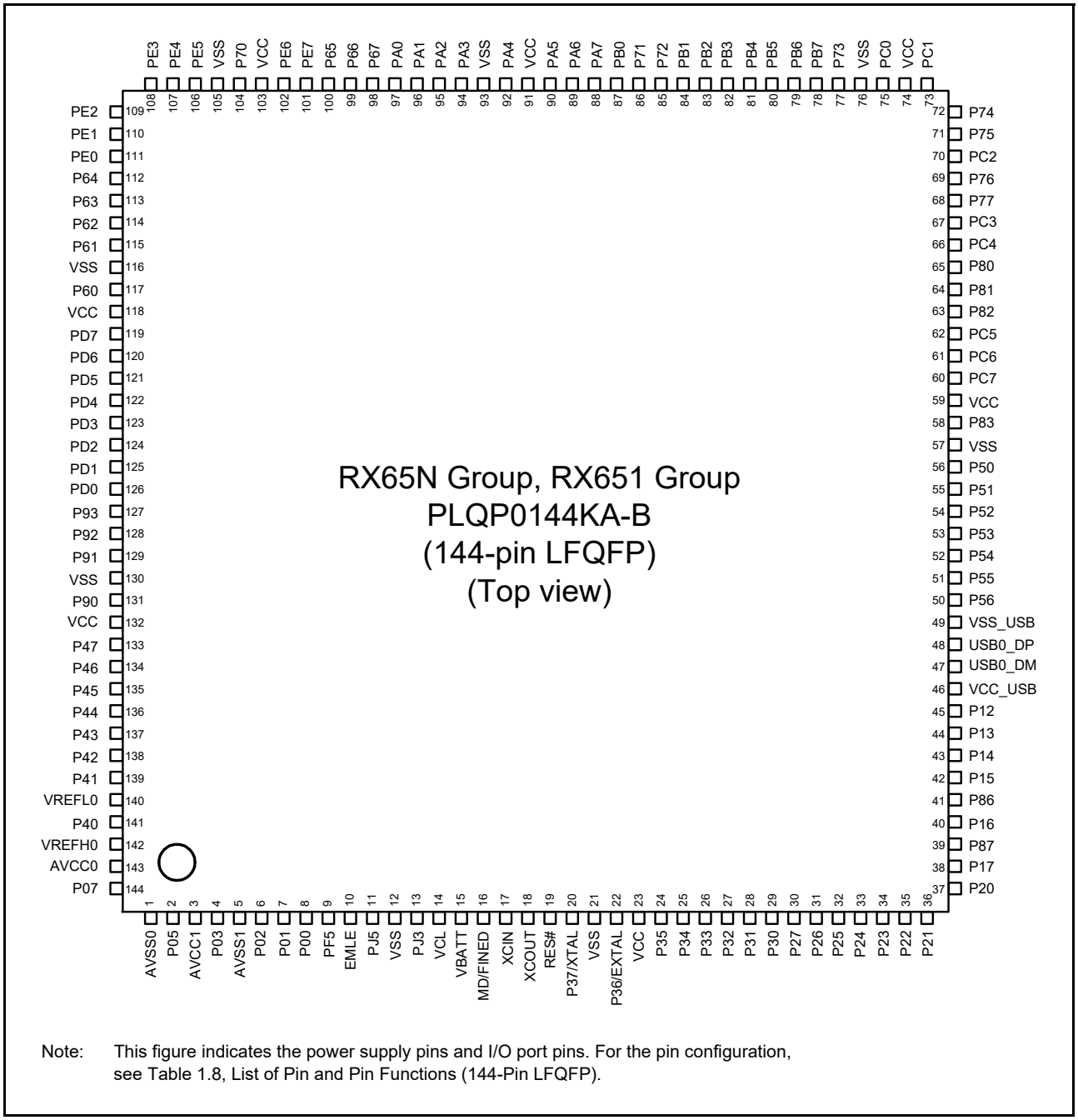
**Figure 1.5 Pin Assignment (176-Pin LFQFP)**

| | A | B | C | D | E | F | G | H | J | K | L | M | N | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 13 | PE3 | PE4 | VSS | PE6 | P67 | PA2 | PA4 | PA7 | PB1 | PB5 | VSS | VCC | P74 | 13 |
| 12 | PE1 | PE2 | P70 | PE5 | P65 | PA1 | VCC | PB0 | PB2 | PB6 | P73 | PC1 | P75 | 12 |
| 11 | P62 | P61 | PE0 | VCC | P66 | VSS | PA6 | P71 | PB4 | PB7 | PC2 | PC0 | PC3 | 11 |
| 10 | VSS | VCC | P63 | PE7 | PA0 | PA3 | PA5 | P72 | PB3 | P76 | PC4 | P77 | P82 | 10 |
| 9 | PD6 | PD4 | PD7 | P64 | | | | | | P80 | PC5 | P81 | PC7 | 9 |
| 8 | PD2 | PD0 | PD3 | P60 | | | | | | VCC | P83 | PC6 | VSS | 8 |
| 7 | P92 | P91 | PD1 | PD5 | | | | | | P51 | P52 | P50 | P55 | 7 |
| 6 | P90 | P47 | VSS | P93 | | | | | | P53 | P56 | VSS_ USB | USB0_ DP | 6 |
| 5 | P45 | P43 | P46 | VCC | P44 | | | | | P54 | P13 | VCC_ USB | USB0_ DM | 5 |
| 4 | P42 | VREFL0 | P41 | P01 | EMLE | VBATT | BSCANP | P35 | P30 | P15 | P24 | P12 | P14 | 4 |
| 3 | P40 | P05 | VREFH0 | P03 | PJ5 | PJ3 | MD/ FINED | VSS | P32 | P31 | P16 | P86 | P87 | 3 |
| 2 | P07 | AVCC0 | P02 | PF5 | VCL | XCOUT | RES# | VCC | P33 | P26 | P23 | P17 | P20 | 2 |
| 1 | AVSS0 | AVCC1 | AVSS1 | P00 | VSS | XIN | XTAL | EXTAL | P34 | P27 | P25 | P22 | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | |

RX65N Group, RX651 Group
PTLG0145KA-A
(145-Pin TFLGA)
(Upper Perspective View)

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (145-Pin TFLGA).

**Figure 1.6 Pin Assignment (145-Pin TFLGA)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (144-Pin LFQFP).

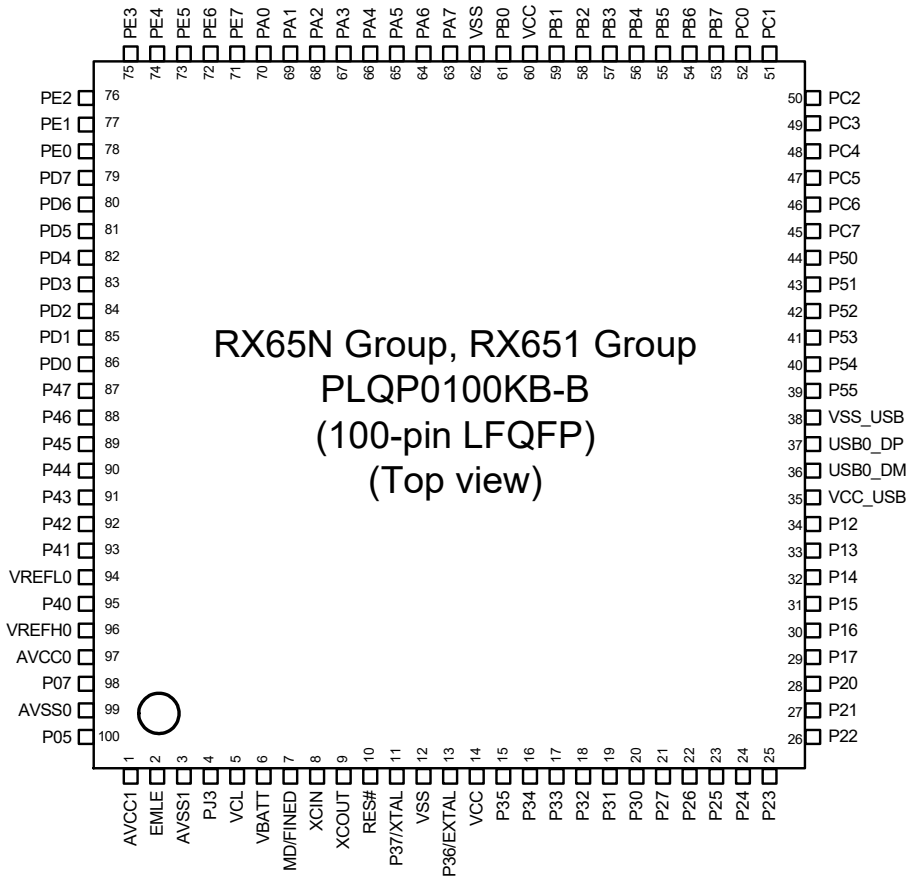
**Figure 1.7 Pin Assignment (144-Pin LFQFP)**

RX65N Group, RX651 Group
PTLG0100JA-A (100-Pin TFLGA)
(Upper Perspective View)

| | A | B | C | D | E | F | G | H | J | K | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | PE2 | PE3 | PE4 | PA0 | PA3 | VSS | VCC | PB7 | PC1 | PC2 | 10 |
| 9 | PE1 | PD7 | PE5 | PA1 | PA5 | PA7 | PB1 | PB6 | PC0 | PC3 | 9 |
| 8 | PE0 | PD6 | PD5 | PE7 | PA4 | PB0 | PB4 | PC6 | PC4 | PC5 | 8 |
| 7 | PD4 | PD3 | PD2 | PE6 | PA6 | PB2 | PB5 | PC7 | P50 | P51 | 7 |
| 6 | PD0 | PD1 | P47 | P46 | PA2 | PB3 | P52 | P54 | VCC_ USB | USB0_ DP | 6 |
| 5 | P43 | P44 | P42 | P45 | P41 | P12 | P53 | P55 | VSS_ USB | USB0_ DM | 5 |
| 4 | VREFL0 | P40 | VREFH0 | VBATT | P34 | P32 | P27 | P15 | P13 | P14 | 4 |
| 3 | P07 | AVCC0 | PJ3 | MD/ FINED | RES# | P35 | P30 | P16 | P17 | P20 | 3 |
| 2 | AVCC1 | AVSS0 | AVSS1 | XCOUT | VSS | VCC | P31 | P25 | P21 | P22 | 2 |
| 1 | P05 | EMLE | VCL | XCIN | XTAL | EXTAL | P33 | P26 | P24 | P23 | 1 |
| | A | B | C | D | E | F | G | H | J | K | |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (100-Pin TFLGA).

**Figure 1.8 Pin Assignment (100-Pin TFLGA)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pin and Pin Functions (100-Pin LFQFP).

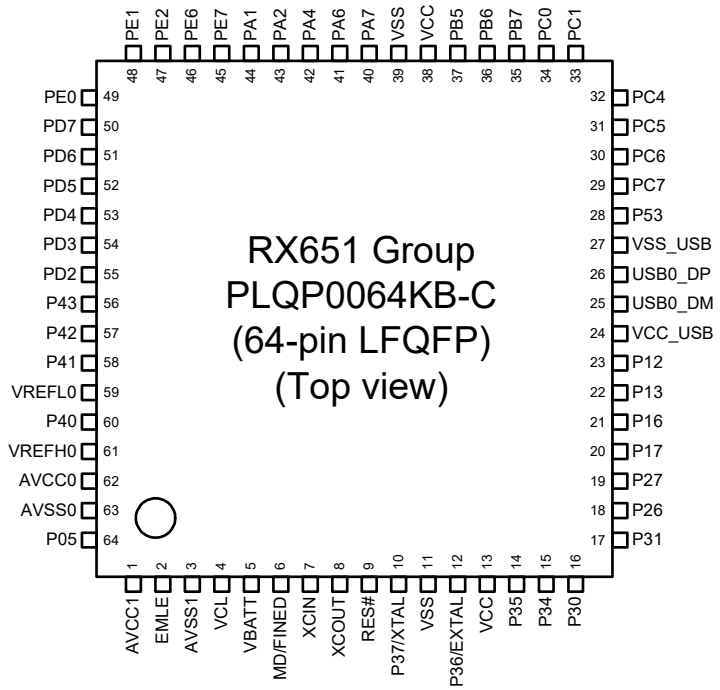
**Figure 1.9 Pin Assignment (100-Pin LFQFP)**

RX651 Group
PTBG0064KB-A (64-Pin TFBGA)
(Upper Perspective View)

| | A | B | C | D | E | F | G | H | |
|---|---|---|---|---|---|---|---|---|---|
| 8 | PE2 | PE6 | PE7 | PA4 | VSS | PB5 | PC0 | PC1 | 8 |
| 7 | PE0 | PE1 | PA1 | PA2 | VCC | PB6 | PC5 | PC4 | 7 |
| 6 | PD7 | PD6 | PD5 | PA6 | PA7 | PB7 | PC7 | PC6 | 6 |
| 5 | PD2 | PD3 | PD4 | P43 | BSCANP | P53 | VSS_USB | USB0_DP | 5 |
| 4 | VREFL0 | P42 | P41 | P40 | P13 | P12 | VCC_USB | USB0_DM | 4 |
| 3 | VREFH0 | AVCC0 | MD/FINED | RES# | P34 | P35 | P30 | P16 | 3 |
| 2 | AVSS0 | AVSS1 | VBATT | XCOUT | VSS | VCC | P31 | P17 | 2 |
| 1 | AVCC1 | EMLE | VCL | XCIN | XTAL | EXTAL | P27 | P26 | 1 |
| | A | B | C | D | E | F | G | H | |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.11, List of Pin and Pin Functions (64-Pin TFBGA).

**Figure 1.10 Pin Assignment (64-Pin TFBGA)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.12, List of Pin and Pin Functions (64-Pin LFQFP).

**Figure 1.11 Pin Assignment (64-Pin LFQFP)**

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| A1 | AVSS0 | | | | | | | | |
| A2 | AVCC0 | | | | | | | | |
| A3 | VREFL0 | | | | | | | | |
| A4 | | P42 | | | | | | IRQ10-DS | AN002 |
| A5 | | P46 | | | | | | IRQ14-DS | AN006 |
| A6 | VCC | | | | | | | | |
| A7 | VSS | | | | | | | | |
| A8 | | P94 | D20/A20 | | | | | | |
| A9 | VCC | | | | | | | | |
| A10 | TRSYNC1 | P97 | D23/A23 | | | | | | |
| A11 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | SSLC2-A | QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B | IRQ6 | AN106 |
| A12 | | P60 | CS0# | | | | | | |
| A13 | | P63 | CAS#/ D2[A2/D2]/ CS3# | | | | | | |
| A14 | | PE1 | D9[A9/D9]/ D1[A1/D1] | MTIOC4C/ MTIOC3B/ PO18 | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | LCD_DATA15-B | | ANEX1 |
| A15 | | PE2 | D10[A10/ D10]/D2[A2/ D2] | MTIOC4A/ PO23/TIC3 | RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B | MMC_D6-B | LCD_DATA14-B | IRQ7-DS | AN100 |
| B1 | | P05 | | | | | | IRQ13 | DA1 |
| B2 | | P07 | | | | | | IRQ15 | ADTRG0# |
| B3 | | P40 | | | | | | IRQ8-DS | AN000 |
| B4 | | P41 | | | | | | IRQ9-DS | AN001 |
| B5 | | P47 | | | | | | IRQ15-DS | AN007 |
| B6 | | P91 | D17/A17 | | SCK7 | | | | AN115 |
| B7 | | P92 | D18/A18 | POE4# | RXD7/SMISO7/ SSCL7 | | | | AN116 |
| B8 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | MOSIC-A/CTX0 | | LCD_DATA23-B | IRQ1 | AN109 |
| B9 | TRDATA5 | P96 | D22/A22 | | | | | | |
| B10 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | SSLC0-A | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B | IRQ4 | AN112 |
| B11 | TRDATA7 | PG1 | D25 | | | | | | |
| B12 | VSS | | | | | | | | |
| B13 | | P64 | WE#/D3[A3/ D3]/CS4# | | | | | | |
| B14 | | PE0 | D8[A8/D8]/ D0[A0/D0] | MTIOC3D | SCK12/SSLB1-B | MMC_D4-B | LCD_DATA16-B | | ANEX0 |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| B15 | | PE3 | D11[A11/D11]/D3[A3/D3] | MTIOC4B/PO26/TOC3/POE8# | ET0_ERXD3/CTS12#/RTS12#/SS12# | MMC_D7-B | LCD_DATA13-B | | AN101 |
| C1 | AVSS1 | | | | | | | | |
| C2 | AVCC1 | | | | | | | | |
| C3 | VREFH0 | | | | | | | | |
| C4 | | P43 | | | | | | IRQ11-DS | AN003 |
| C5 | | P45 | | | | | | IRQ13-DS | AN005 |
| C6 | | P90 | D16/A16 | | TXD7/SMOSI7/SSDA7 | | | | AN114 |
| C7 | | PD0 | D0[A0/D0] | POE4# | | | LCD_EXTCLK-B | IRQ0 | AN108 |
| C8 | | PD2 | D2[A2/D2] | MTIOC4D/TIC2 | MISOC-A/CRX0 | QIO2-B/SDHI_D2-B/MMC_D2-B | LCD_DATA22-B | IRQ2 | AN110 |
| C9 | | PD3 | D3[A3/D3] | MTIOC8D/TOC2/POE8# | RSPCKC-A | QIO3-B/SDHI_D3-B/MMC_D3-B | LCD_DATA21-B | IRQ3 | AN111 |
| C10 | TRDATA6 | PG0 | D24 | | | | | | |
| C11 | VCC | | | | | | | | |
| C12 | | P62 | RAS#/D1[A1/D1]/CS2# | | | | | | |
| C13 | | PE4 | D12[A12/D12]/D4[A4/D4] | MTIOC4D/MTIOC1A/PO28 | ET0_ERXD2/SSLB0-B | | LCD_DATA12-B | | AN102 |
| C14 | VSS | | | | | | | | |
| C15 | | P70 | SDCLK | | | | | | |
| D1 | | P01 | | TMCI0 | RXD6/SMISO6/SSCL6 | | | IRQ9 | AN119 |
| D2 | | P02 | | TMCI1 | SCK6 | | | IRQ10 | AN120 |
| D3 | | P03 | | | | | | IRQ11 | DA0 |
| D4 | | P00 | | TMRI0 | TXD6/SMOSI6/SSDA6 | | | IRQ8 | AN118 |
| D5 | | P44 | | | | | | IRQ12-DS | AN004 |
| D6 | | P93 | D19/A19 | POE0# | CTS7#/RTS7#/SS7# | | | | AN117 |
| D7 | TRDATA4 | P95 | D21/A21 | | | | | | |
| D8 | VSS | | | | | | | | |
| D9 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/POE10# | SSLC1-A | QSPCLK-B/SDHI_CLK-B/MMC_CLK-B | LCD_DATA19-B | IRQ5 | AN113 |
| D10 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | SSLC3-A | QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B | LCD_DATA17-B | IRQ7 | AN107 |
| D11 | | P61 | SDCS#/D0[A0/D0]/CS1# | | | | | | |
| D12 | | PE5 | D13[A13/D13]/D5[A5/D5] | MTIOC4C/MTIOC2B | ET0_RX_CLK/REF50CK0/RSPCKB-B | | LCD_DATA11-B | IRQ5 | AN103 |
| D13 | VCC | | | | | | | | |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| D14 | | PE7 | D15[A15/D15]/D7[A7/D7] | MTIOC6A/TOC1 | MISOB-B | SDHI_WP/MMC_RES#-B | LCD_DATA9-B | IRQ7 | AN105 |
| D15 | | P65 | CKE/CS5# | | | | | | |
| E1 | | PJ5 | | POE8# | CTS2#/RTS2#/SS2# | | | | |
| E2 | EMLE | | | | | | | | |
| E3 | | PF5 | | | | | | IRQ4 | |
| E4 | VSS | | | | | | | | |
| E5 *1 | NC | | | | | | | | |
| E12 | | PE6 | D14[A14/D14]/D6[A6/D6] | MTIOC6C/TIC1 | MOSIB-B | SDHI_CD/MMC_CD-B | LCD_DATA10-B | IRQ6 | AN104 |
| E13 | TRDATA0 | PG2 | D26 | | | | | | |
| E14 | TRDATA1 | PG3 | D27 | | | | | | |
| E15 | | P67 | DQM1/CS7# | MTIOC7C | | | | IRQ15 | |
| F1 | VBATT | | | | | | | | |
| F2 | VCL | | | | | | | | |
| F3 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0# | | | | |
| F4 | BSCANP | | | | | | | | |
| F12 | | P66 | DQM0/CS6# | MTIOC7D | | | | | |
| F13 | TRSYNC | PG4 | D28 | | | | | | |
| F14 | | PA0 | DQM2/BC0#/A0 | MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF | ET0_TX_EN/RMII0_TXD_EN/SSLA1-B | | LCD_DATA8-B | | |
| F15 | VSS | | | | | | | | |
| G1 | XCIN | | | | | | | | |
| G2 | XCOUT | | | | | | | | |
| G3 | MD/FINED | | | | | | | | |
| G4 | TRST# | PF4 | | | | | | | |
| G12 | TRCLK | PG5 | D29 | | | | | | |
| G13 | TRDATA2 | PG6 | D30 | | | | | | |
| G14 | | PA1 | DQM3/A1 | MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17 | ET0_WOL/SCK5/SSLA2-B | | LCD_DATA7-B | IRQ11 | |
| G15 | VCC | | | | | | | | |
| H1 | XTAL | P37 | | | | | | | |
| H2 | VSS | | | | | | | | |
| H3 | RES# | | | | | | | | |
| H4 | UPSEL | P35 | | | | | | NMI | |
| H12 | | PA4 | A4 | MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20 | ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B | | LCD_DATA4-B | IRQ5-DS | |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| H13 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | ET0_MDIO/ RXD5/SMISO5/ SSCL5 | | LCD_DATA5-B | IRQ6-DS | |
| H14 | | PA2 | A2 | MTIOC7A/ PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | LCD_DATA6-B | | |
| H15 | TRDATA3 | PG7 | D31 | | | | | | |
| J1 | EXTAL | P36 | | | | | | | |
| J2 | VCC | | | | | | | | |
| J3 | | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | ET0_LINKSTA/ SCK6/SCK0 | | | IRQ4 | |
| J4 | TMS | PF3 | | | | | | | |
| J12 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | ET0_LINKSTA/ RSPCKA-B | | LCD_DATA3-B | | |
| J13 | VSS | | | | | | | | |
| J14 | | PA7 | A7 | TIOCB2/PO23 | ET0_WOL/ MISOA-B | | LCD_DATA1-B | | |
| J15 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B | | LCD_DATA2-B | | |
| K1 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0 | PCKO | | IRQ3-DS | |
| K2 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN | VSYNC | | IRQ2-DS | |
| K3 | TDI | PF2 | | | RXD1/SMISO1/ SSCL1 | | | | |
| K4 | TCK | PF1 | | | SCK1 | | | | |
| K12 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6# | SDSI_D2-B | LCD_TCON2-B | | |
| K13 | | P71 | A18/CS1# | | ET0_MDIO | | | | |
| K14 | VCC | | | | | | | | |
| K15 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6 | | LCD_DATA0-B | IRQ12 | |
| L1 | | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0-A | | | IRQ1-DS | |
| L2 | | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | | IRQ0-DS | |
| L3 | TDO | PF0 | | | TXD1/SMOSI1/ SSDA1 | | | | |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| L4 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3 | SDHI_CD/HSYNC | | | ADTRG0 # |
| L12 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11 | SDSI_D0-B | | | |
| L13 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6 | SDSI_D3-B | LCD_TC ON1-B | | |
| L14 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6 | | LCD_TC ON3-B | IRQ4-DS | |
| L15 | | P72 | A19/CS2# | | ET0_MDC | | LCD_DA TA23-A | | |
| M1 | | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | SCK1/RSPCKB-A | | | | |
| M2 | | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A | | | | |
| M3 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | SCK3/ USB0_VBUSEN | SDHI_WP/PIXCLK | | | |
| M4 | | P86 | | MTIOC4D/ TIOCA0 | SMISO10/ SSCL10/RXD10 | PIXD1 | | | |
| M5 | | PJ2 | | | TXD8/SMOSI8/ SSDA8/SSLC3-B | | LCD_TC ON2-A | | |
| M6 | | PJ1 | | MTIOC6A | RXD8/SMISO8/ SSCL8/SSLC2-B | | LCD_TC ON3-A | | |
| M7 | | P85 | | MTIOC6C/ TIOCC0 | | | LCD_DA TA1-A | | |
| M8 | | P55 | D0[A0/D0]/ EDREQ0/ WAIT# | MTIOC4D/ TMO3 | ET0_EXOUT/ TXD7/SMOSI7/ SSDA7/MISOC-B/CRX1 | | LCD_DA TA5-A | IRQ10 | |
| M9 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | | |
| M10 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A | MMC_D5-A | LCD_DA TA11-A | | |
| M11 | | P81 | EDACK0 | MTIOC3D/ PO27 | ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10 | QIO3-A/SDHI_CD/ MMC_D3-A | LCD_DA TA13-A | | |
| M12 | | P77 | CS7# | PO23 | ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11 | QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A | LCD_DA TA17-A | | |
| M13 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11 | SDSI_D1-B | | | |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (6/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| M14 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11 | SDSI_CLK-B | LCD_CLK-B | | |
| M15 | | PB4 | A12 | TIOCA4/PO28 | ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11# | SDSI_CMD-B | LCD_TCON0-B | | |
| N1 | VCC | | | | | | | | |
| N2 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0# | SDHI_D1-C/PIXD7 | | | |
| N3 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCURB | SDHI_D0-C/PIXD6 | | | |
| N4 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS | PIXD0 | | IRQ5 | |
| N5 | | P12 | WR3#/BC3# | MTIC5U/ TMCI1 | RXD2/SMISO2/ SSCL2/ SCL0[FM+] | | LCD_TCON1-A | IRQ2 | |
| N6 | | PJ0 | | MTIOC6B | SCK8/SSLC1-B | | LCD_DATA0-A | | |
| N7 | | P84 | | MTIOC6D | | | LCD_DATA2-A | | |
| N8 | | P54 | D1[A1/D1]/ EDACK0/ ALE | MTIOC4B/ TMCI1 | ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/MOSIC-B/ CTX1 | | LCD_DATA6-A | | |
| N9 | | P51 | WR1#/ BC1#/ WAIT# | | SCK2/SSLB2-A | | | | |
| N10 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | MMC_D7-A | LCD_DATA9-A | IRQ14 | |
| N11 | | P82 | EDREQ1 | MTIOC4A/ PO28 | ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10 | MMC_D4-A | LCD_DATA12-A | | |
| N12 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | ET0_TX_ER/ TXD5/SMOSI5/ SSDA5 | QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A | LCD_DATA16-A | | |
| N13 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |
| N14 | | P73 | CS3# | PO16 | ET0_WOL | | LCD_EXTCLK-A | | |
| N15 | VSS | | | | | | | | |
| P1 | VSS | | | | | | | | |
| P2 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | SDHI_D3-C/PIXD3 | | IRQ7 | ADTRG1# |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (7/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| P3 | | P87 | | MTIOC4C/ TIOCA2 | SMOSI10/ SSDA10/TXD10 | SDHI_D2-C/PIXD2 | | | |
| P4 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | LCD_CLK-A | IRQ4 | |
| P5 | VCC_USB | | | | | | | | |
| P6 | VSS_USB | | | | | | | | |
| P7 | | P57 | | | RXD7/SMISO7/ SSCL7/SSLC0-B | | LCD_DATA3-A | | |
| P8 | | P10 | ALE | MTIC5W/ TMRI3 | | | | IRQ0 | |
| P9 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | | |
| P10 | | P83 | EDACK1 | MTIOC4C | ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10# | | LCD_DATA8-A | | |
| P11 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | MMC_D6-A | LCD_DATA10-A | IRQ13 | |
| P12 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A | LCD_DATA15-A | | |
| P13 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A | LCD_DATA19-A | | |
| P14 | | P75 | CS5# | PO20 | ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11# | SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A | LCD_DATA20-A | | |
| P15 | VCC | | | | | | | | |
| R1 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN | SDHI_CLK-C/ PIXD5 | | IRQ9 | |
| R2 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID | SDHI_CMD-C/ PIXD4 | | IRQ8 | |
| R3 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | IRQ6 | ADTRG0# |
| R4 | | P13 | WR2#/BC2# | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/ SDA0[FM+] | | LCD_TCON0-A | IRQ3 | ADTRG1# |
| R5 | | | | | USB0_DM | | | | |
| R6 | | | | | USB0_DP | | | | |
| R7 | | P56 | EDACK1 | MTIOC3C/ TIOCA1 | SCK7/RSPCKC-B | | LCD_DATA4-A | | |
| R8 | | P11 | | MTIC5V/TMCI3 | SCK2 | | LCD_DATA7-A | IRQ1 | |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (8/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| R9 | | P53*2 | BCLK | | | | | | |
| R10 | VSS | | | | | | | | |
| R11 | VCC | | | | | | | | |
| R12 | | P80 | EDREQ0 | MTIOC3B/ PO26 | ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10# | QIO2-A/SDHI_WP/ MMC_D2-A | LCD_DATA14-A | | |
| R13 | | P76 | CS6# | PO22 | ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11 | QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A | LCD_DATA18-A | | |
| R14 | | P74 | A20/CS4# | PO19 | ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11# | | LCD_DATA21-A | | |
| R15 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | LCD_DATA22-A | IRQ12 | |

Note 1. The 176-pin LFBGA does not include the E5 pin.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (1/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 1 | AVSS0 | | | | | | | | |
| 2 | | P05 | | | | | | IRQ13 | DA1 |
| 3 | AVCC1 | | | | | | | | |
| 4 | | P03 | | | | | | IRQ11 | DA0 |
| 5 | AVSS1 | | | | | | | | |
| 6 | | P02 | | TMCI1 | SCK6 | | | IRQ10 | AN120 |
| 7 | | P01 | | TMCI0 | RXD6/SMISO6/ SSCL6 | | | IRQ9 | AN119 |
| 8 | | P00 | | TMRI0 | TXD6/SMOSI6/ SSDA6 | | | IRQ8 | AN118 |
| 9 | | PF5 | | | | | | IRQ4 | |
| 10 | EMLE | | | | | | | | |
| 11 | | PJ5 | | POE8# | CTS2#/RTS2#/ SS2# | | | | |
| 12 | VSS | | | | | | | | |
| 13 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0# | | | | |
| 14 | VCL | | | | | | | | |
| 15 | VBATT | | | | | | | | |
| 16 | NC | | | | | | | | |
| 17 | TRST# | PF4 | | | | | | | |
| 18 | MD/FINED | | | | | | | | |
| 19 | XCIN | | | | | | | | |
| 20 | XCOUT | | | | | | | | |
| 21 | RES# | | | | | | | | |
| 22 | XTAL | P37 | | | | | | | |
| 23 | VSS | | | | | | | | |
| 24 | EXTAL | P36 | | | | | | | |
| 25 | VCC | | | | | | | | |
| 26 | UPSEL | P35 | | | | | | NMI | |
| 27 | | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | ET0_LINKSTA/ SCK6/SCK0 | | | IRQ4 | |
| 28 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0 | PCKO | | IRQ3-DS | |
| 29 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN | VSYNC | | IRQ2-DS | |
| 30 | TMS | PF3 | | | | | | | |
| 31 | TDI | PF2 | | | RXD1/SMISO1/ SSCL1 | | | | |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (2/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 32 | | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0-A | | | IRQ1-DS | |
| 33 | | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | | IRQ0-DS | |
| 34 | TCK | PF1 | | | SCK1 | | | | |
| 35 | TDO | PF0 | | | TXD1/SMOSI1/ SSDA1 | | | | |
| 36 | | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | SCK1/RSPCKB-A | | | | |
| 37 | | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A | | | | |
| 38 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3 | SDHI_CD/HSYNC | | | ADTRG0# |
| 39 | VCC | | | | | | | | |
| 40 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | SCK3/ USB0_VBUSEN | SDHI_WP/PIXCLK | | | |
| 41 | VSS | | | | | | | | |
| 42 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0# | SDHI_D1-C/PIXD7 | | | |
| 43 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCURB | SDHI_D0-C/PIXD6 | | | |
| 44 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN | SDHI_CLK-C/ PIXD5 | | IRQ9 | |
| 45 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID | SDHI_CMD-C/ PIXD4 | | IRQ8 | |
| 46 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | SDHI_D3-C/PIXD3 | | IRQ7 | ADTRG1# |
| 47 | | P87 | | MTIOC4C/ TIOCA2 | SMOSI10/ SSDA10/TXD10 | SDHI_D2-C/PIXD2 | | | |
| 48 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | IRQ6 | ADTRG0# |
| 49 | | P86 | | MTIOC4D/ TIOCA0 | SMISO10/ SSCL10/RXD10 | PIXD1 | | | |
| 50 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS | PIXD0 | | IRQ5 | |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (3/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 51 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | LCD_CLK-A | IRQ4 | |
| 52 | | P13 | WR2#/BC2# | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/ SDA0[FM+] | | LCD_TCON0-A | IRQ3 | ADTRG1# |
| 53 | | P12 | WR3#/ BC3# | MTIC5U/ TMCI1 | RXD2/SMISO2/ SSCL2/ SCL0[FM+] | | LCD_TCON1-A | IRQ2 | |
| 54 | VCC_USB | | | | | | | | |
| 55 | | | | | USB0_DM | | | | |
| 56 | | | | | USB0_DP | | | | |
| 57 | VSS_USB | | | | | | | | |
| 58 | | PJ2 | | | TXD8/SMOSI8/ SSDA8/SSLC3-B | | LCD_TCON2-A | | |
| 59 | | PJ1 | | MTIOC6A | RXD8/SMISO8/ SSCL8/SSLC2-B | | LCD_TCON3-A | | |
| 60 | | PJ0 | | MTIOC6B | SCK8/SSLC1-B | | LCD_DATA0-A | | |
| 61 | | P85 | | MTIOC6C/ TIOCC0 | | | LCD_DATA1-A | | |
| 62 | | P84 | | MTIOC6D | | | LCD_DATA2-A | | |
| 63 | | P57 | | | RXD7/SMISO7/ SSCL7/SSLC0-B | | LCD_DATA3-A | | |
| 64 | | P56 | EDACK1 | MTIOC3C/ TIOCA1 | SCK7/RSPCKC-B | | LCD_DATA4-A | | |
| 65 | | P55 | D0[A0/D0]/ EDREQ0/ WAIT# | MTIOC4D/ TMO3 | ET0_EXOUT/ TXD7/SMOSI7/ SSDA7/MISOC-B/CRX1 | | LCD_DATA5-A | IRQ10 | |
| 66 | | P54 | D1[A1/D1]/ EDACK0/ ALE | MTIOC4B/ TMCI1 | ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/MOSIC-B/ CTX1 | | LCD_DATA6-A | | |
| 67 | | P11 | | MTIC5V/TMCI3 | SCK2 | | LCD_DATA7-A | IRQ1 | |
| 68 | | P10 | ALE | MTIC5W/ TMRI3 | | | | IRQ0 | |
| 69 | | P53*1 | BCLK | | | | | | |
| 70 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | | |
| 71 | | P51 | WR1#/ BC1#/ WAIT# | | SCK2/SSLB2-A | | | | |
| 72 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | | |
| 73 | VSS | | | | | | | | |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (4/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 74 | | P83 | EDACK1 | MTIOC4C | ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10# | | LCD_DATA8-A | | |
| 75 | VCC | | | | | | | | |
| 76 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | MMC_D7-A | LCD_DATA9-A | IRQ14 | |
| 77 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | MMC_D6-A | LCD_DATA10-A | IRQ13 | |
| 78 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A | MMC_D5-A | LCD_DATA11-A | | |
| 79 | | P82 | EDREQ1 | MTIOC4A/ PO28 | ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10 | MMC_D4-A | LCD_DATA12-A | | |
| 80 | | P81 | EDACK0 | MTIOC3D/ PO27 | ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10 | QIO3-A/SDHI_CD/ MMC_D3-A | LCD_DATA13-A | | |
| 81 | | P80 | EDREQ0 | MTIOC3B/ PO26 | ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10# | QIO2-A/SDHI_WP/ MMC_D2-A | LCD_DATA14-A | | |
| 82 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A | LCD_DATA15-A | | |
| 83 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | ET0_TX_ER/ TXD5/SMOSI5/ SSDA5 | QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A | LCD_DATA16-A | | |
| 84 | | P77 | CS7# | PO23 | ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11 | QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A | LCD_DATA17-A | | |
| 85 | | P76 | CS6# | PO22 | ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11 | QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A | LCD_DATA18-A | | |
| 86 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A | LCD_DATA19-A | | |
| 87 | | P75 | CS5# | PO20 | ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11# | SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A | LCD_DATA20-A | | |
| 88 | | P74 | A20/CS4# | PO19 | ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11# | | LCD_DATA21-A | | |
| 89 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | LCD_DATA22-A | IRQ12 | |
| 90 | VCC | | | | | | | | |
| 91 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (5/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 92 | VSS | | | | | | | | |
| 93 | | P73 | CS3# | PO16 | ET0_WOL | | LCD_EXTCLK-A | | |
| 94 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11 | SDSI_D1-B | | | |
| 95 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11 | SDSI_D0-B | | | |
| 96 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11 | SDSI_CLK-B | LCD_CLK-B | | |
| 97 | | PB4 | A12 | TIOCA4/PO28 | ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11# | SDSI_CMD-B | LCD_TCON0-B | | |
| 98 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6 | SDSI_D3-B | LCD_TCON1-B | | |
| 99 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6# | SDSI_D2-B | LCD_TCON2-B | | |
| 100 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6 | | LCD_TCON3-B | IRQ4-DS | |
| 101 | | P72 | A19/CS2# | | ET0_MDC | | LCD_DATA23-A | | |
| 102 | | P71 | A18/CS1# | | ET0_MDIO | | | | |
| 103 | VCC | | | | | | | | |
| 104 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6 | | LCD_DATA0-B | IRQ12 | |
| 105 | VSS | | | | | | | | |
| 106 | | PA7 | A7 | TIOCB2/PO23 | ET0_WOL/ MISOA-B | | LCD_DATA1-B | | |
| 107 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B | | LCD_DATA2-B | | |
| 108 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | ET0_LINKSTA/ RSPCKA-B | | LCD_DATA3-B | | |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (6/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 109 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B | | LCD_DATA4-B | IRQ5-DS | |
| 110 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | ET0_MDIO/ RXD5/SMISO5/ SSCL5 | | LCD_DATA5-B | IRQ6-DS | |
| 111 | TRDATA3 | PG7 | D31 | | | | | | |
| 112 | | PA2 | A2 | MTIOC7A/ PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | LCD_DATA6-B | | |
| 113 | TRDATA2 | PG6 | D30 | | | | | | |
| 114 | | PA1 | DQM3/A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | ET0_WOL/ SCK5/SSLA2-B | | LCD_DATA7-B | IRQ11 | |
| 115 | VCC | | | | | | | | |
| 116 | TRCLK | PG5 | D29 | | | | | | |
| 117 | VSS | | | | | | | | |
| 118 | | PA0 | DQM2/ BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B | | LCD_DATA8-B | | |
| 119 | TRSYNC | PG4 | D28 | | | | | | |
| 120 | | P67 | DQM1/CS7# | MTIOC7C | | | | IRQ15 | |
| 121 | TRDATA1 | PG3 | D27 | | | | | | |
| 122 | | P66 | DQM0/CS6# | MTIOC7D | | | | | |
| 123 | TRDATA0 | PG2 | D26 | | | | | | |
| 124 | | P65 | CKE/CS5# | | | | | | |
| 125 | | PE7 | D15[A15/ D15]/D7[A7/ D7] | MTIOC6A/ TOC1 | MISOB-B | SDHI_WP/ MMC_RES#-B | LCD_DATA9-B | IRQ7 | AN105 |
| 126 | | PE6 | D14[A14/ D14]/D6[A6/ D6] | MTIOC6C/TIC1 | MOSIB-B | SDHI_CD/ MMC_CD-B | LCD_DATA10-B | IRQ6 | AN104 |
| 127 | VCC | | | | | | | | |
| 128 | | P70 | SDCLK | | | | | | |
| 129 | VSS | | | | | | | | |
| 130 | | PE5 | D13[A13/ D13]/D5[A5/ D5] | MTIOC4C/ MTIOC2B | ET0_RX_CLK/ REF50CK0/ RSPCKB-B | | LCD_DATA11-B | IRQ5 | AN103 |
| 131 | | PE4 | D12[A12/ D12]/D4[A4/ D4] | MTIOC4D/ MTIOC1A/ PO28 | ET0_ERXD2/ SSLB0-B | | LCD_DATA12-B | | AN102 |
| 132 | | PE3 | D11[A11/ D11]/D3[A3/ D3] | MTIOC4B/ PO26/TOC3/ POE8# | ET0_ERXD3/ CTS12#/ RTS12#/SS12# | MMC_D7-B | LCD_DATA13-B | | AN101 |
| 133 | | PE2 | D10[A10/ D10]/D2[A2/ D2] | MTIOC4A/ PO23/TIC3 | RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B | MMC_D6-B | LCD_DATA14-B | IRQ7-DS | AN100 |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (7/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 134 | | PE1 | D9[A9/D9]/ D1[A1/D1] | MTIOC4C/ MTIOC3B/ PO18 | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | LCD_DATA15-B | | ANEX1 |
| 135 | | PE0 | D8[A8/D8]/ D0[A0/D0] | MTIOC3D | SCK12/SSLB1-B | MMC_D4-B | LCD_DATA16-B | | ANEX0 |
| 136 | | P64 | WE#/D3[A3/ D3]/CS4# | | | | | | |
| 137 | | P63 | CAS#/ D2[A2/D2]/ CS3# | | | | | | |
| 138 | | P62 | RAS#/ D1[A1/D1]/ CS2# | | | | | | |
| 139 | | P61 | SDCS#/ D0[A0/D0]/ CS1# | | | | | | |
| 140 | VSS | | | | | | | | |
| 141 | | P60 | CS0# | | | | | | |
| 142 | VCC | | | | | | | | |
| 143 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | SSLC3-A | QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B | LCD_DATA17-B | IRQ7 | AN107 |
| 144 | TRDATA7 | PG1 | D25 | | | | | | |
| 145 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | SSLC2-A | QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B | IRQ6 | AN106 |
| 146 | TRDATA6 | PG0 | D24 | | | | | | |
| 147 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ POE10# | SSLC1-A | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DATA19-B | IRQ5 | AN113 |
| 148 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | SSLC0-A | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B | IRQ4 | AN112 |
| 149 | TRSYNC1 | P97 | D23/A23 | | | | | | |
| 150 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | RSPCKC-A | QIO3-B/SDHI_D3-B/MMC_D3-B | LCD_DATA21-B | IRQ3 | AN111 |
| 151 | VSS | | | | | | | | |
| 152 | TRDATA5 | P96 | D22/A22 | | | | | | |
| 153 | VCC | | | | | | | | |
| 154 | | PD2 | D2[A2/D2] | MTIOC4D/TIC2 | MISOC-A/CRX0 | QIO2-B/SDHI_D2-B/MMC_D2-B | LCD_DATA22-B | IRQ2 | AN110 |
| 155 | TRDATA4 | P95 | D21/A21 | | | | | | |
| 156 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | MOSIC-A/CTX0 | | LCD_DATA23-B | IRQ1 | AN109 |
| 157 | | P94 | D20/A20 | | | | | | |
| 158 | | PD0 | D0[A0/D0] | POE4# | | | LCD_EXTCLK-B | IRQ0 | AN108 |
| 159 | | P93 | D19/A19 | POE0# | CTS7#/RTS7#/ SS7# | | | | AN117 |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (8/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 160 | | P92 | D18/A18 | POE4# | RXD7/SMISO7/ SSCL7 | | | | AN116 |
| 161 | | P91 | D17/A17 | | SCK7 | | | | AN115 |
| 162 | VSS | | | | | | | | |
| 163 | | P90 | D16/A16 | | TXD7/SMOSI7/ SSDA7 | | | | AN114 |
| 164 | VCC | | | | | | | | |
| 165 | | P47 | | | | | | IRQ15-DS | AN007 |
| 166 | | P46 | | | | | | IRQ14-DS | AN006 |
| 167 | | P45 | | | | | | IRQ13-DS | AN005 |
| 168 | | P44 | | | | | | IRQ12-DS | AN004 |
| 169 | | P43 | | | | | | IRQ11-DS | AN003 |
| 170 | | P42 | | | | | | IRQ10-DS | AN002 |
| 171 | | P41 | | | | | | IRQ9-DS | AN001 |
| 172 | VREFL0 | | | | | | | | |
| 173 | | P40 | | | | | | IRQ8-DS | AN000 |
| 174 | VREFH0 | | | | | | | | |
| 175 | AVCC0 | | | | | | | | |
| 176 | | P07 | | | | | | IRQ15 | ADTRG0# |

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (1/7)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| A1 | AVSS0 | | | | | | | | |
| A2 | | P07 | | | | | | IRQ15 | ADTRG0# |
| A3 | | P40 | | | | | | IRQ8-DS | AN000 |
| A4 | | P42 | | | | | | IRQ10-DS | AN002 |
| A5 | | P45 | | | | | | IRQ13-DS | AN005 |
| A6 | | P90 | A16 | | TXD7/SMOSI7/SSDA7 | | | | AN114 |
| A7 | | P92 | A18 | POE4# | RXD7/SMISO7/SSCL7 | | | | AN116 |
| A8 | | PD2 | D2[A2/D2] | MTIOC4D/TIC2 | MISOC-A/CRX0 | QIO2-B/SDHI_D2-B/MMC_D2-B | LCD_DATA22-B*1 | IRQ2 | AN110 |
| A9 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/POE4# | SSLC2-A | QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B | LCD_DATA18-B*1 | IRQ6 | AN106 |
| A10 | VSS | | | | | | | | |
| A11 | | P62 | RAS#/D1[A1/D1]*1/CS2# | | | | | | |
| A12 | | PE1 | D9[A9/D9]/D1[A1/D1]*1 | MTIOC4C/MTIOC3B/PO18 | TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B | MMC_D5-B | LCD_DATA15-B*1 | | ANEX1 |
| A13 | | PE3 | D11[A11/D11]/D3[A3/D3]*1 | MTIOC4B/PO26/TOC3/POE8# | ET0_ERXD3/CTS12#/RTS12#/SS12# | MMC_D7-B | LCD_DATA13-B*1 | | AN101 |
| B1 | AVCC1 | | | | | | | | |
| B2 | AVCC0 | | | | | | | | |
| B3 | | P05 | | | | | | IRQ13 | DA1 |
| B4 | VREFL0 | | | | | | | | |
| B5 | | P43 | | | | | | IRQ11-DS | AN003 |
| B6 | | P47 | | | | | | IRQ15-DS | AN007 |
| B7 | | P91 | A17 | | SCK7 | | | | AN115 |
| B8 | | PD0 | D0[A0/D0] | POE4# | | | LCD_EXTCLK-B*1 | IRQ0 | AN108 |
| B9 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | SSLC0-A | QSSL-B/SDHI_CMD-B/MMC_CMD-B | LCD_DATA20-B*1 | IRQ4 | AN112 |
| B10 | VCC | | | | | | | | |
| B11 | | P61 | SDCS#/D0[A0/D0]*1/CS1# | | | | | | |
| B12 | | PE2 | D10[A10/D10]/D2[A2/D2]*1 | MTIOC4A/PO23/TIC3 | RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B | MMC_D6-B | LCD_DATA14-B*1 | IRQ7-DS | AN100 |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/7)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| B13 | | PE4 | D12[A12/D12]/D4[A4/D4]*1 | MTIOC4D/MTIOC1A/PO28 | ET0_ERXD2/SSLB0-B | | LCD_DATA12-B*1 | | AN102 |
| C1 | AVSS1 | | | | | | | | |
| C2 | | P02 | | TMCI1 | SCK6 | | | IRQ10 | AN120 |
| C3 | VREFH0 | | | | | | | | |
| C4 | | P41 | | | | | | IRQ9-DS | AN001 |
| C5 | | P46 | | | | | | IRQ14-DS | AN006 |
| C6 | VSS | | | | | | | | |
| C7 | | PD1 | D1[A1/D1] | MTIOC4B/POE0# | MOSIC-A/CTX0 | | LCD_DATA23-B*1 | IRQ1 | AN109 |
| C8 | | PD3 | D3[A3/D3] | MTIOC8D/TOC2/POE8# | RSPCKC-A | QIO3-B/SDHI_D3-B/MMC_D3-B | LCD_DATA21-B*1 | IRQ3 | AN111 |
| C9 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | SSLC3-A | QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B | LCD_DATA17-B*1 | IRQ7 | AN107 |
| C10 | | P63 | CAS#/D2[A2/D2]*1/CS3# | | | | | | |
| C11 | | PE0 | D8[A8/D8]/D0[A0/D0]*1 | MTIOC3D | SCK12/SSLB1-B | MMC_D4-B | LCD_DATA16-B*1 | | ANEX0 |
| C12 | | P70 | SDCLK | | | | | | |
| C13 | VSS | | | | | | | | |
| D1 | | P00 | | TMRI0 | TXD6/SMOSI6/SSDA6 | | | IRQ8 | AN118 |
| D2 | | PF5 | | | | | | IRQ4 | |
| D3 | | P03 | | | | | | IRQ11 | DA0 |
| D4 | | P01 | | TMCI0 | RXD6/SMISO6/SSCL6 | | | IRQ9 | AN119 |
| D5 | VCC | | | | | | | | |
| D6 | | P93 | A19 | POE0# | CTS7#/RTS7#/SS7# | | | | AN117 |
| D7 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/POE10# | SSLC1-A | QSPCLK-B/SDHI_CLK-B/MMC_CLK-B | LCD_DATA19-B*1 | IRQ5 | AN113 |
| D8 | | P60 | CS0# | | | | | | |
| D9 | | P64 | WE#/D3[A3/D3]*1/CS4# | | | | | | |
| D10 | | PE7 | D15[A15/D15]/D7[A7/D7]*1 | MTIOC6A/TOC1 | MISOB-B | SDHI_WP/MMC_RES#-B | LCD_DATA9-B*1 | IRQ7 | AN105 |
| D11 | VCC | | | | | | | | |
| D12 | | PE5 | D13[A13/D13]/D5[A5/D5]*1 | MTIOC4C/MTIOC2B | ET0_RX_CLK/REF50CK0/RSPCKB-B | | LCD_DATA11-B*1 | IRQ5 | AN103 |
| D13 | | PE6 | D14[A14/D14]/D6[A6/D6]*1 | MTIOC6C/TIC1 | MOSIB-B | SDHI_CD/MMC_CD-B | LCD_DATA10-B*1 | IRQ6 | AN104 |
| E1 | VSS | | | | | | | | |
| E2 | VCL | | | | | | | | |
| E3 | | PJ5 | | POE8# | CTS2#/RTS2#/SS2# | | | | |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/7)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| E4 | EMLE | | | | | | | | |
| E5 | | P44 | | | | | | IRQ12-DS | AN004 |
| E10 | | PA0 | BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B | | LCD_DATA8-B*1 | | |
| E11 | | P66 | DQM0/CS6# | MTIOC7D | | | | | |
| E12 | | P65 | CKE/CS5# | | | | | | |
| E13 | | P67 | DQM1/CS7# | MTIOC7C | | | | IRQ15 | |
| F1 | XCIN | | | | | | | | |
| F2 | XCOUT | | | | | | | | |
| F3 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0# | | | | |
| F4 | VBATT | | | | | | | | |
| F10 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | ET0_MDIO/ RXD5/SMISO5/ SSCL5 | | LCD_DATA5-B*1 | IRQ6-DS | |
| F11 | VSS | | | | | | | | |
| F12 | | PA1 | A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | ET0_WOL/ SCK5/SSLA2-B | | LCD_DATA7-B*1 | IRQ11 | |
| F13 | | PA2 | A2 | MTIOC7A/ PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | LCD_DATA6-B*1 | | |
| G1 | XTAL | P37 | | | | | | | |
| G2 | RES# | | | | | | | | |
| G3 | MD/FINED | | | | | | | | |
| G4 | BSCANP | | | | | | | | |
| G10 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | ET0_LINKSTA/ RSPCKA-B | | LCD_DATA3-B*1 | | |
| G11 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B | | LCD_DATA2-B*1 | | |
| G12 | VCC | | | | | | | | |
| G13 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B | | LCD_DATA4-B*1 | IRQ5-DS | |
| H1 | EXTAL | P36 | | | | | | | |
| H2 | VCC | | | | | | | | |
| H3 | VSS | | | | | | | | |
| H4 | UPSEL | P35 | | | | | | NMI | |
| H10 | | P72 | A19/CS2# | | ET0_MDC | | | | |
| H11 | | P71 | A18/CS1# | | ET0_MDIO | | | | |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (4/7)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| H12 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6 | | LCD_DATA0-B*1 | IRQ12 | |
| H13 | | PA7 | A7 | TIOCB2/PO23 | ET0_WOL/ MISOA-B | | LCD_DATA1-B*1 | | |
| J1 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | ET0_LINKSTA/ SCK6/SCK0 | | | IRQ4 | |
| J2 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0 | PCKO | | IRQ3-DS | |
| J3 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN | VSYNC | | IRQ2-DS | |
| J4 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | | IRQ0-DS | |
| J10 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6 | SDSI_D3-B | LCD_TCON1-B*1 | | |
| J11 | | PB4 | A12 | TIOCA4/PO28 | ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11# | SDSI_CMD-B | LCD_TCON0-B*1 | | |
| J12 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6# | SDSI_D2-B | LCD_TCON2-B*1 | | |
| J13 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6 | | LCD_TCON3-B*1 | IRQ4-DS | |
| K1 | TCK | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | SCK1/RSPCKB-A | | | | |
| K2 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A | | | | |
| K3 | TMS | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0-A | | | IRQ1-DS | |
| K4 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS | PIXD0 | | IRQ5 | |
| K5 | TRDATA2 | P54 | ALE/ D1[A1/D1]*1/ EDACK0 | MTIOC4B/ TMCI1 | ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1 | | | | |
| K6 | | P53*2 | BCLK | | | | | | |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (5/7)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| K7 | | P51 | WR1#/ BC1#/ WAIT# | | SCK2/SSLB2-A | | | | |
| K8 | VCC | | | | | | | | |
| K9 | TRDATA0 | P80 | EDREQ0 | MTIOC3B/ PO26 | ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10# | QIO2-A/SDHI_WP/ MMC_D2-A | | | |
| K10 | TRDATA6 | P76 | CS6# | PO22 | ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11 | QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A | | | |
| K11 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11 | SDSI_D1-B | | | |
| K12 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11 | SDSI_D0-B | | | |
| K13 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11 | SDSI_CLK-B | LCD_CLK-B*1 | | |
| L1 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3 | SDHI_CD*1/ HSYNC | | | ADTRG0# |
| L2 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0# | SDHI_D1-C*1/ PIXD7 | | | |
| L3 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | IRQ6 | ADTRG0# |
| L4 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | SCK3/ USB0_VBUSEN | SDHI_WP*1/ PIXCLK | | | |
| L5 | | P13 | | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/ SDA0[FM+] | | | IRQ3 | ADTRG1# |
| L6 | | P56 | EDACK1 | MTIOC3C/ TIOCA1 | SCK7*1 | | | | |
| L7 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | | |
| L8 | TRCLK | P83 | EDACK1 | MTIOC4C | ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10# | | | | |
| L9 | | PC5 | D3[A3/D3]*1/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A | MMC_D5-A | | | |
| L10 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A | | | |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (6/7)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| L11 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A | | | |
| L12 | TRDATA4 | P73 | CS3# | PO16 | ET0_WOL | | | | |
| L13 | VSS | | | | | | | | |
| M1 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCURB | SDHI_D0-C*1/ PIXD6 | | | |
| M2 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | SDHI_D3-C*1/ PIXD3 | | IRQ7 | ADTRG1# |
| M3 | | P86 | | MTIOC4D/ TIOCA0 | SMISO10/ SSCL10/RXD10 | PIXD1 | | | |
| M4 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/ SCL0[FM+] | | | IRQ2 | |
| M5 | VCC_USB | | | | | | | | |
| M6 | VSS_USB | | | | | | | | |
| M7 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | | |
| M8 | | PC6 | D2[A2/D2]*1/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | MMC_D6-A | | IRQ13 | |
| M9 | TRDATA1 | P81 | EDACK0 | MTIOC3D/ PO27 | ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10 | QIO3-A/SDHI_CD/ MMC_D3-A | | | |
| M10 | TRDATA7 | P77 | CS7# | PO23 | ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11 | QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A | | | |
| M11 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |
| M12 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | | IRQ12 | |
| M13 | VCC | | | | | | | | |
| N1 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN | SDHI_CLK-C*1/ PIXD5 | | IRQ9 | |
| N2 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID | SDHI_CMD-C*1/ PIXD4 | | IRQ8 | |
| N3 | | P87 | | MTIOC4C/ TIOCA2 | SMOSI10/ SSDA10/TXD10 | SDHI_D2-C*1/ PIXD2 | | | |
| N4 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | IRQ4 | |
| N5 | | | | | USB0_DM | | | | |
| N6 | | | | | USB0_DP | | | | |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (7/7)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| N7 | TRDATA3 | P55 | D0[A0/D0]*1/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | ET0_EXOUT/ TXD7*1/ SMOSI7*1/ SSDA7*1/CRX1 | | | IRQ10 | |
| N8 | VSS | | | | | | | | |
| N9 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | MMC_D7-A | | IRQ14 | |
| N10 | TRSYNC | P82 | EDREQ1 | MTIOC4A/ PO28 | ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10 | MMC_D4-A | | | |
| N11 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | ET0_TX_ER/ TXD5/SMOSI5/ SSDA5 | QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A | | | |
| N12 | TRSYNC1 | P75 | CS5# | PO20 | ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11# | SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A | | | |
| N13 | TRDATA5 | P74 | A20/CS4# | PO19 | ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11# | | | | |

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (1/7)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 1 | AVSS0 | | | | | | | | |
| 2 | | P05 | | | | | | IRQ13 | DA1 |
| 3 | AVCC1 | | | | | | | | |
| 4 | | P03 | | | | | | IRQ11 | DA0 |
| 5 | AVSS1 | | | | | | | | |
| 6 | | P02 | | TMCI1 | SCK6 | | | IRQ10 | AN120 |
| 7 | | P01 | | TMCI0 | RXD6/SMISO6/ SSCL6 | | | IRQ9 | AN119 |
| 8 | | P00 | | TMRI0 | TXD6/SMOSI6/ SSDA6 | | | IRQ8 | AN118 |
| 9 | | PF5 | | | | | | IRQ4 | |
| 10 | EMLE | | | | | | | | |
| 11 | | PJ5 | | POE8# | CTS2#/RTS2#/ SS2# | | | | |
| 12 | VSS | | | | | | | | |
| 13 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0# | | | | |
| 14 | VCL | | | | | | | | |
| 15 | VBATT | | | | | | | | |
| 16 | MD/FINED | | | | | | | | |
| 17 | XCIN | | | | | | | | |
| 18 | XCOUT | | | | | | | | |
| 19 | RES# | | | | | | | | |
| 20 | XTAL | P37 | | | | | | | |
| 21 | VSS | | | | | | | | |
| 22 | EXTAL | P36 | | | | | | | |
| 23 | VCC | | | | | | | | |
| 24 | UPSEL | P35 | | | | | | NMI | |
| 25 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | ET0_LINKSTA/ SCK6/SCK0 | | | IRQ4 | |
| 26 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0 | PCKO | | IRQ3-DS | |
| 27 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN | VSYNC | | IRQ2-DS | |
| 28 | TMS | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0-A | | | IRQ1-DS | |
| 29 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | | IRQ0-DS | |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (2/7)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 30 | TCK | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | SCK1/RSPCKB-A | | | | |
| 31 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A | | | | |
| 32 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3 | SDHI_CD*1/ HSYNC | | | ADTRG0# |
| 33 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | SCK3/ USB0_VBUSEN | SDHI_WP*1/ PIXCLK | | | |
| 34 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0# | SDHI_D1-C*1/ PIXD7 | | | |
| 35 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCURB | SDHI_D0-C*1/ PIXD6 | | | |
| 36 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN | SDHI_CLK-C*1/ PIXD5 | | IRQ9 | |
| 37 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID | SDHI_CMD-C*1/ PIXD4 | | IRQ8 | |
| 38 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | SDHI_D3-C*1/ PIXD3 | | IRQ7 | ADTRG1# |
| 39 | | P87 | | MTIOC4C/ TIOCA2 | SMOSI10/ SSDA10/TXD10 | SDHI_D2-C*1/ PIXD2 | | | |
| 40 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | IRQ6 | ADTRG0# |
| 41 | | P86 | | MTIOC4D/ TIOCA0 | SMISO10/ SSCL10/RXD10 | PIXD1 | | | |
| 42 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS | PIXD0 | | IRQ5 | |
| 43 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | IRQ4 | |
| 44 | | P13 | | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/ SDA0[FM+] | | | IRQ3 | ADTRG1# |
| 45 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/ SCL0[FM+] | | | IRQ2 | |
| 46 | VCC_USB | | | | | | | | |
| 47 | | | | | USB0_DM | | | | |
| 48 | | | | | USB0_DP | | | | |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (3/7)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 49 | VSS_USB | | | | | | | | |
| 50 | | P56 | EDACK1 | MTIOC3C/ TIOCA1 | SCK7*1 | | | | |
| 51 | TRDATA3 | P55 | D0[A0/D0]*1/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | ET0_EXOUT/ TXD7*1/ SMOSI7*1/ SSDA7*1/CRX1 | | | IRQ10 | |
| 52 | TRDATA2 | P54 | ALE/D1[A1/ D1]*1/ EDACK0 | MTIOC4B/ TMCI1 | ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1 | | | | |
| 53 | | P53*2 | BCLK | | | | | | |
| 54 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | | |
| 55 | | P51 | WR1#/ BC1#/ WAIT# | | SCK2/SSLB2-A | | | | |
| 56 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | | |
| 57 | VSS | | | | | | | | |
| 58 | TRCLK | P83 | EDACK1 | MTIOC4C | ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10# | | | | |
| 59 | VCC | | | | | | | | |
| 60 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | MMC_D7-A | | IRQ14 | |
| 61 | | PC6 | D2[A2/D2]*1/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | MMC_D6-A | | IRQ13 | |
| 62 | | PC5 | D3[A3/D3]*1/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A | MMC_D5-A | | | |
| 63 | TRSYNC | P82 | EDREQ1 | MTIOC4A/ PO28 | ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10 | MMC_D4-A | | | |
| 64 | TRDATA1 | P81 | EDACK0 | MTIOC3D/ PO27 | ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10 | QIO3-A/SDHI_CD/ MMC_D3-A | | | |
| 65 | TRDATA0 | P80 | EDREQ0 | MTIOC3B/ PO26 | ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10# | QIO2-A/SDHI_WP/ MMC_D2-A | | | |
| 66 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A | | | |
| 67 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | ET0_TX_ER/ TXD5/SMOSI5/ SSDA5 | QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A | | | |
| 68 | TRDATA7 | P77 | CS7# | PO23 | ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11 | QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A | | | |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (4/7)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 69 | TRDATA6 | P76 | CS6# | PO22 | ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11 | QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A | | | |
| 70 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A | | | |
| 71 | TRSYNC1 | P75 | CS5# | PO20 | ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11# | SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A | | | |
| 72 | TRDATA5 | P74 | A20/CS4# | PO19 | ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11# | | | | |
| 73 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | | IRQ12 | |
| 74 | VCC | | | | | | | | |
| 75 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |
| 76 | VSS | | | | | | | | |
| 77 | TRDATA4 | P73 | CS3# | PO16 | ET0_WOL | | | | |
| 78 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11 | SDSI_D1-B | | | |
| 79 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11 | SDSI_D0-B | | | |
| 80 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11 | SDSI_CLK-B | LCD_CLK-B*1 | | |
| 81 | | PB4 | A12 | TIOCA4/PO28 | ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11# | SDSI_CMD-B | LCD_TCON0-B*1 | | |
| 82 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6 | SDSI_D3-B | LCD_TCON1-B*1 | | |
| 83 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6# | SDSI_D2-B | LCD_TCON2-B*1 | | |
| 84 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6 | | LCD_TCON3-B*1 | IRQ4-DS | |
| 85 | | P72 | A19/CS2# | | ET0_MDC | | | | |
| 86 | | P71 | A18/CS1# | | ET0_MDIO | | | | |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (5/7)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 87 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6 | | LCD_DATA0-B*1 | IRQ12 | |
| 88 | | PA7 | A7 | TIOCB2/PO23 | ET0_WOL/ MISOA-B | | LCD_DATA1-B*1 | | |
| 89 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B | | LCD_DATA2-B*1 | | |
| 90 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | ET0_LINKSTA/ RSPCKA-B | | LCD_DATA3-B*1 | | |
| 91 | VCC | | | | | | | | |
| 92 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B | | LCD_DATA4-B*1 | IRQ5-DS | |
| 93 | VSS | | | | | | | | |
| 94 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | ET0_MDIO/ RXD5/SMISO5/ SSCL5 | | LCD_DATA5-B*1 | IRQ6-DS | |
| 95 | | PA2 | A2 | MTIOC7A/ PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | LCD_DATA6-B*1 | | |
| 96 | | PA1 | A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | ET0_WOL/ SCK5/SSLA2-B | | LCD_DATA7-B*1 | IRQ11 | |
| 97 | | PA0 | BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B | | LCD_DATA8-B*1 | | |
| 98 | | P67 | DQM1/CS7# | MTIOC7C | | | | IRQ15 | |
| 99 | | P66 | DQM0/CS6# | MTIOC7D | | | | | |
| 100 | | P65 | CKE/CS5# | | | | | | |
| 101 | | PE7 | D15[A15/ D15]/D7[A7/ D7]*1 | MTIOC6A/ TOC1 | MISOB-B | SDHI_WP/ MMC_RES#-B | LCD_DATA9-B*1 | IRQ7 | AN105 |
| 102 | | PE6 | D14[A14/ D14]/D6[A6/ D6]*1 | MTIOC6C/TIC1 | MOSIB-B | SDHI_CD/ MMC_CD-B | LCD_DATA10-B*1 | IRQ6 | AN104 |
| 103 | VCC | | | | | | | | |
| 104 | | P70 | SDCLK | | | | | | |
| 105 | VSS | | | | | | | | |
| 106 | | PE5 | D13[A13/ D13]/D5[A5/ D5]*1 | MTIOC4C/ MTIOC2B | ET0_RX_CLK/ REF50CK0/ RSPCKB-B | | LCD_DATA11-B*1 | IRQ5 | AN103 |
| 107 | | PE4 | D12[A12/ D12]/D4[A4/ D4]*1 | MTIOC4D/ MTIOC1A/ PO28 | ET0_ERXD2/ SSLB0-B | | LCD_DATA12-B*1 | | AN102 |
| 108 | | PE3 | D11[A11/ D11]/D3[A3/ D3]*1 | MTIOC4B/ PO26/TOC3/ POE8# | ET0_ERXD3/ CTS12#/ RTS12#/SS12# | MMC_D7-B | LCD_DATA13-B*1 | | AN101 |
| 109 | | PE2 | D10[A10/ D10]/D2[A2/ D2]*1 | MTIOC4A/ PO23/TIC3 | RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B | MMC_D6-B | LCD_DATA14-B*1 | IRQ7-DS | AN100 |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (6/7)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 110 | | PE1 | D9[A9/D9]/ D1[A1/D1]*1 | MTIOC4C/ MTIOC3B/ PO18 | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | LCD_DATA15-B*1 | | ANEX1 |
| 111 | | PE0 | D8[A8/D8]/ D0[A0/D0]*1 | MTIOC3D | SCK12/SSLB1-B | MMC_D4-B | LCD_DATA16-B*1 | | ANEX0 |
| 112 | | P64 | WE#/D3[A3/ D3]*1/CS4# | | | | | | |
| 113 | | P63 | CAS#/ D2[A2/D2]*1/ CS3# | | | | | | |
| 114 | | P62 | RAS#/ D1[A1/D1]*1/ CS2# | | | | | | |
| 115 | | P61 | SDCS#/ D0[A0/D0]*1/ CS1# | | | | | | |
| 116 | VSS | | | | | | | | |
| 117 | | P60 | CS0# | | | | | | |
| 118 | VCC | | | | | | | | |
| 119 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | SSLC3-A | QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B | LCD_DATA17-B*1 | IRQ7 | AN107 |
| 120 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | SSLC2-A | QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B*1 | IRQ6 | AN106 |
| 121 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ POE10# | SSLC1-A | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DATA19-B*1 | IRQ5 | AN113 |
| 122 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | SSLC0-A | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B*1 | IRQ4 | AN112 |
| 123 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | RSPCKC-A | QIO3-B/SDHI_D3-B/MMC_D3-B | LCD_DATA21-B*1 | IRQ3 | AN111 |
| 124 | | PD2 | D2[A2/D2] | MTIOC4D/TIC2 | MISOC-A/CRX0 | QIO2-B/SDHI_D2-B/MMC_D2-B | LCD_DATA22-B*1 | IRQ2 | AN110 |
| 125 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | MOSIC-A/CTX0 | | LCD_DATA23-B*1 | IRQ1 | AN109 |
| 126 | | PD0 | D0[A0/D0] | POE4# | | | LCD_EXTCLK-B*1 | IRQ0 | AN108 |
| 127 | | P93 | A19 | POE0# | CTS7#/RTS7#/ SS7# | | | | AN117 |
| 128 | | P92 | A18 | POE4# | RXD7/SMISO7/ SSCL7 | | | | AN116 |
| 129 | | P91 | A17 | | SCK7 | | | | AN115 |
| 130 | VSS | | | | | | | | |
| 131 | | P90 | A16 | | TXD7/SMOSI7/ SSDA7 | | | | AN114 |
| 132 | VCC | | | | | | | | |
| 133 | | P47 | | | | | | IRQ15-DS | AN007 |
| 134 | | P46 | | | | | | IRQ14-DS | AN006 |
| 135 | | P45 | | | | | | IRQ13-DS | AN005 |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (7/7)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 136 | | P44 | | | | | | IRQ12-DS | AN004 |
| 137 | | P43 | | | | | | IRQ11-DS | AN003 |
| 138 | | P42 | | | | | | IRQ10-DS | AN002 |
| 139 | | P41 | | | | | | IRQ9-DS | AN001 |
| 140 | VREFL0 | | | | | | | | |
| 141 | | P40 | | | | | | IRQ8-DS | AN000 |
| 142 | VREFH0 | | | | | | | | |
| 143 | AVCC0 | | | | | | | | |
| 144 | | P07 | | | | | | IRQ15 | ADTRG0# |

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (1/5)**

| Pin Number 100-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| A1 | | P05 | | | | | | IRQ13 | DA1 |
| A2 | AVCC1 | | | | | | | | |
| A3 | | P07 | | | | | | IRQ15 | ADTRG0# |
| A4 | VREFL0 | | | | | | | | |
| A5 | | P43 | | | | | | IRQ11-DS | AN003 |
| A6 | | PD0 | D0[A0/D0] | POE4# | | | LCD_EXTCLK-B*1 | IRQ0 | AN108 |
| A7 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | SSLC0-A | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B*1 | IRQ4 | AN112 |
| A8 | | PE0 | D8[A8/D8]/ D0[A0/D0]*1 | MTIOC3D | SCK12/SSLB1-B | MMC_D4-B | LCD_DATA16-B*1 | | ANEX0 |
| A9 | | PE1 | D9[A9/D9]/ D1[A1/D1]*1 | MTIOC4C/ MTIOC3B/ PO18 | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | LCD_DATA15-B*1 | | ANEX1 |
| A10 | | PE2 | D10[A10/ D10]/D2[A2/ D2]*1 | MTIOC4A/ PO23/TIC3 | RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B | MMC_D6-B | LCD_DATA14-B*1 | IRQ7-DS | AN100 |
| B1 | EMLE | | | | | | | | |
| B2 | AVSS0 | | | | | | | | |
| B3 | AVCC0 | | | | | | | | |
| B4 | | P40 | | | | | | IRQ8-DS | AN000 |
| B5 | | P44 | | | | | | IRQ12-DS | AN004 |
| B6 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | MOSIC-A/CTX0 | | LCD_DATA23-B*1 | IRQ1 | AN109 |
| B7 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | RSPCKC-A | QIO3-B/SDHI_D3-B/MMC_D3-B | LCD_DATA21-B*1 | IRQ3 | AN111 |
| B8 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | SSLC2-A | QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B*1 | IRQ6 | AN106 |
| B9 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | SSLC3-A | QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B | LCD_DATA17-B*1 | IRQ7 | AN107 |
| B10 | | PE3 | D11[A11/ D11]/D3[A3/ D3]*1 | MTIOC4B/ PO26/TOC3/ POE8# | ET0_ERXD3/ CTS12#/ RTS12#/SS12# | MMC_D7-B | LCD_DATA13-B*1 | | AN101 |
| C1 | VCL | | | | | | | | |
| C2 | AVSS1 | | | | | | | | |
| C3 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0# | | | | |
| C4 | VREFH0 | | | | | | | | |
| C5 | | P42 | | | | | | IRQ10-DS | AN002 |
| C6 | | P47 | | | | | | IRQ15-DS | AN007 |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/5)**

| Pin Number 100-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| C7 | | PD2 | D2[A2/D2] | MTIOC4D/TIC2 | MISOC-A/CRX0 | QIO2-B/SDHI_D2-B/MMC_D2-B | LCD_DATA22-B*1 | IRQ2 | AN110 |
| C8 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ POE10# | SSLC1-A | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DATA19-B*1 | IRQ5 | AN113 |
| C9 | | PE5 | D13[A13/ D13]/D5[A5/ D5]*1 | MTIOC4C/ MTIOC2B | ET0_RX_CLK/ REF50CK0/ RSPCKB-B | | LCD_DATA11-B*1 | IRQ5 | AN103 |
| C10 | | PE4 | D12[A12/ D12]/D4[A4/ D4]*1 | MTIOC4D/ MTIOC1A/ PO28 | ET0_ERXD2/ SSLB0-B | | LCD_DATA12-B*1 | | AN102 |
| D1 | XCIN | | | | | | | | |
| D2 | XCOUT | | | | | | | | |
| D3 | MD/FINED | | | | | | | | |
| D4 | VBATT | | | | | | | | |
| D5 | | P45 | | | | | | IRQ13-DS | AN005 |
| D6 | | P46 | | | | | | IRQ14-DS | AN006 |
| D7 | | PE6 | D14[A14/ D14]/D6[A6/ D6]*1 | MTIOC6C/TIC1 | MOSIB-B | SDHI_CD/ MMC_CD-B | LCD_DATA10-B*1 | IRQ6 | AN104 |
| D8 | | PE7 | D15[A15/ D15]/D7[A7/ D7]*1 | MTIOC6A/ TOC1 | MISOB-B | SDHI_WP/ MMC_RES#-B | LCD_DATA9-B*1 | IRQ7 | AN105 |
| D9 | | PA1 | A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | ET0_WOL/ SCK5/SSLA2-B | | LCD_DATA7-B*1 | IRQ11 | |
| D10 | | PA0 | BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B | | LCD_DATA8-B*1 | | |
| E1 | XTAL | P37 | | | | | | | |
| E2 | VSS | | | | | | | | |
| E3 | RES# | | | | | | | | |
| E4 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | ET0_LINKSTA/ SCK6/SCK0 | | | IRQ4 | |
| E5 | | P41 | | | | | | IRQ9-DS | AN001 |
| E6 | | PA2 | A2 | MTIOC7A/ PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | LCD_DATA6-B*1 | | |
| E7 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B | | LCD_DATA2-B*1 | | |
| E8 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B | | LCD_DATA4-B*1 | IRQ5-DS | |
| E9 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | ET0_LINKSTA/ RSPCKA-B | | LCD_DATA3-B*1 | | |
| E10 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | ET0_MDIO/ RXD5/SMISO5/ SSCL5 | | LCD_DATA5-B*1 | IRQ6-DS | |
| F1 | EXTAL | P36 | | | | | | | |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/5)**

| Pin Number 100-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| F2 | VCC | | | | | | | | |
| F3 | UPSEL | P35 | | | | | | NMI | |
| F4 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN | | | IRQ2-DS | |
| F5 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/ SCL0[FM+] | | | IRQ2 | |
| F6 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | ET0_RX_ER/ RMII0_RX_ER/ SCK6 | SDSI_D3-B | LCD_TCON1-B*1 | | |
| F7 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | ET0_RX_CLK/ REF50CK0/ CTS6#/RTS6#/ SS6# | SDSI_D2-B | LCD_TCON2-B*1 | | |
| F8 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | ET0_ERXD1/ RMII0_RXD1/ RXD6/SMISO6/ SSCL6 | | LCD_DATA0-B*1 | IRQ12 | |
| F9 | | PA7 | A7 | TIOCB2/PO23 | ET0_WOL/ MISOA-B | | LCD_DATA1-B*1 | | |
| F10 | VSS | | | | | | | | |
| G1 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0 | | | IRQ3-DS | |
| G2 | TMS | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0-A | | | IRQ1-DS | |
| G3 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | | IRQ0-DS | |
| G4 | TCK | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | SCK1/RSPCKB-A | | | | |
| G5 | | P53*2 | BCLK | | | | | | |
| G6 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | | |
| G7 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11 | SDSI_CLK-B | LCD_CLK-B*1 | | |
| G8 | | PB4 | A12 | TIOCA4/PO28 | ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11# | SDSI_CMD-B | LCD_TCON0-B*1 | | |
| G9 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | ET0_ERXD0/ RMII0_RXD0/ TXD6/SMOSI6/ SSDA6 | | LCD_TCON3-B*1 | IRQ4-DS | |
| G10 | VCC | | | | | | | | |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/5)**

| Pin Number 100-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| H1 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A | | | | |
| H2 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3 | | | | ADTRG0# |
| H3 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | IRQ6 | ADTRG0# |
| H4 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS | | | IRQ5 | |
| H5 | | P55 | D0[A0/D0]*1/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | ET0_EXOUT/ CRX1 | | | IRQ10 | |
| H6 | | P54 | ALE/D1[A1/ D1]*1/ EDACK0 | MTIOC4B/ TMCI1 | ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1 | | | | |
| H7 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | | | IRQ14 | |
| H8 | | PC6 | D2[A2/D2]*1/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | | | IRQ13 | |
| H9 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11 | SDSI_D0-B | | | |
| H10 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11 | SDSI_D1-B | | | |
| J1 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | SCK3/ USB0_VBUSEN | | | | |
| J2 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN | | | IRQ9 | |
| J3 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | | | IRQ7 | ADTRG1# |
| J4 | | P13 | | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/ SDA0[FM+] | | | IRQ3 | ADTRG1# |
| J5 | VSS_USB | | | | | | | | |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (5/5)**

| Pin Number 100-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| J6 | VCC_USB | | | | | | | | |
| J7 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | | |
| J8 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | | | | |
| J9 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |
| J10 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | | IRQ12 | |
| K1 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0# | | | | |
| K2 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCURB | | | | |
| K3 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID | | | IRQ8 | |
| K4 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | IRQ4 | |
| K5 | | | | | USB0_DM | | | | |
| K6 | | | | | USB0_DP | | | | |
| K7 | | P51 | WR1#/ BC1#/ WAIT# | | SCK2/SSLB2-A | | | | |
| K8 | | PC5 | D3[A3/D3]*1/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A | | | | |
| K9 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | ET0_TX_ER/ TXD5/SMOSI5/ SSDA5 | | | | |
| K10 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | | | | |

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (1/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 1 | AVCC1 | | | | | | | | |
| 2 | EMLE | | | | | | | | |
| 3 | AVSS1 | | | | | | | | |
| 4 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0# | | | | |
| 5 | VCL | | | | | | | | |
| 6 | VBATT | | | | | | | | |
| 7 | MD/FINED | | | | | | | | |
| 8 | XCIN | | | | | | | | |
| 9 | XCOUT | | | | | | | | |
| 10 | RES# | | | | | | | | |
| 11 | XTAL | P37 | | | | | | | |
| 12 | VSS | | | | | | | | |
| 13 | EXTAL | P36 | | | | | | | |
| 14 | VCC | | | | | | | | |
| 15 | UPSEL | P35 | | | | | | NMI | |
| 16 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | ET0_LINKSTA/ SCK6/SCK0 | | | IRQ4 | |
| 17 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0 | | | IRQ3-DS | |
| 18 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN | | | IRQ2-DS | |
| 19 | TMS | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0-A | | | IRQ1-DS | |
| 20 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | | IRQ0-DS | |
| 21 | TCK | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | SCK1/RSPCKB-A | | | | |
| 22 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A | | | | |
| 23 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3 | | | | ADTRG0# |
| 24 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | SCK3/ USB0_VBUSEN | | | | |
| 25 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0# | | | | |

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (2/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 26 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCURB | | | | |
| 27 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN | | | IRQ9 | |
| 28 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID | | | IRQ8 | |
| 29 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | | | IRQ7 | ADTRG1# |
| 30 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | IRQ6 | ADTRG0# |
| 31 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS | | | IRQ5 | |
| 32 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | IRQ4 | |
| 33 | | P13 | | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/ SDA0[FM+] | | | IRQ3 | ADTRG1# |
| 34 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/ SCL0[FM+] | | | IRQ2 | |
| 35 | VCC_USB | | | | | | | | |
| 36 | | | | | USB0_DM | | | | |
| 37 | | | | | USB0_DP | | | | |
| 38 | VSS_USB | | | | | | | | |
| 39 | | P55 | D0[A0/D0]*1/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | ET0_EXOUT/ CRX1 | | | IRQ10 | |
| 40 | | P54 | ALE/D1[A1/ D1]*1/ EDACK0 | MTIOC4B/ TMCI1 | ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1 | | | | |
| 41 | | P53*2 | BCLK | | | | | | |
| 42 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | | |
| 43 | | P51 | WR1#/ BC1#/ WAIT# | | SCK2/SSLB2-A | | | | |
| 44 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | | |

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 45 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | | | IRQ14 | |
| 46 | | PC6 | D2[A2/D2]*1/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | | | IRQ13 | |
| 47 | | PC5 | D3[A3/D3]*1/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A | | | | |
| 48 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | | | | |
| 49 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | ET0_TX_ER/ TXD5/SMOSI5/ SSDA5 | | | | |
| 50 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | | | | |
| 51 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | | IRQ12 | |
| 52 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |
| 53 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11 | SDSI_D1-B | | | |
| 54 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11 | SDSI_D0-B | | | |
| 55 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11 | SDSI_CLK-B | LCD_CLK-B*1 | | |
| 56 | | PB4 | A12 | TIOCA4/PO28 | ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11# | SDSI_CMD-B | LCD_TCON0-B*1 | | |
| 57 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | ET0_RX_ER/ RMII0_RX_ER/ SCK6 | SDSI_D3-B | LCD_TCON1-B*1 | | |
| 58 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | ET0_RX_CLK/ REF50CK0/ CTS6#/RTS6#/ SS6# | SDSI_D2-B | LCD_TCON2-B*1 | | |
| 59 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | ET0_ERXD0/ RMII0_RXD0/ TXD6/SMOSI6/ SSDA6 | | LCD_TCON3-B*1 | IRQ4-DS | |

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (4/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 60 | VCC | | | | | | | | |
| 61 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | ET0_ERXD1/ RMII0_RXD1/ RXD6/SMISO6/ SSCL6 | | LCD_DATA0-B*1 | IRQ12 | |
| 62 | VSS | | | | | | | | |
| 63 | | PA7 | A7 | TIOCB2/PO23 | ET0_WOL/ MISOA-B | | LCD_DATA1-B*1 | | |
| 64 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B | | LCD_DATA2-B*1 | | |
| 65 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | ET0_LINKSTA/ RSPCKA-B | | LCD_DATA3-B*1 | | |
| 66 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B | | LCD_DATA4-B*1 | IRQ5-DS | |
| 67 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | ET0_MDIO/ RXD5/SMISO5/ SSCL5 | | LCD_DATA5-B*1 | IRQ6-DS | |
| 68 | | PA2 | A2 | MTIOC7A/ PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | LCD_DATA6-B*1 | | |
| 69 | | PA1 | A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | ET0_WOL/ SCK5/SSLA2-B | | LCD_DATA7-B*1 | IRQ11 | |
| 70 | | PA0 | BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B | | LCD_DATA8-B*1 | | |
| 71 | | PE7 | D15[A15/ D15]/D7[A7/ D7]*1 | MTIOC6A/ TOC1 | MISOB-B | SDHI_WP/ MMC_RES#-B | LCD_DATA9-B*1 | IRQ7 | AN105 |
| 72 | | PE6 | D14[A14/ D14]/D6[A6/ D6]*1 | MTIOC6C/TIC1 | MOSIB-B | SDHI_CD/ MMC_CD-B | LCD_DATA10-B*1 | IRQ6 | AN104 |
| 73 | | PE5 | D13[A13/ D13]/D5[A5/ D5]*1 | MTIOC4C/ MTIOC2B | ET0_RX_CLK/ REF50CK0/ RSPCKB-B | | LCD_DATA11-B*1 | IRQ5 | AN103 |
| 74 | | PE4 | D12[A12/ D12]/D4[A4/ D4]*1 | MTIOC4D/ MTIOC1A/ PO28 | ET0_ERXD2/ SSLB0-B | | LCD_DATA12-B*1 | | AN102 |
| 75 | | PE3 | D11[A11/ D11]/D3[A3/ D3]*1 | MTIOC4B/ PO26/TOC3/ POE8# | ET0_ERXD3/ CTS12#/ RTS12#/SS12# | MMC_D7-B | LCD_DATA13-B*1 | | AN101 |
| 76 | | PE2 | D10[A10/ D10]/D2[A2/ D2]*1 | MTIOC4A/ PO23/TIC3 | RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B | MMC_D6-B | LCD_DATA14-B*1 | IRQ7-DS | AN100 |
| 77 | | PE1 | D9[A9/D9]/ D1[A1/D1]*1 | MTIOC4C/ MTIOC3B/ PO18 | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | LCD_DATA15-B*1 | | ANEX1 |
| 78 | | PE0 | D8[A8/D8]/ D0[A0/D0]*1 | MTIOC3D | SCK12/SSLB1-B | MMC_D4-B | LCD_DATA16-B*1 | | ANEX0 |

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (5/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 79 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | SSLC3-A | QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B | LCD_DATA17-B*1 | IRQ7 | AN107 |
| 80 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | SSLC2-A | QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B*1 | IRQ6 | AN106 |
| 81 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ POE10# | SSLC1-A | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DATA19-B*1 | IRQ5 | AN113 |
| 82 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | SSLC0-A | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B*1 | IRQ4 | AN112 |
| 83 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | RSPCKC-A | QIO3-B/SDHI_D3-B/MMC_D3-B | LCD_DATA21-B*1 | IRQ3 | AN111 |
| 84 | | PD2 | D2[A2/D2] | MTIOC4D/TIC2 | MISOC-A/CRX0 | QIO2-B/SDHI_D2-B/MMC_D2-B | LCD_DATA22-B*1 | IRQ2 | AN110 |
| 85 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | MOSIC-A/CTX0 | | LCD_DATA23-B*1 | IRQ1 | AN109 |
| 86 | | PD0 | D0[A0/D0] | POE4# | | | LCD_EXTCLK-B*1 | IRQ0 | AN108 |
| 87 | | P47 | | | | | | IRQ15-DS | AN007 |
| 88 | | P46 | | | | | | IRQ14-DS | AN006 |
| 89 | | P45 | | | | | | IRQ13-DS | AN005 |
| 90 | | P44 | | | | | | IRQ12-DS | AN004 |
| 91 | | P43 | | | | | | IRQ11-DS | AN003 |
| 92 | | P42 | | | | | | IRQ10-DS | AN002 |
| 93 | | P41 | | | | | | IRQ9-DS | AN001 |
| 94 | VREFL0 | | | | | | | | |
| 95 | | P40 | | | | | | IRQ8-DS | AN000 |
| 96 | VREFH0 | | | | | | | | |
| 97 | AVCC0 | | | | | | | | |
| 98 | | P07 | | | | | | IRQ15 | ADTRG0# |
| 99 | AVSS0 | | | | | | | | |
| 100 | | P05 | | | | | | IRQ13 | DA1 |

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Table 1.11 List of Pin and Pin Functions (64-Pin TFBGA) (1/2)**

| Pin Number 64-Pin TFBGA | Power Supply Clock System Control | I/O Port | Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC) | Communication (SCI, RSPI, RIIC, USB) | Memory Interface (QSPI, SDHI) | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|
| A1 | AVCC1 | | | | | | |
| A2 | AVSS0 | | | | | | |
| A3 | VREFH0 | | | | | | |
| A4 | VREFL0 | | | | | | |
| A5 | | PD2 | MTIOC4D/TIC2 | | QIO2-B/SDHI_D2-B | IRQ2 | AN110 |
| A6 | | PD7 | MTIC5U/POE0# | | QMI-B/QIO1-B/ SDHI_D1-B | IRQ7 | AN107 |
| A7 | | PE0 | MTIOC3D | SCK12 | | | ANEX0 |
| A8 | | PE2 | MTIOC4A/TIC3 | RXD12/SSCL12/ RXDX12 | | IRQ7-DS | |
| B1 | EMLE | | | | | | |
| B2 | AVSS1 | | | | | | |
| B3 | AVCC0 | | | | | | |
| B4 | | P42 | | | | IRQ10-DS | AN002 |
| B5 | | PD3 | MTIOC8D/TOC2/ POE8# | | QIO3-B/SDHI_D3-B | IRQ3 | AN111 |
| B6 | | PD6 | MTIC5V/MTIOC8A/ POE4# | | QMO-B/QIO0-B/ SDHI_D0-B | IRQ6 | AN106 |
| B7 | | PE1 | MTIOC4C/MTIOC3B | TXD12/SSDA12/ TXDX12/SIOX12 | | | ANEX1 |
| B8 | | PE6 | MTIOC6C/TIC1 | | SDHI_CD | IRQ6 | |
| C1 | VCL | | | | | | |
| C2 | VBATT | | | | | | |
| C3 | MD/FINED | | | | | | |
| C4 | | P41 | | | | IRQ9-DS | AN001 |
| C5 | | PD4 | MTIOC8B/POE11# | | QSSL-B/SDHI_CMD-B | IRQ4 | AN112 |
| C6 | | PD5 | MTIC5W/MTIOC8C/ POE10# | | QSPCLK-B/ SDHI_CLK-B | IRQ5 | AN113 |
| C7 | | PA1 | MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0 | SCK5 | | IRQ11 | |
| C8 | | PE7 | MTIOC6A/TOC1 | | SDHI_WP | IRQ7 | |
| D1 | XCIN | | | | | | |
| D2 | XCOUT | | | | | | |
| D3 | RES# | | | | | | |
| D4 | | P40 | | | | IRQ8-DS | AN000 |
| D5 | | P43 | | | | IRQ11-DS | AN003 |
| D6 | | PA6 | MTIC5V/MTCLKB/ TIOCA2/TMCI3/ POE10# | CTS5#/RTS5#/SS5# | | | |
| D7 | | PA2 | MTIOC7A | RXD5/SMISO5/ SSCL5 | | | |
| D8 | | PA4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0 | TXD5/SMOSI5/ SSDA5 | | IRQ5-DS | |
| E1 | XTAL | P37 | | | | | |
| E2 | VSS | | | | | | |
| E3 | TRST# | P34 | MTIOC0A/TMCI3/ POE10# | | | IRQ4 | |
| E4 | | P13 | MTIOC0B/TIOCA5/ TMO3 | TXD2/SSDA2/ SDA0[FM+] | | IRQ3 | ADTRG1# |
| E5 | BSCANP | | | | | | |

**Table 1.11 List of Pin and Pin Functions (64-Pin TFBGA) (2/2)**

| Pin Number 64-Pin TFBGA | Power Supply Clock System Control | I/O Port | Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC) | Communication (SCI, RSPI, RIIC, USB) | Memory Interface (QSPI, SDHI) | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|
| E6 | | PA7 | TIOCB2 | | | | |
| E7 | VCC | | | | | | |
| E8 | VSS | | | | | | |
| F1 | EXTAL | P36 | | | | | |
| F2 | VCC | | | | | | |
| F3 | UPSEL | P35 | | | | NMI | |
| F4 | | P12 | TMCI1 | RXD2/SSCL2/ SCL0[FM+] | | IRQ2 | |
| F5 | | P53 | | | | | |
| F6 | | PB7 | MTIOC3B/TIOCB5 | TXD9/SSDA9/ SSDA11/TXD11 | | | |
| F7 | | PB6 | MTIOC3D/TIOCA5 | RXD9/SSCL9/ SSCL11/RXD11 | | | |
| F8 | | PB5 | MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/ POE4# | SCK9/SCK11 | | | |
| G1 | TCK | P27 | MTIOC2B/TMCI3 | SCK1/RSPCKB-A | | | |
| G2 | TMS | P31 | MTIOC4D/TMCI2/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0-A | | IRQ1-DS | |
| G3 | TDI | P30 | MTIOC4B/TMRI3/ RTCIC0/POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | IRQ0-DS | |
| G4 | VCC_USB | | | | | | |
| G5 | VSS_USB | | | | | | |
| G6 | UB | PC7 | MTIOC3A/MTCLKB/ TMO2/TOC0/ CACREF | TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ MISOA-A | | IRQ14 | |
| G7 | | PC5 | MTIOC3B/MTCLKD/ TMRI2 | SCK8/SCK10/ RSPCKA-A | | | |
| G8 | | PC0 | MTIOC3C/TCLKC | SSLA1-A | | IRQ14 | |
| H1 | TDO | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/MOSIB-A | | | |
| H2 | | P17 | MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/ TCLKD/TMO1/ POE8# | SCK1/TXD3/SSDA3/ SDA2-DS | | IRQ7 | ADTRG1# |
| H3 | | P16 | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SSCL3/SCL2-DS/ USB0_VBUS | | IRQ6 | ADTRG0# |
| H4 | | | | USB0_DM | | | |
| H5 | | | | USB0_DP | | | |
| H6 | | PC6 | MTIOC3C/MTCLKA/ TMCI2/TIC0 | RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ MOSIA-A | | IRQ13 | |
| H7 | | PC4 | MTIOC3D/MTCLKC/ TMCI1/POE0# | CTS8#/RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | | | |
| H8 | | PC1 | MTIOC3A/TCLKD | SSLA2-A | | IRQ12 | |

**Table 1.12 List of Pin and Pin Functions (64-Pin LFQFP) (1/2)**

| Pin Number 64-Pin LFQFP | Power Supply Clock System Control | I/O Port | Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC) | Communication (SCI, RSPI, RIIC, USB) | Memory Interface (QSPI, SDHI) | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|
| 1 | AVCC1 | | | | | | |
| 2 | EMLE | | | | | | |
| 3 | AVSS1 | | | | | | |
| 4 | VCL | | | | | | |
| 5 | VBATT | | | | | | |
| 6 | MD/FINED | | | | | | |
| 7 | XCIN | | | | | | |
| 8 | XCOUT | | | | | | |
| 9 | RES# | | | | | | |
| 10 | XTAL | P37 | | | | | |
| 11 | VSS | | | | | | |
| 12 | EXTAL | P36 | | | | | |
| 13 | VCC | | | | | | |
| 14 | UPSEL | P35 | | | | NMI | |
| 15 | TRST# | P34 | MTIOC0A/TMCI3/ POE10# | | | IRQ4 | |
| 16 | TDI | P30 | MTIOC4B/TMRI3/ RTCIC0/POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | IRQ0-DS | |
| 17 | TMS | P31 | MTIOC4D/TMCI2/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0-A | | IRQ1-DS | |
| 18 | TDO | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/MOSIB-A | | | |
| 19 | TCK | P27 | MTIOC2B/TMCI3 | SCK1/RSPCKB-A | | | |
| 20 | | P17 | MTIOC3A/MTIOC3B/ MTIOC4B/TIOCB0/ TCLKD/TMO1/ POE8# | SCK1/TXD3/SSDA3/ SDA2-DS | | IRQ7 | ADTRG1# |
| 21 | | P16 | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SSCL3/SCL2-DS/ USB0_VBUS | | IRQ6 | ADTRG0# |
| 22 | | P13 | MTIOC0B/TIOCA5/ TMO3 | TXD2/SSDA2/ SDA0[FM+] | | IRQ3 | ADTRG1# |
| 23 | | P12 | TMCI1 | RXD2/SSCL2/ SCL0[FM+] | | IRQ2 | |
| 24 | VCC_USB | | | | | | |
| 25 | | | | USB0_DM | | | |
| 26 | | | | USB0_DP | | | |
| 27 | VSS_USB | | | | | | |
| 28 | | P53 | | | | | |
| 29 | UB | PC7 | MTIOC3A/MTCLKB/ TMO2/TOC0/ CACREF | TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ MISOA-A | | IRQ14 | |
| 30 | | PC6 | MTIOC3C/MTCLKA/ TMCI2/TIC0 | RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ MOSIA-A | | IRQ13 | |
| 31 | | PC5 | MTIOC3B/MTCLKD/ TMRI2 | SCK8/SCK10/ RSPCKA-A | | | |
| 32 | | PC4 | MTIOC3D/MTCLKC/ TMCI1/POE0# | CTS8#/RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | | | |

**Table 1.12 List of Pin and Pin Functions (64-Pin LFQFP) (2/2)**

| Pin Number 64-Pin LFQFP | Power Supply Clock System Control | I/O Port | Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC) | Communication (SCI, RSPI, RIIC, USB) | Memory Interface (QSPI, SDHI) | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|
| 33 | | PC1 | MTIOC3A/TCLKD | SSLA2-A | | IRQ12 | |
| 34 | | PC0 | MTIOC3C/TCLKC | SSLA1-A | | IRQ14 | |
| 35 | | PB7 | MTIOC3B/TIOCB5 | TXD9/SSDA9/ SSDA11/TXD11 | | | |
| 36 | | PB6 | MTIOC3D/TIOCA5 | RXD9/SSCL9/ SSCL11/RXD11 | | | |
| 37 | | PB5 | MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/ POE4# | SCK9/SCK11 | | | |
| 38 | VCC | | | | | | |
| 39 | VSS | | | | | | |
| 40 | | PA7 | TIOCB2 | | | | |
| 41 | | PA6 | MTIC5V/MTCLKB/ TIOCA2/TMCI3/ POE10# | CTS5#/RTS5#/SS5# | | | |
| 42 | | PA4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0 | TXD5/SMOSI5/ SSDA5 | | IRQ5-DS | |
| 43 | | PA2 | MTIOC7A | RXD5/SMISO5/ SSCL5 | | | |
| 44 | | PA1 | MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0 | SCK5 | | IRQ11 | |
| 45 | | PE7 | MTIOC6A/TOC1 | | SDHI_WP | IRQ7 | |
| 46 | | PE6 | MTIOC6C/TIC1 | | SDHI_CD | IRQ6 | |
| 47 | | PE2 | MTIOC4A/TIC3 | RXD12/SSCL12/ RXDX12 | | IRQ7-DS | |
| 48 | | PE1 | MTIOC4C/MTIOC3B | TXD12/SSDA12/ TXDX12/SIOX12 | | | ANEX1 |
| 49 | | PE0 | MTIOC3D | SCK12 | | | ANEX0 |
| 50 | | PD7 | MTIC5U/POE0# | | QMI-B/QIO1-B/ SDHI_D1-B | IRQ7 | AN107 |
| 51 | | PD6 | MTIC5V/MTIOC8A/ POE4# | | QMO-B/QIO0-B/ SDHI_D0-B | IRQ6 | AN106 |
| 52 | | PD5 | MTIC5W/MTIOC8C/ POE10# | | QSPCLK-B/ SDHI_CLK-B | IRQ5 | AN113 |
| 53 | | PD4 | MTIOC8B/POE11# | | QSSL-B/SDHI_CMD-B | IRQ4 | AN112 |
| 54 | | PD3 | MTIOC8D/TOC2/ POE8# | | QIO3-B/SDHI_D3-B | IRQ3 | AN111 |
| 55 | | PD2 | MTIOC4D/TIC2 | | QIO2-B/SDHI_D2-B | IRQ2 | AN110 |
| 56 | | P43 | | | | IRQ11-DS | AN003 |
| 57 | | P42 | | | | IRQ10-DS | AN002 |
| 58 | | P41 | | | | IRQ9-DS | AN001 |
| 59 | VREFL0 | | | | | | |
| 60 | | P40 | | | | IRQ8-DS | AN000 |
| 61 | VREFH0 | | | | | | |
| 62 | AVCC0 | | | | | | |
| 63 | AVSS0 | | | | | | |
| 64 | | P05 | | | | IRQ13 | DA1 |

# 2. CPU

Figure 2.1 shows register set of the CPU.

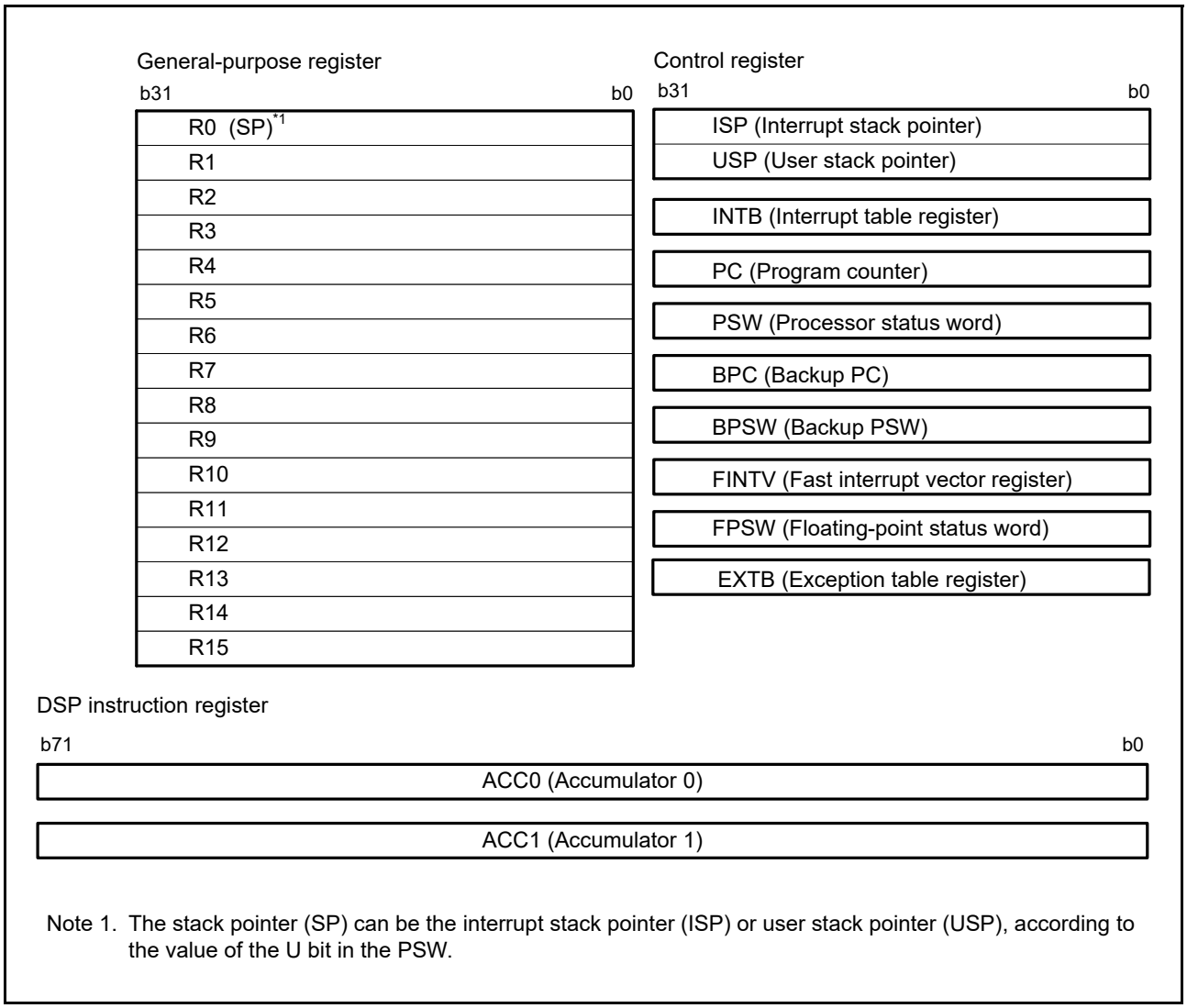



**Figure 2.1 Register Set of the CPU**

## 2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.
R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

## 2.2 Control Registers

### (1) Interrupt Stack Pointer (ISP) / User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

### (2) Exception Table Register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.

### (3) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.

### (4) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

### (5) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

### (6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

### (7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

### (8) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

### (9) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

## 2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.

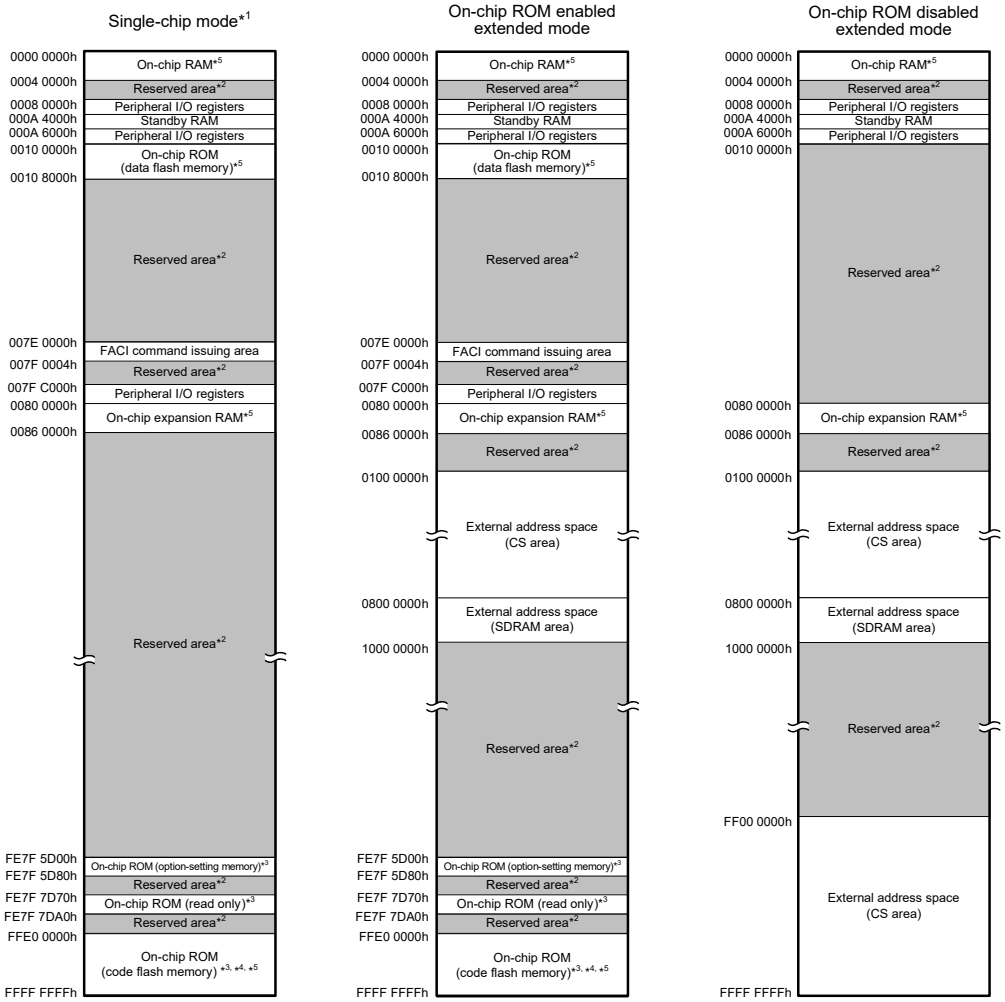
Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

# 3. Address Space

## 3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



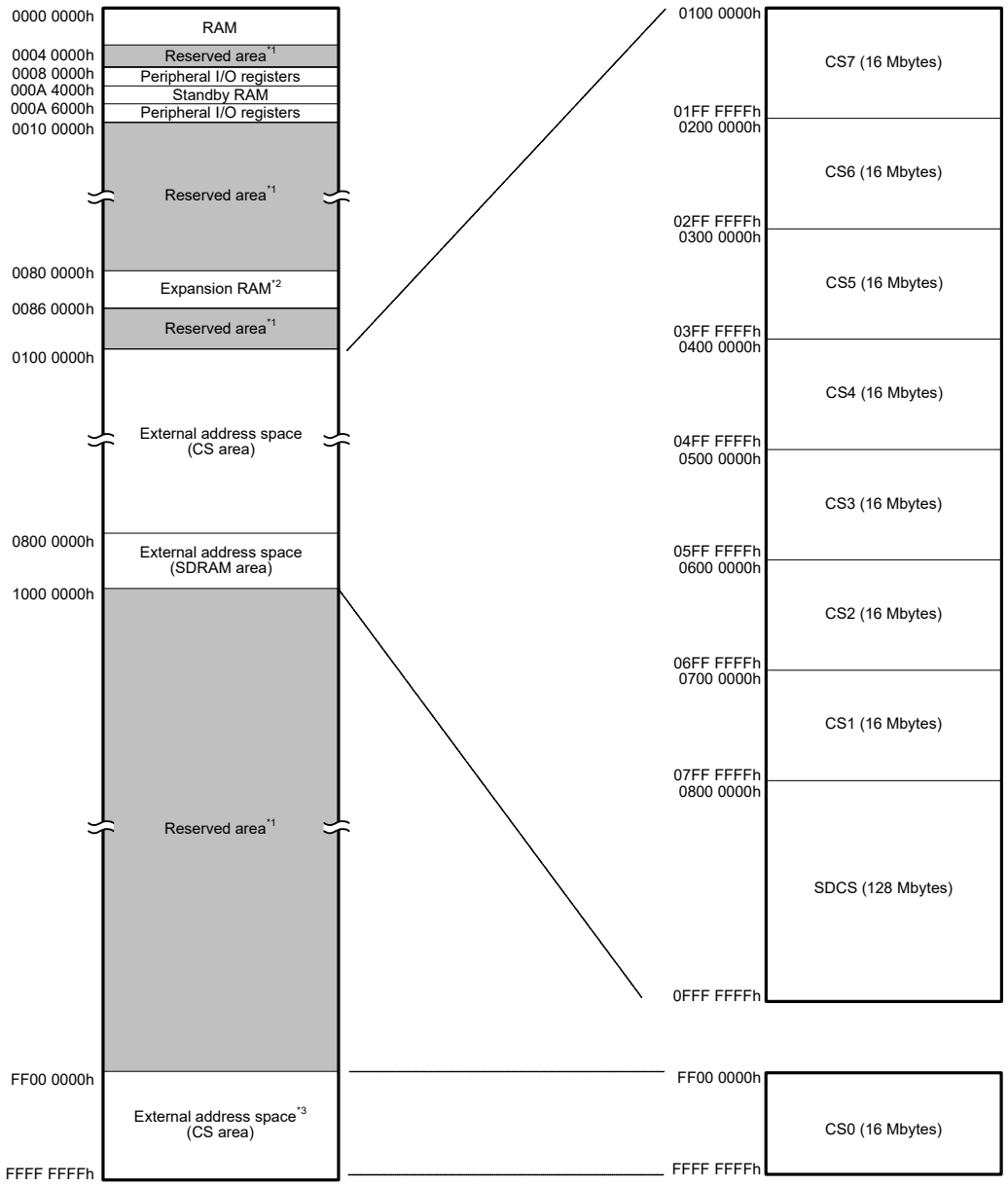

Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. Reserved areas should not be accessed.
Note 3. The access cycle is 1 cycle, 2 cycles, and 3 cycles while the ROMWT[1:0] bits are 00b, 01b, and 10b respectively.
Note 4. The on-chip ROM (code flash memory) can be used in linear mode, where the user area forms a single area, or in dual mode, where the user area is divided into two banks. For details, refer to section 59.2, Structure of Memory in section 59, Flash Memory in the User's Manual: Hardware.
Note 5. The capacities of the code flash memory, data flash memory, and RAM differ depending on the products.

| Code Flash Memory | | | Data Flash Memory | | RAM | |
|---|---|---|---|---|---|---|
| Capacity | Address | | Capacity | Address | Capacity | Address |
| | Linear mode | Dual mode (BANKSEL.BANKSWP[2:0] = 111b) | | | | |
| 2 Mbytes | FFE0 0000h to FFFF FFFFh | bank 1: FFE0 0000h to FFEF FFFFh | 32 Kbytes | 0010 0000h to 0010 7FFFh | 640 Kbytes | 0000 0000h to 0003 FFFFh |
| | | bank 0: FFF0 0000h to FFFF FFFFh | | | | 0080 0000h to 0085 FFFFh |
| 1.5 Mbytes | FFE8 0000h to FFFF FFFFh | bank 1: FFE4 0000h to FFEF FFFFh | 32 Kbytes | 0010 0000h to 0010 7FFFh | 640 Kbytes | 0000 0000h to 0003 FFFFh |
| | | bank 0: FFF4 0000h to FFFF FFFFh | | | | 0080 0000h to 0085 FFFFh |
| 1 Mbyte | FFF0 0000h to FFFF FFFFh | — | — | — | 256 Kbytes | 0000 0000h to 0003 FFFFh |
| 768 Kbytes | FFF4 0000h to FFFF FFFFh | — | — | — | 256 Kbytes | 0000 0000h to 0003 FFFFh |
| 512 Kbytes | FFF8 0000h to FFFF FFFFh | — | — | — | 256 Kbytes | 0000 0000h to 0003 FFFFh |

**Figure 3.1 Memory Map in Each Operating Mode**

## 3.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7) and SDRAM area (SDCS). The CS areas are divided into up to eight areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.
Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM area (SDCS) in on-chip ROM disabled extended mode.




Note 1. Reserved areas should not be accessed.
Note 2. This area is only included in products with at least 1.5 Mbytes of code flash memory.
Note 3. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure on this section, Memory Map in Each Operating Mode.

**Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)**

# 4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

## (1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

## (2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

**[Examples of cases requiring special care]**

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

### (3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

### (4) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

### (5) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

## 4.1 I/O Register Addresses (Address Order)

**Table 4.1 List of I/O Registers (Address Order) (1 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 0000h | SYSTEM | Mode Monitor Register | MDMONR | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 0006h | SYSTEM | System Control Register 0 | SYSCR0 | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 0008h | SYSTEM | System Control Register 1 | SYSCR1 | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 000Ch | SYSTEM | Standby Control Register | SBYCR | 16 | 16 | 3 ICLK | | Low Power Consumption |
| 0008 0010h | SYSTEM | Module Stop Control Register A | MSTPCRA | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0014h | SYSTEM | Module Stop Control Register B | MSTPCRB | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0018h | SYSTEM | Module Stop Control Register C | MSTPCRC | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 001Ch | SYSTEM | Module Stop Control Register D | MSTPCRD | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0020h | SYSTEM | System Clock Control Register | SCKCR | 32 | 32 | 3 ICLK | | Clock Generation Circuit |
| 0008 0024h | SYSTEM | System Clock Control Register 2 | SCKCR2 | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 0026h | SYSTEM | System Clock Control Register 3 | SCKCR3 | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 0028h | SYSTEM | PLL Control Register | PLLCR | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 002Ah | SYSTEM | PLL Control Register 2 | PLLCR2 | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0030h | SYSTEM | External Bus Clock Control Register | BCKCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0032h | SYSTEM | Main Clock Oscillator Control Register | MOSCCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0033h | SYSTEM | Sub-Clock Oscillator Control Register | SOSCCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0034h | SYSTEM | Low-Speed On-Chip Oscillator Control Register | LOCOCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0035h | SYSTEM | IWDT-Dedicated On-Chip Oscillator Control Register | ILOCOCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0036h | SYSTEM | High-Speed On-Chip Oscillator Control Register | HOCOCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0037h | SYSTEM | High-Speed On-Chip Oscillator Control Register 2 | HOCOCR2 | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 003Ch | SYSTEM | Oscillation Stabilization Flag Register | OSCOVFSR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |

**Table 4.1 List of I/O Registers (Address Order) (2 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 0040h | SYSTEM | Oscillation Stop Detection Control Register | OSTDCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0041h | SYSTEM | Oscillation Stop Detection Status Register | OSTDSR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 00A0h | SYSTEM | Operating Power Control Register | OPCCR | 8 | 8 | 3 ICLK | | Low Power Consumption |
| 0008 00A1h | SYSTEM | Sleep Mode Return Clock Source Switching Register | RSTCKCR | 8 | 8 | 3 ICLK | | Low Power Consumption |
| 0008 00A2h | SYSTEM | Main Clock Oscillator Wait Control Register | MOSCWTCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 00A3h | SYSTEM | Sub-Clock Oscillator Wait Control Register | SOSCWTCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 00C0h | SYSTEM | Reset Status Register 2 | RSTSR2 | 8 | 8 | 3 ICLK | | Resets |
| 0008 00C2h | SYSTEM | Software Reset Register | SWRR | 16 | 16 | 3 ICLK | | Resets |
| 0008 00E0h | SYSTEM | Voltage Monitoring 1 Circuit Control Register 1 | LVD1CR1 | 8 | 8 | 3 ICLK | | LVDA |
| 0008 00E1h | SYSTEM | Voltage Monitoring 1 Circuit Status Register | LVD1SR | 8 | 8 | 3 ICLK | | LVDA |
| 0008 00E2h | SYSTEM | Voltage Monitoring 2 Circuit Control Register 1 | LVD2CR1 | 8 | 8 | 3 ICLK | | LVDA |
| 0008 00E3h | SYSTEM | Voltage Monitoring 2 Circuit Status Register | LVD2SR | 8 | 8 | 3 ICLK | | LVDA |
| 0008 03FEh | SYSTEM | Protect Register | PRCR | 16 | 16 | 3 ICLK | | Register Write Protection Function |
| 0008 1000h | FLASH | ROM Cache Enable Register | ROMCE | 16 | 16 | 2 ICLK | | Flash |
| 0008 1004h | FLASH | ROM Cache Invalidate Register | ROMCIV | 16 | 16 | 2 ICLK | | Flash |
| 0008 101Ch | SYSTEM | ROM Wait Cycle Setting Register | ROMWT | 8 | 8 | 2 ICLK | | Clock Generation Circuit |
| 0008 1200h | RAM | RAM Operating Mode Control Register | RAMMODE | 8 | 8 | 2 ICLK | | RAM |
| 0008 1201h | RAM | RAM Error Status Register | RAMSTS | 8 | 8 | 2 ICLK | | RAM |
| 0008 1204h | RAM | RAM Protection Register | RAMPRCR | 8 | 8 | 2 ICLK | | RAM |
| 0008 1208h | RAM | RAM Error Address Capture Register | RAMECAD | 32 | 32 | 2 ICLK | | RAM |
| 0008 1240h | RAM | Expansion RAM Operating Mode Control Register | EXRAMMODE | 8 | 8 | 2 ICLK | | RAM |
| 0008 1241h | RAM | Expansion RAM Error Status Register | EXRAMSTS | 8 | 8 | 2 ICLK | | RAM |
| 0008 1244h | RAM | Expansion RAM Protection Register | EXRAMPRCR | 8 | 8 | 2 ICLK | | RAM |
| 0008 1248h | RAM | Expansion RAM Error Address Capture Register | EXRAMECAD | 32 | 32 | 2 ICLK | | RAM |
| 0008 1300h | BSC | Bus Error Status Clear Register | BERCLR | 8 | 8 | 2 ICLK | | Buses |
| 0008 1304h | BSC | Bus Error Monitoring Enable Register | BEREN | 8 | 8 | 2 ICLK | | Buses |
| 0008 1308h | BSC | Bus Error Status Register 1 | BERSR1 | 8 | 8 | 2 ICLK | | Buses |
| 0008 130Ah | BSC | Bus Error Status Register 2 | BERSR2 | 16 | 16 | 2 ICLK | | Buses |
| 0008 1310h | BSC | Bus Priority Control Register | BUSPRI | 16 | 16 | 2 ICLK | | Buses |
| 0008 2000h | DMAC0 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2004h | DMAC0 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2008h | DMAC0 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 200Ch | DMAC0 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2010h | DMAC0 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2013h | DMAC0 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | DMACAa |

**Table 4.1 List of I/O Registers (Address Order) (3 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 2014h | DMAC0 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2018h | DMAC0 | DMA Offset Register | DMOFR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 201Ch | DMAC0 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 201Dh | DMAC0 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 201Eh | DMAC0 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 201Fh | DMAC0 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2040h | DMAC1 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2044h | DMAC1 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2048h | DMAC1 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 204Ch | DMAC1 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2050h | DMAC1 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2053h | DMAC1 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2054h | DMAC1 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 205Ch | DMAC1 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 205Dh | DMAC1 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 205Eh | DMAC1 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 205Fh | DMAC1 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2080h | DMAC2 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2084h | DMAC2 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2088h | DMAC2 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 208Ch | DMAC2 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2090h | DMAC2 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2093h | DMAC2 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2094h | DMAC2 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 209Ch | DMAC2 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 209Dh | DMAC2 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 209Eh | DMAC2 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 209Fh | DMAC2 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 20C0h | DMAC3 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 20C4h | DMAC3 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 20C8h | DMAC3 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 20CCh | DMAC3 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 20D0h | DMAC3 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 20D3h | DMAC3 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 20D4h | DMAC3 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 20DCh | DMAC3 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 20DDh | DMAC3 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 20DEh | DMAC3 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 20DFh | DMAC3 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2100h | DMAC4 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2104h | DMAC4 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2108h | DMAC4 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 210Ch | DMAC4 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2110h | DMAC4 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2113h | DMAC4 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2114h | DMAC4 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 211Ch | DMAC4 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 211Dh | DMAC4 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 211Eh | DMAC4 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 211Fh | DMAC4 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACAa |

**Table 4.1 List of I/O Registers (Address Order) (4 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 2140h | DMAC5 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2144h | DMAC5 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2148h | DMAC5 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 214Ch | DMAC5 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2150h | DMAC5 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2153h | DMAC5 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2154h | DMAC5 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 215Ch | DMAC5 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 215Dh | DMAC5 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 215Eh | DMAC5 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 215Fh | DMAC5 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2180h | DMAC6 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2184h | DMAC6 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 2188h | DMAC6 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 218Ch | DMAC6 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2190h | DMAC6 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 2193h | DMAC6 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2194h | DMAC6 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 219Ch | DMAC6 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 219Dh | DMAC6 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 219Eh | DMAC6 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 219Fh | DMAC6 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 21C0h | DMAC7 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 21C4h | DMAC7 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 21C8h | DMAC7 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | DMACAa |
| 0008 21CCh | DMAC7 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 21D0h | DMAC7 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 21D3h | DMAC7 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 21D4h | DMAC7 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | DMACAa |
| 0008 21DCh | DMAC7 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 21DDh | DMAC7 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 21DEh | DMAC7 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 21DFh | DMAC7 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2200h | DMAC | DMAC Module Start Register | DMAST | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2204h | DMAC | DMAC74 Interrupt Status Monitor Register | DMIST | 8 | 8 | 2 ICLK | | DMACAa |
| 0008 2400h | DTC | DTC Control Register | DTCCR | 8 | 8 | 2 ICLK | | DTCb |
| 0008 2404h | DTC | DTC Vector Base Register | DTCVBR | 32 | 32 | 2 ICLK | | DTCb |
| 0008 2408h | DTC | DTC Address Mode Register | DTCADMOD | 8 | 8 | 2 ICLK | | DTCb |
| 0008 240Ch | DTC | DTC Module Start Register | DTCST | 8 | 8 | 2 ICLK | | DTCb |
| 0008 240Eh | DTC | DTC Status Register | DTCSTS | 16 | 16 | 2 ICLK | | DTCb |
| 0008 2410h | DTC | DTC Index Table Base Register | DTCIBR | 32 | 32 | 2 ICLK | | DTCb |
| 0008 2414h | DTC | DTC Operation Register | DTCOR | 8 | 8 | 2 ICLK | | DTCb |
| 0008 2416h | DTC | DTC Sequence Transfer Enable Register | DTCSQE | 16 | 16 | 2 ICLK | | DTCb |
| 0008 2418h | DTC | DTC Address Displacement Register | DTCDISP | 32 | 32 | 2 ICLK | | DTCb |
| 0008 2800h | EXDMAC0 | EXDMA Source Address Register | EDMSAR | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2804h | EXDMAC0 | EXDMA Destination Address Register | EDMDAR | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2808h | EXDMAC0 | EXDMA Transfer Count Register | EDMCRA | 32 | 32 | 1, 2 BCLK | | EXDMACa |

**Table 4.1 List of I/O Registers (Address Order) (5 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 280Ch | EXDMAC0 | EXDMA Block Transfer Count Register | EDMCRB | 16 | 16 | 1, 2 BCLK | | EXDMACa |
| 0008 2810h | EXDMAC0 | EXDMA Transfer Mode Register | EDMTMD | 16 | 16 | 1, 2 BCLK | | EXDMACa |
| 0008 2812h | EXDMAC0 | EXDMA Output Setting Register | EDMOMD | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2813h | EXDMAC0 | EXDMA Interrupt Setting Register | EDMINT | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2814h | EXDMAC0 | EXDMA Address Mode Register | EDMAMD | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2818h | EXDMAC0 | EXDMA Offset Register | EDMOFR | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 281Ch | EXDMAC0 | EXDMA Transfer Enable Register | EDMCNT | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 281Dh | EXDMAC0 | EXDMA Software Start Register | EDMREQ | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 281Eh | EXDMAC0 | EXDMA Status Register | EDMSTS | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2820h | EXDMAC0 | EXDMA External Request Sense Mode Register | EDMRMD | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2821h | EXDMAC0 | EXDMA External Request Flag Register | EDMERF | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2822h | EXDMAC0 | EXDMA Peripheral Request Flag Register | EDMPRF | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2840h | EXDMAC1 | EXDMA Source Address Register | EDMSAR | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2844h | EXDMAC1 | EXDMA Destination Address Register | EDMDAR | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2848h | EXDMAC1 | EXDMA Transfer Count Register | EDMCRA | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 284Ch | EXDMAC1 | EXDMA Block Transfer Count Register | EDMCRB | 16 | 16 | 1, 2 BCLK | | EXDMACa |
| 0008 2850h | EXDMAC1 | EXDMA Transfer Mode Register | EDMTMD | 16 | 16 | 1, 2 BCLK | | EXDMACa |
| 0008 2852h | EXDMAC1 | EXDMA Output Setting Register | EDMOMD | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2853h | EXDMAC1 | EXDMA Interrupt Setting Register | EDMINT | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2854h | EXDMAC1 | EXDMA Address Mode Register | EDMAMD | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 285Ch | EXDMAC1 | EXDMA Transfer Enable Register | EDMCNT | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 285Dh | EXDMAC1 | EXDMA Software Start Register | EDMREQ | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 285Eh | EXDMAC1 | EXDMA Status Register | EDMSTS | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2860h | EXDMAC1 | EXDMA External Request Sense Mode Register | EDMRMD | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2861h | EXDMAC1 | EXDMA External Request Flag Register | EDMERF | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2862h | EXDMAC1 | EXDMA Peripheral Request Flag Register | EDMPRF | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2A00h | EXDMAC | EXDMAC Module Start Register | EDMAST | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE0h | EXDMAC | Cluster Buffer Register 0 | CLSBR0 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE4h | EXDMAC | Cluster Buffer Register 1 | CLSBR1 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE8h | EXDMAC | Cluster Buffer Register 2 | CLSBR2 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BECh | EXDMAC | Cluster Buffer Register 3 | CLSBR3 | 32 | 32 | 1, 2 BCLK | | EXDMACa |

**Table 4.1 List of I/O Registers (Address Order) (6 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 2BF0h | EXDMAC | Cluster Buffer Register 4 | CLSBR4 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF4h | EXDMAC | Cluster Buffer Register 5 | CLSBR5 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF8h | EXDMAC | Cluster Buffer Register 6 | CLSBR6 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BFCh | EXDMAC | Cluster Buffer Register 7 | CLSBR7 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 3002h | BSC | CS0 Mode Register | CS0MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3004h | BSC | CS0 Wait Control Register 1 | CS0WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3008h | BSC | CS0 Wait Control Register 2 | CS0WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3012h | BSC | CS1 Mode Register | CS1MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3014h | BSC | CS1 Wait Control Register 1 | CS1WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3018h | BSC | CS1 Wait Control Register 2 | CS1WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3022h | BSC | CS2 Mode Register | CS2MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3024h | BSC | CS2 Wait Control Register 1 | CS2WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3028h | BSC | CS2 Wait Control Register 2 | CS2WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3032h | BSC | CS3 Mode Register | CS3MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3034h | BSC | CS3 Wait Control Register 1 | CS3WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3038h | BSC | CS3 Wait Control Register 2 | CS3WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3042h | BSC | CS4 Mode Register | CS4MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3044h | BSC | CS4 Wait Control Register 1 | CS4WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3048h | BSC | CS4 Wait Control Register 2 | CS4WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3052h | BSC | CS5 Mode Register | CS5MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3054h | BSC | CS5 Wait Control Register 1 | CS5WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3058h | BSC | CS5 Wait Control Register 2 | CS5WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3062h | BSC | CS6 Mode Register | CS6MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3064h | BSC | CS6 Wait Control Register 1 | CS6WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3068h | BSC | CS6 Wait Control Register 2 | CS6WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3072h | BSC | CS7 Mode Register | CS7MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3074h | BSC | CS7 Wait Control Register 1 | CS7WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3078h | BSC | CS7 Wait Control Register 2 | CS7WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3802h | BSC | CS0 Control Register | CS0CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 380Ah | BSC | CS0 Recovery Cycle Register | CS0REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3812h | BSC | CS1 Control Register | CS1CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 381Ah | BSC | CS1 Recovery Cycle Register | CS1REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3822h | BSC | CS2 Control Register | CS2CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 382Ah | BSC | CS2 Recovery Cycle Register | CS2REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3832h | BSC | CS3 Control Register | CS3CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 383Ah | BSC | CS3 Recovery Cycle Register | CS3REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3842h | BSC | CS4 Control Register | CS4CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 384Ah | BSC | CS4 Recovery Cycle Register | CS4REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3852h | BSC | CS5 Control Register | CS5CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 385Ah | BSC | CS5 Recovery Cycle Register | CS5REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3862h | BSC | CS6 Control Register | CS6CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 386Ah | BSC | CS6 Recovery Cycle Register | CS6REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3872h | BSC | CS7 Control Register | CS7CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 387Ah | BSC | CS7 Recovery Cycle Register | CS7REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3880h | BSC | CS Recovery Cycle Insertion Enable Register | CSRECEN | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3C00h | BSC | SDC Control Register | SDCCR | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C01h | BSC | SDC Mode Register | SDCMOD | 8 | 8 | 1, 2 BCLK | | Buses |

**Table 4.1 List of I/O Registers (Address Order) (7 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 3C02h | BSC | SDRAM Access Mode Register | SDAMOD | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C10h | BSC | SDRAM Self-Refresh Control Register | SDSELF | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C14h | BSC | SDRAM Refresh Control Register | SDRFCR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3C16h | BSC | SDRAM Auto-Refresh Control Register | SDRFEN | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C20h | BSC | SDRAM Initialization Sequence Control Register | SDICR | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C24h | BSC | SDRAM Initialization Register | SDIR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3C40h | BSC | SDRAM Address Register | SDADR | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 3C44h | BSC | SDRAM Timing Register | SDTR | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3C48h | BSC | SDRAM Mode Register | SDMOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3C50h | BSC | SDRAM Status Register | SDSR | 8 | 8 | 1, 2 BCLK | | Buses |
| 0008 6400h | MPU | Region-0 Start Page Number Register | RSPAGE0 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6404h | MPU | Region-0 End Page Number Register | REPAGE0 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6408h | MPU | Region-1 Start Page Number Register | RSPAGE1 | 32 | 32 | 1 ICLK | | MPU |
| 0008 640Ch | MPU | Region-1 End Page Number Register | REPAGE1 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6410h | MPU | Region-2 Start Page Number Register | RSPAGE2 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6414h | MPU | Region-2 End Page Number Register | REPAGE2 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6418h | MPU | Region-3 Start Page Number Register | RSPAGE3 | 32 | 32 | 1 ICLK | | MPU |
| 0008 641Ch | MPU | Region-3 End Page Number Register | REPAGE3 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6420h | MPU | Region-4 Start Page Number Register | RSPAGE4 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6424h | MPU | Region-4 End Page Number Register | REPAGE4 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6428h | MPU | Region-5 Start Page Number Register | RSPAGE5 | 32 | 32 | 1 ICLK | | MPU |
| 0008 642Ch | MPU | Region-5 End Page Number Register | REPAGE5 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6430h | MPU | Region-6 Start Page Number Register | RSPAGE6 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6434h | MPU | Region-6 End Page Number Register | REPAGE6 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6438h | MPU | Region-7 Start Page Number Register | RSPAGE7 | 32 | 32 | 1 ICLK | | MPU |
| 0008 643Ch | MPU | Region-7 End Page Number Register | REPAGE7 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6500h | MPU | Memory-Protection Enable Register | MPEN | 32 | 32 | 1 ICLK | | MPU |
| 0008 6504h | MPU | Background Access Control Register | MPBAC | 32 | 32 | 1 ICLK | | MPU |
| 0008 6508h | MPU | Memory-Protection Error Status-Clearing Register | MPECLR | 32 | 32 | 1 ICLK | | MPU |
| 0008 650Ch | MPU | Memory-Protection Error Status Register | MPESTS | 32 | 32 | 1 ICLK | | MPU |
| 0008 6514h | MPU | Data Memory-Protection Error Address Register | MPDEA | 32 | 32 | 1 ICLK | | MPU |
| 0008 6520h | MPU | Region Search Address Register | MPSA | 32 | 32 | 1 ICLK | | MPU |
| 0008 6524h | MPU | Region Search Operation Register | MPOPS | 16 | 16 | 1 ICLK | | MPU |
| 0008 6526h | MPU | Region Invalidation Operation Register | MPOPI | 16 | 16 | 1 ICLK | | MPU |
| 0008 6528h | MPU | Instruction-Hit Region Register | MHITI | 32 | 32 | 1 ICLK | | MPU |
| 0008 652Ch | MPU | Data-Hit Region Register | MHITD | 32 | 32 | 1 ICLK | | MPU |
| 0008 7010h to 0008 70FFh | ICU | Interrupt Request Register 016 to Interrupt Request Register 255 | IR016 to IR255 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 711Ah to 0008 71FFh | ICU | DTC Transfer Request Enable Register 026 to DTC Transfer Request Enable Register 255 | DTCER026 to DTCER255 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7202h to 0008 721Fh | ICU | Interrupt Request Enable Register 02 to Interrupt Request Enable Register 1F | IER02 to IER1F | 8 | 8 | 2 ICLK | | ICUB |
| 0008 72E0h | ICU | Software Interrupt Generation Register | SWINTR | 8 | 8 | 2 ICLK | | ICUB |
| 0008 72E1h | ICU | Software Interrupt 2 Generation Register | SWINT2R | 8 | 8 | 2 ICLK | | ICUB |
| 0008 72F0h | ICU | Fast Interrupt Set Register | FIR | 16 | 16 | 2 ICLK | | ICUB |
| 0008 7300h to 0008 73FFh | ICU | Interrupt Source Priority Register 000 to Interrupt Source Priority Register 255 | IPR000 to IPR255 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7400h | ICU | DMAC Trigger Select Register 0 | DMRSR0 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7404h | ICU | DMAC Trigger Select Register 1 | DMRSR1 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7408h | ICU | DMAC Trigger Select Register 2 | DMRSR2 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 740Ch | ICU | DMAC Trigger Select Register 3 | DMRSR3 | 8 | 8 | 2 ICLK | | ICUB |

**Table 4.1 List of I/O Registers (Address Order) (8 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 7410h | ICU | DMAC Trigger Select Register 4 | DMRSR4 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7414h | ICU | DMAC Trigger Select Register 5 | DMRSR5 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7418h | ICU | DMAC Trigger Select Register 6 | DMRSR6 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 741Ch | ICU | DMAC Trigger Select Register 7 | DMRSR7 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7500h to 0008 750Fh | ICU | IRQ Control Register 0 to IRQ Control Register 15 | IRQCR0 to IRQCR15 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7520h | ICU | IRQ Pin Digital Filter Enable Register 0 | IRQFLTE0 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7521h | ICU | IRQ Pin Digital Filter Enable Register 1 | IRQFLTE1 | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7528h | ICU | IRQ Pin Digital Filter Setting Register 0 | IRQFLTC0 | 16 | 16 | 2 ICLK | | ICUB |
| 0008 752Ah | ICU | IRQ Pin Digital Filter Setting Register 1 | IRQFLTC1 | 16 | 16 | 2 ICLK | | ICUB |
| 0008 7580h | ICU | Non-Maskable Interrupt Status Register | NMISR | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7581h | ICU | Non-Maskable Interrupt Enable Register | NMIER | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7582h | ICU | Non-Maskable Interrupt Status Clear Register | NMICLR | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7583h | ICU | NMI Pin Interrupt Control Register | NMICR | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7590h | ICU | NMI Pin Digital Filter Enable Register | NMIFLTE | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7594h | ICU | NMI Pin Digital Filter Setting Register | NMIFLTC | 8 | 8 | 2 ICLK | | ICUB |
| 0008 7600h | ICU | Group BE0 Interrupt Request Register | GRPBE0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7630h | ICU | Group BL0 Interrupt Request Register | GRPBL0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7634h | ICU | Group BL1 Interrupt Request Register | GRPBL1 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7638h | ICU | Group BL2 Interrupt Request Register | GRPBL2 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7640h | ICU | Group BE0 Interrupt Request Enable Register | GENBE0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7670h | ICU | Group BL0 Interrupt Request Enable Register | GENBL0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7674h | ICU | Group BL1 Interrupt Request Enable Register | GENBL1 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7678h | ICU | Group BL2 Interrupt Request Enable Register | GENBL2 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7680h | ICU | Group BE0 Interrupt Clear Register | GCRBE0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7700h | ICU | Software Configurable Interrupt B Request Register 0 | PIBR0 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7701h | ICU | Software Configurable Interrupt B Request Register 1 | PIBR1 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7702h | ICU | Software Configurable Interrupt B Request Register 2 | PIBR2 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7703h | ICU | Software Configurable Interrupt B Request Register 3 | PIBR3 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7704h | ICU | Software Configurable Interrupt B Request Register 4 | PIBR4 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7705h | ICU | Software Configurable Interrupt B Request Register 5 | PIBR5 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7706h | ICU | Software Configurable Interrupt B Request Register 6 | PIBR6 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7707h | ICU | Software Configurable Interrupt B Request Register 7 | PIBR7 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7708h | ICU | Software Configurable Interrupt B Request Register 8 | PIBR8 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7709h | ICU | Software Configurable Interrupt B Request Register 9 | PIBR9 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 770Ah | ICU | Software Configurable Interrupt B Request Register A | PIBRA | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 770Bh | ICU | Software Configurable Interrupt B Request Register B | PIBRB | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7780h | ICU | Software Configurable Interrupt B Source Select Register X128 | SLIBXR128 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7781h | ICU | Software Configurable Interrupt B Source Select Register X129 | SLIBXR129 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7782h | ICU | Software Configurable Interrupt B Source Select Register X130 | SLIBXR130 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |

**Table 4.1 List of I/O Registers (Address Order) (9 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 7783h | ICU | Software Configurable Interrupt B Source Select Register X131 | SLIBXR131 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7784h | ICU | Software Configurable Interrupt B Source Select Register X132 | SLIBXR132 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7785h | ICU | Software Configurable Interrupt B Source Select Register X133 | SLIBXR133 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7786h | ICU | Software Configurable Interrupt B Source Select Register X134 | SLIBXR134 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7787h | ICU | Software Configurable Interrupt B Source Select Register X135 | SLIBXR135 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7788h | ICU | Software Configurable Interrupt B Source Select Register X136 | SLIBXR136 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7789h | ICU | Software Configurable Interrupt B Source Select Register X137 | SLIBXR137 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 778Ah | ICU | Software Configurable Interrupt B Source Select Register X138 | SLIBXR138 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 778Bh | ICU | Software Configurable Interrupt B Source Select Register X139 | SLIBXR139 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 778Ch | ICU | Software Configurable Interrupt B Source Select Register X140 | SLIBXR140 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 778Dh | ICU | Software Configurable Interrupt B Source Select Register X141 | SLIBXR141 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 778Eh | ICU | Software Configurable Interrupt B Source Select Register X142 | SLIBXR142 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 778Fh | ICU | Software Configurable Interrupt B Source Select Register X143 | SLIBXR143 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7790h | ICU | Software Configurable Interrupt B Source Select Register 144 | SLIBR144 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7791h | ICU | Software Configurable Interrupt B Source Select Register 145 | SLIBR145 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7792h | ICU | Software Configurable Interrupt B Source Select Register 146 | SLIBR146 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7793h | ICU | Software Configurable Interrupt B Source Select Register 147 | SLIBR147 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7794h | ICU | Software Configurable Interrupt B Source Select Register 148 | SLIBR148 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7795h | ICU | Software Configurable Interrupt B Source Select Register 149 | SLIBR149 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7796h | ICU | Software Configurable Interrupt B Source Select Register 150 | SLIBR150 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7797h | ICU | Software Configurable Interrupt B Source Select Register 151 | SLIBR151 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7798h | ICU | Software Configurable Interrupt B Source Select Register 152 | SLIBR152 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7799h | ICU | Software Configurable Interrupt B Source Select Register 153 | SLIBR153 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 779Ah | ICU | Software Configurable Interrupt B Source Select Register 154 | SLIBR154 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 779Bh | ICU | Software Configurable Interrupt B Source Select Register 155 | SLIBR155 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 779Ch | ICU | Software Configurable Interrupt B Source Select Register 156 | SLIBR156 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 779Dh | ICU | Software Configurable Interrupt B Source Select Register 157 | SLIBR157 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 779Eh | ICU | Software Configurable Interrupt B Source Select Register 158 | SLIBR158 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 779Fh | ICU | Software Configurable Interrupt B Source Select Register 159 | SLIBR159 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A0h | ICU | Software Configurable Interrupt B Source Select Register 160 | SLIBR160 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A1h | ICU | Software Configurable Interrupt B Source Select Register 161 | SLIBR161 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |

**Table 4.1 List of I/O Registers (Address Order) (10 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 77A2h | ICU | Software Configurable Interrupt B Source Select Register 162 | SLIBR162 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A3h | ICU | Software Configurable Interrupt B Source Select Register 163 | SLIBR163 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A4h | ICU | Software Configurable Interrupt B Source Select Register 164 | SLIBR164 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A5h | ICU | Software Configurable Interrupt B Source Select Register 165 | SLIBR165 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A6h | ICU | Software Configurable Interrupt B Source Select Register 166 | SLIBR166 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A7h | ICU | Software Configurable Interrupt B Source Select Register 167 | SLIBR167 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A8h | ICU | Software Configurable Interrupt B Source Select Register 168 | SLIBR168 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77A9h | ICU | Software Configurable Interrupt B Source Select Register 169 | SLIBR169 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77AAh | ICU | Software Configurable Interrupt B Source Select Register 170 | SLIBR170 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77ABh | ICU | Software Configurable Interrupt B Source Select Register 171 | SLIBR171 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77ACh | ICU | Software Configurable Interrupt B Source Select Register 172 | SLIBR172 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77ADh | ICU | Software Configurable Interrupt B Source Select Register 173 | SLIBR173 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77AEh | ICU | Software Configurable Interrupt B Source Select Register 174 | SLIBR174 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77AFh | ICU | Software Configurable Interrupt B Source Select Register 175 | SLIBR175 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B0h | ICU | Software Configurable Interrupt B Source Select Register 176 | SLIBR176 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B1h | ICU | Software Configurable Interrupt B Source Select Register 177 | SLIBR177 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B2h | ICU | Software Configurable Interrupt B Source Select Register 178 | SLIBR178 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B3h | ICU | Software Configurable Interrupt B Source Select Register 179 | SLIBR179 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B4h | ICU | Software Configurable Interrupt B Source Select Register 180 | SLIBR180 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B5h | ICU | Software Configurable Interrupt B Source Select Register 181 | SLIBR181 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B6h | ICU | Software Configurable Interrupt B Source Select Register 182 | SLIBR182 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B7h | ICU | Software Configurable Interrupt B Source Select Register 183 | SLIBR183 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B8h | ICU | Software Configurable Interrupt B Source Select Register 184 | SLIBR184 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77B9h | ICU | Software Configurable Interrupt B Source Select Register 185 | SLIBR185 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BAh | ICU | Software Configurable Interrupt B Source Select Register 186 | SLIBR186 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BBh | ICU | Software Configurable Interrupt B Source Select Register 187 | SLIBR187 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BCh | ICU | Software Configurable Interrupt B Source Select Register 188 | SLIBR188 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BDh | ICU | Software Configurable Interrupt B Source Select Register 189 | SLIBR189 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BEh | ICU | Software Configurable Interrupt B Source Select Register 190 | SLIBR190 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BFh | ICU | Software Configurable Interrupt B Source Select Register 191 | SLIBR191 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C0h | ICU | Software Configurable Interrupt B Source Select Register 192 | SLIBR192 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |

**Table 4.1 List of I/O Registers (Address Order) (11 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 77C1h | ICU | Software Configurable Interrupt B Source Select Register 193 | SLIBR193 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C2h | ICU | Software Configurable Interrupt B Source Select Register 194 | SLIBR194 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C3h | ICU | Software Configurable Interrupt B Source Select Register 195 | SLIBR195 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C4h | ICU | Software Configurable Interrupt B Source Select Register 196 | SLIBR196 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C5h | ICU | Software Configurable Interrupt B Source Select Register 197 | SLIBR197 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C6h | ICU | Software Configurable Interrupt B Source Select Register 198 | SLIBR198 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C7h | ICU | Software Configurable Interrupt B Source Select Register 199 | SLIBR199 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C8h | ICU | Software Configurable Interrupt B Source Select Register 200 | SLIBR200 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C9h | ICU | Software Configurable Interrupt B Source Select Register 201 | SLIBR201 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CAh | ICU | Software Configurable Interrupt B Source Select Register 202 | SLIBR202 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CBh | ICU | Software Configurable Interrupt B Source Select Register 203 | SLIBR203 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CCh | ICU | Software Configurable Interrupt B Source Select Register 204 | SLIBR204 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CDh | ICU | Software Configurable Interrupt B Source Select Register 205 | SLIBR205 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CEh | ICU | Software Configurable Interrupt B Source Select Register 206 | SLIBR206 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CFh | ICU | Software Configurable Interrupt B Source Select Register 207 | SLIBR207 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7830h | ICU | Group AL0 Interrupt Request Register | GRPAL0 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7834h | ICU | Group AL1 Interrupt Request Register | GRPAL1 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7870h | ICU | Group AL0 Interrupt Request Enable Register | GENAL0 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7874h | ICU | Group AL1 Interrupt Request Enable Register | GENAL1 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7900h | ICU | Software Configurable Interrupt A Request Register 0 | PIAR0 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7901h | ICU | Software Configurable Interrupt A Request Register 1 | PIAR1 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7902h | ICU | Software Configurable Interrupt A Request Register 2 | PIAR2 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7903h | ICU | Software Configurable Interrupt A Request Register 3 | PIAR3 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7904h | ICU | Software Configurable Interrupt A Request Register 4 | PIAR4 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7905h | ICU | Software Configurable Interrupt A Request Register 5 | PIAR5 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 790Bh | ICU | Software Configurable Interrupt A Request Register B | PIARB | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D0h | ICU | Software Configurable Interrupt A Source Select Register 208 | SLIAR208 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D1h | ICU | Software Configurable Interrupt A Source Select Register 209 | SLIAR209 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D2h | ICU | Software Configurable Interrupt A Source Select Register 210 | SLIAR210 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D3h | ICU | Software Configurable Interrupt A Source Select Register 211 | SLIAR211 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D4h | ICU | Software Configurable Interrupt A Source Select Register 212 | SLIAR212 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D5h | ICU | Software Configurable Interrupt A Source Select Register 213 | SLIAR213 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D6h | ICU | Software Configurable Interrupt A Source Select Register 214 | SLIAR214 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |

**Table 4.1 List of I/O Registers (Address Order) (12 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 79D7h | ICU | Software Configurable Interrupt A Source Select Register 215 | SLIAR215 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D8h | ICU | Software Configurable Interrupt A Source Select Register 216 | SLIAR216 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D9h | ICU | Software Configurable Interrupt A Source Select Register 217 | SLIAR217 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79DAh | ICU | Software Configurable Interrupt A Source Select Register 218 | SLIAR218 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79DBh | ICU | Software Configurable Interrupt A Source Select Register 219 | SLIAR219 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79DCh | ICU | Software Configurable Interrupt A Source Select Register 220 | SLIAR220 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79DDh | ICU | Software Configurable Interrupt A Source Select Register 221 | SLIAR221 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79DEh | ICU | Software Configurable Interrupt A Source Select Register 222 | SLIAR222 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79DFh | ICU | Software Configurable Interrupt A Source Select Register 223 | SLIAR223 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E0h | ICU | Software Configurable Interrupt A Source Select Register 224 | SLIAR224 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E1h | ICU | Software Configurable Interrupt A Source Select Register 225 | SLIAR225 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E2h | ICU | Software Configurable Interrupt A Source Select Register 226 | SLIAR226 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E3h | ICU | Software Configurable Interrupt A Source Select Register 227 | SLIAR227 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E4h | ICU | Software Configurable Interrupt A Source Select Register 228 | SLIAR228 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E5h | ICU | Software Configurable Interrupt A Source Select Register 229 | SLIAR229 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E6h | ICU | Software Configurable Interrupt A Source Select Register 230 | SLIAR230 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E7h | ICU | Software Configurable Interrupt A Source Select Register 231 | SLIAR231 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E8h | ICU | Software Configurable Interrupt A Source Select Register 232 | SLIAR232 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79E9h | ICU | Software Configurable Interrupt A Source Select Register 233 | SLIAR233 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79EAh | ICU | Software Configurable Interrupt A Source Select Register 234 | SLIAR234 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79EBh | ICU | Software Configurable Interrupt A Source Select Register 235 | SLIAR235 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79ECh | ICU | Software Configurable Interrupt A Source Select Register 236 | SLIAR236 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79EDh | ICU | Software Configurable Interrupt A Source Select Register 237 | SLIAR237 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79EEh | ICU | Software Configurable Interrupt A Source Select Register 238 | SLIAR238 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79EFh | ICU | Software Configurable Interrupt A Source Select Register 239 | SLIAR239 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F0h | ICU | Software Configurable Interrupt A Source Select Register 240 | SLIAR240 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F1h | ICU | Software Configurable Interrupt A Source Select Register 241 | SLIAR241 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F2h | ICU | Software Configurable Interrupt A Source Select Register 242 | SLIAR242 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F3h | ICU | Software Configurable Interrupt A Source Select Register 243 | SLIAR243 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F4h | ICU | Software Configurable Interrupt A Source Select Register 244 | SLIAR244 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F5h | ICU | Software Configurable Interrupt A Source Select Register 245 | SLIAR245 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |

**Table 4.1 List of I/O Registers (Address Order) (13 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 79F6h | ICU | Software Configurable Interrupt A Source Select Register 246 | SLIAR246 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F7h | ICU | Software Configurable Interrupt A Source Select Register 247 | SLIAR247 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F8h | ICU | Software Configurable Interrupt A Source Select Register 248 | SLIAR248 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F9h | ICU | Software Configurable Interrupt A Source Select Register 249 | SLIAR249 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FAh | ICU | Software Configurable Interrupt A Source Select Register 250 | SLIAR250 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FBh | ICU | Software Configurable Interrupt A Source Select Register 251 | SLIAR251 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FCh | ICU | Software Configurable Interrupt A Source Select Register 252 | SLIAR252 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FDh | ICU | Software Configurable Interrupt A Source Select Register 253 | SLIAR253 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FEh | ICU | Software Configurable Interrupt A Source Select Register 254 | SLIAR254 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FFh | ICU | Software Configurable Interrupt A Source Select Register 255 | SLIAR255 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7A00h | ICU | Software Configurable Interrupt Source Select Register Write Protect Register | SLIPRCR | 8 | 8 | 2 ICLK to 1 PCLKA/B | 2 ICLK | ICUB |
| 0008 7A01h | ICU | EXDMAC Trigger Select Register | SELEXDR | 8 | 8 | 2 ICLK to 1 PCLKA/B | 2 ICLK | ICUB |
| 0008 8000h | CMT | Compare Match Timer Start Register 0 | CMSTR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8002h | CMT0 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8004h | CMT0 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8006h | CMT0 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8008h | CMT1 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 800Ah | CMT1 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 800Ch | CMT1 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8010h | CMT | Compare Match Timer Start Register 1 | CMSTR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8012h | CMT2 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8014h | CMT2 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8016h | CMT2 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8018h | CMT3 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 801Ah | CMT3 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 801Ch | CMT3 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8020h | WDT | WDT Refresh Register | WDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8022h | WDT | WDT Control Register | WDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8024h | WDT | WDT Status Register | WDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8026h | WDT | WDT Reset Control Register | WDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8030h | IWDT | IWDT Refresh Register | IWDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8032h | IWDT | IWDT Control Register | IWDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8034h | IWDT | IWDT Status Register | IWDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8036h | IWDT | IWDT Reset Control Register | IWDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8038h | IWDT | IWDT Count Stop Control Register | IWDTCSTPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8040h | DA | D/A Data Register 0 | DADR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8042h | DA | D/A Data Register 1 | DADR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8044h | DA | D/A Control Register | DACR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8045h | DA | Data Register Format Select Register | DADPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8046h | DA | D/A A/D Synchronous Start Control Register | DAADSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8048h | DA | D/A Output Amplifier Control Register | DAAMPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 805Ch | DA | D/A Output Amplifier Stabilization Wait Control Register | DAASWCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8100h | TPUA | Timer Start Register | TSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |

**Table 4.1 List of I/O Registers (Address Order) (14 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 8101h | TPUA | Timer Synchronous Register | TSYR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8108h | TPU0 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8109h | TPU1 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 810Ah | TPU2 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 810Bh | TPU3 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 810Ch | TPU4 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 810Dh | TPU5 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8110h | TPU0 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8111h | TPU0 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8112h | TPU0 | Timer I/O Control Register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8113h | TPU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8114h | TPU0 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8115h | TPU0 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8116h | TPU0 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8118h | TPU0 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 811Ah | TPU0 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 811Ch | TPU0 | Timer General Register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 811Eh | TPU0 | Timer General Register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8120h | TPU1 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8121h | TPU1 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8122h | TPU1 | Timer I/O Control Register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8124h | TPU1 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8125h | TPU1 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8126h | TPU1 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8128h | TPU1 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 812Ah | TPU1 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8130h | TPU2 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8131h | TPU2 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8132h | TPU2 | Timer I/O Control Register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8134h | TPU2 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8135h | TPU2 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8136h | TPU2 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8138h | TPU2 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 813Ah | TPU2 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8140h | TPU3 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8141h | TPU3 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8142h | TPU3 | Timer I/O Control Register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8143h | TPU3 | Timer I/O Control Register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8144h | TPU3 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8145h | TPU3 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8146h | TPU3 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8148h | TPU3 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 814Ah | TPU3 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 814Ch | TPU3 | Timer General Register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 814Eh | TPU3 | Timer General Register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8150h | TPU4 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8151h | TPU4 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8152h | TPU4 | Timer I/O Control Register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8154h | TPU4 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8155h | TPU4 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |

**Table 4.1 List of I/O Registers (Address Order) (15 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 8156h | TPU4 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8158h | TPU4 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 815Ah | TPU4 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8160h | TPU5 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8161h | TPU5 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8162h | TPU5 | Timer I/O Control Register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8164h | TPU5 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8165h | TPU5 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8166h | TPU5 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8168h | TPU5 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 816Ah | TPU5 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 81E6h | PPG0 | PPG Output Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81E7h | PPG0 | PPG Output Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81E8h | PPG0 | Next Data Enable Register H | NDERH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81E9h | PPG0 | Next Data Enable Register L | NDERL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EAh | PPG0 | Output Data Register H | PODRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EBh | PPG0 | Output Data Register L | PODRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81ECh | PPG0 | Next Data Register H | NDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EDh | PPG0 | Next Data Register L | NDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EEh | PPG0 | Next Data Register H2 | NDRH2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81EFh | PPG0 | Next Data Register L2 | NDRL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F0h | PPG1 | PPG Trigger Select Register | PTRSLR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F6h | PPG1 | PPG Output Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F7h | PPG1 | PPG Output Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F8h | PPG1 | Next Data Enable Register H | NDERH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81F9h | PPG1 | Next Data Enable Register L | NDERL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FAh | PPG1 | Output Data Register H | PODRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FBh | PPG1 | Output Data Register L | PODRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FCh | PPG1 | Next Data Register H | NDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FDh | PPG1 | Next Data Register L | NDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FEh | PPG1 | Next Data Register H2 | NDRH2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 81FFh | PPG1 | Next Data Register L2 | NDRL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG |
| 0008 8200h | TMR0 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8201h | TMR1 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8202h | TMR0 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8203h | TMR1 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8204h | TMR0 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8204h | TMR01 | Time Constant Register A | TCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8205h | TMR1 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8206h | TMR0 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8206h | TMR01 | Time Constant Register B | TCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8207h | TMR1 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8208h | TMR0 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8208h | TMR01 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8209h | TMR1 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Ah | TMR0 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Ah | TMR01 | Timer Counter Control Register | TCCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Bh | TMR1 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Ch | TMR0 | Timer Counter Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Dh | TMR1 | Timer Counter Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |

**Table 4.1 List of I/O Registers (Address Order) (16 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 8210h | TMR2 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8211h | TMR3 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8212h | TMR2 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8213h | TMR3 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8214h | TMR2 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8214h | TMR23 | Time Constant Register A | TCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8215h | TMR3 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8216h | TMR2 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8216h | TMR23 | Time Constant Register B | TCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8217h | TMR3 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8218h | TMR2 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8218h | TMR23 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8219h | TMR3 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Ah | TMR2 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Ah | TMR23 | Timer Counter Control Register | TCCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Bh | TMR3 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Ch | TMR2 | Timer Counter Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Dh | TMR3 | Timer Counter Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8280h | CRC | CRC Control Register | CRCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CRCA |
| 0008 8284h | CRC | CRC Data Input Register | CRCDIR | 32 | 8, 32 | 2, 3 PCLKB | 2 ICLK | CRCA |
| 0008 8288h | CRC | CRC Data Output Register | CRCDOR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CRCA |
| 0008 8300h | RIIC0 | I²C-bus Control Register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8301h | RIIC0 | I²C-bus Control Register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8302h | RIIC0 | I²C-bus Mode Register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8303h | RIIC0 | I²C-bus Mode Register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8304h | RIIC0 | I²C-bus Mode Register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8305h | RIIC0 | I²C-bus Function Enable Register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8306h | RIIC0 | I²C-bus Status Enable Register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8307h | RIIC0 | I²C-bus Interrupt Enable Register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8308h | RIIC0 | I²C-bus Status Register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8309h | RIIC0 | I²C-bus Status Register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Ah | RIIC0 | Slave Address Register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Bh | RIIC0 | Slave Address Register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Ch | RIIC0 | Slave Address Register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Dh | RIIC0 | Slave Address Register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Eh | RIIC0 | Slave Address Register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Fh | RIIC0 | Slave Address Register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8310h | RIIC0 | I²C-bus Bit Rate Low-Level Register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8311h | RIIC0 | I²C-bus Bit Rate High-Level Register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8312h | RIIC0 | I²C-bus Transmit Data Register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8313h | RIIC0 | I²C-bus Receive Data Register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8320h | RIIC1 | I²C-bus Control Register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8321h | RIIC1 | I²C-bus Control Register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8322h | RIIC1 | I²C-bus Mode Register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8323h | RIIC1 | I²C-bus Mode Register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8324h | RIIC1 | I²C-bus Mode Register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8325h | RIIC1 | I²C-bus Function Enable Register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8326h | RIIC1 | I²C-bus Status Enable Register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8327h | RIIC1 | I²C-bus Interrupt Enable Register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |

**Table 4.1 List of I/O Registers (Address Order) (17 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 8328h | RIIC1 | I²C-bus Status Register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8329h | RIIC1 | I²C-bus Status Register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 832Ah | RIIC1 | Slave Address Register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 832Bh | RIIC1 | Slave Address Register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 832Ch | RIIC1 | Slave Address Register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 832Dh | RIIC1 | Slave Address Register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 832Eh | RIIC1 | Slave Address Register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 832Fh | RIIC1 | Slave Address Register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8330h | RIIC1 | I²C-bus Bit Rate Low-Level Register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8331h | RIIC1 | I²C-bus Bit Rate High-Level Register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8332h | RIIC1 | I²C-bus Transmit Data Register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8333h | RIIC1 | I²C-bus Receive Data Register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8340h | RIIC2 | I²C-bus Control Register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8341h | RIIC2 | I²C-bus Control Register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8342h | RIIC2 | I²C-bus Mode Register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8343h | RIIC2 | I²C-bus Mode Register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8344h | RIIC2 | I²C-bus Mode Register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8345h | RIIC2 | I²C-bus Function Enable Register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8346h | RIIC2 | I²C-bus Status Enable Register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8347h | RIIC2 | I²C-bus Interrupt Enable Register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8348h | RIIC2 | I²C-bus Status Register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8349h | RIIC2 | I²C-bus Status Register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Ah | RIIC2 | Slave Address Register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Bh | RIIC2 | Slave Address Register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Ch | RIIC2 | Slave Address Register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Dh | RIIC2 | Slave Address Register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Eh | RIIC2 | Slave Address Register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 834Fh | RIIC2 | Slave Address Register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8350h | RIIC2 | I²C-bus Bit Rate Low-Level Register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8351h | RIIC2 | I²C-bus Bit Rate High-Level Register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8352h | RIIC2 | I²C-bus Transmit Data Register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8353h | RIIC2 | I²C-bus Receive Data Register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8500h | MMCIF | Command Setting Register | CECMDSET | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8508h | MMCIF | Argument Register | CEARG | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 850Ch | MMCIF | Automatically Issued CMD12 Argument Register | CEARGCMD12 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8510h | MMCIF | Command Control Register | CECMDCTRL | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8514h | MMCIF | Transfer Block Setting Register | CEBLOCKSET | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8518h | MMCIF | Clock Control Register | CECLKCTRL | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 851Ch | MMCIF | Buffer Access Setting Register | CEBUFACC | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8520h | MMCIF | Response Register 3 | CERESP3 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8524h | MMCIF | Response Register 2 | CERESP2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8528h | MMCIF | Response Register 1 | CERESP1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 852Ch | MMCIF | Response Register 0 | CERESP0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8530h | MMCIF | Automatically Issued CMD12 Response Register | CERESPCMD12 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8534h | MMCIF | Data Register | CEDATA | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 853Ch | MMCIF | Boot Operation Setting Register | CEBOOT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8540h | MMCIF | Interrupt Status Flag Register | CEINT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8544h | MMCIF | Interrupt Request Enable Register | CEINTEN | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |

**Table 4.1 List of I/O Registers (Address Order) (18 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 8548h | MMCIF | Status Register 1 | CEHOSTSTS 1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 854Ch | MMCIF | Status Register 2 | CEHOSTSTS 2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8570h | MMCIF | MMC Detection and Port Control Register | CEDETECT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 8574h | MMCIF | Special Mode Setting Register | CEADDMOD E | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 857Ch | MMCIF | Version Register | CEVERSION | 32 | 32 | 2, 3 PCLKB | 2 ICLK | MMCIF |
| 0008 9000h | S12AD | A/D Control Register | ADCSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9004h | S12AD | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9008h | S12AD | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 900Ch | S12AD | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 900Eh | S12AD | A/D Control Extended Register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9010h | S12AD | A/D Conversion Start Trigger Select Register | ADSTRGR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9014h | S12AD | A/D Channel Select Register B0 | ADANSB0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9018h | S12AD | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 901Eh | S12AD | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9020h | S12AD | A/D Data Register 0 | ADDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9022h | S12AD | A/D Data Register 1 | ADDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9024h | S12AD | A/D Data Register 2 | ADDR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9026h | S12AD | A/D Data Register 3 | ADDR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9028h | S12AD | A/D Data Register 4 | ADDR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 902Ah | S12AD | A/D Data Register 5 | ADDR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 902Ch | S12AD | A/D Data Register 6 | ADDR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 902Eh | S12AD | A/D Data Register 7 | ADDR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9063h | S12AD | A/D Conversion Time Setting Protection Release Register | ADSAMPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9066h | S12AD | A/D Sample-and-Hold Circuit Control Register | ADSHCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 906Eh | S12AD | A/D Conversion Time Setting Register | ADSAM | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 907Ah | S12AD | A/D Disconnection Detection Control Register | ADDISCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 907Ch | S12AD | A/D Sample-and-Hold Operating Mode Select Register | ADSHMSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9080h | S12AD | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9084h | S12AD | A/D Data Duplication Register A | ADDBLDRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9086h | S12AD | A/D Data Duplication Register B | ADDBLDRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 908Ch | S12AD | A/D Comparison Function Window A/B Status Monitoring Register | ADWINMON | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9090h | S12AD | A/D Comparison Function Control Register | ADCMPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9094h | S12AD | A/D Comparison Function Window A Channel Select Register 0 | ADCMPANSR 0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9098h | S12AD | A/D Comparison Function Window A Comparison Condition Setting Register 0 | ADCMPLR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 909Ch | S12AD | A/D Comparison Function Window A Lower Level Setting Register | ADCMPDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 909Eh | S12AD | A/D Comparison Function Window A Upper Level Setting Register | ADCMPDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90A0h | S12AD | A/D Comparison Function Window A Channel Status Register 0 | ADCMPSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90A6h | S12AD | A/D Comparison Function Window B Channel Select Register | ADCMPBNS R | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90A8h | S12AD | A/D Comparison Function Window B Lower Level Setting Register | ADWINLLB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90AAh | S12AD | A/D Comparison Function Window B Upper Level Setting Register | ADWINULB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |

**Table 4.1 List of I/O Registers (Address Order) (19 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 90ACh | S12AD | A/D Comparison Function Window B Channel Status Register | ADCMPBSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90D4h | S12AD | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90D9h | S12AD | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90E0h | S12AD | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90E1h | S12AD | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90E2h | S12AD | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90E3h | S12AD | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90E4h | S12AD | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90E5h | S12AD | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90E6h | S12AD | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 90E7h | S12AD | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9100h | S12AD1 | A/D Control Register | ADCSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9104h | S12AD1 | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9106h | S12AD1 | A/D Channel Select Register A1 | ADANSA1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9108h | S12AD1 | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 910Ah | S12AD1 | A/D-Converted Value Addition/Average Function Channel Select Register 1 | ADADS1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 910Ch | S12AD1 | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 910Eh | S12AD1 | A/D Control Extended Register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9110h | S12AD1 | A/D Conversion Start Trigger Select Register | ADSTRGR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9112h | S12AD1 | A/D Conversion Extended Input Control Register | ADEXICR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9114h | S12AD1 | A/D Channel Select Register B0 | ADANSB0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9116h | S12AD1 | A/D Channel Select Register B1 | ADANSB1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9118h | S12AD1 | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 911Ah | S12AD1 | A/D Temperature Sensor Data Register | ADTSDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 911Ch | S12AD1 | A/D Internal Reference Voltage Data Register | ADOCDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 911Eh | S12AD1 | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9120h | S12AD1 | A/D Data Register 0 | ADDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9122h | S12AD1 | A/D Data Register 1 | ADDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9124h | S12AD1 | A/D Data Register 2 | ADDR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9126h | S12AD1 | A/D Data Register 3 | ADDR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9128h | S12AD1 | A/D Data Register 4 | ADDR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 912Ah | S12AD1 | A/D Data Register 5 | ADDR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 912Ch | S12AD1 | A/D Data Register 6 | ADDR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 912Eh | S12AD1 | A/D Data Register 7 | ADDR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9130h | S12AD1 | A/D Data Register 8 | ADDR8 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9132h | S12AD1 | A/D Data Register 9 | ADDR9 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9134h | S12AD1 | A/D Data Register 10 | ADDR10 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9136h | S12AD1 | A/D Data Register 11 | ADDR11 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9138h | S12AD1 | A/D Data Register 12 | ADDR12 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 913Ah | S12AD1 | A/D Data Register 13 | ADDR13 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 913Ch | S12AD1 | A/D Data Register 14 | ADDR14 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 913Eh | S12AD1 | A/D Data Register 15 | ADDR15 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9140h | S12AD1 | A/D Data Register 16 | ADDR16 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9142h | S12AD1 | A/D Data Register 17 | ADDR17 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9144h | S12AD1 | A/D Data Register 18 | ADDR18 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9146h | S12AD1 | A/D Data Register 19 | ADDR19 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9148h | S12AD1 | A/D Data Register 20 | ADDR20 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |

**Table 4.1 List of I/O Registers (Address Order) (20 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 9163h | S12AD1 | A/D Conversion Time Setting Protection Release Register | ADSAMPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 916Eh | S12AD1 | A/D Conversion Time Setting Register | ADSAM | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 917Ah | S12AD1 | A/D Disconnection Detection Control Register | ADDISCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9180h | S12AD1 | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9184h | S12AD1 | A/D Data Duplication Register A | ADDBLDRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9186h | S12AD1 | A/D Data Duplication Register B | ADDBLDRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 918Ch | S12AD1 | A/D Comparison Function Window A/B Status Monitoring Register | ADWINMON | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9190h | S12AD1 | A/D Comparison Function Control Register | ADCMPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9192h | S12AD1 | A/D Comparison Function Window A Extended Input Select Register | ADCMPANSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9193h | S12AD1 | A/D Comparison Function Window A Extended Input Comparison Condition Setting Register | ADCMPLER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9194h | S12AD1 | A/D Comparison Function Window A Channel Select Register 0 | ADCMPANSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9196h | S12AD1 | A/D Comparison Function Window A Channel Select Register 1 | ADCMPANSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9198h | S12AD1 | A/D Comparison Function Window A Comparison Condition Setting Register 0 | ADCMPLR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 919Ah | S12AD1 | A/D Comparison Function Window A Comparison Condition Setting Register 1 | ADCMPLR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 919Ch | S12AD1 | A/D Comparison Function Window A Lower Level Setting Register | ADCMPDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 919Eh | S12AD1 | A/D Comparison Function Window A Upper Level Setting Register | ADCMPDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91A0h | S12AD1 | A/D Comparison Function Window A Channel Status Register 0 | ADCMPSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91A2h | S12AD1 | A/D Comparison Function Window A Channel Status Register 1 | ADCMPSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91A4h | S12AD1 | A/D Comparison Function Window A Extended Input Channel Status Register | ADCMPSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91A6h | S12AD1 | A/D Comparison Function Window B Channel Select Register | ADCMPBNSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91A8h | S12AD1 | A/D Comparison Function Window B Lower Level Setting Register | ADWINLLB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91AAh | S12AD1 | A/D Comparison Function Window B Upper Level Setting Register | ADWINULB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91ACh | S12AD1 | A/D Comparison Function Window B Channel Status Register | ADCMPBSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91D4h | S12AD1 | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91D6h | S12AD1 | A/D Channel Select Register C1 | ADANSC1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91D8h | S12AD1 | A/D Group C Extended Input Control Register | ADGCEXCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91D9h | S12AD1 | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91DDh | S12AD1 | A/D Sampling State Register L | ADSSTRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91DEh | S12AD1 | A/D Sampling State Register T | ADSSTRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91DFh | S12AD1 | A/D Sampling State Register O | ADSSTRO | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E0h | S12AD1 | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E1h | S12AD1 | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E2h | S12AD1 | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E3h | S12AD1 | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E4h | S12AD1 | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E5h | S12AD1 | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E6h | S12AD1 | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E7h | S12AD1 | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E8h | S12AD1 | A/D Sampling State Register 8 | ADSSTR8 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E9h | S12AD1 | A/D Sampling State Register 9 | ADSSTR9 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |

**Table 4.1 List of I/O Registers (Address Order) (21 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 91EAh | S12AD1 | A/D Sampling State Register 10 | ADSSTR10 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EBh | S12AD1 | A/D Sampling State Register 11 | ADSSTR11 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91ECh | S12AD1 | A/D Sampling State Register 12 | ADSSTR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EDh | S12AD1 | A/D Sampling State Register 13 | ADSSTR13 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EEh | S12AD1 | A/D Sampling State Register 14 | ADSSTR14 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EFh | S12AD1 | A/D Sampling State Register 15 | ADSSTR15 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9E00h | QSPI | QSPI Control Register | SPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E01h | QSPI | QSPI Slave Select Polarity Register | SSLP | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E02h | QSPI | QSPI Pin Control Register | SPPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E03h | QSPI | QSPI Status Register | SPSR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E04h | QSPI | QSPI Data Register | SPDR | 32 | 8, 16, 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E08h | QSPI | QSPI Sequence Control Register | SPSCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E09h | QSPI | QSPI Sequence Status Register | SPSSR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Ah | QSPI | QSPI Bit Rate Register | SPBR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Bh | QSPI | QSPI Data Control Register | SPDCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Ch | QSPI | QSPI Clock Delay Register | SPCKD | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Dh | QSPI | QSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Eh | QSPI | QSPI Next-Access Delay Register | SPND | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E10h | QSPI | QSPI Command Register 0 | SPCMD0 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E12h | QSPI | QSPI Command Register 1 | SPCMD1 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E14h | QSPI | QSPI Command Register 2 | SPCMD2 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E16h | QSPI | QSPI Command Register 3 | SPCMD3 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E18h | QSPI | QSPI Buffer Control Register | SPBFCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E1Ah | QSPI | QSPI Buffer Data Count Set Register | SPBDCR | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E1Ch | QSPI | QSPI Transfer Data Length Multiplier Setting Register 0 | SPBMUL0 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E20h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 1 | SPBMUL1 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E24h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 2 | SPBMUL2 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E28h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 3 | SPBMUL3 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 A000h | SCI0 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A000h | SMCI0 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A001h | SCI0 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A002h | SCI0 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A002h | SMCI0 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A003h | SCI0 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A004h | SCI0 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A004h | SMCI0 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A005h | SCI0 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (22 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A006h | SCI0 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A006h | SMCI0 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A007h | SCI0 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A008h | SCI0 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A009h | SCI0 | I²C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A00Ah | SCI0 | I²C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A00Bh | SCI0 | I²C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A00Ch | SCI0 | I²C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A00Dh | SCI0 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A00Eh | SCI0 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A00Fh | SCI0 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A00Eh | SCI0 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A010h | SCI0 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A011h | SCI0 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A010h | SCI0 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A012h | SCI0 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A020h | SCI1 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A020h | SMCI1 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A021h | SCI1 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A022h | SCI1 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A022h | SMCI1 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A023h | SCI1 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A024h | SCI1 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (23 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A024h | SMCI1 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A025h | SCI1 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A026h | SCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A026h | SMCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A027h | SCI1 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A028h | SCI1 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A029h | SCI1 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A02Ah | SCI1 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A02Bh | SCI1 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A02Ch | SCI1 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A02Dh | SCI1 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A02Eh | SCI1 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A02Fh | SCI1 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A02Eh | SCI1 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A030h | SCI1 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A031h | SCI1 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A030h | SCI1 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A032h | SCI1 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A040h | SCI2 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A040h | SMCI2 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A041h | SCI2 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A042h | SCI2 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A042h | SMCI2 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (24 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A043h | SCI2 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A044h | SCI2 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A044h | SMCI2 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A045h | SCI2 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A046h | SCI2 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A046h | SMCI2 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A047h | SCI2 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A048h | SCI2 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A049h | SCI2 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A04Ah | SCI2 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A04Bh | SCI2 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A04Ch | SCI2 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A04Dh | SCI2 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A04Eh | SCI2 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A04Fh | SCI2 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A04Eh | SCI2 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A050h | SCI2 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A051h | SCI2 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A050h | SCI2 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A052h | SCI2 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A060h | SCI3 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A060h | SMCI3 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A061h | SCI3 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (25 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A062h | SCI3 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A062h | SMCI3 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A063h | SCI3 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A064h | SCI3 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A064h | SMCI3 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A065h | SCI3 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A066h | SCI3 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A066h | SMCI3 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A067h | SCI3 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A068h | SCI3 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A069h | SCI3 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A06Ah | SCI3 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A06Bh | SCI3 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A06Ch | SCI3 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A06Dh | SCI3 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A06Eh | SCI3 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A06Fh | SCI3 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A06Eh | SCI3 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A070h | SCI3 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A071h | SCI3 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A070h | SCI3 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A072h | SCI3 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A080h | SCI4 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (26 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A080h | SMCI4 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A081h | SCI4 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A082h | SCI4 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A082h | SMCI4 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A083h | SCI4 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A084h | SCI4 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A084h | SMCI4 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A085h | SCI4 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A086h | SCI4 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A086h | SMCI4 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A087h | SCI4 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A088h | SCI4 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A089h | SCI4 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A08Ah | SCI4 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A08Bh | SCI4 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A08Ch | SCI4 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A08Dh | SCI4 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A08Eh | SCI4 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A08Fh | SCI4 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A08Eh | SCI4 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A090h | SCI4 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A091h | SCI4 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A090h | SCI4 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (27 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A092h | SCI4 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A0h | SCI5 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A0h | SMCI5 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A1h | SCI5 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A2h | SCI5 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A2h | SMCI5 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A3h | SCI5 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A4h | SCI5 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A4h | SMCI5 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A5h | SCI5 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A6h | SCI5 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A6h | SMCI5 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A7h | SCI5 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A8h | SCI5 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0A9h | SCI5 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0AAh | SCI5 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0ABh | SCI5 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0ACh | SCI5 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0ADh | SCI5 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0AEh | SCI5 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0AFh | SCI5 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0AEh | SCI5 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0B0h | SCI5 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (28 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A0B1h | SCI5 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0B0h | SCI5 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0B2h | SCI5 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C0h | SCI6 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C0h | SMCI6 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C1h | SCI6 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C2h | SCI6 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C2h | SMCI6 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C3h | SCI6 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C4h | SCI6 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C4h | SMCI6 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C5h | SCI6 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C6h | SCI6 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C6h | SMCI6 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C7h | SCI6 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C8h | SCI6 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0C9h | SCI6 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0CAh | SCI6 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0CBh | SCI6 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0CCh | SCI6 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0CDh | SCI6 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0CEh | SCI6 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0CFh | SCI6 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (29 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A0CEh | SCI6 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0D0h | SCI6 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0D1h | SCI6 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0D0h | SCI6 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0D2h | SCI6 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E0h | SCI7 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E0h | SMCI7 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E1h | SCI7 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E2h | SCI7 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E2h | SMCI7 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E3h | SCI7 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E4h | SCI7 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E4h | SMCI7 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E5h | SCI7 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E6h | SCI7 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E6h | SMCI7 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E7h | SCI7 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E8h | SCI7 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0E9h | SCI7 | I²C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0EAh | SCI7 | I²C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0EBh | SCI7 | I²C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0ECh | SCI7 | I²C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0EDh | SCI7 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (30 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A0EEh | SCI7 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0EFh | SCI7 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0EEh | SCI7 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0F0h | SCI7 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0F1h | SCI7 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0F0h | SCI7 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A0F2h | SCI7 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A100h | SCI8 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A100h | SMCI8 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A101h | SCI8 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A102h | SCI8 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A102h | SMCI8 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A103h | SCI8 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A104h | SCI8 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A104h | SMCI8 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A105h | SCI8 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A106h | SCI8 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A106h | SMCI8 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A107h | SCI8 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A108h | SCI8 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A109h | SCI8 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A10Ah | SCI8 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A10Bh | SCI8 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (31 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A10Ch | SCI8 | I²C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A10Dh | SCI8 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A10Eh | SCI8 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A10Fh | SCI8 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A10Eh | SCI8 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A110h | SCI8 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A111h | SCI8 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A110h | SCI8 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A112h | SCI8 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A120h | SCI9 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A120h | SMCI9 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A121h | SCI9 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A122h | SCI9 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A122h | SMCI9 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A123h | SCI9 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A124h | SCI9 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A124h | SMCI9 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A125h | SCI9 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A126h | SCI9 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A126h | SMCI9 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A127h | SCI9 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A128h | SCI9 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A129h | SCI9 | I²C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (32 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A12Ah | SCI9 | I²C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A12Bh | SCI9 | I²C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A12Ch | SCI9 | I²C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A12Dh | SCI9 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A12Eh | SCI9 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A12Fh | SCI9 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A12Eh | SCI9 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A130h | SCI9 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A131h | SCI9 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A130h | SCI9 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A132h | SCI9 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 AC00h | SDHI | Command Register | SDCMD | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC08h | SDHI | Argument Register | SDARG | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC10h | SDHI | Data Stop Register | SDSTOP | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC14h | SDHI | Block Count Register | SDBLKCNT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC18h | SDHI | Response Register 10 | SDRSP10 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC20h | SDHI | Response Register 32 | SDRSP32 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC28h | SDHI | Response Register 54 | SDRSP54 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC30h | SDHI | Response Register 76 | SDRSP76 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC38h | SDHI | SD Status Register 1 | SDSTS1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC3Ch | SDHI | SD Status Register 2 | SDSTS2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC40h | SDHI | SD Interrupt Mask Register 1 | SDIMSK1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC44h | SDHI | SD Interrupt Mask Register 2 | SDIMSK2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC48h | SDHI | SDHI Clock Control Register | SDCLKCR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC4Ch | SDHI | Transfer Data Size Register | SDSIZE | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC50h | SDHI | Card Access Option Register | SDOPT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC58h | SDHI | SD Error Status Register 1 | SDERSTS1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC5Ch | SDHI | SD Error Status Register 2 | SDERSTS2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC60h | SDHI | SD Buffer Register | SDBUFR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC68h | SDHI | SDIO Mode Control Register | SDIOMD | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC6Ch | SDHI | SDIO Status Register | SDIOSTS | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 AC70h | SDHI | SDIO Interrupt Mask Register | SDIOIMSK | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 ADB0h | SDHI | DMA Transfer Enable Register | SDDMAEN | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 ADC0h | SDHI | SDHI Software Reset Register | SDRST | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 ADC4h | SDHI | Version Register | SDVER | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 ADE0h | SDHI | Swap Control Register | SDSWAP | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDHI |
| 0008 B000h | CAC | CAC Control Register 0 | CACR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |

**Table 4.1 List of I/O Registers (Address Order) (33 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 B001h | CAC | CAC Control Register 1 | CACR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B002h | CAC | CAC Control Register 2 | CACR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B003h | CAC | CAC Interrupt Request Enable Register | CAICR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B004h | CAC | CAC Status Register | CASTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B006h | CAC | CAC Upper-Limit Value Setting Register | CAULVR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B008h | CAC | CAC Lower-Limit Value Setting Register | CALLVR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B00Ah | CAC | CAC Counter Buffer Register | CACNTBR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B080h | DOC | DOC Control Register | DOCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | DOC |
| 0008 B082h | DOC | DOC Data Input Register | DODIR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | DOC |
| 0008 B084h | DOC | DOC Data Setting Register | DODSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | DOC |
| 0008 B100h | ELC | Event Link Control Register | ELCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B101h | ELC | Event Link Setting Register 0 | ELSR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B104h | ELC | Event Link Setting Register 3 | ELSR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B105h | ELC | Event Link Setting Register 4 | ELSR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B108h | ELC | Event Link Setting Register 7 | ELSR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B10Bh | ELC | Event Link Setting Register 10 | ELSR10 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B10Ch | ELC | Event Link Setting Register 11 | ELSR11 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B10Dh | ELC | Event Link Setting Register 12 | ELSR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B10Eh | ELC | Event Link Setting Register 13 | ELSR13 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B110h | ELC | Event Link Setting Register 15 | ELSR15 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B111h | ELC | Event Link Setting Register 16 | ELSR16 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B113h | ELC | Event Link Setting Register 18 | ELSR18 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B114h | ELC | Event Link Setting Register 19 | ELSR19 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B115h | ELC | Event Link Setting Register 20 | ELSR20 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B116h | ELC | Event Link Setting Register 21 | ELSR21 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B117h | ELC | Event Link Setting Register 22 | ELSR22 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B118h | ELC | Event Link Setting Register 23 | ELSR23 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B119h | ELC | Event Link Setting Register 24 | ELSR24 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Ah | ELC | Event Link Setting Register 25 | ELSR25 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Bh | ELC | Event Link Setting Register 26 | ELSR26 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Ch | ELC | Event Link Setting Register 27 | ELSR27 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Dh | ELC | Event Link Setting Register 28 | ELSR28 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Fh | ELC | Event Link Option Setting Register A | ELOPA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B120h | ELC | Event Link Option Setting Register B | ELOPB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B121h | ELC | Event Link Option Setting Register C | ELOPC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B122h | ELC | Event Link Option Setting Register D | ELOPD | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B123h | ELC | Port Group Setting Register 1 | PGR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B124h | ELC | Port Group Setting Register 2 | PGR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B125h | ELC | Port Group Control Register 1 | PGC1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B126h | ELC | Port Group Control Register 2 | PGC2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B127h | ELC | Port Buffer Register 1 | PDBF1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B128h | ELC | Port Buffer Register 2 | PDBF2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B129h | ELC | Event Link Port Setting Register 0 | PEL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Ah | ELC | Event Link Port Setting Register 1 | PEL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Bh | ELC | Event Link Port Setting Register 2 | PEL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Ch | ELC | Event Link Port Setting Register 3 | PEL3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Dh | ELC | Event Link Software Event Generation Register | ELSEGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B131h | ELC | Event Link Setting Register 33 | ELSR33 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B133h | ELC | Event Link Setting Register 35 | ELSR35 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B134h | ELC | Event Link Setting Register 36 | ELSR36 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |

**Table 4.1 List of I/O Registers (Address Order) (34 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 B135h | ELC | Event Link Setting Register 37 | ELSR37 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B136h | ELC | Event Link Setting Register 38 | ELSR38 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B13Dh | ELC | Event Link Setting Register 45 | ELSR45 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B13Fh | ELC | Event Link Option Setting Register F | ELOPF | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B141h | ELC | Event Link Option Setting Register H | ELOPH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B300h | SCI12 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B300h | SMCI12 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B301h | SCI12 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B302h | SCI12 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B302h | SMCI12 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B303h | SCI12 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B304h | SCI12 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B304h | SMCI12 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B305h | SCI12 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B306h | SCI12 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B306h | SMCI12 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B307h | SCI12 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B308h | SCI12 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B309h | SCI12 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B30Ah | SCI12 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B30Bh | SCI12 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B30Ch | SCI12 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B30Dh | SCI12 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B30Eh | SCI12 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B30Fh | SCI12 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B30Eh | SCI12 | Transmit Data Register HL | TDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIh |
| 0008 B310h | SCI12 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B311h | SCI12 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B310h | SCI12 | Receive Data Register HL | RDRHL | 16 | 16 | 4, 5 PCLKB | 2 ICLK | SCIh |
| 0008 B312h | SCI12 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B320h | SCI12 | Extended Serial Module Enable Register | ESMER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B321h | SCI12 | Control Register 0 | CR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B322h | SCI12 | Control Register 1 | CR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B323h | SCI12 | Control Register 2 | CR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B324h | SCI12 | Control Register 3 | CR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B325h | SCI12 | Port Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B326h | SCI12 | Interrupt Control Register | ICR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B327h | SCI12 | Status Register | STR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B328h | SCI12 | Status Clear Register | STCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B329h | SCI12 | Control Field 0 Data Register | CF0DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B32Ah | SCI12 | Control Field 0 Compare Enable Register | CF0CR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B32Bh | SCI12 | Control Field 0 Receive Data Register | CF0RR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B32Ch | SCI12 | Primary Control Field 1 Data Register | PCF1DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B32Dh | SCI12 | Secondary Control Field 1 Data Register | SCF1DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B32Eh | SCI12 | Control Field 1 Compare Enable Register | CF1CR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B32Fh | SCI12 | Control Field 1 Receive Data Register | CF1RR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B330h | SCI12 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B331h | SCI12 | Timer Mode Register | TMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B332h | SCI12 | Timer Prescaler Register | TPRE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |
| 0008 B333h | SCI12 | Timer Count Register | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIh |

**Table 4.1 List of I/O Registers (Address Order) (35 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C000h | PORT0 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C001h | PORT1 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C002h | PORT2 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C003h | PORT3 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C004h | PORT4 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C005h | PORT5 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C006h | PORT6 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C007h | PORT7 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C008h | PORT8 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C009h | PORT9 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Ah | PORTA | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Bh | PORTB | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Ch | PORTC | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Dh | PORTD | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Eh | PORTE | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Fh | PORTF | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C010h | PORTG | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C012h | PORTJ | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C020h | PORT0 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C021h | PORT1 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C022h | PORT2 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C023h | PORT3 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C024h | PORT4 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C025h | PORT5 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C026h | PORT6 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C027h | PORT7 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C028h | PORT8 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C029h | PORT9 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Ah | PORTA | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Bh | PORTB | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Ch | PORTC | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Dh | PORTD | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Eh | PORTE | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Fh | PORTF | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C030h | PORTG | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C032h | PORTJ | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C040h | PORT0 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C041h | PORT1 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C042h | PORT2 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C043h | PORT3 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C044h | PORT4 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C045h | PORT5 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C046h | PORT6 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C047h | PORT7 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C048h | PORT8 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C049h | PORT9 | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Ah | PORTA | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Bh | PORTB | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Ch | PORTC | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Dh | PORTD | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |

**Table 4.1 List of I/O Registers (Address Order) (36 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C04Eh | PORTE | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C04Fh | PORTF | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C050h | PORTG | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C052h | PORTJ | Port Input Register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C060h | PORT0 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C061h | PORT1 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C062h | PORT2 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C063h | PORT3 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C064h | PORT4 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C065h | PORT5 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C066h | PORT6 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C067h | PORT7 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C068h | PORT8 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C069h | PORT9 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Ah | PORTA | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Bh | PORTB | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Ch | PORTC | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Dh | PORTD | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Eh | PORTE | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Fh | PORTF | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C070h | PORTG | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C072h | PORTJ | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C080h | PORT0 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C081h | PORT0 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C082h | PORT1 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C083h | PORT1 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C084h | PORT2 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C085h | PORT2 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C086h | PORT3 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C087h | PORT3 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C088h | PORT4 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C089h | PORT4 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ah | PORT5 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Bh | PORT5 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ch | PORT6 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Dh | PORT6 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Eh | PORT7 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Fh | PORT7 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C090h | PORT8 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C091h | PORT8 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C092h | PORT9 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C093h | PORT9 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C094h | PORTA | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C095h | PORTA | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C096h | PORTB | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C097h | PORTB | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C098h | PORTC | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C099h | PORTC | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Ah | PORTD | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Bh | PORTD | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |

**Table 4.1 List of I/O Registers (Address Order) (37 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C09Ch | PORTE | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Dh | PORTE | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Eh | PORTF | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Fh | PORTF | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A0h | PORTG | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A1h | PORTG | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A4h | PORTJ | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A5h | PORTJ | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C0h | PORT0 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C1h | PORT1 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C2h | PORT2 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C3h | PORT3 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C4h | PORT4 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C5h | PORT5 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C6h | PORT6 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C7h | PORT7 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C8h | PORT8 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C9h | PORT9 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CAh | PORTA | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CBh | PORTB | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CCh | PORTC | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CDh | PORTD | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CEh | PORTE | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CFh | PORTF | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0D0h | PORTG | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0D2h | PORTJ | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E0h | PORT0 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E1h | PORT1 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E2h | PORT2 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E5h | PORT5 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E7h | PORT7 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E8h | PORT8 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E9h | PORT9 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EAh | PORTA | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EBh | PORTB | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0ECh | PORTC | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EDh | PORTD | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EEh | PORTE | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0F0h | PORTG | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0F2h | PORTJ | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C100h | MPC | CS Output Enable Register | PFCSE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C102h | MPC | CS Output Pin Select Register 0 | PFCSS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C103h | MPC | CS Output Pin Select Register 1 | PFCSS1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C104h | MPC | Address Output Enable Register 0 | PFAOE0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C105h | MPC | Address Output Enable Register 1 | PFAOE1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C106h | MPC | External Bus Control Register 0 | PFBCR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C107h | MPC | External Bus Control Register 1 | PFBCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C108h | MPC | External Bus Control Register 2 | PFBCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C109h | MPC | External Bus Control Register 3 | PFBCR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C10Eh | MPC | Ethernet Control Register | PFENET | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |

**Table 4.1 List of I/O Registers (Address Order) (38 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C11Fh | MPC | Write-Protect Register | PWPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C128h | PORT0 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C129h | PORT1 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C12Ah | PORT2 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C12Bh | PORT3 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C12Dh | PORT5 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C12Fh | PORT7 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C130h | PORT8 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C131h | PORT9 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C132h | PORTA | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C133h | PORTB | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C134h | PORTC | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C135h | PORTD | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C136h | PORTE | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C138h | PORTG | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C13Ah | PORTJ | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C140h | MPC | P00 Pin Function Control Register | P00PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C141h | MPC | P01 Pin Function Control Register | P01PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C142h | MPC | P02 Pin Function Control Register | P02PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C143h | MPC | P03 Pin Function Control Register | P03PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C145h | MPC | P05 Pin Function Control Register | P05PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C147h | MPC | P07 Pin Function Control Register | P07PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C148h | MPC | P10 Pin Function Control Register | P10PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C149h | MPC | P11 Pin Function Control Register | P11PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Ah | MPC | P12 Pin Function Control Register | P12PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Bh | MPC | P13 Pin Function Control Register | P13PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Ch | MPC | P14 Pin Function Control Register | P14PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Dh | MPC | P15 Pin Function Control Register | P15PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Eh | MPC | P16 Pin Function Control Register | P16PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Fh | MPC | P17 Pin Function Control Register | P17PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C150h | MPC | P20 Pin Function Control Register | P20PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C151h | MPC | P21 Pin Function Control Register | P21PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C152h | MPC | P22 Pin Function Control Register | P22PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C153h | MPC | P23 Pin Function Control Register | P23PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C154h | MPC | P24 Pin Function Control Register | P24PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C155h | MPC | P25 Pin Function Control Register | P25PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C156h | MPC | P26 Pin Function Control Register | P26PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C157h | MPC | P27 Pin Function Control Register | P27PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C158h | MPC | P30 Pin Function Control Register | P30PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C159h | MPC | P31 Pin Function Control Register | P31PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Ah | MPC | P32 Pin Function Control Register | P32PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Bh | MPC | P33 Pin Function Control Register | P33PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Ch | MPC | P34 Pin Function Control Register | P34PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C160h | MPC | P40 Pin Function Control Register | P40PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C161h | MPC | P41 Pin Function Control Register | P41PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C162h | MPC | P42 Pin Function Control Register | P42PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C163h | MPC | P43 Pin Function Control Register | P43PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C164h | MPC | P44 Pin Function Control Register | P44PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C165h | MPC | P45 Pin Function Control Register | P45PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C166h | MPC | P46 Pin Function Control Register | P46PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |

**Table 4.1 List of I/O Registers (Address Order) (39 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C167h | MPC | P47 Pin Function Control Register | P47PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C168h | MPC | P50 Pin Function Control Register | P50PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C169h | MPC | P51 Pin Function Control Register | P51PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Ah | MPC | P52 Pin Function Control Register | P52PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Ch | MPC | P54 Pin Function Control Register | P54PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Dh | MPC | P55 Pin Function Control Register | P55PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Eh | MPC | P56 Pin Function Control Register | P56PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Fh | MPC | P57 Pin Function Control Register | P57PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C176h | MPC | P66 Pin Function Control Register | P66PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C177h | MPC | P67 Pin Function Control Register | P67PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C179h | MPC | P71 Pin Function Control Register | P71PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Ah | MPC | P72 Pin Function Control Register | P72PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Bh | MPC | P73 Pin Function Control Register | P73PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Ch | MPC | P74 Pin Function Control Register | P74PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Dh | MPC | P75 Pin Function Control Register | P75PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Eh | MPC | P76 Pin Function Control Register | P76PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Fh | MPC | P77 Pin Function Control Register | P77PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C180h | MPC | P80 Pin Function Control Register | P80PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C181h | MPC | P81 Pin Function Control Register | P81PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C182h | MPC | P82 Pin Function Control Register | P82PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C183h | MPC | P83 Pin Function Control Register | P83PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C184h | MPC | P84 Pin Function Control Register | P84PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C185h | MPC | P85 Pin Function Control Register | P85PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C186h | MPC | P86 Pin Function Control Register | P86PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C187h | MPC | P87 Pin Function Control Register | P87PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C188h | MPC | P90 Pin Function Control Register | P90PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C189h | MPC | P91 Pin Function Control Register | P91PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C18Ah | MPC | P92 Pin Function Control Register | P92PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C18Bh | MPC | P93 Pin Function Control Register | P93PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C190h | MPC | PA0 Pin Function Control Register | PA0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C191h | MPC | PA1 Pin Function Control Register | PA1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C192h | MPC | PA2 Pin Function Control Register | PA2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C193h | MPC | PA3 Pin Function Control Register | PA3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C194h | MPC | PA4 Pin Function Control Register | PA4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C195h | MPC | PA5 Pin Function Control Register | PA5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C196h | MPC | PA6 Pin Function Control Register | PA6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C197h | MPC | PA7 Pin Function Control Register | PA7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C198h | MPC | PB0 Pin Function Control Register | PB0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C199h | MPC | PB1 Pin Function Control Register | PB1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Ah | MPC | PB2 Pin Function Control Register | PB2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Bh | MPC | PB3 Pin Function Control Register | PB3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Ch | MPC | PB4 Pin Function Control Register | PB4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Dh | MPC | PB5 Pin Function Control Register | PB5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Eh | MPC | PB6 Pin Function Control Register | PB6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Fh | MPC | PB7 Pin Function Control Register | PB7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A0h | MPC | PC0 Pin Function Control Register | PC0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A1h | MPC | PC1 Pin Function Control Register | PC1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A2h | MPC | PC2 Pin Function Control Register | PC2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A3h | MPC | PC3 Pin Function Control Register | PC3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A4h | MPC | PC4 Pin Function Control Register | PC4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |

**Table 4.1 List of I/O Registers (Address Order) (40 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C1A5h | MPC | PC5 Pin Function Control Register | PC5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A6h | MPC | PC6 Pin Function Control Register | PC6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A7h | MPC | PC7 Pin Function Control Register | PC7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A8h | MPC | PD0 Pin Function Control Register | PD0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A9h | MPC | PD1 Pin Function Control Register | PD1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1AAh | MPC | PD2 Pin Function Control Register | PD2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1ABh | MPC | PD3 Pin Function Control Register | PD3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1ACh | MPC | PD4 Pin Function Control Register | PD4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1ADh | MPC | PD5 Pin Function Control Register | PD5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1AEh | MPC | PD6 Pin Function Control Register | PD6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1AFh | MPC | PD7 Pin Function Control Register | PD7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B0h | MPC | PE0 Pin Function Control Register | PE0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B1h | MPC | PE1 Pin Function Control Register | PE1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B2h | MPC | PE2 Pin Function Control Register | PE2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B3h | MPC | PE3 Pin Function Control Register | PE3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B4h | MPC | PE4 Pin Function Control Register | PE4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B5h | MPC | PE5 Pin Function Control Register | PE5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B6h | MPC | PE6 Pin Function Control Register | PE6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B7h | MPC | PE7 Pin Function Control Register | PE7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B8h | MPC | PF0 Pin Function Control Register | PF0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B9h | MPC | PF1 Pin Function Control Register | PF1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1BAh | MPC | PF2 Pin Function Control Register | PF2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1BDh | MPC | PF5 Pin Function Control Register | PF5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1D0h | MPC | PJ0 Pin Function Control Register | PJ0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1D1h | MPC | PJ1 Pin Function Control Register | PJ1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1D2h | MPC | PJ2 Pin Function Control Register | PJ2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1D3h | MPC | PJ3 Pin Function Control Register | PJ3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1D5h | MPC | PJ5 Pin Function Control Register | PJ5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C280h | SYSTEM | Deep Standby Control Register | DPSBYCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C282h | SYSTEM | Deep Standby Interrupt Enable Register 0 | DPSIER0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C283h | SYSTEM | Deep Standby Interrupt Enable Register 1 | DPSIER1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C284h | SYSTEM | Deep Standby Interrupt Enable Register 2 | DPSIER2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C285h | SYSTEM | Deep Standby Interrupt Enable Register 3 | DPSIER3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C286h | SYSTEM | Deep Standby Interrupt Flag Register 0 | DPSIFR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C287h | SYSTEM | Deep Standby Interrupt Flag Register 1 | DPSIFR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C288h | SYSTEM | Deep Standby Interrupt Flag Register 2 | DPSIFR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |

**Table 4.1 List of I/O Registers (Address Order) (41 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C289h | SYSTEM | Deep Standby Interrupt Flag Register 3 | DPSIFR3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Ah | SYSTEM | Deep Standby Interrupt Edge Register 0 | DPSIEGR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Bh | SYSTEM | Deep Standby Interrupt Edge Register 1 | DPSIEGR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Ch | SYSTEM | Deep Standby Interrupt Edge Register 2 | DPSIEGR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Dh | SYSTEM | Deep Standby Interrupt Edge Register 3 | DPSIEGR3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C290h | SYSTEM | Reset Status Register 0 | RSTSR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Resets |
| 0008 C291h | SYSTEM | Reset Status Register 1 | RSTSR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Resets |
| 0008 C293h | SYSTEM | Main Clock Oscillator Forced Oscillation Control Register | MOFCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Clock Generation Circuit |
| 0008 C294h | SYSTEM | High-Speed On-Chip Oscillator Power Supply Control Register | HOCOPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Clock Generation Circuit |
| 0008 C296h | FLASH | Flash P/E Protect Register | FWEPROR | 8 | 8 | 2 ICLK | | Flash |
| 0008 C297h | SYSTEM | Voltage Monitoring Circuit Control Register | LVCMPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C298h | SYSTEM | Voltage Detection Level Select Register | LVDLVLR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C29Ah | SYSTEM | Voltage Monitoring 1 Circuit Control Register 0 | LVD1CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C29Bh | SYSTEM | Voltage Monitoring 2 Circuit Control Register 0 | LVD2CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C2A0h to 0008 C2BFh | SYSTEM | Deep Standby Backup Register 0 to Deep Standby Backup Register 31 | DPSBKR0 to DPSBKR31 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C400h | RTC | 64-Hz Counter | R64CNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C402h | RTC | Second Counter | RSECCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C402h | RTC | Binary Counter 0 | BCNT0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C404h | RTC | Minute Counter | RMINCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C404h | RTC | Binary Counter 1 | BCNT1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C406h | RTC | Hour Counter | RHRCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C406h | RTC | Binary Counter 2 | BCNT2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C408h | RTC | Day-of-Week Counter | RWKCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C408h | RTC | Binary Counter 3 | BCNT3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C40Ah | RTC | Date Counter | RDAYCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C40Ch | RTC | Month Counter | RMONCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C40Eh | RTC | Year Counter | RYRCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C410h | RTC | Second Alarm Register | RSECAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C410h | RTC | Binary Counter 0 Alarm Register | BCNT0AR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C412h | RTC | Minute Alarm Register | RMINAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C412h | RTC | Binary Counter 1 Alarm Register | BCNT1AR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C414h | RTC | Hour Alarm Register | RHRAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C414h | RTC | Binary Counter 2 Alarm Register | BCNT2AR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C416h | RTC | Day-of-Week Alarm Register | RWKAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |

**Table 4.1 List of I/O Registers (Address Order) (42 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C416h | RTC | Binary Counter 3 Alarm Register | BCNT3AR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C418h | RTC | Date Alarm Register | RDAYAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C418h | RTC | Binary Counter 0 Alarm Enable Register | BCNT0AER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Ah | RTC | Month Alarm Register | RMONAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Ah | RTC | Binary Counter 1 Alarm Enable Register | BCNT1AER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Ch | RTC | Year Alarm Register | RYRAR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Ch | RTC | Binary Counter 2 Alarm Enable Register | BCNT2AER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Eh | RTC | Year Alarm Enable Register | RYRAREN | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C41Eh | RTC | Binary Counter 3 Alarm Enable Register | BCNT3AER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C422h | RTC | RTC Control Register 1 | RCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C424h | RTC | RTC Control Register 2 | RCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C426h | RTC | RTC Control Register 3 | RCR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C428h | RTC | RTC Control Register 4 | RCR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C42Ah | RTC | Frequency Register H | RFRH | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C42Ch | RTC | Frequency Register L | RFRL | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C42Eh | RTC | Time Error Adjustment Register | RADJ | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C440h | RTC | Time Capture Control Register 0 | RTCCR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C442h | RTC | Time Capture Control Register 1 | RTCCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C444h | RTC | Time Capture Control Register 2 | RTCCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C452h | RTC | Second Capture Register 0 | RSECCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C452h | RTC | BCNT0 Capture Register 0 | BCNT0CP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C454h | RTC | Minute Capture Register 0 | RMINCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C454h | RTC | BCNT1 Capture Register 0 | BCNT1CP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C456h | RTC | Hour Capture Register 0 | RHRCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C456h | RTC | BCNT2 Capture Register 0 | BCNT2CP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C45Ah | RTC | Date Capture Register 0 | RDAYCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C45Ah | RTC | BCNT3 Capture Register 0 | BCNT3CP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C45Ch | RTC | Month Capture Register 0 | RMONCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C462h | RTC | Second Capture Register 1 | RSECCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C462h | RTC | BCNT0 Capture Register 1 | BCNT0CP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C464h | RTC | Minute Capture Register 1 | RMINCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C464h | RTC | BCNT1 Capture Register 1 | BCNT1CP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C466h | RTC | Hour Capture Register 1 | RHRCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C466h | RTC | BCNT2 Capture Register 1 | BCNT2CP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C46Ah | RTC | Date Capture Register 1 | RDAYCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C46Ah | RTC | BCNT3 Capture Register 1 | BCNT3CP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C46Ch | RTC | Month Capture Register 1 | RMONCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C472h | RTC | Second Capture Register 2 | RSECCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C472h | RTC | BCNT0 Capture Register 2 | BCNT0CP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C474h | RTC | Minute Capture Register 2 | RMINCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C474h | RTC | BCNT1 Capture Register 2 | BCNT1CP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C476h | RTC | Hour Capture Register 2 | RHRCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C476h | RTC | BCNT2 Capture Register 2 | BCNT2CP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C47Ah | RTC | Date Capture Register 2 | RDAYCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C47Ah | RTC | BCNT3 Capture Register 2 | BCNT3CP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C47Ch | RTC | Month Capture Register 2 | RMONCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCd |
| 0008 C4C0h | POE3 | Input Level Control/Status Register 1 | ICSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4C2h | POE3 | Output Level Control/Status Register 1 | OCSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4C4h | POE3 | Input Level Control/Status Register 2 | ICSR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4C6h | POE3 | Output Level Control/Status Register 2 | OCSR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |

**Table 4.1 List of I/O Registers (Address Order) (43 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C4C8h | POE3 | Input Level Control/Status Register 3 | ICSR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4CAh | POE3 | Software Port Output Enable Register | SPOER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4CBh | POE3 | Port Output Enable Control Register 1 | POECR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4CCh | POE3 | Port Output Enable Control Register 2 | POECR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4D0h | POE3 | Port Output Enable Control Register 4 | POECR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4D2h | POE3 | Port Output Enable Control Register 5 | POECR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4D6h | POE3 | Input Level Control/Status Register 4 | ICSR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4D8h | POE3 | Input Level Control/Status Register 5 | ICSR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4DAh | POE3 | Active Level Setting Register 1 | ALR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4DCh | POE3 | Input Level Control/Status Register 6 | ICSR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4E4h | POE3 | MTU0 Pin Select Register 1 | M0SELR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4E5h | POE3 | MTU0 Pin Select Register 2 | M0SELR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4E6h | POE3 | MTU3 Pin Select Register | M3SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4E7h | POE3 | MTU4 Pin Select Register 1 | M4SELR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4E8h | POE3 | MTU4 Pin Select Register 2 | M4SELR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C4EAh | POE3 | MTU6 Pin Select Register | M6SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3a |
| 0008 C500h | TEMPS | Temperature Sensor Control Register | TSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TEMPS |
| 0008 C5C0h | DA | D/A A/D Synchronous Unit Select Register | DAADUSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0009 0200h to 0009 03FFh | CAN0 | Mailbox Register 0 to Mailbox Register 31 | MB0 to MB31 | 128 | 8, 16, 32*2 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0400h to 0009 041Fh | CAN0 | Mask Register 0 to Mask Register 7 | MKR0 to MKR7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0420h | CAN0 | FIFO Received ID Compare Register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0424h | CAN0 | FIFO Received ID Compare Register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0428h | CAN0 | Mask Invalid Register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 042Ch | CAN0 | Mailbox Interrupt Enable Register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0820h to 0009 083Fh | CAN0 | Message Control Register 0 to Message Control Register 31 | MCTL0 to MCTL31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0840h | CAN0 | Control Register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0842h | CAN0 | Status Register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0844h | CAN0 | Bit Configuration Register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0848h | CAN0 | Receive FIFO Control Register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0849h | CAN0 | Receive FIFO Pointer Control Register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Ah | CAN0 | Transmit FIFO Control Register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Bh | CAN0 | Transmit FIFO Pointer Control Register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Ch | CAN0 | Error Interrupt Enable Register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Dh | CAN0 | Error Interrupt Factor Judge Register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Eh | CAN0 | Receive Error Count Register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Fh | CAN0 | Transmit Error Count Register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0850h | CAN0 | Error Code Store Register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0851h | CAN0 | Channel Search Support Register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0852h | CAN0 | Mailbox Search Status Register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0853h | CAN0 | Mailbox Search Mode Register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0854h | CAN0 | Time Stamp Register | TSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0856h | CAN0 | Acceptance Filter Support Register | AFSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0858h | CAN0 | Test Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1200h to 0009 13FFh | CAN1 | Mailbox Register 0 to Mailbox Register 31 | MB0 to MB31 | 128 | 8, 16, 32*2 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1400h to 0009 141Fh | CAN1 | Mask Register 0 to Mask Register 7 | MKR0 to MKR7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |

**Table 4.1 List of I/O Registers (Address Order) (44 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 1420h | CAN1 | FIFO Received ID Compare Register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1424h | CAN1 | FIFO Received ID Compare Register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1428h | CAN1 | Mask Invalid Register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 142Ch | CAN1 | Mailbox Interrupt Enable Register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1820h to 0009 183Fh | CAN1 | Message Control Register 0 to Message Control Register 31 | MCTL0 to MCTL31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1840h | CAN1 | Control Register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1842h | CAN1 | Status Register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1844h | CAN1 | Bit Configuration Register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1848h | CAN1 | Receive FIFO Control Register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1849h | CAN1 | Receive FIFO Pointer Control Register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Ah | CAN1 | Transmit FIFO Control Register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Bh | CAN1 | Transmit FIFO Pointer Control Register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Ch | CAN1 | Error Interrupt Enable Register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Dh | CAN1 | Error Interrupt Factor Judge Register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Eh | CAN1 | Receive Error Count Register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Fh | CAN1 | Transmit Error Count Register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1850h | CAN1 | Error Code Store Register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1851h | CAN1 | Channel Search Support Register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1852h | CAN1 | Mailbox Search Status Register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1853h | CAN1 | Mailbox Search Mode Register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1854h | CAN1 | Time Stamp Register | TSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1856h | CAN1 | Acceptance Filter Support Register | AFSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1858h | CAN1 | Test Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 4200h | CMTW0 | Timer Start Register | CMWSTR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4204h | CMTW0 | Timer Control Register | CMWCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4208h | CMTW0 | Timer I/O Control Register | CMWIOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4210h | CMTW0 | Timer Counter | CMWCNT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4214h | CMTW0 | Compare Match Constant Register | CMWCOR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4218h | CMTW0 | Input Capture Register 0 | CMWICR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 421Ch | CMTW0 | Input Capture Register 1 | CMWICR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4220h | CMTW0 | Output Compare Register 0 | CMWOCR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4224h | CMTW0 | Output Compare Register 1 | CMWOCR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4280h | CMTW1 | Timer Start Register | CMWSTR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4284h | CMTW1 | Timer Control Register | CMWCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4288h | CMTW1 | Timer I/O Control Register | CMWIOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4290h | CMTW1 | Timer Counter | CMWCNT | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4294h | CMTW1 | Compare Match Constant Register | CMWCOR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 4298h | CMTW1 | Input Capture Register 0 | CMWICR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 429Ch | CMTW1 | Input Capture Register 1 | CMWICR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 42A0h | CMTW1 | Output Compare Register 0 | CMWOCR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 42A4h | CMTW1 | Output Compare Register 1 | CMWOCR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 5000h | SDSI | FN1 Access Control Register | FN1ACCR | 32 | 32 | 10, 11 PCLKB | 2 to 6 ICLK | SDSI |
| 0009 5004h | SDSI | Interrupt Enable Control Register 1 | INTENCR1 | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 5005h | SDSI | Interrupt Status Register 1 | INTSR1 | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 5006h | SDSI | SD Command Control Register | SDCMDCR | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 5007h | SDSI | SD Command Access Address 0 Register | SDCADD0R | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 5008h | SDSI | SD Command Access Address 1 Register | SDCADD1R | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |

**Table 4.1 List of I/O Registers (Address Order) (45 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 5009h | SDSI | SD Command Access Address 2 Register | SDCADD2R | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 500Ah | SDSI | SDSI Control Register 1 | SDSICR1 | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 500Bh | SDSI | DMA Control Register 1 | DMACR1 | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 500Ch | SDSI | Block Counter | BLKCNT | 16 | 16 | 8, 9 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 500Eh | SDSI | Byte Counter | BYTCNT | 16 | 16 | 8, 9 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 5010h | SDSI | DMA Transfer Address Register | DMATRADDR | 32 | 32 | 10, 11 PCLKB | 2 to 6 ICLK | SDSI |
| 0009 5100h | SDSI | SDSI Control Register 2 | SDSICR2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5104h | SDSI | SDSI Control Register 3 | SDSICR3 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5108h | SDSI | Interrupt Enable Control Register 2 | INTENCR2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 510Ch | SDSI | Interrupt Status Register 2 | INTSR2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5110h | SDSI | DMA Control Register 2 | DMACR2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5200h to 0009 526Bh | SDSI | CIS Data Register 0 to 26 | CISDATAR0 to 26 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5270h | SDSI | FBR Setting Register 1 | FBR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5274h | SDSI | FBR Setting Register 2 | FBR2 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5278h | SDSI | FBR Setting Register 3 | FBR3 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 527Ch | SDSI | FBR Setting Register 4 | FBR4 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5280h | SDSI | FBR Setting Register 5 | FBR5 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | SDSI |
| 0009 5800h to 0009 58FFh | SDSI | FN1 Data Register 10 to 163 | FN1DATAR10 to 163 | 32 | 8, 32 | 10, 11 PCLKB | 2 to 6 ICLK | SDSI |
| 0009 5900h to 0009 59FFh | SDSI | FN1 Data Register 20 to 263 | FN1DATAR20 to 263 | 32 | 8, 32 | 10, 11 PCLKB | 2 to 6 ICLK | SDSI |
| 0009 5A00h to 0009 5AFFh | SDSI | FN1 Data Register 30 to 363 | FN1DATAR30 to 363 | 32 | 8, 32 | 10, 11 PCLKB | 2 to 6 ICLK | SDSI |
| 0009 5B00h | SDSI | FN1 Interrupt Vector Register | FN1INTVECR | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 5B01h | SDSI | FN1 Interrupt Clear Register | FN1INTCLRR | 8 | 8 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 0009 5C00h to 0009 5FFFh | SDSI | FN1 Data Register 50 to 5255 | FN1DATAR50 to 5255 | 32 | 8, 32 | 7, 8 PCLKB | 2 to 5 ICLK | SDSI |
| 000A 0000h | USB0 | System Configuration Control Register | SYSCFG | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0004h | USB0 | System Configuration Status Register 0 | SYSSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0008h | USB0 | Device State Control Register 0 | DVSTCTR0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0014h | USB0 | CFIFO Port Register | CFIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0018h | USB0 | D0FIFO Port Register | D0FIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 001Ch | USB0 | D1FIFO Port Register | D1FIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0020h | USB0 | CFIFO Port Select Register | CFIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0022h | USB0 | CFIFO Port Control Register | CFIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0028h | USB0 | D0FIFO Port Select Register | D0FIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Ah | USB0 | D0FIFO Port Control Register | D0FIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Ch | USB0 | D1FIFO Port Select Register | D1FIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Eh | USB0 | D1FIFO Port Control Register | D1FIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0030h | USB0 | Interrupt Enable Register 0 | INTENB0 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0032h | USB0 | Interrupt Enable Register 1 | INTENB1 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0036h | USB0 | BRDY Interrupt Enable Register | BRDYENB | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0038h | USB0 | NRDY Interrupt Enable Register | NRDYENB | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |

**Table 4.1 List of I/O Registers (Address Order) (46 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000A 003Ah | USB0 | BEMP Interrupt Enable Register | BEMPENB | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 003Ch | USB0 | SOF Output Configuration Register | SOFCFG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0040h | USB0 | Interrupt Status Register 0 | INTSTS0 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0042h | USB0 | Interrupt Status Register 1 | INTSTS1 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0046h | USB0 | BRDY Interrupt Status Register | BRDYSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0048h | USB0 | NRDY Interrupt Status Register | NRDYSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 004Ah | USB0 | BEMP Interrupt Status Register | BEMPSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 004Ch | USB0 | Frame Number Register | FRMNUM | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 004Eh | USB0 | Device State Change Register | DVCHGR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0050h | USB0 | USB Address Register | USBADDR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0054h | USB0 | USB Request Type Register | USBREQ | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0056h | USB0 | USB Request Value Register | USBVAL | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0058h | USB0 | USB Request Index Register | USBINDX | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 005Ah | USB0 | USB Request Length Register | USBLENG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 005Ch | USB0 | DCP Configuration Register | DCPCFG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 005Eh | USB0 | DCP Maximum Packet Size Register | DCPMAXP | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0060h | USB0 | DCP Control Register | DCPCTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0064h | USB0 | Pipe Window Select Register | PIPESEL | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0068h | USB0 | Pipe Configuration Register | PIPECFG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 006Ch | USB0 | Pipe Maximum Packet Size Register | PIPEMAXP | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 006Eh | USB0 | Pipe Cycle Control Register | PIPEPERI | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0070h | USB0 | PIPE1 Control Register | PIPE1CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0072h | USB0 | PIPE2 Control Register | PIPE2CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0074h | USB0 | PIPE3 Control Register | PIPE3CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0076h | USB0 | PIPE4 Control Register | PIPE4CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0078h | USB0 | PIPE5 Control Register | PIPE5CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |

**Table 4.1 List of I/O Registers (Address Order) (47 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000A 007Ah | USB0 | PIPE6 Control Register | PIPE6CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 007Ch | USB0 | PIPE7 Control Register | PIPE7CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 007Eh | USB0 | PIPE8 Control Register | PIPE8CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0080h | USB0 | PIPE9 Control Register | PIPE9CTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0090h | USB0 | PIPE1 Transaction Counter Enable Register | PIPE1TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0092h | USB0 | PIPE1 Transaction Counter Register | PIPE1TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0094h | USB0 | PIPE2 Transaction Counter Enable Register | PIPE2TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0096h | USB0 | PIPE2 Transaction Counter Register | PIPE2TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0098h | USB0 | PIPE3 Transaction Counter Enable Register | PIPE3TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 009Ah | USB0 | PIPE3 Transaction Counter Register | PIPE3TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 009Ch | USB0 | PIPE4 Transaction Counter Enable Register | PIPE4TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 009Eh | USB0 | PIPE4 Transaction Counter Register | PIPE4TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00A0h | USB0 | PIPE5 Transaction Counter Enable Register | PIPE5TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00A2h | USB0 | PIPE5 Transaction Counter Register | PIPE5TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00D0h | USB0 | Device Address 0 Configuration Register | DEVADD0 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00D2h | USB0 | Device Address 1 Configuration Register | DEVADD1 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00D4h | USB0 | Device Address 2 Configuration Register | DEVADD2 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00D6h | USB0 | Device Address 3 Configuration Register | DEVADD3 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00D8h | USB0 | Device Address 4 Configuration Register | DEVADD4 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00DAh | USB0 | Device Address 5 Configuration Register | DEVADD5 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 00F0h | USB0 | PHY Cross Point Adjustment Register | PHYSLEW | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0400h | USB | Deep Standby USB Transceiver Control/Pin Monitoring Register | DPUSR0R | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0404h | USB | Deep Standby USB Suspend/Resume Interrupt Register | DPUSR1R | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*1 | USBb |
| 000A 0500h | PDC | PDC Control Register 0 | PCCR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0504h | PDC | PDC Control Register 1 | PCCR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0508h | PDC | PDC Status Register | PCSR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 050Ch | PDC | PDC Pin Monitor Register | PCMONR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0510h | PDC | PDC Receive Data Register | PCDR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0514h | PDC | Vertical Capture Register | VCR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0518h | PDC | Horizontal Capture Register | HCR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |

**Table 4.1 List of I/O Registers (Address Order) (48 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 0000h | EDMAC 0 | EDMAC Mode Register | EDMR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0008h | EDMAC 0 | EDMAC Transmit Request Register | EDTRR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0010h | EDMAC 0 | EDMAC Receive Request Register | EDRRR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0018h | EDMAC 0 | Transmit Descriptor List Start Address Register | TDLAR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0020h | EDMAC 0 | Receive Descriptor List Start Address Register | RDLAR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0028h | EDMAC 0 | ETHERC/EDMAC Status Register | EESR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0030h | EDMAC 0 | ETHERC/EDMAC Status Interrupt Enable Register | EESIPR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0038h | EDMAC 0 | ETHERC/EDMAC Transmit/Receive Status Copy Enable Register | TRSCER | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0040h | EDMAC 0 | Missed-Frame Counter Register | RMFCR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0048h | EDMAC 0 | Transmit FIFO Threshold Register | TFTR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0050h | EDMAC 0 | FIFO Depth Register | FDR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0058h | EDMAC 0 | Receive Method Control Register | RMCR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0064h | EDMAC 0 | Transmit FIFO Underflow Counter | TFUCR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0068h | EDMAC 0 | Receive FIFO Overflow Counter | RFOCR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 006Ch | EDMAC 0 | Independent Output Signal Setting Register | IOSR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0070h | EDMAC 0 | Flow Control Start FIFO Threshold Setting Register | FCFTR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0078h | EDMAC 0 | Receive Data Padding Insert Register | RPADIR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 007Ch | EDMAC 0 | Transmit Interrupt Setting Register | TRIMD | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 00C8h | EDMAC 0 | Receive Buffer Write Address Register | RBWAR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 00CCh | EDMAC 0 | Receive Descriptor Fetch Address Register | RDFAR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 00D4h | EDMAC 0 | Transmit Buffer Read Address Register | TBRAR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 00D8h | EDMAC 0 | Transmit Descriptor Fetch Address Register | TDFAR | 32 | 32 | 4, 5 PCLKA | 1 to 3 ICLK | EDMACa |
| 000C 0100h | ETHERC0 | ETHERC Mode Register | ECMR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0108h | ETHERC0 | Receive Frame Maximum Length Register | RFLR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0110h | ETHERC0 | ETHERC Status Register | ECSR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0118h | ETHERC0 | ETHERC Interrupt Enable Register | ECSIPR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0120h | ETHERC0 | PHY Interface Register | PIR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0128h | ETHERC0 | PHY Status Register | PSR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0140h | ETHERC0 | Random Number Generation Counter Limit Setting Register | RDMLR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0150h | ETHERC0 | Interpacket Gap Register | IPGR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0154h | ETHERC0 | Automatic PAUSE Frame Register | APR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |

**Table 4.1 List of I/O Registers (Address Order) (49 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 0158h | ETHERC0 | Manual PAUSE Frame Register | MPR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0160h | ETHERC0 | Received PAUSE Frame Counter | RFCF | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0164h | ETHERC0 | PAUSE Frame Retransmit Count Setting Register | TPAUSER | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 0168h | ETHERC0 | PAUSE Frame Retransmit Counter | TPAUSECR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 016Ch | ETHERC0 | Broadcast Frame Receive Count Setting Register | BCFRR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01C0h | ETHERC0 | MAC Address Upper Bit Register | MAHR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01C8h | ETHERC0 | MAC Address Lower Bit Register | MALR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01D0h | ETHERC0 | Transmit Retry Over Counter Register | TROCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01D4h | ETHERC0 | Late Collision Detect Counter Register | CDCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01D8h | ETHERC0 | Lost Carrier Counter Register | LCCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01DCh | ETHERC0 | Carrier Not Detect Counter Register | CNDCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01E4h | ETHERC0 | CRC Error Frame Receive Counter Register | CEFCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01E8h | ETHERC0 | Frame Receive Error Counter Register | FRECR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01ECh | ETHERC0 | Too-Short Frame Receive Counter Register | TSFRCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01F0h | ETHERC0 | Too-Long Frame Receive Counter Register | TLFRCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01F4h | ETHERC0 | Received Alignment Error Frame Counter Register | RFCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 01F8h | ETHERC0 | Multicast Address Frame Receive Counter Register | MAFCR | 32 | 32 | 13, 14 PCLKA | 1 to 7 ICLK | ETHERC |
| 000C 1200h | MTU3 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1201h | MTU4 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1202h | MTU3 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1203h | MTU4 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1204h | MTU3 | Timer I/O Control Register H | TIORH | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1205h | MTU3 | Timer I/O Control Register L | TIORL | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1206h | MTU4 | Timer I/O Control Register H | TIORH | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1207h | MTU4 | Timer I/O Control Register L | TIORL | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1208h | MTU3 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1209h | MTU4 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 120Ah | MTU | Timer Output Master Enable Register A | TOERA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 120Dh | MTU | Timer Gate Control Register A | TGCRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 120Eh | MTU | Timer Output Control Register 1A | TOCR1A | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 120Fh | MTU | Timer Output Control Register 2A | TOCR2A | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1210h | MTU3 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1212h | MTU4 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1214h | MTU | Timer Cycle Data Register A | TCDRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1216h | MTU | Timer Dead Time Data Register A | TDDRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1218h | MTU3 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 121Ah | MTU3 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 121Ch | MTU4 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 121Eh | MTU4 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1220h | MTU | Timer Subcounter A | TCNTSA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (50 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1222h | MTU | Timer Cycle Buffer Register A | TCBRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1224h | MTU3 | Timer General Register C | TGRC | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1226h | MTU3 | Timer General Register D | TGRD | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1228h | MTU4 | Timer General Register C | TGRC | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 122Ah | MTU4 | Timer General Register D | TGRD | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 122Ch | MTU3 | Timer Status Register | TSR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 122Dh | MTU4 | Timer Status Register | TSR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1230h | MTU | Timer Interrupt Skipping Set Register 1A | TITCR1A | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1231h | MTU | Timer Interrupt Skipping Counter 1A | TITCNT1A | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1232h | MTU | Timer Buffer Transfer Set Register A | TBTERA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1234h | MTU | Timer Dead Time Enable Register A | TDERA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1236h | MTU | Timer Output Level Buffer Register A | TOLBRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1238h | MTU3 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1239h | MTU4 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 123Ah | MTU | Timer Interrupt Skipping Mode Register A | TITMRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 123Bh | MTU | Timer Interrupt Skipping Set Register 2A | TITCR2A | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 123Ch | MTU | Timer Interrupt Skipping Counter 2A | TITCNT2A | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1240h | MTU4 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1244h | MTU4 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1246h | MTU4 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1248h | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 124Ah | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 124Ch | MTU3 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 124Dh | MTU4 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1260h | MTU | Timer Waveform Control Register A | TWCRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1270h | MTU | Timer Mode Register 2A | TMDR2A | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1272h | MTU3 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1274h | MTU4 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1276h | MTU4 | Timer General Register F | TGRF | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1280h | MTU | Timer Start Register A | TSTRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1281h | MTU | Timer Synchronous Register A | TSYRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1282h | MTU | Timer Counter Synchronous Start Register | TCSYSTR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1284h | MTU | Timer Read/Write Enable Register A | TRWERA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1290h | MTU0 | Noise Filter Control Register 0 | NFCR0 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1291h | MTU1 | Noise Filter Control Register 1 | NFCR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1292h | MTU2 | Noise Filter Control Register 2 | NFCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1293h | MTU3 | Noise Filter Control Register 3 | NFCR3 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1294h | MTU4 | Noise Filter Control Register 4 | NFCR4 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1298h | MTU8 | Noise Filter Control Register 8 | NFCR8 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1299h | MTU0 | Noise Filter Control Register C | NFCRC | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1300h | MTU0 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1301h | MTU0 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1302h | MTU0 | Timer I/O Control Register H | TIORH | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1303h | MTU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1304h | MTU0 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1306h | MTU0 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1308h | MTU0 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (51 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 130Ah | MTU0 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 130Ch | MTU0 | Timer General Register C | TGRC | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 130Eh | MTU0 | Timer General Register D | TGRD | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1320h | MTU0 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1322h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1324h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1326h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1328h | MTU0 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1380h | MTU1 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1381h | MTU1 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1382h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1384h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1385h | MTU1 | Timer Status Register | TSR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1386h | MTU1 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1388h | MTU1 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 138Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1390h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1391h | MTU1 | Timer Mode Register 3 | TMDR3 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1394h | MTU1 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 13A0h | MTU1 | Timer Longword Counter | TCNTLW | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 13A4h | MTU1 | Timer Longword General Register | TGRALW | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 13A8h | MTU1 | Timer Longword General Register | TGRBLW | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1400h | MTU2 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1401h | MTU2 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1402h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1404h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1405h | MTU2 | Timer Status Register | TSR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1406h | MTU2 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1408h | MTU2 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 140Ah | MTU2 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 140Ch | MTU2 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1600h | MTU8 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1601h | MTU8 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1602h | MTU8 | Timer I/O Control Register H | TIORH | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1603h | MTU8 | Timer I/O Control Register L | TIORL | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1604h | MTU8 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1606h | MTU8 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1608h | MTU8 | Timer Counter | TCNT | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 160Ch | MTU8 | Timer General Register A | TGRA | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1610h | MTU8 | Timer General Register B | TGRB | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1614h | MTU8 | Timer General Register C | TGRC | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1618h | MTU8 | Timer General Register D | TGRD | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A00h | MTU6 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A01h | MTU7 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A02h | MTU6 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A03h | MTU7 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A04h | MTU6 | Timer I/O Control Register H | TIORH | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A05h | MTU6 | Timer I/O Control Register L | TIORL | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A06h | MTU7 | Timer I/O Control Register H | TIORH | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A07h | MTU7 | Timer I/O Control Register L | TIORL | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (52 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1A08h | MTU6 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A09h | MTU7 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A0Ah | MTU | Timer Output Master Enable Register B | TOERB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A0Eh | MTU | Timer Output Control Register 1B | TOCR1B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A0Fh | MTU | Timer Output Control Register 2B | TOCR2B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A10h | MTU6 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A12h | MTU7 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A14h | MTU | Timer Cycle Data Register B | TCDRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A16h | MTU | Timer Dead Time Data Register B | TDDRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A18h | MTU6 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A1Ah | MTU6 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A1Ch | MTU7 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A1Eh | MTU7 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A20h | MTU | Timer Subcounter B | TCNTSB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A22h | MTU | Timer Cycle Buffer Register B | TCBRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A24h | MTU6 | Timer General Register C | TGRC | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A26h | MTU6 | Timer General Register D | TGRD | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A28h | MTU7 | Timer General Register C | TGRC | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A2Ah | MTU7 | Timer General Register D | TGRD | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A2Ch | MTU6 | Timer Status Register | TSR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A2Dh | MTU7 | Timer Status Register | TSR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A30h | MTU | Timer Interrupt Skipping Set Register 1B | TITCR1B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A31h | MTU | Timer Interrupt Skipping Counter 1B | TITCNT1B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A32h | MTU | Timer Buffer Transfer Set Register B | TBTERB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A34h | MTU | Timer Dead Time Enable Register B | TDERB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A36h | MTU | Timer Output Level Buffer Register B | TOLBRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A38h | MTU6 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A39h | MTU7 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A3Ah | MTU | Timer Interrupt Skipping Mode Register B | TITMRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A3Bh | MTU | Timer Interrupt Skipping Set Register 2B | TITCR2B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A3Ch | MTU | Timer Interrupt Skipping Counter 2B | TITCNT2B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A40h | MTU7 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A44h | MTU7 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A46h | MTU7 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A48h | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A4Ah | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A4Ch | MTU6 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A4Dh | MTU7 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A50h | MTU6 | Timer Synchronous Clear Register | TSYCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A60h | MTU | Timer Waveform Control Register B | TWCRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A70h | MTU | Timer Mode Register 2B | TMDR2B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A72h | MTU6 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A74h | MTU7 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A76h | MTU7 | Timer General Register F | TGRF | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A80h | MTU | Timer Start Register B | TSTRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A81h | MTU | Timer Synchronous Register B | TSYRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A84h | MTU | Timer Read/Write Enable Register B | TRWERB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (53 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1A93h | MTU6 | Noise Filter Control Register 6 | NFCR6 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A94h | MTU7 | Noise Filter Control Register 7 | NFCR7 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A95h | MTU5 | Noise Filter Control Register 5 | NFCR5 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C80h | MTU5 | Timer Counter U | TCNTU | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C82h | MTU5 | Timer General Register U | TGRU | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C84h | MTU5 | Timer Control Register U | TCRU | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C85h | MTU5 | Timer Control Register 2 | TCR2U | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C86h | MTU5 | Timer I/O Control Register U | TIORU | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C90h | MTU5 | Timer Counter V | TCNTV | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C92h | MTU5 | Timer General Register V | TGRV | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C94h | MTU5 | Timer Control Register V | TCRV | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C95h | MTU5 | Timer Control Register 2 | TCR2V | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C96h | MTU5 | Timer I/O Control Register V | TIORV | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA0h | MTU5 | Timer Counter W | TCNTW | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA2h | MTU5 | Timer General Register W | TGRW | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA4h | MTU5 | Timer Control Register W | TCRW | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA5h | MTU5 | Timer Control Register 2 | TCR2W | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA6h | MTU5 | Timer I/O Control Register W | TIORW | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CB2h | MTU5 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CB4h | MTU5 | Timer Start Register | TSTR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CB6h | MTU5 | Timer Compare Match Clear Register | TCNTCMPCLR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 5800h | BSC | Extended Bus Master Priority Control Register | EBMAPCR | 32 | 32 | 1, 2 PCLKA | 1 ICLK | BSC |
| 000D 0040h | SCI10 | Serial Mode Register | SMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0040h | SMCI10 | Serial Mode Register | SMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0041h | SCI10 | Bit Rate Register | BRR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0042h | SCI10 | Serial Control Register | SCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0042h | SMCI10 | Serial Control Register | SCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0043h | SCI10 | Transmit Data Register | TDR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0044h | SCI10 | Serial Status Register | SSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0044h | SMCI10 | Serial Status Register | SSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0044h | SCI10 | Serial Status Register | SSRFIFO | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0045h | SCI10 | Receive Data Register | RDR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0046h | SCI10 | Smart Card Mode Register | SCMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0046h | SMCI10 | Smart Card Mode Register | SCMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0047h | SCI10 | Serial Extended Mode Register | SEMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0048h | SCI10 | Noise Filter Setting Register | SNFR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0049h | SCI10 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Ah | SCI10 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Bh | SCI10 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Ch | SCI10 | $I^2C$ Status Register | SISR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Dh | SCI10 | SPI Mode Register | SPMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Eh | SCI10 | Transmit Data Register H | TDRH | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Fh | SCI10 | Transmit Data Register L | TDRL | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Eh | SCI10 | Transmit Data Register HL | TDRHL | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 004Eh | SCI10 | Transmit FIFO Data Register | FTDR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Fh | SCI10 | Transmit FIFO Data Register | FTDR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 004Eh | SCI10 | Transmit FIFO Data Register | FTDR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0050h | SCI10 | Receive Data Register H | RDRH | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0051h | SCI10 | Receive Data Register L | RDRL | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |

**Table 4.1 List of I/O Registers (Address Order) (54 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000D 0050h | SCI10 | Receive Data Register HL | RDRHL | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0050h | SCI10 | Receive FIFO Data Register | FRDR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0051h | SCI10 | Receive FIFO Data Register | FRDR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0050h | SCI10 | Receive FIFO Data Register | FRDR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0052h | SCI10 | Modulation Duty Register | MDDR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0053h | SCI10 | Data Comparison Control Register | DCCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0054h | SCI10 | FIFO Control Register | FCR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0055h | SCI10 | FIFO Control Register | FCR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0054h | SCI10 | FIFO Control Register | FCR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0056h | SCI10 | FIFO Data Count Register | FDR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0057h | SCI10 | FIFO Data Count Register | FDR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0056h | SCI10 | FIFO Data Count Register | FDR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0058h | SCI10 | Line Status Register | LSR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0059h | SCI10 | Line Status Register | LSR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0058h | SCI10 | Line Status Register | LSR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 005Ah | SCI10 | Comparison Data Register | CDR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 005Bh | SCI10 | Comparison Data Register | CDR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 005Ah | SCI10 | Comparison Data Register | CDR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 005Ch | SCI10 | Serial Port Register | SPTR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0060h | SCI11 | Serial Mode Register | SMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0060h | SMCI11 | Serial Mode Register | SMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0061h | SCI11 | Bit Rate Register | BRR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0062h | SCI11 | Serial Control Register | SCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0062h | SMCI11 | Serial Control Register | SCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0063h | SCI11 | Transmit Data Register | TDR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0064h | SCI11 | Serial Status Register | SSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0064h | SMCI11 | Serial Status Register | SSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0064h | SCI11 | Serial Status Register | SSRFIFO | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0065h | SCI11 | Receive Data Register | RDR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0066h | SCI11 | Smart Card Mode Register | SCMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0066h | SMCI11 | Smart Card Mode Register | SCMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0067h | SCI11 | Serial Extended Mode Register | SEMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0068h | SCI11 | Noise Filter Setting Register | SNFR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0069h | SCI11 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Ah | SCI11 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Bh | SCI11 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Ch | SCI11 | $I^2C$ Status Register | SISR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Dh | SCI11 | SPI Mode Register | SPMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Eh | SCI11 | Transmit Data Register H | TDRH | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Fh | SCI11 | Transmit Data Register L | TDRL | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Eh | SCI11 | Transmit Data Register HL | TDRHL | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 006Eh | SCI11 | Transmit FIFO Data Register | FTDR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Fh | SCI11 | Transmit FIFO Data Register | FTDR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 006Eh | SCI11 | Transmit FIFO Data Register | FTDR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0070h | SCI11 | Receive Data Register H | RDRH | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0071h | SCI11 | Receive Data Register L | RDRL | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0070h | SCI11 | Receive Data Register HL | RDRHL | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0070h | SCI11 | Receive FIFO Data Register | FRDR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0071h | SCI11 | Receive FIFO Data Register | FRDR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0070h | SCI11 | Receive FIFO Data Register | FRDR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |

**Table 4.1 List of I/O Registers (Address Order) (55 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000D 0072h | SCI11 | Modulation Duty Register | MDDR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0073h | SCI11 | Data Comparison Control Register | DCCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0074h | SCI11 | FIFO Control Register | FCR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0075h | SCI11 | FIFO Control Register | FCR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0074h | SCI11 | FIFO Control Register | FCR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0076h | SCI11 | FIFO Data Count Register | FDR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0077h | SCI11 | FIFO Data Count Register | FDR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0076h | SCI11 | FIFO Data Count Register | FDR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 0078h | SCI11 | Line Status Register | LSR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0079h | SCI11 | Line Status Register | LSR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0078h | SCI11 | Line Status Register | LSR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 007Ah | SCI11 | Comparison Data Register | CDR.H | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 007Bh | SCI11 | Comparison Data Register | CDR.L | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 007Ah | SCI11 | Comparison Data Register | CDR | 16 | 16 | 5, 6 PCLKA | 1 to 3 ICLK | SCIi |
| 000D 007Ch | SCI11 | Serial Port Register | SPTR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0100h | RSPI0 | RSPI Control Register | SPCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0101h | RSPI0 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0102h | RSPI0 | RSPI Pin Control Register | SPPCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0103h | RSPI0 | RSPI Status Register | SPSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0104h | RSPI0 | RSPI Data Register | SPDR | 32 | 8, 16, 32 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0108h | RSPI0 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0109h | RSPI0 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 010Ah | RSPI0 | RSPI Bit Rate Register | SPBR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 010Bh | RSPI0 | RSPI Data Control Register | SPDCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 010Ch | RSPI0 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 010Dh | RSPI0 | RSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 010Eh | RSPI0 | RSPI Next-Access Delay Register | SPND | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 010Fh | RSPI0 | RSPI Control Register 2 | SPCR2 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0110h | RSPI0 | RSPI Command Register 0 | SPCMD0 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0112h | RSPI0 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0114h | RSPI0 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0116h | RSPI0 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0118h | RSPI0 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 011Ah | RSPI0 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 011Ch | RSPI0 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 011Eh | RSPI0 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0120h | RSPI0 | RSPI Data Control Register 2 | SPDCR2 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0140h | RSPI1 | RSPI Control Register | SPCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0141h | RSPI1 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0142h | RSPI1 | RSPI Pin Control Register | SPPCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0143h | RSPI1 | RSPI Status Register | SPSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0144h | RSPI1 | RSPI Data Register | SPDR | 32 | 8, 16, 32 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0148h | RSPI1 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0149h | RSPI1 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 014Ah | RSPI1 | RSPI Bit Rate Register | SPBR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 014Bh | RSPI1 | RSPI Data Control Register | SPDCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 014Ch | RSPI1 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 014Dh | RSPI1 | RSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 014Eh | RSPI1 | RSPI Next-Access Delay Register | SPND | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |

**Table 4.1 List of I/O Registers (Address Order) (56 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000D 014Fh | RSPI1 | RSPI Control Register 2 | SPCR2 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0150h | RSPI1 | RSPI Command Register 0 | SPCMD0 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0152h | RSPI1 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0154h | RSPI1 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0156h | RSPI1 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0158h | RSPI1 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 015Ah | RSPI1 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 015Ch | RSPI1 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 015Eh | RSPI1 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0160h | RSPI1 | RSPI Data Control Register 2 | SPDCR2 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0300h | RSPI2 | RSPI Control Register | SPCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0301h | RSPI2 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0302h | RSPI2 | RSPI Pin Control Register | SPPCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0303h | RSPI2 | RSPI Status Register | SPSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0304h | RSPI2 | RSPI Data Register | SPDR | 32 | 8, 16, 32 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0308h | RSPI2 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0309h | RSPI2 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 030Ah | RSPI2 | RSPI Bit Rate Register | SPBR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 030Bh | RSPI2 | RSPI Data Control Register | SPDCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 030Ch | RSPI2 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 030Dh | RSPI2 | RSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 030Eh | RSPI2 | RSPI Next-Access Delay Register | SPND | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 030Fh | RSPI2 | RSPI Control Register 2 | SPCR2 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0310h | RSPI2 | RSPI Command Register 0 | SPCMD0 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0312h | RSPI2 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0314h | RSPI2 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0316h | RSPI2 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0318h | RSPI2 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 031Ah | RSPI2 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 031Ch | RSPI2 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 031Eh | RSPI2 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000D 0320h | RSPI2 | RSPI Data Control Register 2 | SPDCR2 | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | RSPIc |
| 000E 0000h to 000E 03FCh | GLCDC | Graphic 1 Color Look-up Table 0[0 to 255] | GR1CLUT0[0 to 255] | 32 | 32 | 5, 6 PCLKA*3 | 1, 2 ICLK*3 | GLCDC |
| 000E 0400h to 000E 07FCh | GLCDC | Graphic 1 Color Look-up Table 1[0 to 255] | GR1CLUT1[0 to 255] | 32 | 32 | 5, 6 PCLKA*3 | 1, 2 ICLK*3 | GLCDC |
| 000E 0800h to 000E 0BFCh | GLCDC | Graphic 2 Color Look-up Table 0[0 to 255] | GR2CLUT0[0 to 255] | 32 | 32 | 5, 6 PCLKA*3 | 1, 2 ICLK*3 | GLCDC |
| 000E 0C00h to 000E 0FFCh | GLCDC | Graphic 2 Color Look-up Table 1[0 to 255] | GR2CLUT1[0 to 255] | 32 | 32 | 5, 6 PCLKA*3 | 1, 2 ICLK*3 | GLCDC |
| 000E 1000h | GLCDC | Background Generating Block Operation Control Register | BGEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1004h | GLCDC | Free-Running Period Register | BGPERI | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1008h | GLCDC | Synchronization Position Register | BGSYNC | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 100Ch | GLCDC | Vertical Size Register | BGVSIZE | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1010h | GLCDC | Horizontal Size Register | BGHSIZE | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1014h | GLCDC | Background Color Register | BGCOLOR | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1018h | GLCDC | Background Generating Block Status Monitor Register | BGMON | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1100h | GLCDC | Graphic 1 Register Update Control Register | GR1VEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |

**Table 4.1 List of I/O Registers (Address Order) (57 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000E 1104h | GLCDC | Graphic 1 Frame Buffer Read Control Register | GR1FLMRD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 110Ch | GLCDC | Graphic 1 Frame Buffer Control Register 2 | GR1FLM2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1110h | GLCDC | Graphic 1 Frame Buffer Control Register 3 | GR1FLM3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1118h | GLCDC | Graphic 1 Frame Buffer Control Register 5 | GR1FLM5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 111Ch | GLCDC | Graphic 1 Frame Buffer Control Register 6 | GR1FLM6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1120h | GLCDC | Graphic 1 Alpha Blending Control Register 1 | GR1AB1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1124h | GLCDC | Graphic 1 Alpha Blending Control Register 2 | GR1AB2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1128h | GLCDC | Graphic 1 Alpha Blending Control Register 3 | GR1AB3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 112Ch | GLCDC | Graphic 1 Alpha Blending Control Register 4 | GR1AB4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1130h | GLCDC | Graphic 1 Alpha Blending Control Register 5 | GR1AB5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1134h | GLCDC | Graphic 1 Alpha Blending Control Register 6 | GR1AB6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1138h | GLCDC | Graphic 1 Alpha Blending Control Register 7 | GR1AB7 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 113Ch | GLCDC | Graphic 1 Alpha Blending Control Register 8 | GR1AB8 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1140h | GLCDC | Graphic 1 Alpha Blending Control Register 9 | GR1AB9 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 114Ch | GLCDC | Graphic 1 Background Color Control Register | GR1BASE | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1150h | GLCDC | Graphic 1 CLUT/Interrupt Control Register | GR1CLUTINT | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1154h | GLCDC | Graphic 1 Status Monitor Register | GR1MON | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1200h | GLCDC | Graphic 2 Register Update Control Register | GR2VEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1204h | GLCDC | Graphic 2 Frame Buffer Read Control Register | GR2FLMRD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 120Ch | GLCDC | Graphic 2 Frame Buffer Control Register 2 | GR2FLM2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1210h | GLCDC | Graphic 2 Frame Buffer Control Register 3 | GR2FLM3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1218h | GLCDC | Graphic 2 Frame Buffer Control Register 5 | GR2FLM5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 121Ch | GLCDC | Graphic 2 Frame Buffer Control Register 6 | GR2FLM6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1220h | GLCDC | Graphic 2 Alpha Blending Control Register 1 | GR2AB1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1224h | GLCDC | Graphic 2 Alpha Blending Control Register 2 | GR2AB2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1228h | GLCDC | Graphic 2 Alpha Blending Control Register 3 | GR2AB3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 122Ch | GLCDC | Graphic 2 Alpha Blending Control Register 4 | GR2AB4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1230h | GLCDC | Graphic 2 Alpha Blending Control Register 5 | GR2AB5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1234h | GLCDC | Graphic 2 Alpha Blending Control Register 6 | GR2AB6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1238h | GLCDC | Graphic 2 Alpha Blending Control Register 7 | GR2AB7 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 123Ch | GLCDC | Graphic 2 Alpha Blending Control Register 8 | GR2AB8 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1240h | GLCDC | Graphic 2 Alpha Blending Control Register 9 | GR2AB9 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 124Ch | GLCDC | Graphic 2 Background Color Control Register | GR2BASE | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1250h | GLCDC | Graphic 2 CLUT/Interrupt Control Register | GR2CLUTINT | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1254h | GLCDC | Graphic 2 Status Monitor Register | GR2MON | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1300h | GLCDC | Gamma Correction G Block Register Update Control Register | GAMGVEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1304h | GLCDC | Gamma Correction Block Function Switch Register | GAMSW | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1308h | GLCDC | Gamma Correction G Table Setting Register 1 | GAMGLUT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 130Ch | GLCDC | Gamma Correction G Table Setting Register 2 | GAMGLUT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1310h | GLCDC | Gamma Correction G Table Setting Register 3 | GAMGLUT3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1314h | GLCDC | Gamma Correction G Table Setting Register 4 | GAMGLUT4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1318h | GLCDC | Gamma Correction G Table Setting Register 5 | GAMGLUT5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 131Ch | GLCDC | Gamma Correction G Table Setting Register 6 | GAMGLUT6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1320h | GLCDC | Gamma Correction G Table Setting Register 7 | GAMGLUT7 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1324h | GLCDC | Gamma Correction G Table Setting Register 8 | GAMGLUT8 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1328h | GLCDC | Gamma Correction G Area Setting Register 1 | GAMGAREA1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 132Ch | GLCDC | Gamma Correction G Area Setting Register 2 | GAMGAREA2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1330h | GLCDC | Gamma Correction G Area Setting Register 3 | GAMGAREA3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1334h | GLCDC | Gamma Correction G Area Setting Register 4 | GAMGAREA4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |

**Table 4.1 List of I/O Registers (Address Order) (58 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000E 1338h | GLCDC | Gamma Correction G Area Setting Register 5 | GAMGAREA5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1340h | GLCDC | Gamma Correction B Block Register Update Control Register | GAMBVEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1348h | GLCDC | Gamma Correction B Table Setting Register 1 | GAMBLUT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 134Ch | GLCDC | Gamma Correction B Table Setting Register 2 | GAMBLUT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1350h | GLCDC | Gamma Correction B Table Setting Register 3 | GAMBLUT3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1354h | GLCDC | Gamma Correction B Table Setting Register 4 | GAMBLUT4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1358h | GLCDC | Gamma Correction B Table Setting Register 5 | GAMBLUT5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 135Ch | GLCDC | Gamma Correction B Table Setting Register 6 | GAMBLUT6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1360h | GLCDC | Gamma Correction B Table Setting Register 7 | GAMBLUT7 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1364h | GLCDC | Gamma Correction B Table Setting Register 8 | GAMBLUT8 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1368h | GLCDC | Gamma Correction B Area Setting Register 1 | GAMBAREA1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 136Ch | GLCDC | Gamma Correction B Area Setting Register 2 | GAMBAREA2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1370h | GLCDC | Gamma Correction B Area Setting Register 3 | GAMBAREA3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1374h | GLCDC | Gamma Correction B Area Setting Register 4 | GAMBAREA4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1378h | GLCDC | Gamma Correction B Area Setting Register 5 | GAMBAREA5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1380h | GLCDC | Gamma Correction R Block Register Update Control Register | GAMRVEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1388h | GLCDC | Gamma Correction R Table Setting Register 1 | GAMRLUT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 138Ch | GLCDC | Gamma Correction R Table Setting Register 2 | GAMRLUT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1390h | GLCDC | Gamma Correction R Table Setting Register 3 | GAMRLUT3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1394h | GLCDC | Gamma Correction R Table Setting Register 4 | GAMRLUT4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1398h | GLCDC | Gamma Correction R Table Setting Register 5 | GAMRLUT5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 139Ch | GLCDC | Gamma Correction R Table Setting Register 6 | GAMRLUT6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13A0h | GLCDC | Gamma Correction R Table Setting Register 7 | GAMRLUT7 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13A4h | GLCDC | Gamma Correction R Table Setting Register 8 | GAMRLUT8 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13A8h | GLCDC | Gamma Correction R Area Setting Register 1 | GAMRAREA1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13ACh | GLCDC | Gamma Correction R Area Setting Register 2 | GAMRAREA2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13B0h | GLCDC | Gamma Correction R Area Setting Register 3 | GAMRAREA3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13B4h | GLCDC | Gamma Correction R Area Setting Register 4 | GAMRAREA4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13B8h | GLCDC | Gamma Correction R Area Setting Register 5 | GAMRAREA5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13C0h | GLCDC | Output Control Block Register Update Control Register | OUTVEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13C4h | GLCDC | Output Interface Register | OUTSET | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13C8h | GLCDC | Brightness Adjustment Register 1 | BRIGHT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13CCh | GLCDC | Brightness Adjustment Register 2 | BRIGHT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13D0h | GLCDC | Contrast Adjustment Register | CONTRAST | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13D4h | GLCDC | Panel Dither Control Register | PANELDTHA | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13E4h | GLCDC | Output Phase Control Register | CLKPHASE | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1404h | GLCDC | Reference Timing Setting Register | TCONTIM | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1408h | GLCDC | Vertical Timing Setting Register A1 | TCONSTVA1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 140Ch | GLCDC | Vertical Timing Setting Register A2 | TCONSTVA2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1410h | GLCDC | Vertical Timing Setting Register B1 | TCONSTVB1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1414h | GLCDC | Vertical Timing Setting Register B2 | TCONSTVB2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1418h | GLCDC | Horizontal Timing Setting Register A1 | TCONSTHA1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 141Ch | GLCDC | Horizontal Timing Setting Register A2 | TCONSTHA2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1420h | GLCDC | Horizontal Timing Setting Register B1 | TCONSTHB1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1424h | GLCDC | Horizontal Timing Setting Register B2 | TCONSTHB2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1428h | GLCDC | Data Enable Polarity Setting Register | TCONDE | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1440h | GLCDC | Status Detection Control Register | DTCTEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1444h | GLCDC | Interrupt Request Enable Control Register | INTEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |

**Table 4.1 List of I/O Registers (Address Order) (59 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000E 1448h | GLCDC | Detected Status Clear Register | STCLR | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 144Ch | GLCDC | Detected Status Monitor Register | STMON | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1450h | GLCDC | Panel Clock Control Register | PANELCLK | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 3000h | DRW2D | Geometry Control Register | CONTROL | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3000h | DRW2D | Status Register | STATUS | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3004h | DRW2D | Surface Control Register | CONTROL2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3004h | DRW2D | Hardware Version Register | HWVER | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3010h | DRW2D | Limiter 1 Start Value Register | L1START | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3014h | DRW2D | Limiter 2 Start Value Register | L2START | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3018h | DRW2D | Limiter 3 Start Value Register | L3START | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 301Ch | DRW2D | Limiter 4 Start Value Register | L4START | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3020h | DRW2D | Limiter 5 Start Value Register | L5START | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3024h | DRW2D | Limiter 6 Start Value Register | L6START | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3028h | DRW2D | Limiter 1 X-Axis Increment Register | L1XADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 302Ch | DRW2D | Limiter 2 X-Axis Increment Register | L2XADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3030h | DRW2D | Limiter 3 X-Axis Increment Register | L3XADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3034h | DRW2D | Limiter 4 X-Axis Increment Register | L4XADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3038h | DRW2D | Limiter 5 X-Axis Increment Register | L5XADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 303Ch | DRW2D | Limiter 6 X-Axis Increment Register | L6XADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3040h | DRW2D | Limiter 1 Y-Axis Increment Register | L1YADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3044h | DRW2D | Limiter 2 Y-Axis Increment Register | L2YADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3048h | DRW2D | Limiter 3 Y-Axis Increment Register | L3YADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 304Ch | DRW2D | Limiter 4 Y-Axis Increment Register | L4YADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3050h | DRW2D | Limiter 5 Y-Axis Increment Register | L5YADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3054h | DRW2D | Limiter 6 Y-Axis Increment Register | L6YADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3058h | DRW2D | Limiter 1 Band Width Parameter Register | L1BAND | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 305Ch | DRW2D | Limiter 2 Band Width Parameter Register | L2BAND | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3064h | DRW2D | Base Color Register | COLOR1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3068h | DRW2D | Secondary Color Register | COLOR2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3074h | DRW2D | Pattern Register | PATTERN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3078h | DRW2D | Bounding Box Dimension Register | SIZE | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 307Ch | DRW2D | Frame Buffer Pitch Register | PITCH | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3080h | DRW2D | Frame Buffer Base Address Register | ORIGIN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3090h | DRW2D | U Limiter Start Value Register | LUST | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3094h | DRW2D | U Limiter X-Axis Increment Register | LUXADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 3098h | DRW2D | U Limiter Y-Axis Increment Register | LUYADD | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 309Ch | DRW2D | V Limiter Start Value Integer Part Register | LVSTI | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30A0h | DRW2D | V Limiter Start Value Fractional Part Register | LVSTF | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30A4h | DRW2D | V Limiter X-Axis Increment Integer Part Register | LVXADDI | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30A8h | DRW2D | V Limiter Y-Axis Increment Integer Part Register | LVYADDI | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30ACh | DRW2D | V Limiter Increment Fractional Parts Register | LVYXADDF | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30B4h | DRW2D | Texels Per Texture Line Register | TEXPITCH | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30B8h | DRW2D | Texture Mask Register | TEXMSK | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30BCh | DRW2D | Texture Base Address Register | TEXORG | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30C0h | DRW2D | Interrupt Control Register | IRQCTL | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30C4h | DRW2D | Cache Control Register | CACHECTL | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30C8h | DRW2D | Display List Start Address Register | DLISTST | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30CCh | DRW2D | Performance Counter 1 | PERFCNT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30D0h | DRW2D | Performance Counter 2 | PERFCNT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30D4h | DRW2D | Performance Counters Control Register | PERFTRG | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |

**Table 4.1 List of I/O Registers (Address Order) (60 / 60)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000E 30DCh | DRW2D | CLUT Start Address Register | TEXCLADDR | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30E0h | DRW2D | CLUT Data Register | TEXCLDATA | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30E4h | DRW2D | CLUT Offset Register | TEXCLOFST | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 000E 30E8h | DRW2D | Chroma Key Register | COLKEY | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | DRW2D |
| 007F C040h | FLASH | Data Flash Memory Access Frequency Setting Register | EEPFCLK | 8 | 8 | 2 FCLK | | Flash |
| FE7F 5D00h | OFSM | Endian Select Register | MDE | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D04h | OFSM | Option Function Select Register 0 | OFS0 | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D08h | OFSM | Option Function Select Register 1 | OFS1 | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D10h | OFSM | TM Identification Data Register | TMINF | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D20h | OFSM | Bank Select Register | BANKSEL | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D40h | OFSM | Serial Programmer Command Control Register | SPCC | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D48h | OFSM | TM Enable Flag Register | TMEF | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D50h | OFSM | OCD/Serial Programmer ID Setting Register | OSIS | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D64h | OFSM | Flash Access Window Setting Register | FAW | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 5D70h | OFSM | ROM Code Protection Register | ROMCODE | 32 | 32 | 1 to 3 ICLK | | Option-Setting Memory |
| FE7F 7D7Ch | TEMPS | Temperature Sensor Calibration Data Register | TSCDR | 32 | 32 | 1 to 3 ICLK | | TEMPS |
| FE7F 7D90h | FLASH | Unique ID Register 0 | UIDR0 | 32 | 32 | 1 to 3 ICLK | | Flash |
| FE7F 7D94h | FLASH | Unique ID Register 1 | UIDR1 | 32 | 32 | 1 to 3 ICLK | | Flash |
| FE7F 7D98h | FLASH | Unique ID Register 2 | UIDR2 | 32 | 32 | 1 to 3 ICLK | | Flash |
| FE7F 7D9Ch | FLASH | Unique ID Register 3 | UIDR3 | 32 | 32 | 1 to 3 ICLK | | Flash |

Note 1. When the register is accessed while the USB is operating, a delay may be generated in accessing.
Note 2. The address must end with 0h, 4h, 8h, or Ch when access is made in 32-bit units. The address must end with 0h, 2h, 4h, 6h, 8h, Ah, Ch, or Eh when access is made in 16-bit units.
Note 3. When the register is accessed while the GLCDC is operating, a delay may be generated in accessing.

# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Rating**

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

| Item | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | | VCC, VCC_USB | –0.3 to +4.0 | V |
| $V_{BATT}$ power supply voltage | | $V_{BATT}$ | –0.3 to +4.0 | V |
| Input voltage (except for ports for 5 V tolerant*1) | | $V_{in}$ | –0.3 to VCC + 0.3 (up to 4.0) | V |
| Input voltage (ports for 5 V tolerant*1) | | $V_{in}$ | –0.3 to VCC + 4.0 (up to 5.8) | V |
| Reference power supply voltage | | VREFH0 | –0.3 to AVCC0 + 0.3 (up to 4.0) | V |
| Analog power supply voltage | | AVCC0, AVCC1*2 | –0.3 to +4.0 | V |
| Analog input voltage | | $V_{AN}$ | –0.3 to AVCC + 0.3 (up to 4.0) | V |
| Junction temperature | D version | $T_j$ | –40 to +105 | °C |
| | G version | $T_j$ | –40 to +125 | °C |
| Storage temperature | | $T_{stg}$ | –55 to +125 | °C |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS. When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

**Table 5.2 Recommended Operating Conditions**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply voltage*1 | VCC | 2.7 | — | 3.6 | V |
| | VSS | — | 0 | — | V |
| $V_{BATT}$ power supply voltage | $V_{BATT}$ | 2.0 | — | 3.6 | V |
| USB power supply voltage | VCC_USB | — | VCC | — | V |
| | VSS_USB | — | 0 | — | V |
| Analog power supply voltage*1, *2 | AVCC0 | — | VCC | — | V |
| | AVSS0 | — | 0 | — | V |
| | AVCC1 | — | VCC | — | V |
| | AVSS1 | — | 0 | — | V |
| | VREFH0 | 2.7 | — | AVCC0 | V |
| | VREFL0 | — | 0 | — | V |
| Input voltage (except for 5 V tolerant ports, except for ports 03, 05 and 40 to 47)*3 | $V_{in}$ | –0.3 | — | VCC + 0.3 | V |
| Input voltage (ports 03, 05 and 40 to 47) | $V_{in}$ | –0.3 | — | AVCC + 0.3 | V |
| Input voltage (5V tolerant ports 11 to 17, ports 20 and 21, ports 30 to 33, port 67, and ports C0 to C3)*4 | $V_{in}$ | –0.3 | — | VCC + 3.6 (up to 5.5) | V |
| Input voltage (5V tolerant port 07) | $V_{in}$ | –0.3 | — | AVCC + 3.6 (up to 5.5) | V |
| Operating temperature (D version) | $T_{opr}$ | –40 | — | 85 | °C |
| Operating temperature (G version) | $T_{opr}$ | –40 | — | 105 | °C |

Note 1. Comply with the following potential condition: VCC = AVCC0 = AVCC1 = VCC_USB

Note 2. For details, see section 53.6.11, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

Note 3. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 4. For P32, P31, and P30, input as follows when the $V_{BATT}$ power supply is selected.
$V_{in}$ Min. = –0.3, Max. = $V_{BATT}$ + 0.3 ($V_{BATT}$ = 2.0 to 3.6 V)

## 5.2 DC Characteristics

**Table 5.3 DC Characteristics (1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | IRQ input pin*1<br>MTU input pin*1<br>POE3 input pin*1<br>TPU input pin*1<br>TMR input pin*1<br>CMTW input pin*1<br>SCI input pin*1<br>CAN input pin*1<br>CAC input pin*1<br>ADTRG# input pin*1<br>QSPI input pin*1<br>RES#, NMI, TCK | $V_{IH}$ | VCC × 0.8 | — | — | V | |
| | | $V_{IL}$ | — | — | VCC × 0.2 | | |
| | | $\Delta V_T$ | VCC × 0.06 | — | — | | |
| | RIIC input pin (except for SMBus) | $V_{IH}$ | VCC × 0.7 | — | — | | |
| | | $V_{IL}$ | — | — | VCC × 0.3 | | |
| | | $\Delta V_T$ | VCC × 0.05 | — | — | | |
| | Ports for 5 V tolerant*2 | $V_{IH}$ | VCC × 0.8 | — | — | | |
| | | $V_{IL}$ | — | — | VCC × 0.2 | | |
| | Other input pins excluding ports for 5 V tolerant*3 | $V_{IH}$ | VCC × 0.8 | — | — | | |
| | | $V_{IL}$ | — | — | VCC × 0.2 | | |
| Input high voltage (except for Schmitt trigger input pin) | MD pin, EMLE | $V_{IH}$ | VCC × 0.9 | — | — | V | |
| | EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SDHI input pin, MMC input pin, PDC input pin, SDSI input pin | | VCC × 0.8 | — | — | | |
| | ETHERC input pin | | 2.3 | — | — | | |
| | D0 to D31 | | VCC × 0.7 | — | — | | |
| | RIIC (SMBus) | | 2.1 | — | — | | |
| Input low voltage (except for Schmitt trigger input pin) | MD pin, EMLE | $V_{IL}$ | — | — | VCC × 0.1 | V | |
| | EXTAL, RSPI input pin, ETHERC input pin, EXDMAC input pin, WAIT#, SDHI input pin, MMC input pin, PDC input pin, SDSI input pin | | — | — | VCC × 0.2 | | |
| | D0 to D31 | | — | — | VCC × 0.3 | | |
| | RIIC (SMBus) | | — | — | 0.8 | | |

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.
Note 3. For P32, P31, and P30, input as follows when the $V_{BATT}$ power supply is selected.
$V_{IH}$ Min. = $V_{BATT}$ × 0.8, $V_{IL}$ Max. = $V_{BATT}$ × 0.2 ($V_{BATT}$ = 2.0 to 3.6 V)

**Table 5.4 DC Characteristics (2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output high voltage | All output pins | $V_{OH}$ | VCC – 0.5 | — | — | V | $I_{OH}$ = –1 mA |
| Output low voltage | All output pins (except for RIIC pins and ETHERC output pin) | $V_{OL}$ | — | — | 0.5 | V | $I_{OL}$ = 1.0 mA |
| | RIIC output pin | | — | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | | — | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| | RIIC output pin (only P12 and P13 in channel 0) | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 15.0 mA (ICFER.FMPE = 1) |
| | | | — | 0.4 | — | | $I_{OL}$ = 20.0 mA (ICFER.FMPE = 1) |
| | ETHERC output pin | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.0 mA |
| Input leakage current | RES#, MD pin, EMLE*1, BSCANP*1, NMI | $\lvert I_{in} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| Three-state leakage current (off state) | Other than ports for 5 V tolerant | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| | Ports for 5 V tolerant | | — | — | 5.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = 5.5 V |
| Input pull-up resistor current | Other than P35 | $I_p$ | –300 | — | –10 | µA | VCC = 2.7 to 3.6 V<br>$V_{in}$ = 0 V |
| Input pull-down resistor current | EMLE, BSCANP | $I_p$ | 10 | — | 300 | µA | $V_{in}$ = VCC |
| Input capacitance | All input pins (except for ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM) | $C_{in}$ | — | — | 8 | pF | Vbias = 0 V<br>Vamp = 20 mV<br>f = 1 MHz<br>$T_a$ = 25°C |
| | Ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM | | — | — | 16 | | |

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when $V_{in}$ = 0 V.

**Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | | Symbol | D version | | G version | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typ. | Max. | Typ. | Max. | | |
| Supply current*1 | High-speed operating mode | Full operation*2 | | $I_{CC}$*3 | — | 40 | — | 45 | mA | ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 60 MHz, FCLK = 60 MHz, BCLK = 120 MHz, BCLK pin = 60 MHz |
| | | Normal operation | Peripheral module clocks are supplied *4 | | 22 | — | 22 | — | | |
| | | | Peripheral module clocks are stopped *4, *5 | | 12 | — | 12 | — | | |
| | | Core Mark | Peripheral module clocks are stopped *4, *5 | | 15 | — | 15 | — | | |
| | | Sleep mode: Peripheral module clocks are supplied*4 | | | 16 | 24 | 16 | 28 | | |
| | | All module clock stop mode (reference value) | | | 8 | 15 | 8 | 19 | | |
| | Low-speed operating mode 1: Peripheral module clocks are stopped*4 | | | | 1.1 | — | 1.1 | — | | All clocks 1 MHz |
| | Low-speed operating mode 2: Peripheral module clocks are stopped*4 | | | | 1.1 | — | 1.1 | — | | All clocks 32.768 kHz |
| | Software standby mode | | | | 1.6 | 6.4 | 1.6 | 9.8 | | |
| | Deep software standby mode | Power is supplied to the standby RAM and USB resume detecting unit (USB0 only) | | | 15.5 | 61 | 15.5 | 85 | μA | |
| | | Power is not supplied to the standby RAM and USB resume detecting unit (USB0 only) | Low power consumption function of the power-on reset circuit is disabled*6 | | 11.5 | 38 | 11.5 | 48 | | |
| | | | Low power consumption function of the power-on reset circuit is enabled*7 | | 4.9 | 29 | 4.9 | 39 | | |
| | | Increase current by operating RTC | When a low $C_L$ crystal is in use | | 1 | — | 1 | — | | |
| | | | When a standard $C_L$ crystal is in use | | 2 | — | 2 | — | | |
| | When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function) | | When a low $C_L$ crystal is in use | | 0.9 | — | 0.9 | — | | $V_{BATT}$ = 2.0 V, VCC = 0 V |
| | | | | | 1.6 | — | 1.6 | — | | $V_{BATT}$ = 3.3 V, VCC = 0 V |
| | | | When a standard $C_L$ crystal is in use | | 1.7 | — | 1.7 | — | | $V_{BATT}$ = 2.0 V, VCC = 0 V |
| | | | | | 3.3 | — | 3.3 | — | | $V_{BATT}$ = 3.3 V, VCC = 0 V |
| | Inrush current on release from deep software standby mode | Inrush current*8 | | $I_{RUSH}$ | — | 70 | — | 70 | mA | |
| | | Total inrush current*8 | | $E_{RUSH}$ | — | 1.0 | — | 1.0 | μC | |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied.
Note 3. $I_{CC}$ depends on the f (ICLK) as follows (when ICLK/PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 2 : 1 : 2 : 1 and EXTAL = 12 MHz).
- D version
  $I_{CC}$ max = 0.31 × f + 6.5 (full operation in high-speed operating mode)
  $I_{CC}$ typ = 0.16 × f + 2.8 (normal operation in high-speed operating mode)
  $I_{CC}$ typ = 0.1 × f + 1.0 (ICLK 1 MHz max) (low-speed operating mode 1)
  $I_{CC}$ max = 0.15 × f + 6.5 (sleep mode)
- G version
  $I_{CC}$ max = 0.33 × f + 9 (full operation in high-speed operating mode)
  $I_{CC}$ typ = 0.16 × f + 2.8 (normal operation in high-speed operating mode)
  $I_{CC}$ typ = 0.1 × f + 1.0 (ICLK 1 MHz max) (low-speed operating mode 1)
  $I_{CC}$ max = 0.21 × f + 9 (sleep mode)

Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:
ICLK = 120 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = BCLK pin = 3.75 MHz (divided by 64).

Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.
Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.
Note 8. Reference value

### Table 5.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | | Symbol | D version | | G version | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typ. | Max. | Typ. | Max. | | |
| Supply current*1 | High-speed operating mode | Full operation*2 | | $I_{CC}$*3 | — | 60 | — | 73 | mA | ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 60 MHz, FCLK = 60 MHz, BCLK = 120 MHz, BCLK pin = 60 MHz |
| | | Normal operation | Peripheral module clocks are supplied*4 | | 26 | — | 26 | — | | |
| | | | Peripheral module clocks are stopped *4, *5 | | 13 | — | 13 | — | | |
| | | Core Mark | Peripheral module clocks are stopped *4, *5 | | 17 | — | 17 | — | | |
| | | Sleep mode: Peripheral module clocks are supplied *4 | | | 20 | 38 | 20 | 52 | | |
| | | All module clock stop mode (reference value) | | | 9 | 26 | 9 | 39 | | |
| | | Increased by BGO operation *8 | Reading from the code flash memory while the data flash memory is being programmed | | 6 | — | 6 | — | | |
| | | | Reading from the code flash memory while the code flash memory is being programmed | | 7 | — | 7 | — | | |
| | | Increased by Trusted Secure IP operation | | | — | 12 | — | 12 | | |
| | Low-speed operating mode 1: Peripheral module clocks are stopped*4 | | | | 1.6 | — | 1.6 | — | | All clocks 1 MHz |
| | Low-speed operating mode 2: Peripheral module clocks are stopped*4 | | | | 1.6 | — | 1.6 | — | | All clocks 32.768 kHz |
| | Software standby mode | | | | 1.6 | 13 | 1.6 | 22.4 | | |
| | Deep software standby mode | Power is supplied to the standby RAM and USB resume detecting unit (USB0 only) | | | 15.5 | 70 | 15.5 | 98 | μA | |
| | | Power is not supplied to the standby RAM and USB resume detecting unit (USB0 only) | Low power consumption function of the power-on reset circuit is disabled*6 | | 11.5 | 42 | 11.5 | 54 | | |
| | | | Low power consumption function of the power-on reset circuit is enabled*7 | | 4.9 | 32 | 4.9 | 47 | | |
| | | Increase current by operating RTC | When a low $C_L$ crystal is in use | | 1 | — | 1 | — | | |
| | | | When a standard $C_L$ crystal is in use | | 2 | — | 2 | — | | |
| | When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function) | | When a low $C_L$ crystal is in use | | 0.9 | — | 0.9 | — | | $V_{BATT}$ = 2.0 V, VCC = 0 V |
| | | | | | 1.6 | — | 1.6 | — | | $V_{BATT}$ = 3.3 V, VCC = 0 V |
| | | | When a standard $C_L$ crystal is in use | | 1.7 | — | 1.7 | — | | $V_{BATT}$ = 2.0 V, VCC = 0 V |
| | | | | | 3.3 | — | 3.3 | — | | $V_{BATT}$ = 3.3 V, VCC = 0 V |
| | Inrush current on release from deep software standby mode | | Inrush current*9 | $I_{RUSH}$ | — | 130 | — | 130 | mA | |
| | | | Total inrush current*9 | $E_{RUSH}$ | — | 1.0 | — | 1.0 | μC | |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied.
Note 3. $I_{CC}$ depends on the f (ICLK) as follows (when ICLK/PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 2 : 1 : 2 : 1 and EXTAL = 12 MHz).
- D version
  $I_{CC}$ max = 0.38 × f + 14 (full operation in high-speed operating mode)
  $I_{CC}$ typ = 0.18 × f + 4 (normal operation in high-speed operating mode)

$I_{CC}$ typ = 0.1 × f + 1.5 (ICLK 1 MHz max) (low-speed operating mode 1)
$I_{CC}$ max = 0.2 × f + 14 (sleep mode)

- G version
  $I_{CC}$ max = 0.44 × f + 20 (full operation in high-speed operating mode)
  $I_{CC}$ typ = 0.18 × f + 4 (normal operation in high-speed operating mode)
  $I_{CC}$ typ = 0.1 × f + 1.5 (ICLK 1 MHz max) (low-speed operating mode 1)
  $I_{CC}$ max = 0.27 × f + 20 (sleep mode)

Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:
ICLK = 120 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = BCLK pin = 3.75 MHz (divided by 64).
Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.
Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.
Note 8. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.
Note 9. Reference value

### Table 5.7 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | D version | | | G version | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Analog power supply current*1 | During 12-bit A/D conversion (unit 0) | | $AI_{CC}$ | — | 0.8 | 1 | — | 0.8 | 1 | mA | IAVCC0_AD |
| | During 12-bit A/D conversion (unit 0) with channel dedicated sample-and-hold circuits (3 channels) | | | — | 1.7 | 2.5 | — | 1.7 | 2.5 | mA | IAVCC0_AD + SH |
| | During 12-bit A/D conversion (unit 1) | | | — | 0.6 | 1 | — | 0.6 | 1 | mA | IAVCC1_AD |
| | During 12-bit A/D conversion (unit 1) + temperature sensor | | | — | 0.7 | 1.1 | — | 0.7 | 1.1 | mA | IAVCC1_AD + TEMP |
| | During D/A conversion (per unit) | Unbuffered output | | — | 0.25 | 0.4 | — | 0.25 | 0.4 | mA | IAVCC1_DA |
| | | Buffered output | | — | 0.75 | 1.1 | — | 0.75 | 1.1 | mA | |
| | Waiting for A/D, D/A, and temperature sensor conversion (all units) | | | — | 0.9 | 1.4 | — | 0.9 | 1.4 | mA | IAVCC0 + IAVCC1 |
| | A/D, D/A, and temperature sensor are in standby mode (all units) | | | — | 1.4 | 6.7 | — | 1.4 | 9.0 | µA | IAVCC0 + IAVCC1 |
| Reference power supply current | During 12-bit A/D conversion (unit 0) | | $AI_{REFH}$ | — | 38 | 60 | — | 38 | 60 | µA | IVREFH0 |
| | Waiting for 12-bit A/D conversion (unit 0) | | | — | 0.07 | 0.5 | — | 0.07 | 0.6 | µA | IVREFH0 |
| | 12-bit A/D converter in module stop status (unit 0) | | | — | 0.07 | 0.4 | — | 0.07 | 0.5 | µA | IVREFH0 |
| USB operating current | Low speed | USB0 | $I_{CCUSBLS}$ | — | 3.7 | 6.5 | — | 3.7 | 6.5 | mA | VCC_USB |
| | Full speed | USB0 | $I_{CCUSBFS}$ | — | 4.2 | 10 | — | 4.2 | 10 | mA | VCC_USB |
| RAM retension voltage | | | $V_{RAM}$ | 2.7 | — | — | 2.7 | — | — | V | |
| VCC rising gradient | | | SrVCC | 8.4 | — | 20000 | 8.4 | — | 20000 | µs/V | |
| VCC falling gradient*2 | | | SfVCC | 8.4 | — | — | 8.4 | — | — | µs/V | |

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D converter (unit 1) and D/A converter.
Note 2. This applies when $V_{BATT}$ is used.

**Table 5.8 Permissible Output Currents**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output low current (average value per pin) | All output pins*1 | Normal drive | $I_{OL}$ | — | — | 2.0 | mA |
| | All output pins*2 | High drive | $I_{OL}$ | — | — | 3.8 | mA |
| | All output pins*3 | High-speed interface high-drive | $I_{OL}$ | — | — | 7.5 | mA |
| Permissible output low current (max. value per pin) | All output pins*1 | Normal drive | $I_{OL}$ | — | — | 4.0 | mA |
| | All output pins*2 | High drive | $I_{OL}$ | — | — | 7.6 | mA |
| | All output pins*3 | High-speed interface high-drive | $I_{OL}$ | — | — | 15 | mA |
| Permissible output low current (total) | Total of all output pins | | $\Sigma I_{OL}$ | — | — | 80 | mA |
| Permissible output high current (average value per pin) | All output pins*1 | Normal drive | $I_{OH}$ | — | — | –2.0 | mA |
| | All output pins*2 | High drive | $I_{OH}$ | — | — | –3.8 | mA |
| | All output pins*3 | High-speed interface high-drive | $I_{OH}$ | — | — | –7.5 | mA |
| Permissible output high current (max. value per pin) | All output pins*1 | Normal drive | $I_{OH}$ | — | — | –4.0 | mA |
| | All output pins*2 | High drive | $I_{OH}$ | — | — | –7.6 | mA |
| | All output pins*3 | High-speed interface high-drive | $I_{OH}$ | — | — | –15 | mA |
| Permissible output high current (total) | Total of all output pins | | $\Sigma I_{OH}$ | — | — | –80 | mA |

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

**Table 5.9 Thermal Resistance Value (Reference)**

| Item | Package | Symbol | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Thermal resistance | 176-pin LFQFP (PLQP0176KB-A) | $\theta_{ja}$ | 48.0 | °C/W | JESD51-2 and JESD51-7 compliant |
| | 144-pin LFQFP (PLQP0144KA-B) | | 50.9 | | |
| | 100-pin LFQFP (PLQP0100KB-B) | | 52.5 | | |
| | 64-pin LFQFP (PLQP0064KB-C) | | 53.7 | | |
| | 177-pin TFLGA (PTLG0177KA-A) | | 36.3 | | JESD51-2 and JESD51-9 compliant |
| | 176-pin LFBGA (PLBG0176GA-A) | | 35.4 | | |
| | 145-pin TFLGA (PTLG0145KA-A) | | 34.6 | | |
| | 100-pin TFLGA (PTLG0100JA-A) | | 34.1 | | |
| | 64-pin TFBGA (PTBG0064KB-A) | | 35.3 | | |
| | 176-pin LFQFP (PLQP0176KB-A) | $\Psi_{jt}$ | 1.0 | °C/W | JESD51-2 and JESD51-7 compliant |
| | 144-pin LFQFP (PLQP0144KA-B) | | 1.5 | | |
| | 100-pin LFQFP (PLQP0100KB-B) | | 1.5 | | |
| | 64-pin LFQFP (PLQP0064KB-C) | | 1.5 | | |
| | 177-pin TFLGA (PTLG0177KA-A) | | 0.3 | | JESD51-2 and JESD51-9 compliant |
| | 176-pin LFBGA (PLBG0176GA-A) | | 0.3 | | |
| | 145-pin TFLGA (PTLG0145KA-A) | | 0.4 | | |
| | 100-pin TFLGA (PTLG0100JA-A) | | 0.4 | | |
| | 64-pin TFBGA (PTBG0064KB-A) | | 0.5 | | |

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

## 5.3 AC Characteristics

### Table 5.10 Operating Frequency (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | | f | — | — | 120 | MHz |
| | Peripheral module clock (PCLKA) | | | — | — | 120 | |
| | Peripheral module clock (PCLKB) | | | — | — | 60 | |
| | Peripheral module clock (PCLKC) | | | — | — | 60 | |
| | Peripheral module clock (PCLKD) | | | — | — | 60 | |
| | Flash-IF clock (FCLK) | | | —*1 | — | 60 | |
| | External bus clock (BCLK) | Package of 144 pins or more | | — | — | 120 | |
| | | 100-pin package | | — | — | 60 | |
| | BCLK pin output | Package of 144 pins or more | | — | — | 60 | |
| | | 100-pin package | | — | — | 30 | |
| | SDRAM clock (SDCLK) | Package of 144 pins or more | | — | — | 60 | |
| | SDCLK pin output | Package of 144 pins or more | | — | — | 60 | |

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

### Table 5.11 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | | f | — | — | 1 | MHz |
| | Peripheral module clock (PCLKA) | | | — | — | 1 | |
| | Peripheral module clock (PCLKB) | | | — | — | 1 | |
| | Peripheral module clock (PCLKC)*1 | | | — | — | 1 | |
| | Peripheral module clock (PCLKD)*1 | | | — | — | 1 | |
| | Flash-IF clock (FCLK) | | | — | — | 1 | |
| | External bus clock (BCLK) | Package of 144 pins or more | | — | — | 1 | |
| | | 100-pin package | | — | — | 1 | |
| | BCLK pin output | Package of 144 pins or more | | — | — | 1 | |
| | | 100-pin package | | — | — | 1 | |
| | SDRAM clock (SDCLK) | Package of 144 pins or more | | — | — | 1 | |
| | SDCLK pin output | Package of 144 pins or more | | — | — | 1 | |

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

**Table 5.12 Operating Frequency (Low-Speed Operating Mode 2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | | f | 32 | — | 264 | kHz |
| | Peripheral module clock (PCLKA) | | | — | — | 264 | |
| | Peripheral module clock (PCLKB) | | | — | — | 264 | |
| | Peripheral module clock (PCLKC)*1 | | | — | — | 264 | |
| | Peripheral module clock (PCLKD)*1 | | | — | — | 264 | |
| | Flash-IF clock (FCLK) | | | 32 | — | 264 | |
| | External bus clock (BCLK) | Package of 144 pins or more | | — | — | 264 | |
| | | 100-pin package | | — | — | 264 | |
| | BCLK pin output | Package of 144 pins or more | | — | — | 264 | |
| | | 100-pin package | | — | — | 264 | |
| | SDRAM clock (SDCLK) | Package of 144 pins or more | | — | — | 264 | |
| | SDCLK pin output | Package of 144 pins or more | | — | — | 264 | |

Note 1. The 12-bit A/D converter cannot be used.

### 5.3.1 Reset Timing

**Table 5.13 Reset Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RES# pulse width | Power-on | $t_{RESWP}$ | 1 | — | — | ms | Figure 5.1 |
| | Deep software standby mode | $t_{RESWD}$ | 0.6 | — | — | ms | Figure 5.2 |
| | Software standby mode, low-speed operating mode 2 | $t_{RESWS}$ | 0.3 | — | — | ms | |
| | Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory | $t_{RESWF}$ | 200 | — | — | µs | |
| | Other than above | $t_{RESW}$ | 200 | — | — | µs | |
| Waiting time after release from the RES# pin reset | | $t_{RESWT}$ | 54 | — | 55 | $t_{Lcyc}$ | Figure 5.1 |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | | $t_{RESW2}$ | 100 | — | 108 | $t_{Lcyc}$ | |

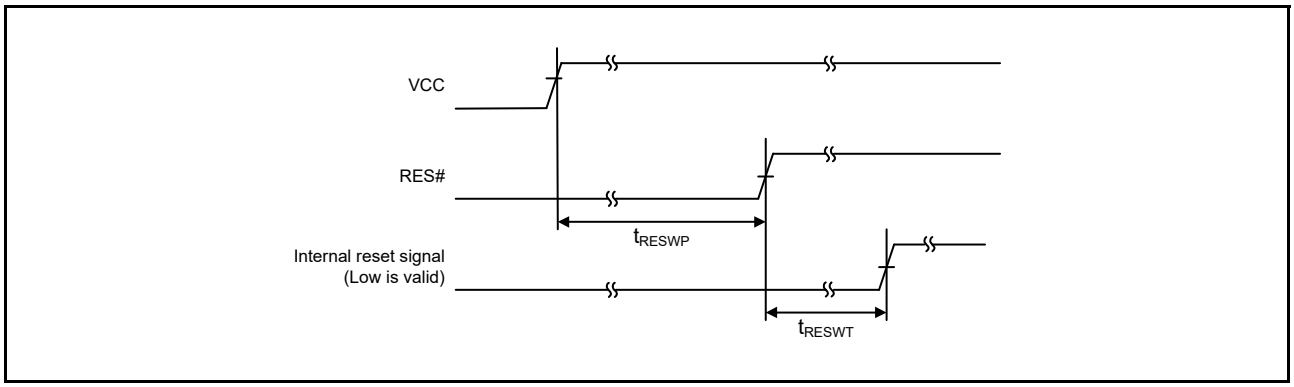



**Figure 5.1 Reset Input Timing at Power-On**

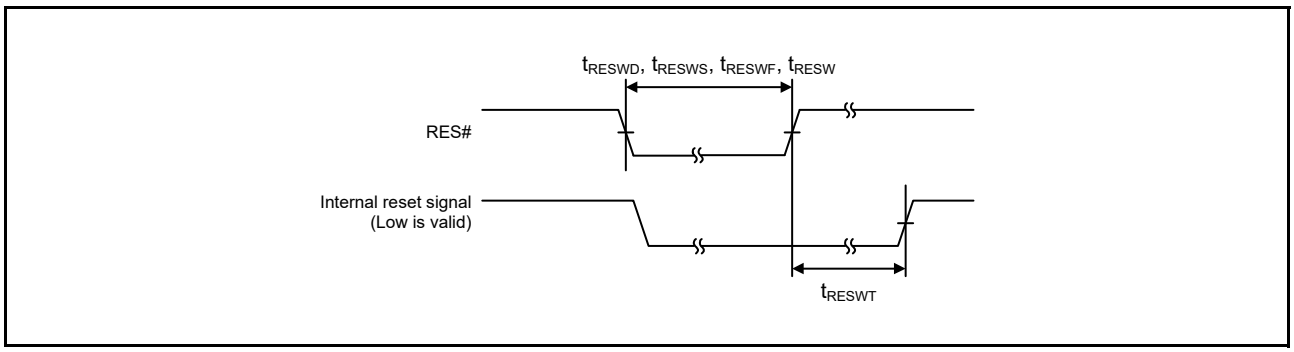



**Figure 5.2 Reset Input Timing**

## 5.3.2 Clock Timing

**Table 5.14 BCLK Pin Output, SDCLK Pin Output Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| BCLK pin output cycle time | Package of 144 pins or more | $t_{Bcyc}$ | 16.6 | — | — | ns | Figure 5.3 |
| | 100-pin package | | 33.2 | — | — | ns | |
| BCLK pin output high pulse width | | $t_{CH}$ | 3.3 | — | — | ns | |
| BCLK pin output low pulse width | | $t_{CL}$ | 3.3 | — | — | ns | |
| BCLK pin output rising time | | $t_{Cr}$ | — | — | 5 | ns | |
| BCLK pin output falling time | | $t_{Cf}$ | — | — | 5 | ns | |
| SDCLK pin output cycle time | Package of 144 pins or more | $t_{Bcyc}$ | 16.6 | — | — | ns | |
| SDCLK pin output high pulse width | | $t_{CH}$ | 3.3 | — | — | ns | |
| SDCLK pin output low pulse width | | $t_{CL}$ | 3.3 | — | — | ns | |
| SDCLK pin output rising time | | $t_{Cr}$ | — | — | 5 | ns | |
| SDCLK pin output falling time | | $t_{Cf}$ | — | — | 5 | ns | |

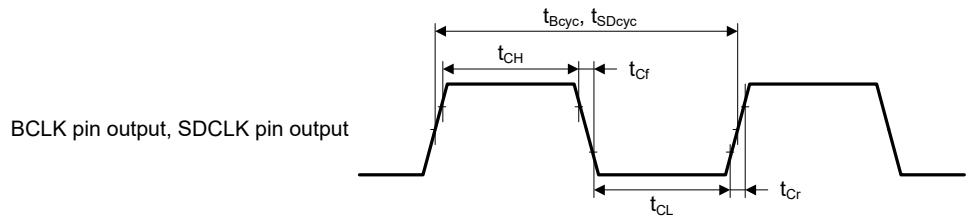



**Figure 5.3 BCLK Pin and SDCLK Pin Output Timing**

### Table 5.15 EXTAL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| EXTAL external clock input cycle time | $t_{EXcyc}$ | 41.66 | — | — | ns | Figure 5.4 |
| EXTAL external clock input frequency | $f_{EXMAIN}$ | — | — | 24 | MHz | |
| EXTAL external clock input high pulse width | $t_{EXH}$ | 15.83 | — | — | ns | |
| EXTAL external clock input low pulse width | $t_{EXL}$ | 15.83 | — | — | ns | |
| EXTAL external clock rising time | $t_{EXr}$ | — | — | 5 | ns | |
| EXTAL external clock falling time | $t_{EXf}$ | — | — | 5 | ns | |

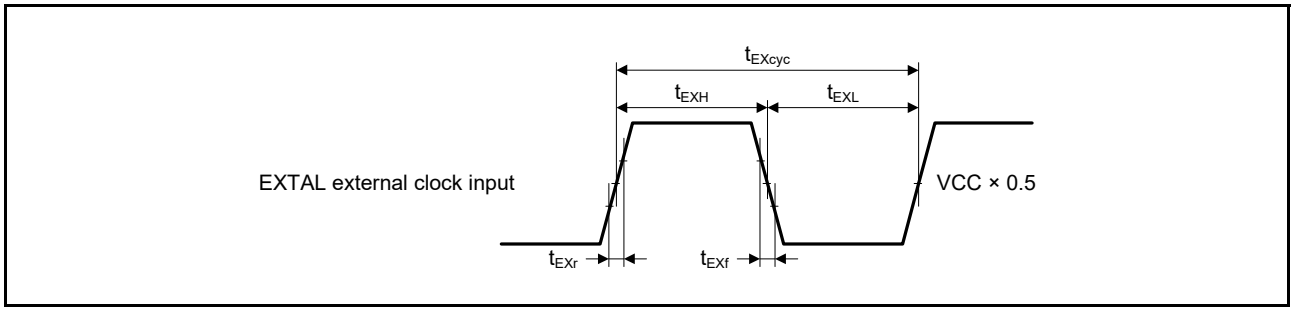



**Figure 5.4 EXTAL External Clock Input Timing**

### Table 5.16 Main Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Main clock oscillation frequency | $f_{MAIN}$ | 8 | — | 24 | MHz | |
| Main clock oscillator stabilization time (crystal) | $t_{MAINOSC}$ | — | — | —*1 | ms | Figure 5.5 |
| Main clock oscillation stabilization wait time (crystal) | $t_{MAINOSCWT}$ | — | — | —*2 | ms | |

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / $f_{LOCO}$

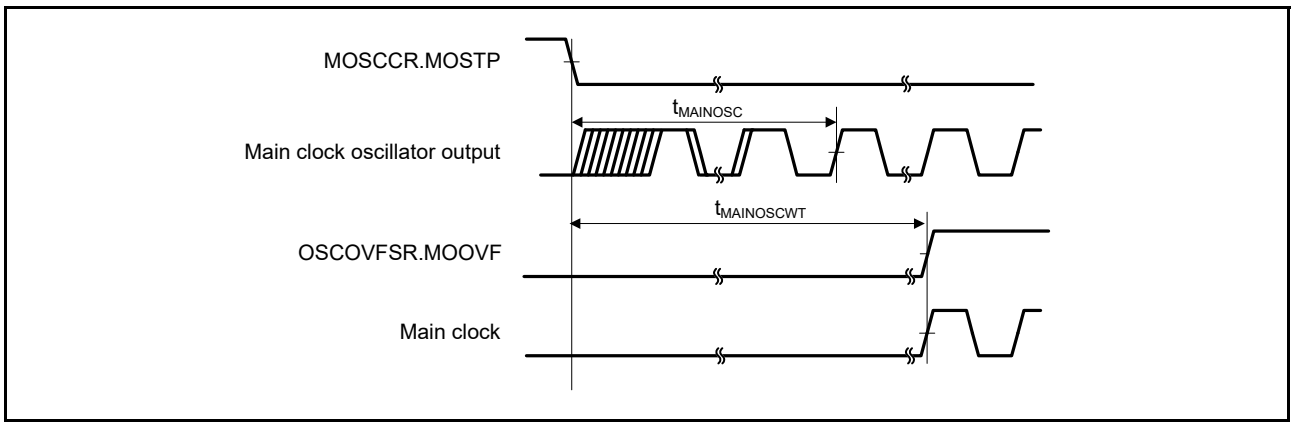



**Figure 5.5 Main Clock Oscillation Start Timing**

**Table 5.17 LOCO and IWDT-Dedicated Low-Speed Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| LOCO clock cycle time | $t_{Lcyc}$ | 4.63 | 4.16 | 3.78 | µs | |
| LOCO clock oscillation frequency | $f_{LOCO}$ | 216 | 240 | 264 | kHz | |
| LOCO clock oscillation stabilization wait time | $t_{LOCOWT}$ | — | — | 44 | µs | Figure 5.6 |
| IWDT-dedicated low-speed clock cycle time | $t_{ILcyc}$ | 9.26 | 8.33 | 7.57 | µs | |
| IWDT-dedicated low-speed clock oscillation frequency | $f_{ILOCO}$ | 108 | 120 | 132 | kHz | |
| IWDT-dedicated low-speed clock oscillation stabilization wait time | $t_{ILOCOWT}$ | — | 142 | 190 | µs | Figure 5.7 |

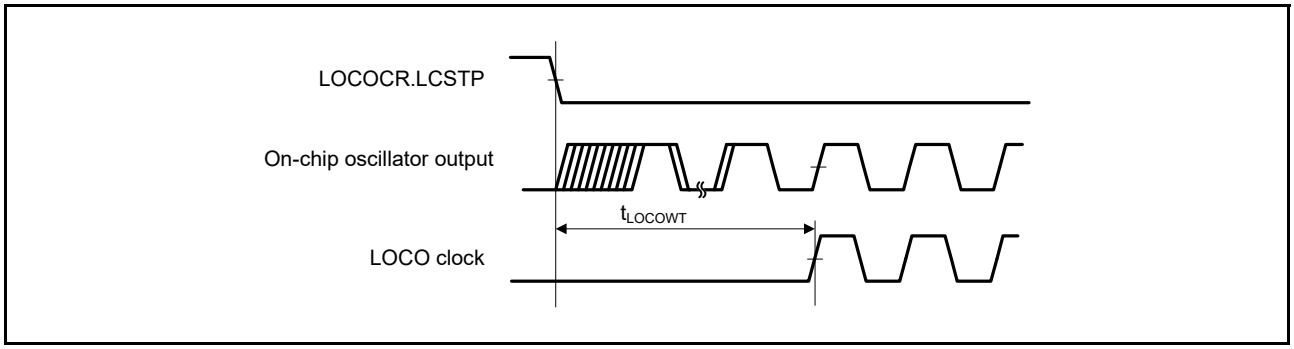



**Figure 5.6 LOCO Clock Oscillation Start Timing**

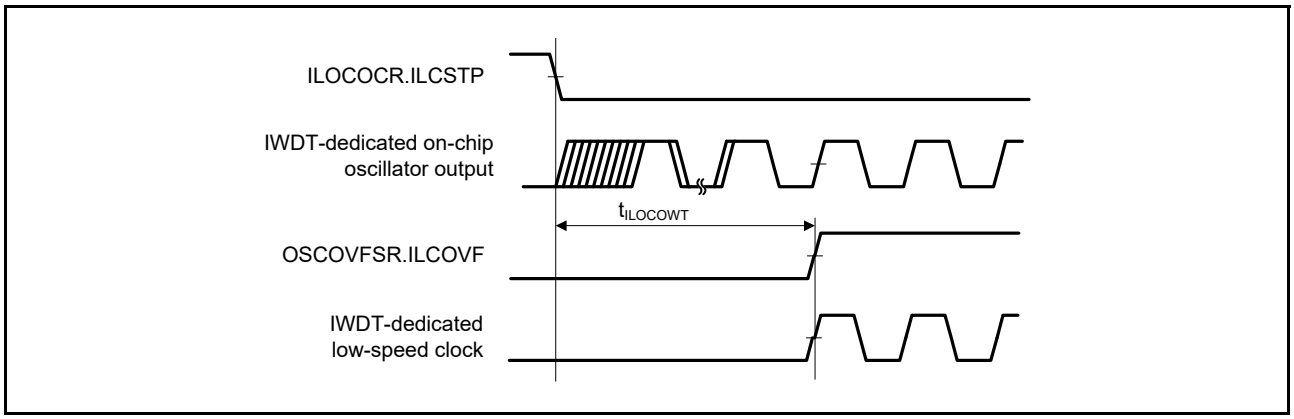



**Figure 5.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing**

**Table 5.18 HOCO Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| HOCO clock oscillation frequency | $f_{HOCO}$ | 15.61 | 16 | 16.39 | MHz | –20°C ≤ $T_a$ ≤ 105°C |
| | | 17.56 | 18 | 18.44 | MHz | |
| | | 19.52 | 20 | 20.48 | MHz | |
| | | 15.52 | 16 | 16.48 | MHz | –40°C ≤ $T_a$ < –20°C |
| | | 17.46 | 18 | 18.54 | MHz | |
| | | 19.4 | 20 | 20.6 | MHz | |
| HOCO clock oscillation stabilization wait time | $t_{HOCOWT}$ | — | 105 | 149 | µs | Figure 5.8 |
| HOCO clock power supply stabilization time | $t_{HOCOP}$ | — | — | 150 | µs | Figure 5.9 |

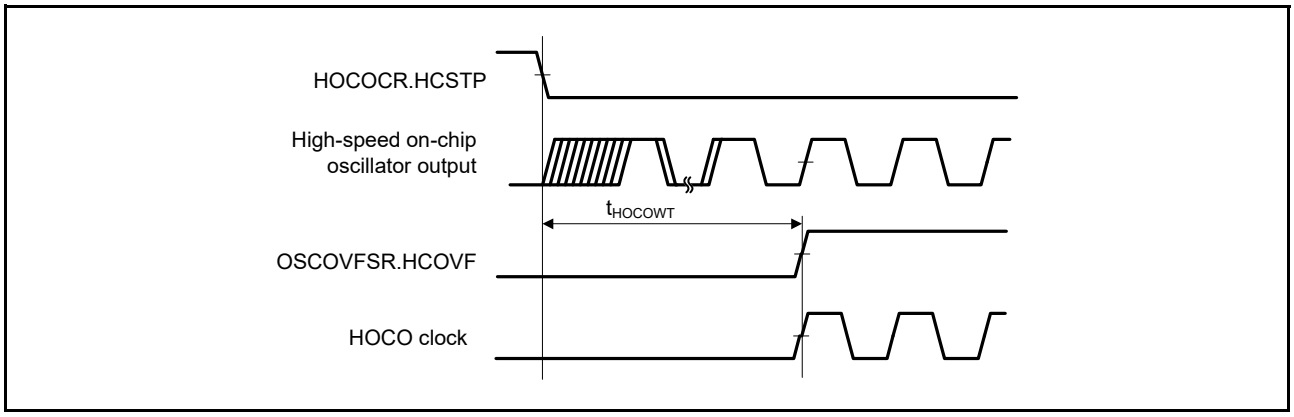



**Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)**

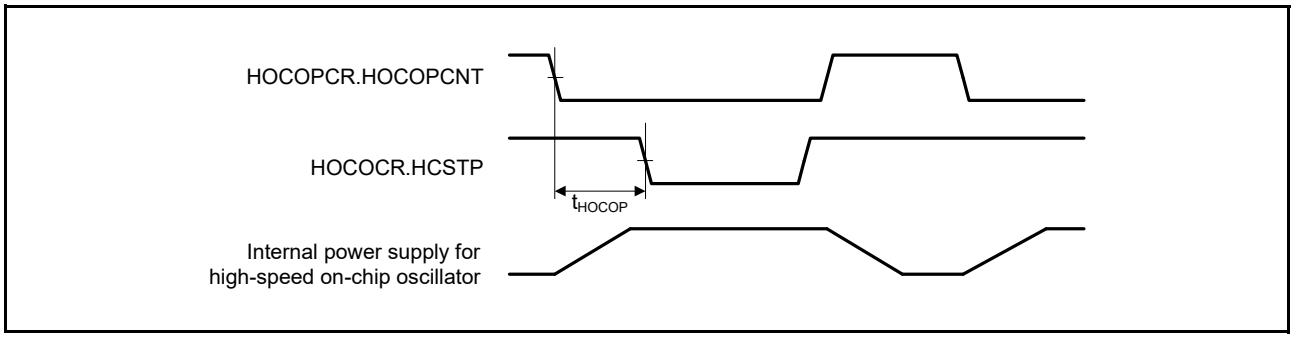



**Figure 5.9 High-Speed On-Chip Oscillator Power Supply Control Timing**

**Table 5.19 PLL Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| PLL clock oscillation frequency | $f_{PLL}$ | 120 | — | 240 | MHz | |
| PLL clock oscillation stabilization wait time | $t_{PLLWT}$ | — | 259 | 320 | µs | Figure 5.10 |

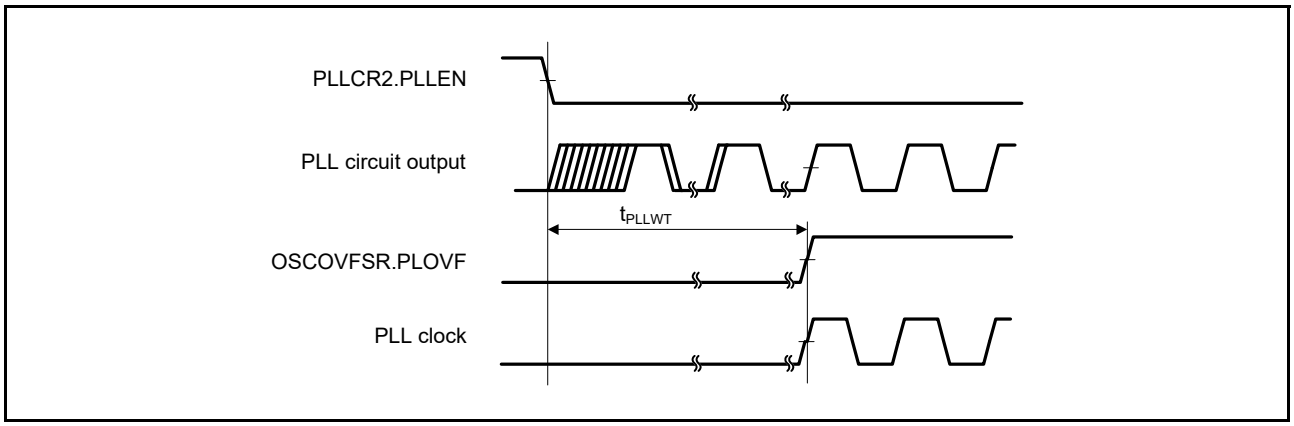



**Figure 5.10 PLL Clock Oscillation Start Timing**

**Table 5.20 Sub-Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$V_{BATT}$ = 2.0 to 3.6 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sub-clock oscillation frequency | $f_{SUB}$ | — | 32.768 | — | kHz | |
| Sub-clock oscillation stabilization time | $t_{SUBOSC}$ | — | — | *1 | s | Figure 5.11 |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | — | — | *2 | s | |

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the SOSCWTCR.SSTS[7:0] bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.
$t_{SUBOSCWT}$ = [(SSTS[7:0] bits × 16384) + 10] / $f_{LOCO}$

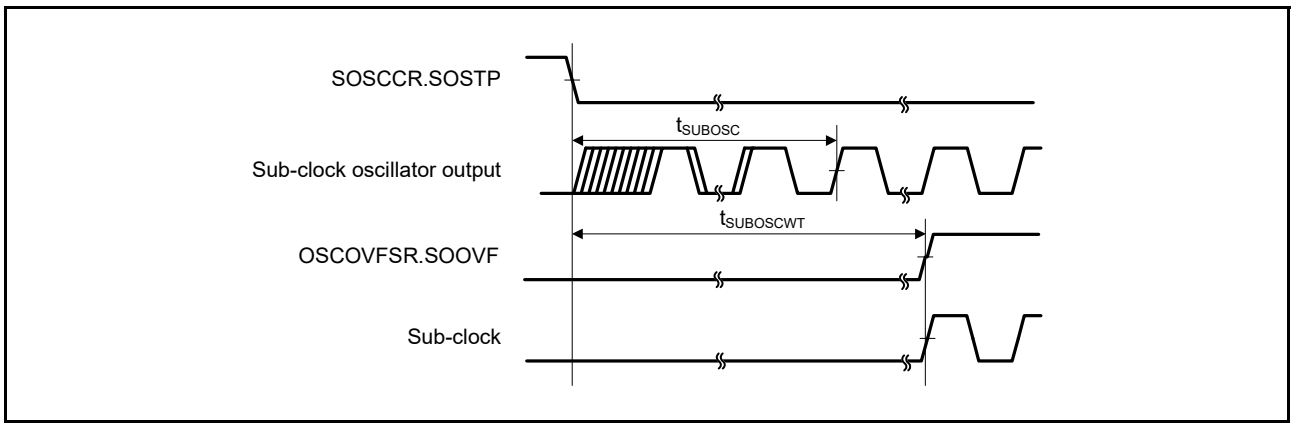



**Figure 5.11 Sub-Clock Oscillation Start Timing**

## 5.3.3 Timing of Recovery from Low Power Consumption Modes

**Table 5.21 Timing of Recovery from Low Power Consumption Modes (1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $t_{SBYOSCWT}$*2 | $t_{SBYSEQ}$*3 | | |
| Recovery time from software standby mode *1 | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | $t_{SBYMC}$ | — | — | {(MSTS[7:0] bit × 32) + 76} / 0.216 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{MAIN}$ | µs | Figure 5.12 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | | | {(MSTS[7:0] bit × 32) + 138} / 0.216 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | | | 352 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{EXMAIN}$ | | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | | | 639 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | Sub-clock oscillator operating | | $t_{SBYSC}$ | | | {(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10 / $f_{FCLK}$ | 100 + 4 / $f_{ICLK}$ + 2n / $f_{SUE}$ | | |
| | High-speed on-chip oscillator operating | High-speed on-chip oscillator operating | $t_{SBYHO}$ | | | 454 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{HOCO}$ | | |
| | | High-speed on-chip oscillator operating and PLL circuit operating | $t_{SBYPH}$ | | | 741 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | Low-speed on-chip oscillator operating*4 | | $t_{SBYLO}$ | | | 338 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{LOCO}$ | | |

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer ($t_{SBYSEQ}$).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when $f_{ICLK}$:$f_{FCLK}$ = 1:1, 2:1, or 4:1.

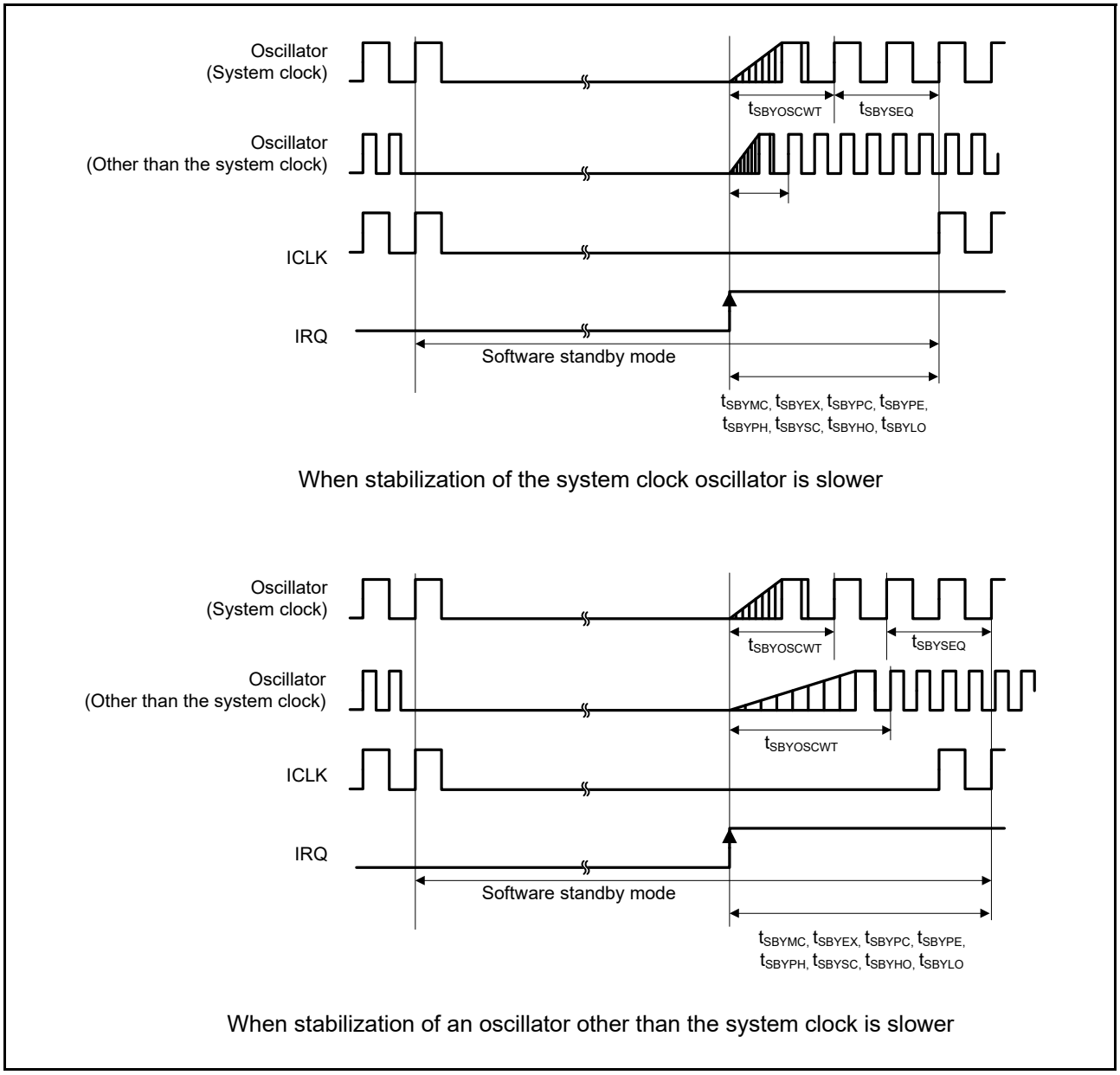



**Figure 5.12 Software Standby Mode Recovery Timing**

**Table 5.22 Timing of Recovery from Low Power Consumption Modes (2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Recovery time from deep software standby mode | $t_{DSBY}$ | — | — | 0.9 | ms | Figure 5.13 |
| Wait time after recovery from deep software standby mode | $t_{DSBYWT}$ | 23 | — | 24 | $t_{Lcyc}$ | |

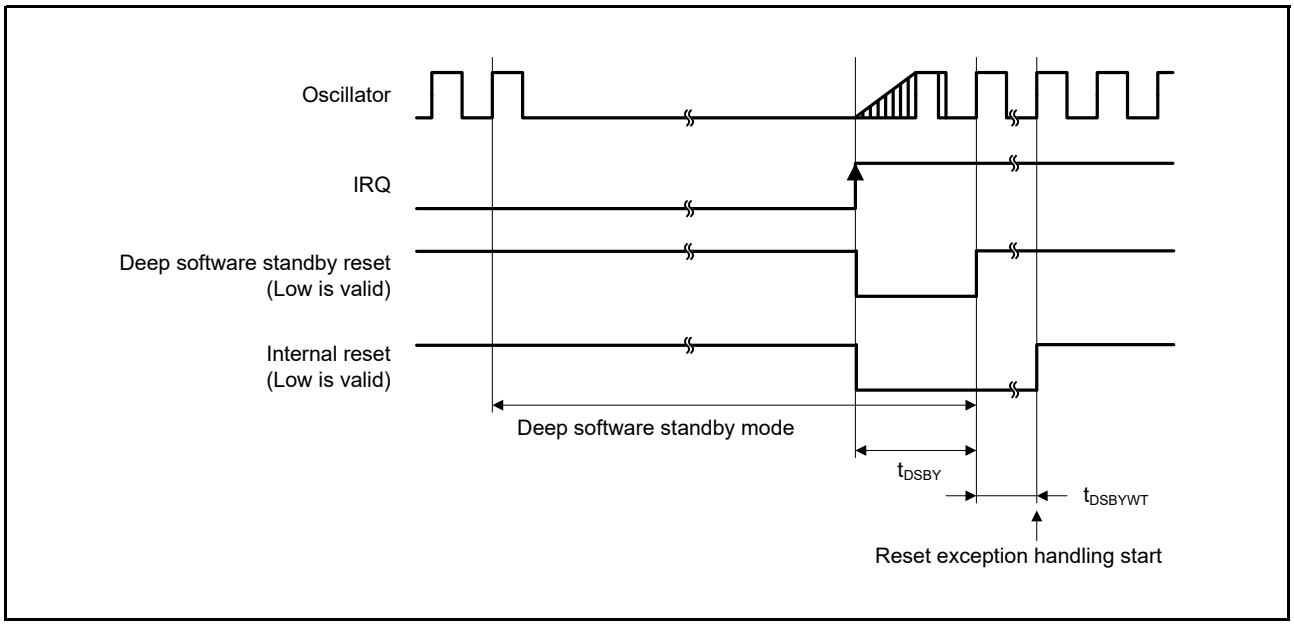



**Figure 5.13 Deep Software Standby Mode Recovery Timing**

## 5.3.4 Control Signal Timing

**Table 5.23 Control Signal Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | Symbol | Min.*1 | Typ. | Max. | Unit | Test Conditions*1 |
|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | $t_{PBcyc}$ × 2 ≤ 200 ns, Figure 5.14 |
| | | $t_{PBcyc}$ × 2 | — | — | ns | $t_{PBcyc}$ × 2 > 200 ns, Figure 5.14 |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | $t_{PBcyc}$ × 2 ≤ 200 ns, Figure 5.15 |
| | | $t_{PBcyc}$ × 2 | — | — | ns | $t_{PBcyc}$ × 2 > 200 ns, Figure 5.15 |

Note 1. $t_{PBcyc}$: PCLKB cycle

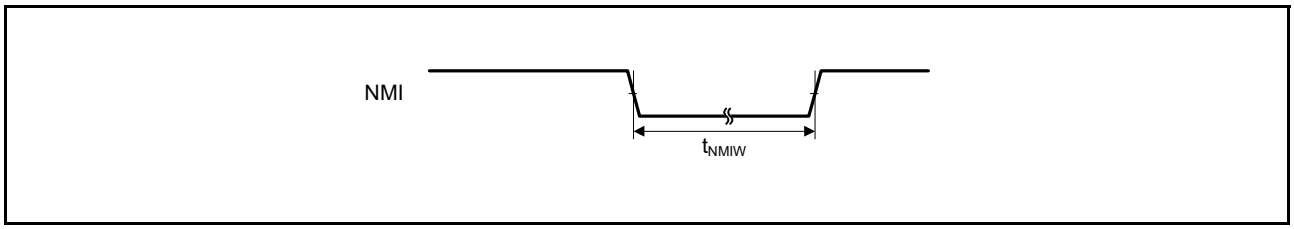



**Figure 5.14 NMI Interrupt Input Timing**

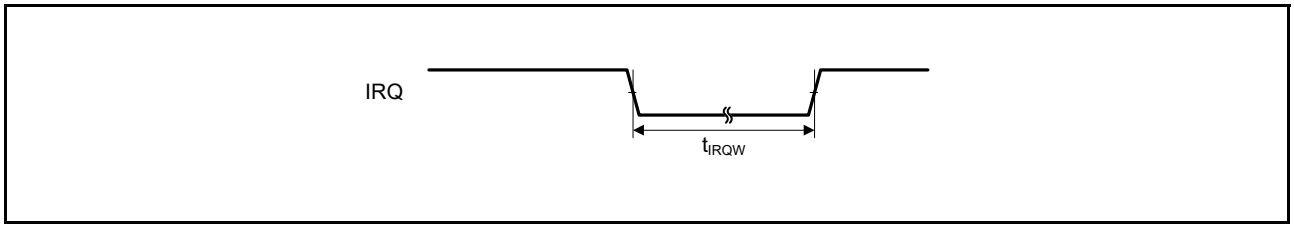



**Figure 5.15 IRQ Interrupt Input Timing**

## 5.3.5 Bus Timing

**Table 5.24 Bus Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 12.5 | ns | Figure 5.16 to Figure 5.21 |
| Byte control delay time | $t_{BCD}$ | — | 12.5 | ns | |
| CS# delay time | $t_{CSD}$ | — | 12.5 | ns | |
| ALE delay time | $t_{ALED}$ | — | 12.5 | ns | |
| RD# delay time | $t_{RSD}$ | — | 12.5 | ns | |
| Read data setup time | $t_{RDS}$ | 12.5 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 12.5 | ns | |
| Write data delay time | $t_{WDD}$ | — | 12.5 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 12.5 | — | ns | Figure 5.22 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |
| Address delay time 2 (SDRAM) | $t_{AD2}$ | 1 | 12.5 | ns | Figure 5.23 |
| CS# delay time 2 (SDRAM) | $t_{CSD2}$ | 1 | 12.5 | ns | |
| DQM delay time (SDRAM) | $t_{DQMD}$ | 1 | 12.5 | ns | |
| CKE delay time (SDRAM) | $t_{CKED}$ | 1 | 12.5 | ns | |
| Read data setup time 2 (SDRAM) | $t_{RDS2}$ | 10 | — | ns | |
| Read data hold time 2 (SDRAM) | $t_{RDH2}$ | 0 | — | ns | |
| Write data delay time 2 (SDRAM) | $t_{WDD2}$ | — | 12.5 | ns | |
| Write data hold time 2 (SDRAM) | $t_{WDH2}$ | 1 | — | ns | |
| WE# delay time (SDRAM) | $t_{WED}$ | 1 | 12.5 | ns | |
| RAS# delay time (SDRAM) | $t_{RASD}$ | 1 | 12.5 | ns | |
| CAS# delay time (SDRAM) | $t_{CASD}$ | 1 | 12.5 | ns | |

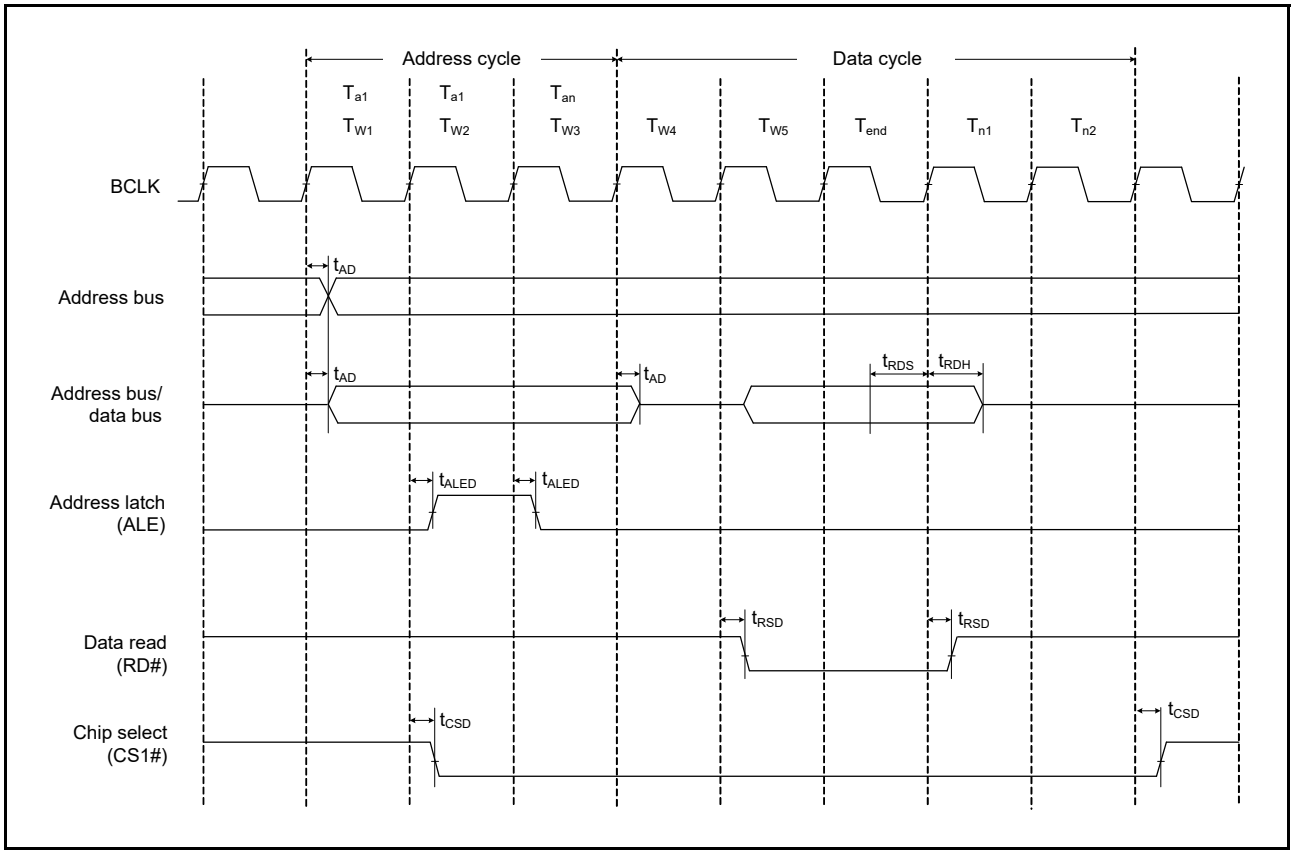



**Figure 5.16 Address/Data Multiplexed Bus Read Access Timing**

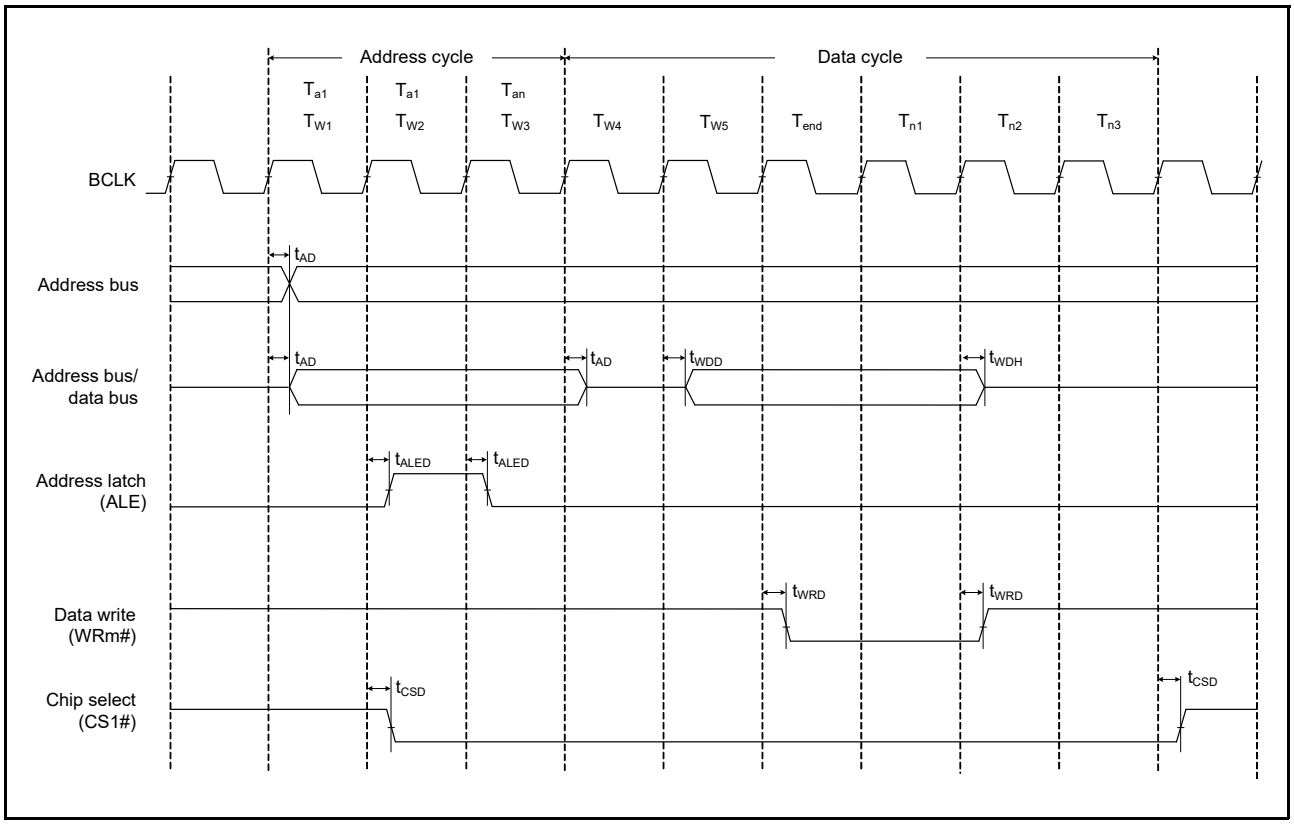



**Figure 5.17 Address/Data Multiplexed Bus Write Access Timing**

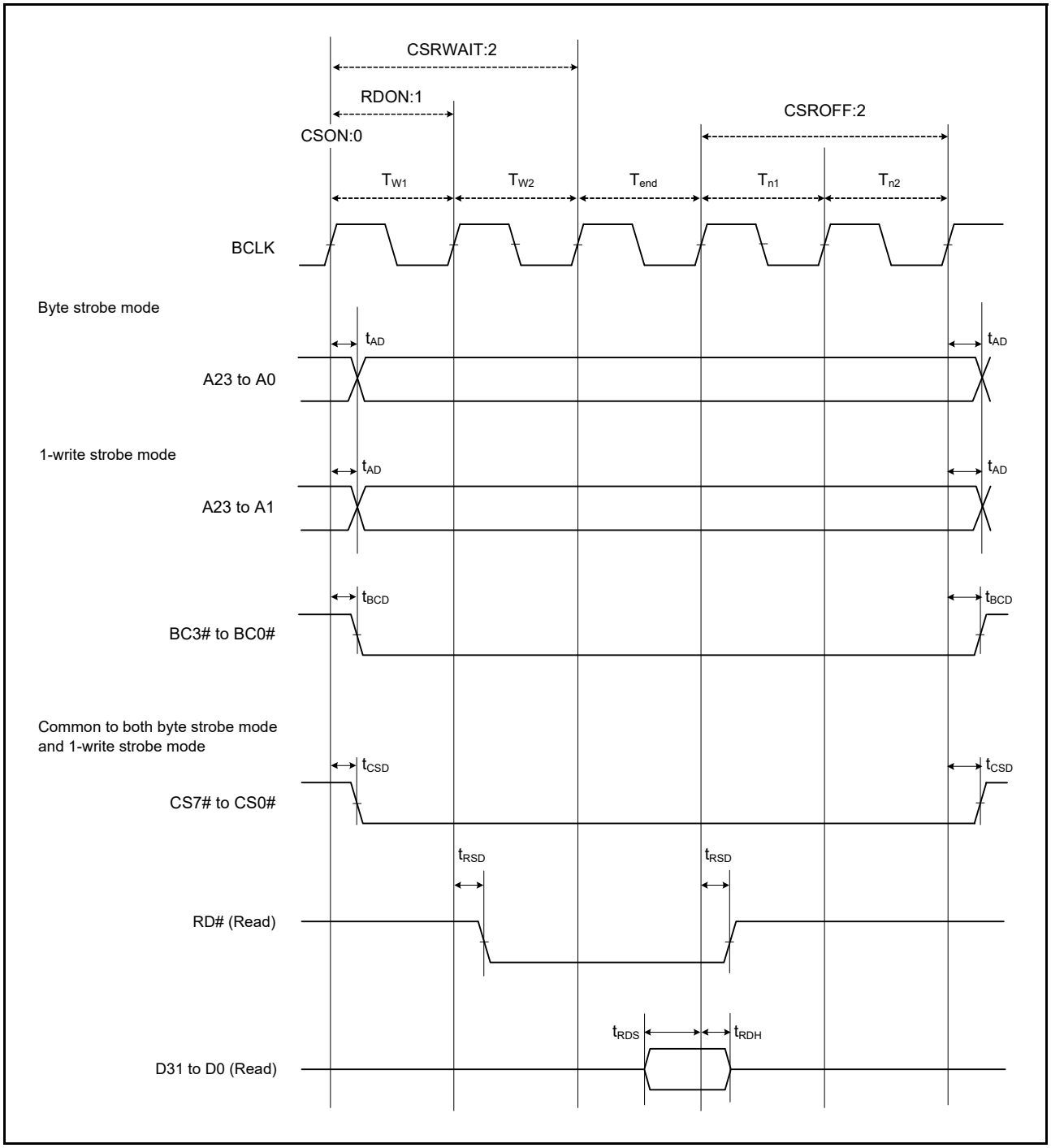
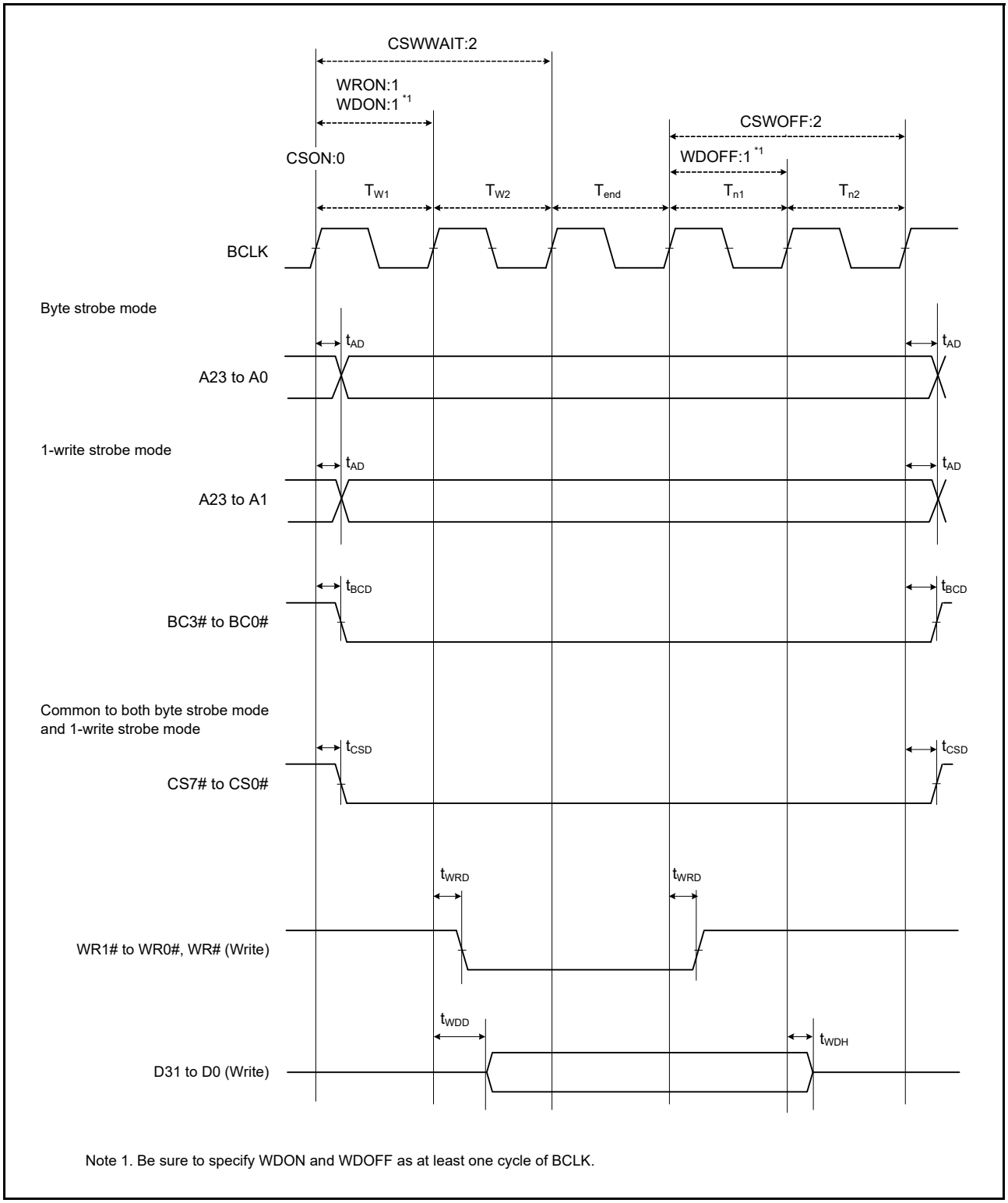



**Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)**




Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

**Figure 5.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)**

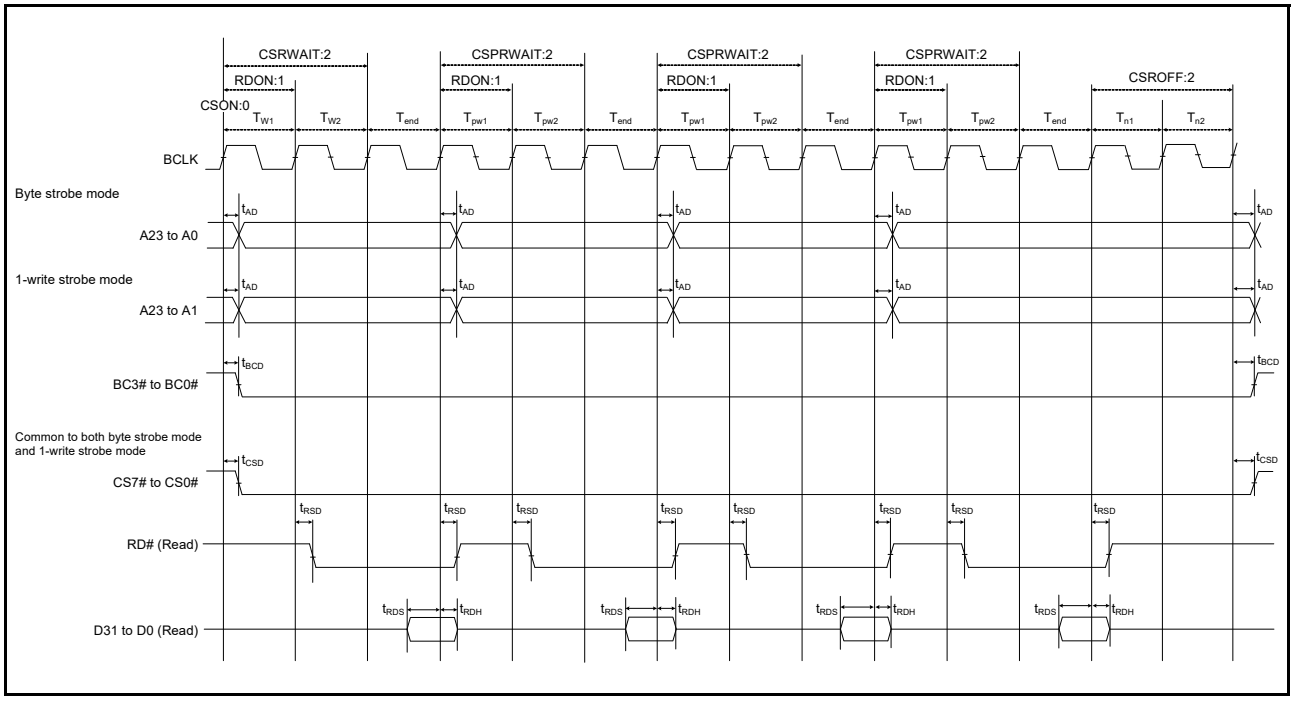
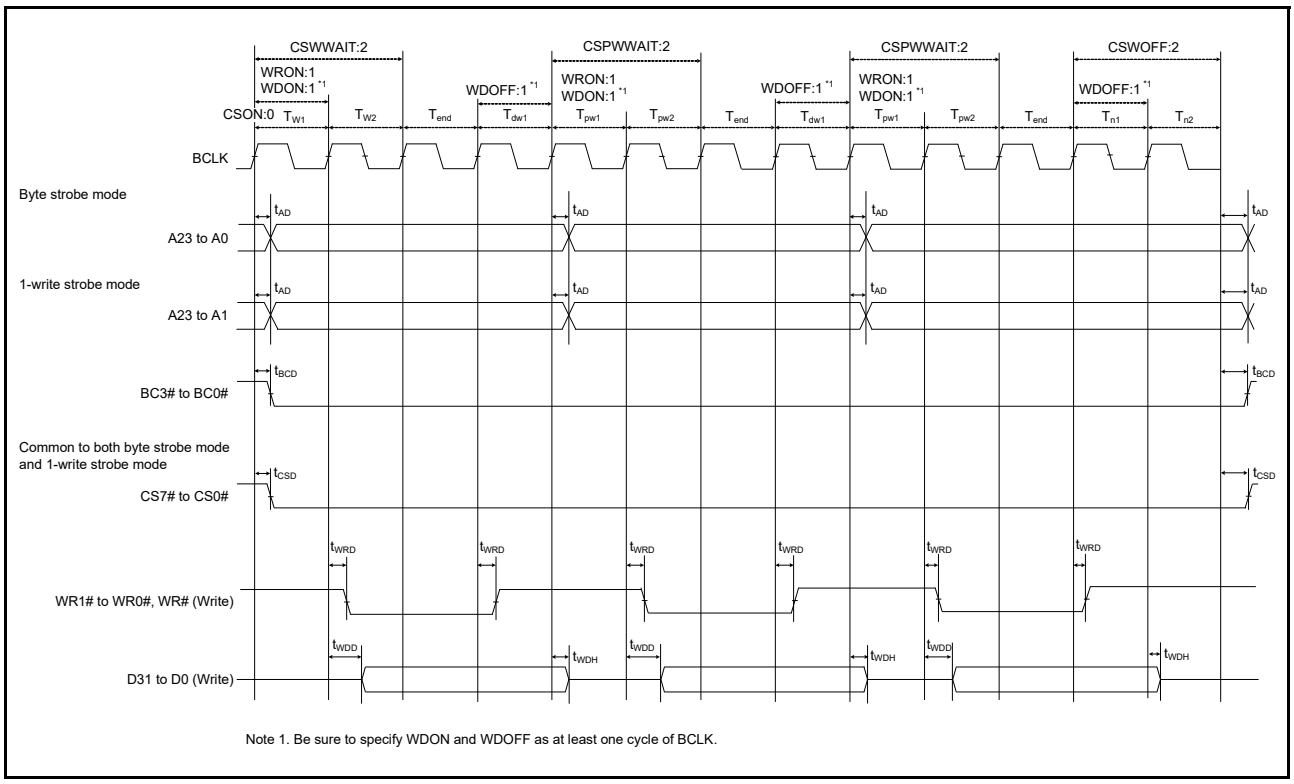



**Figure 5.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)**




Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

**Figure 5.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)**

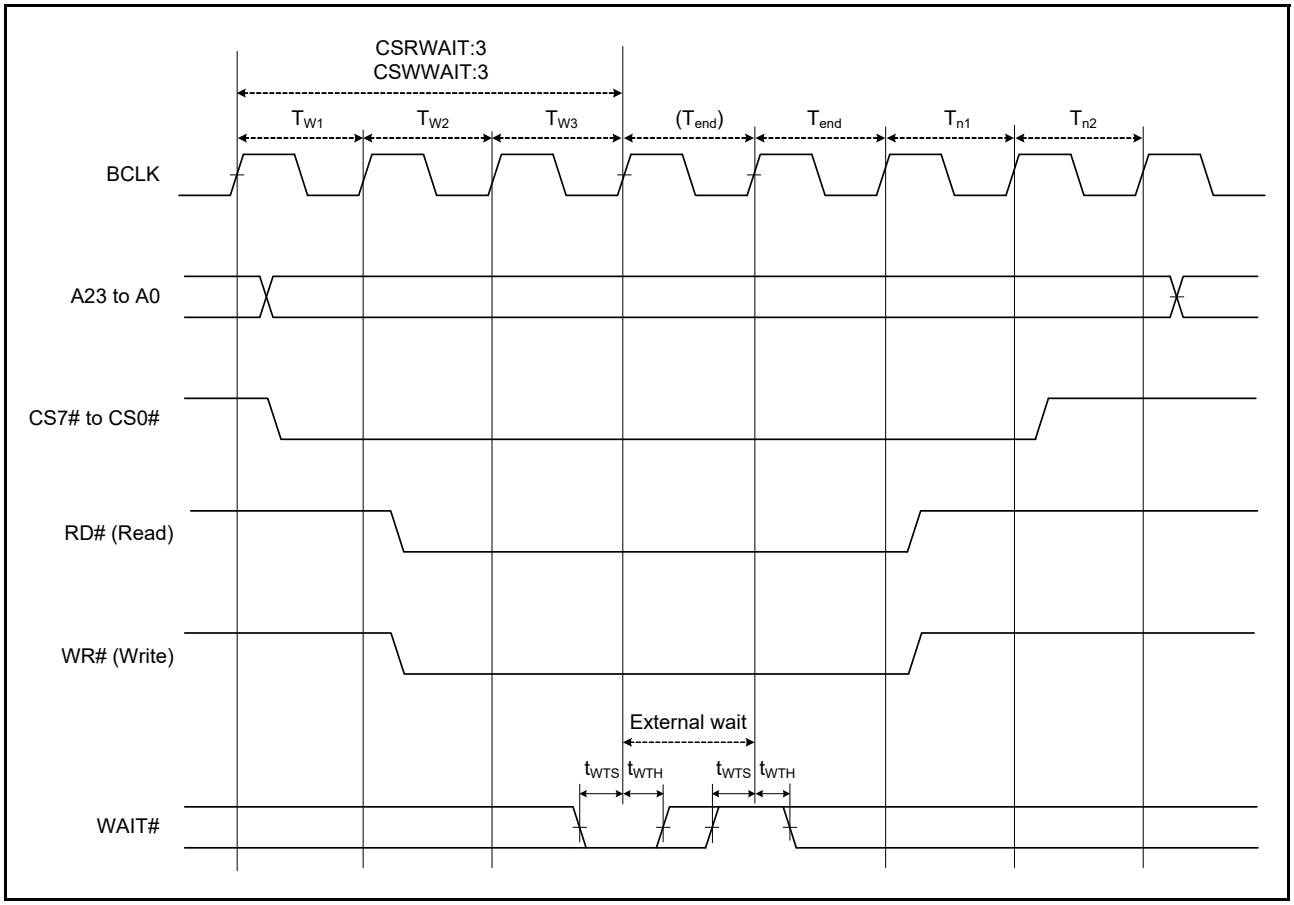
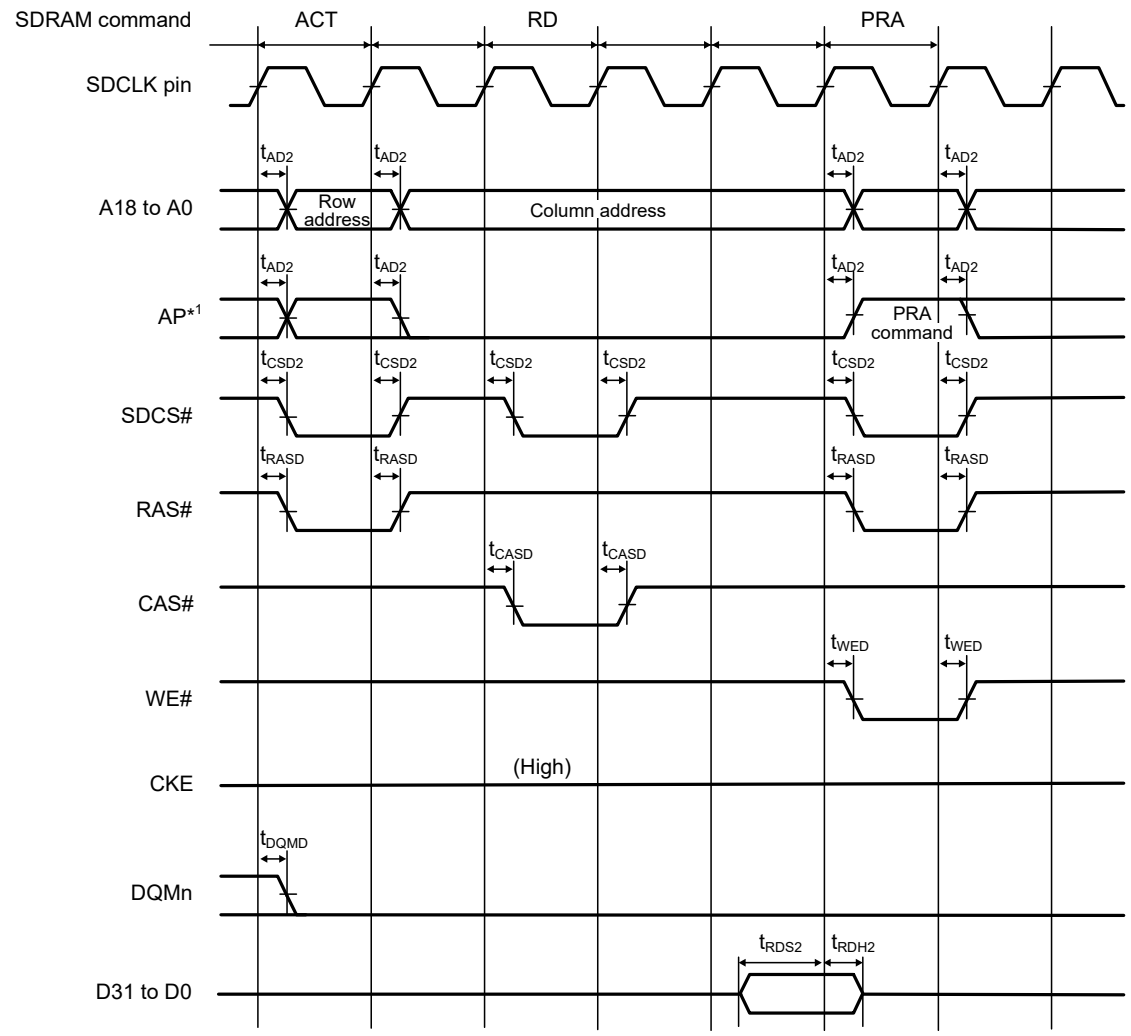
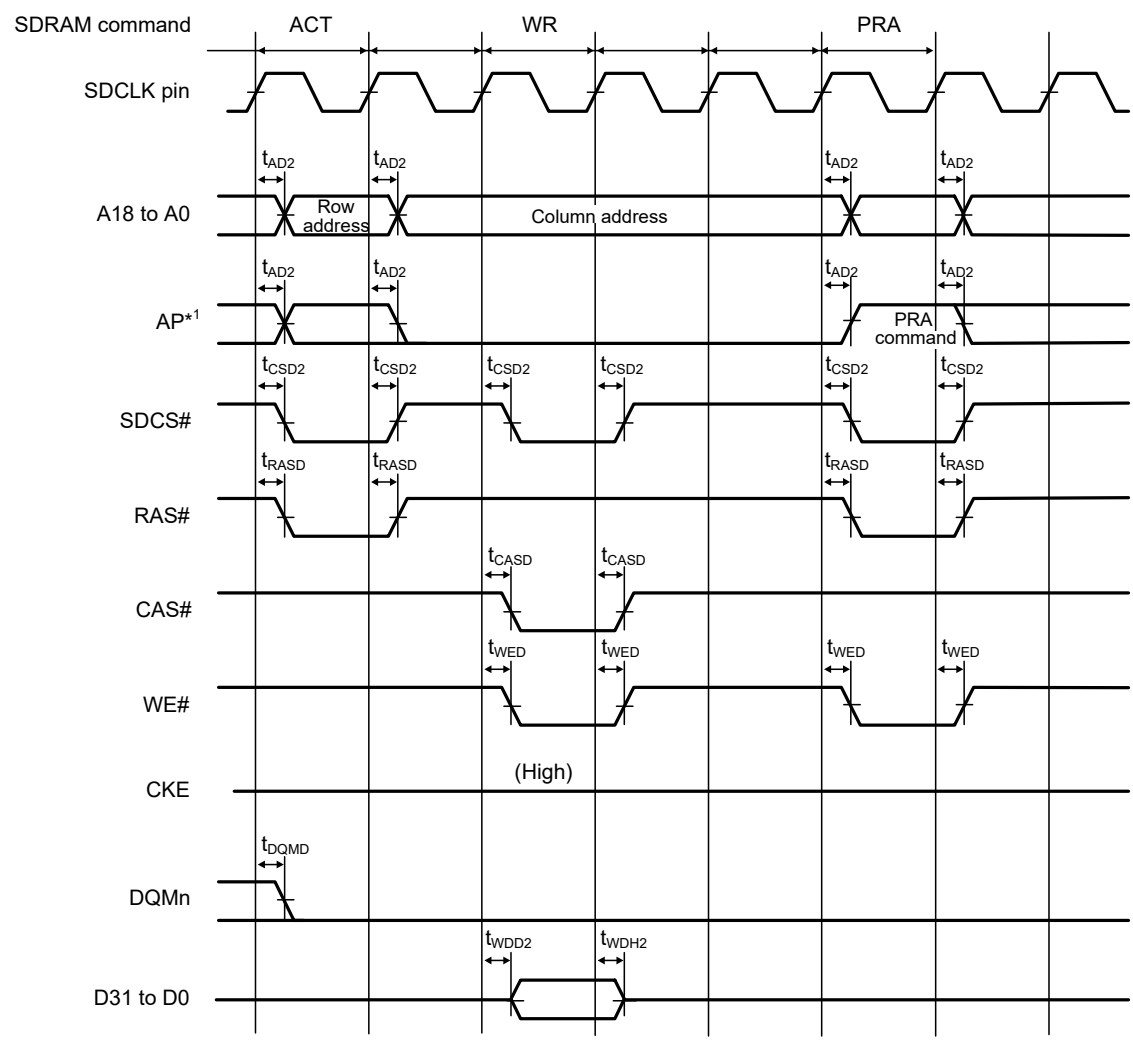



**Figure 5.22 External Bus Timing/External Wait Control**



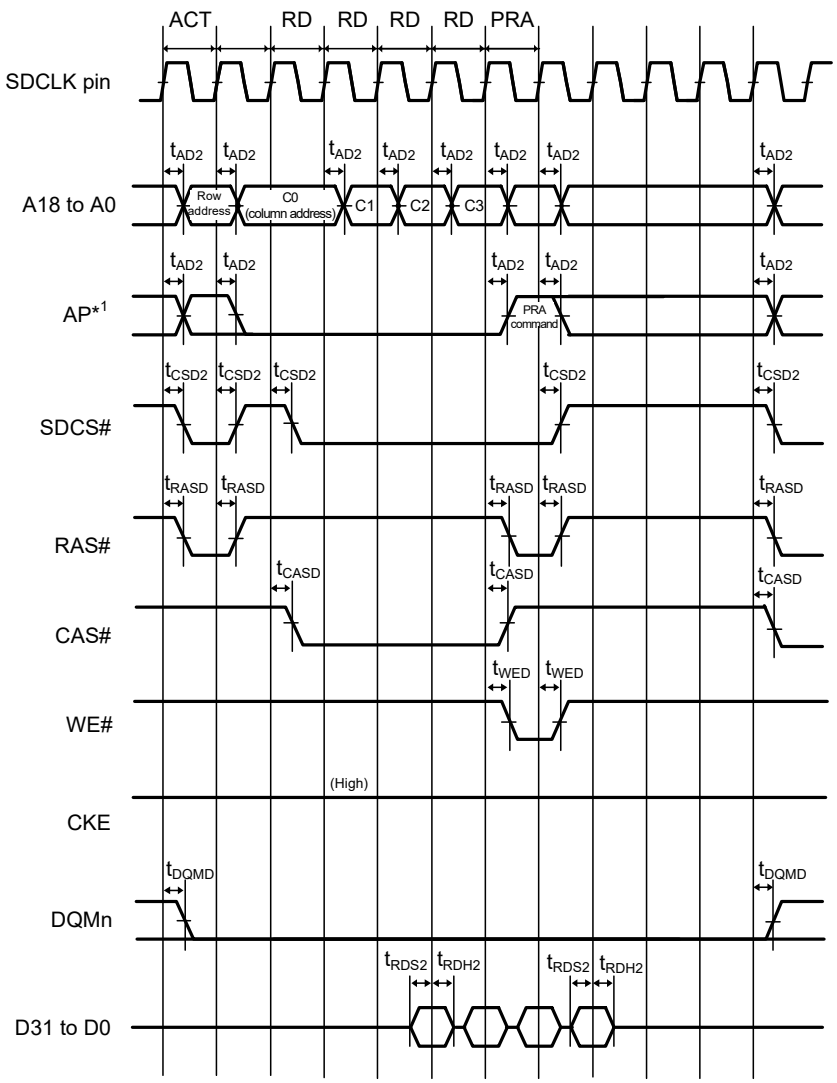

Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.23 SDRAM Space Single Read Bus Timing**



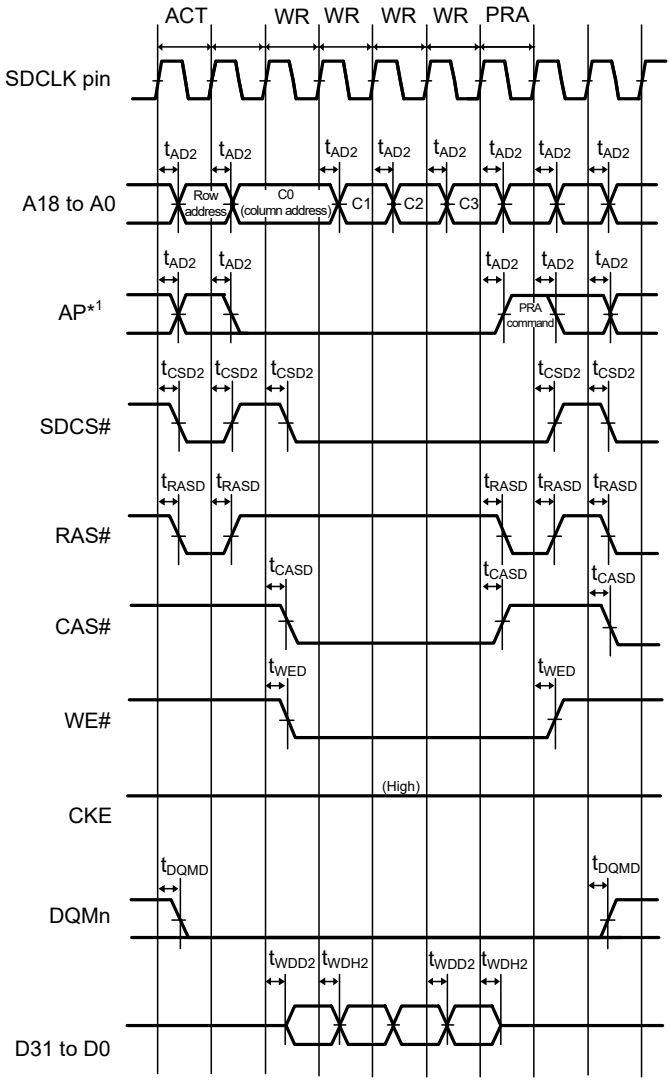

Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.24 SDRAM Space Single Write Bus Timing**



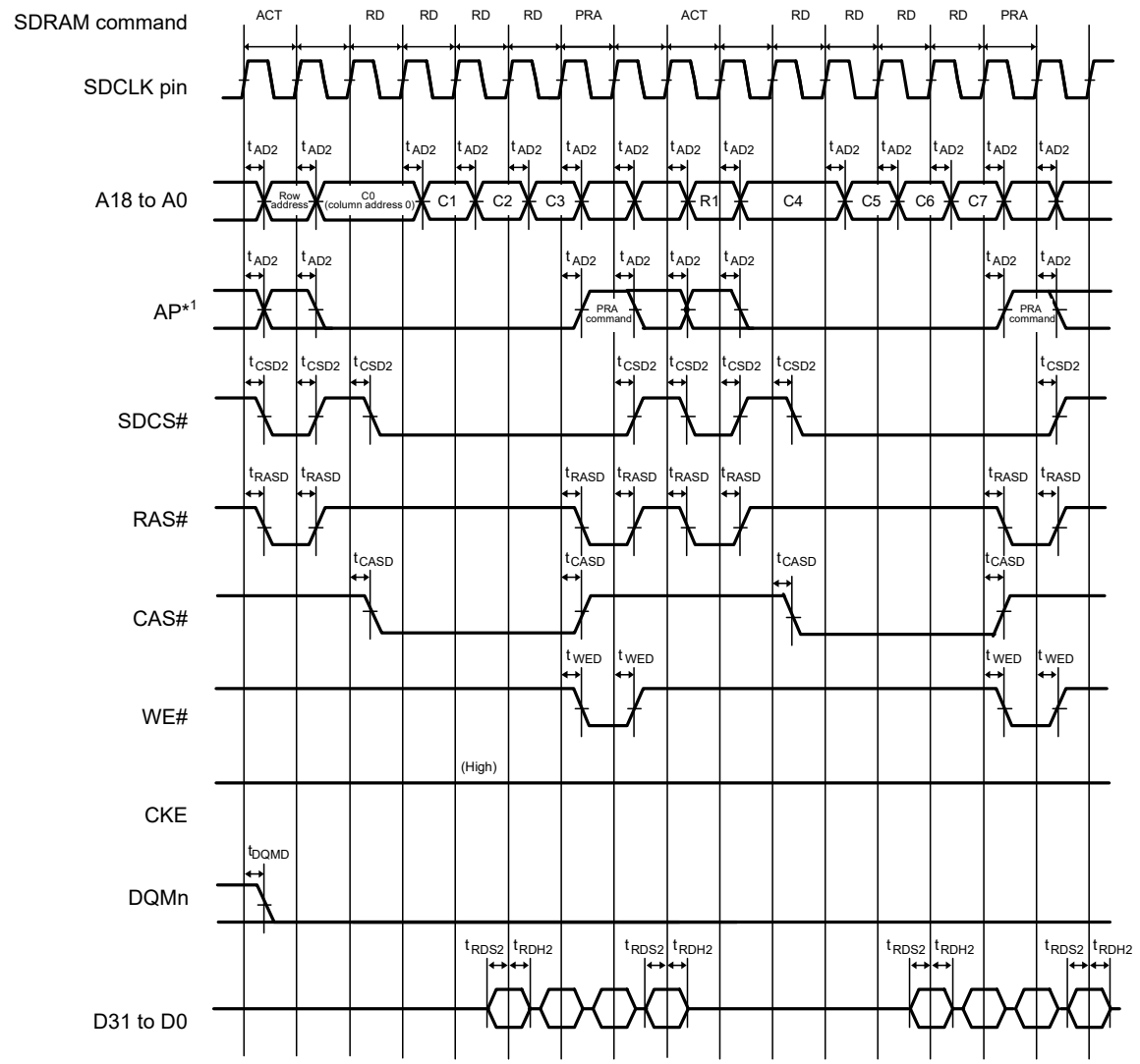

Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.25 SDRAM Space Multiple Read Bus Timing**



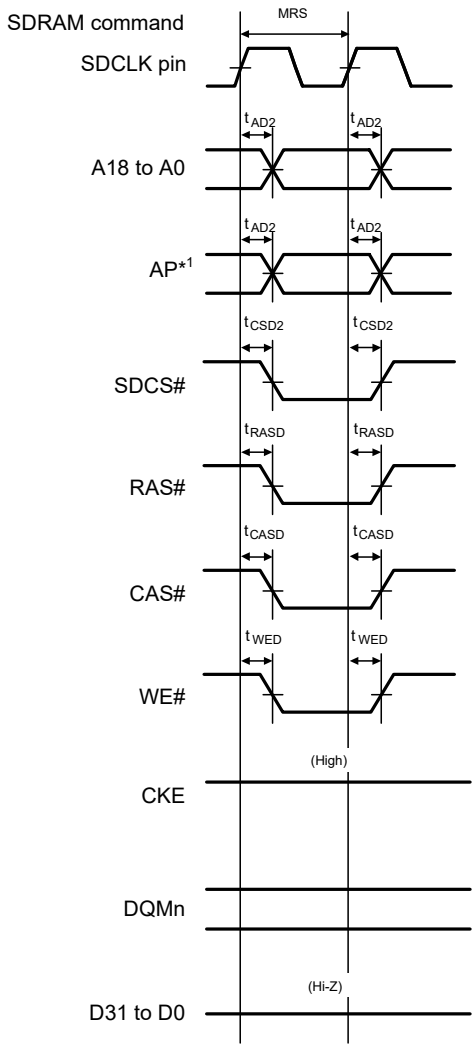

Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.26 SDRAM Space Multiple Write Bus Timing**



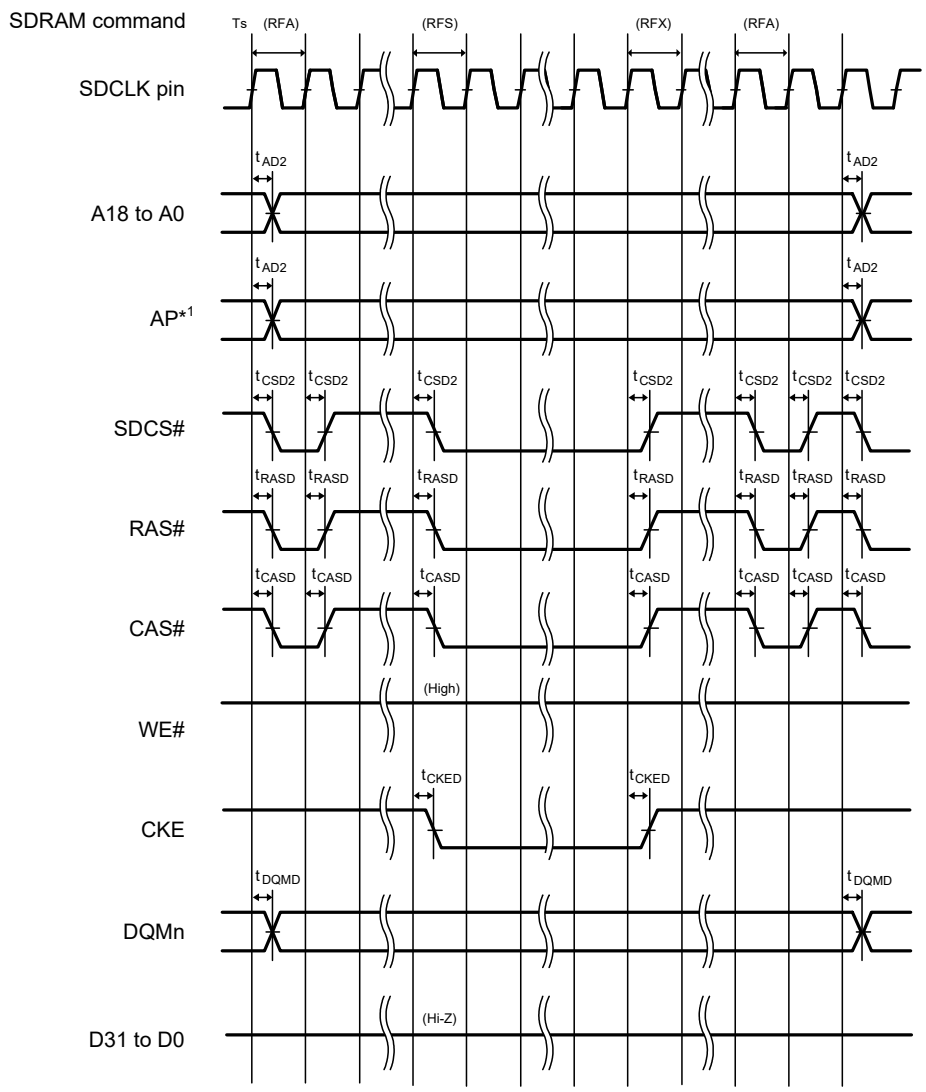

Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.27 SDRAM Space Multiple Read Line Stride Bus Timing**




Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.28 SDRAM Space Mode Register Set Bus Timing**




Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.29 SDRAM Space Self-Refresh Bus Timing**

## 5.3.6 EXDMAC Timing

**Table 5.25 EXDMAC Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| EXDMAC | EDREQ setup time | $t_{EDRQS}$ | 13 | — | ns | Figure 5.30 |
| | EDREQ hold time | $t_{EDRQH}$ | 2 | — | ns | |
| | EDACK delay time | $t_{EDACD}$ | — | 13 | ns | Figure 5.31, Figure 5.32 |

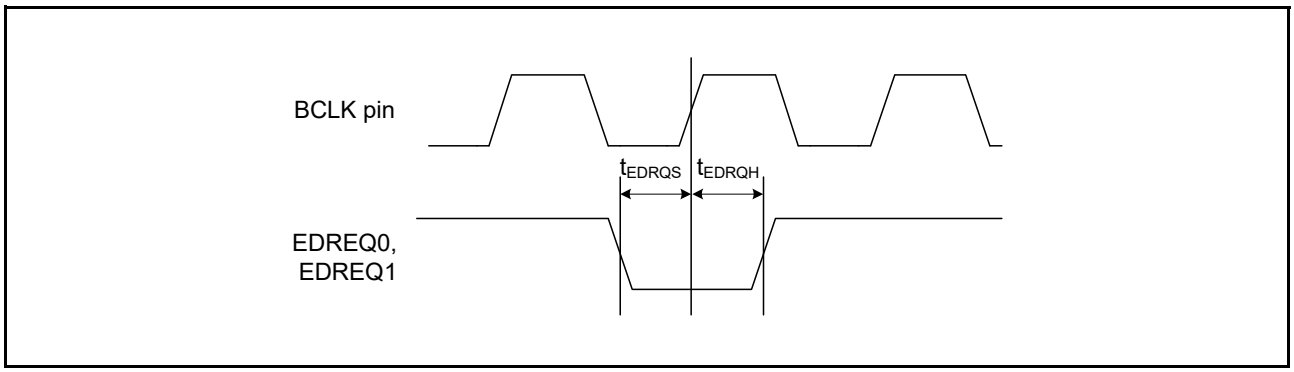



**Figure 5.30 EDREQ0 and EDREQ1 Input Timing**

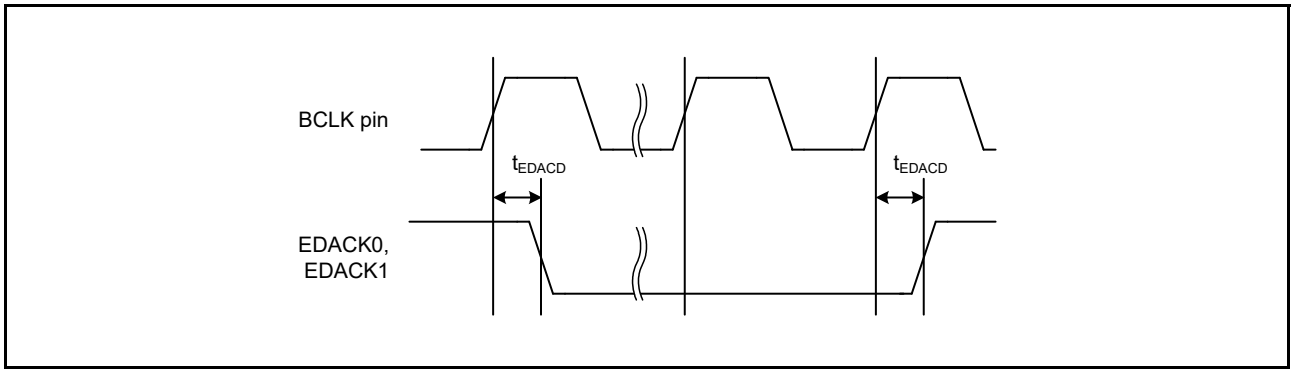



**Figure 5.31 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)**

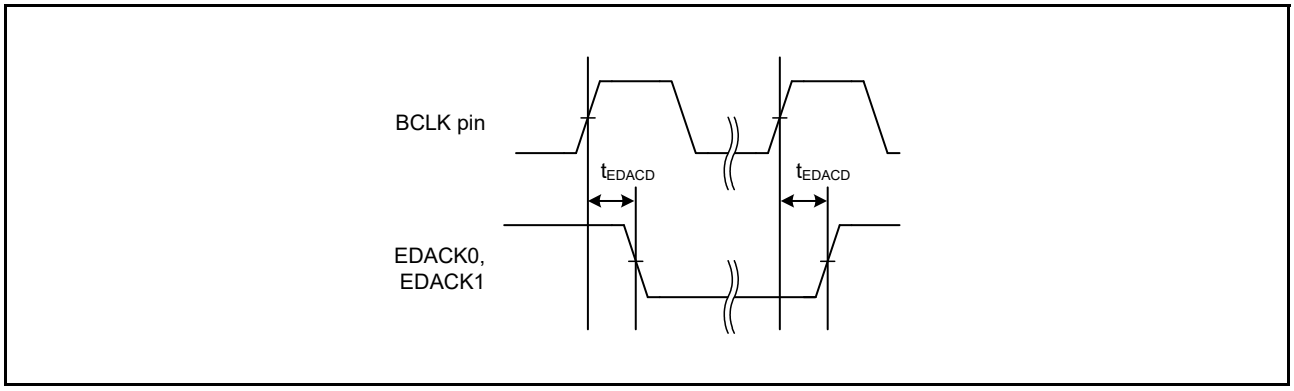



**Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

## 5.3.7 Timing of On-Chip Peripheral Modules

**Table 5.26 I/O Port Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | $t_{PRW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.33 |

Note 1. $t_{PBcyc}$: PCLKB cycle

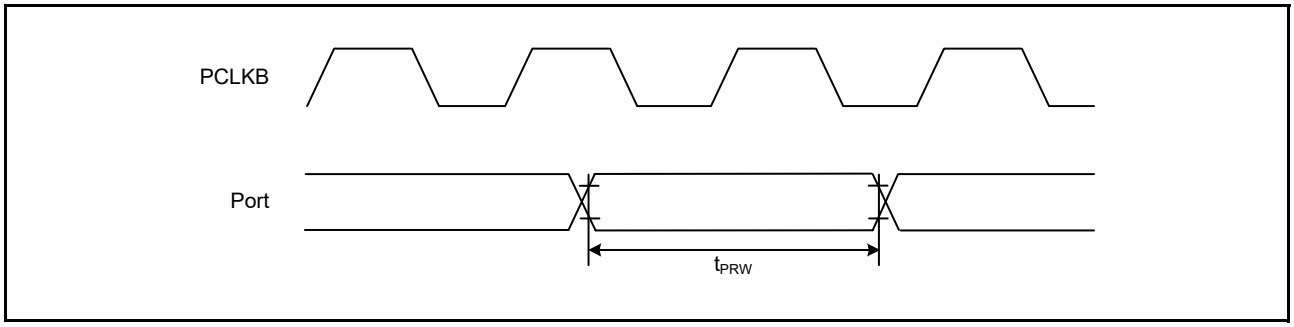



**Figure 5.33 I/O Port Input Timing**

**Table 5.27 TPU Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| TPU | Input capture input pulse width | Single-edge setting | $t_{TICW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.34 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{TCKWH}$, $t_{TCKWL}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.35 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

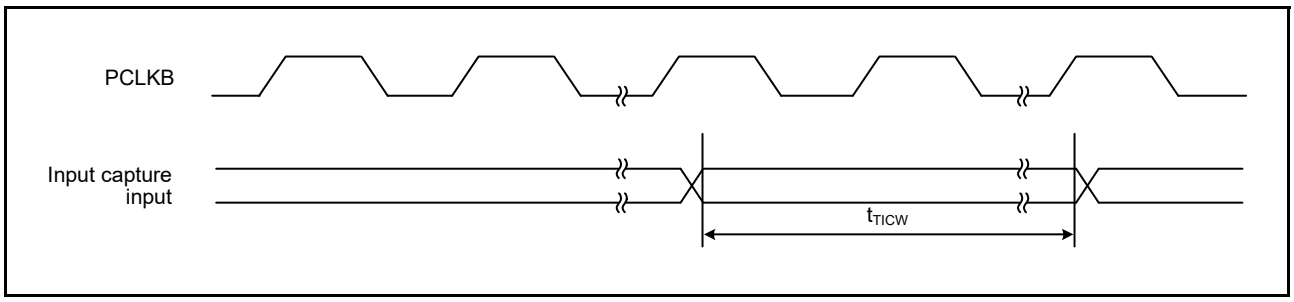



**Figure 5.34 TPU Input Capture Input Timing**

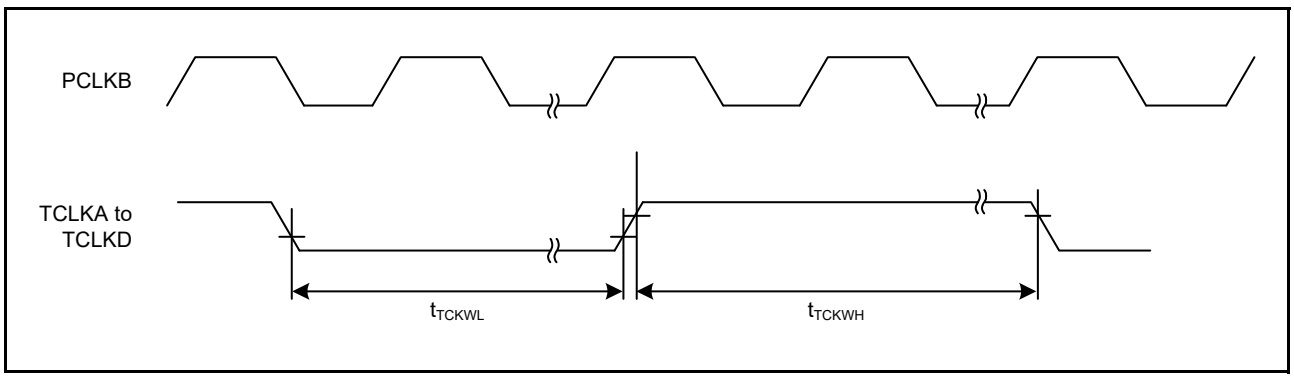



**Figure 5.35 TPU Clock Input Timing**

### Table 5.28 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| TMR | Timer clock pulse width | Single-edge setting | $t_{TMCWH}$, $t_{TMCWL}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.36 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

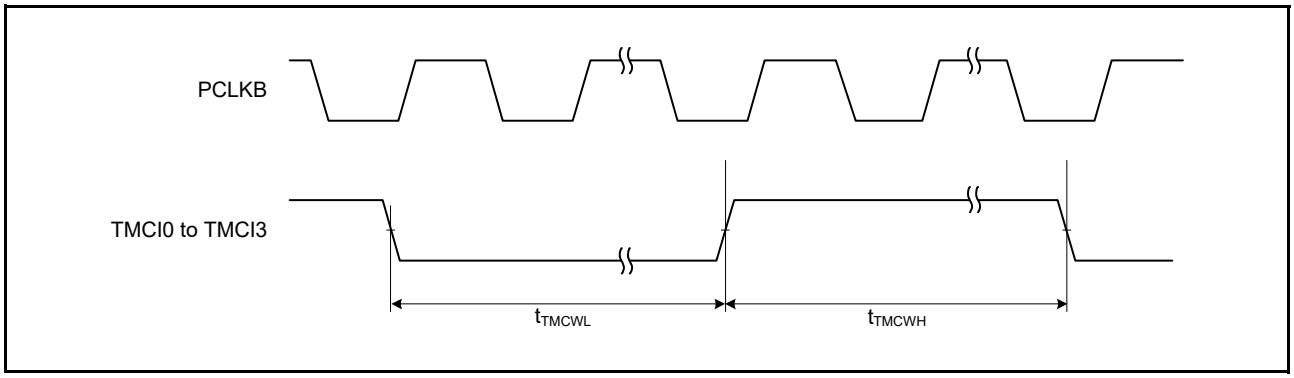



**Figure 5.36 TMR Clock Input Timing**

### Table 5.29 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| CMTW | Input capture input pulse width | Single-edge setting | $t_{CMTWTICW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.37 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

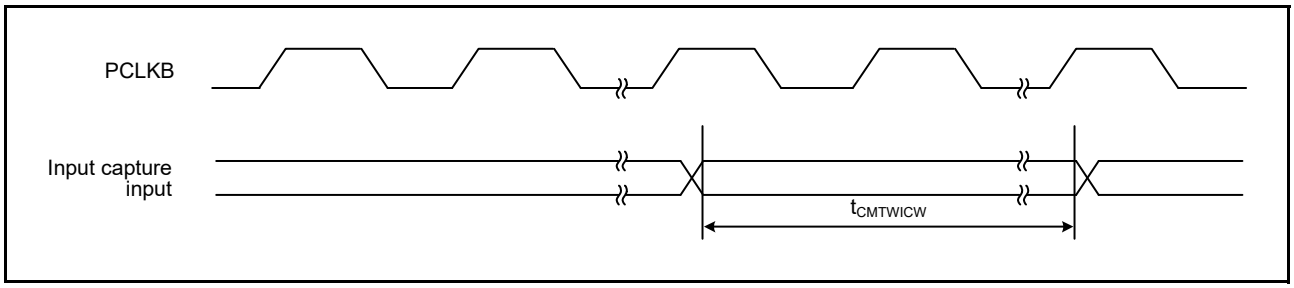



**Figure 5.37 CMTW Input Capture Input Timing**

**Table 5.30 MTU3 Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| MTU3 | Input capture input pulse width | Single-edge setting | $t_{MTICW}$ | 1.5 | — | $t_{PAcyc}$ | Figure 5.38 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{MTCKWH}$, $t_{MTCKWL}$ | 1.5 | — | $t_{PAcyc}$ | Figure 5.39 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

Note 1. $t_{PAcyc}$: PCLKA cycle

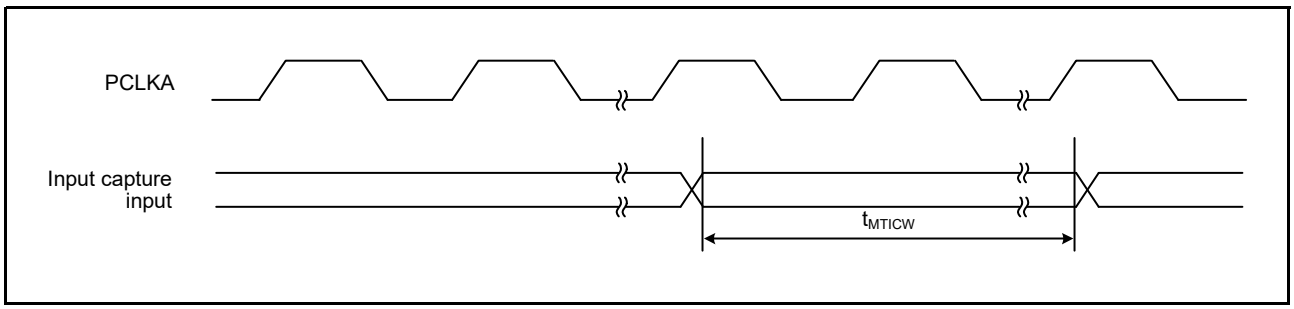



**Figure 5.38 MTU3 Input Capture Input Timing**

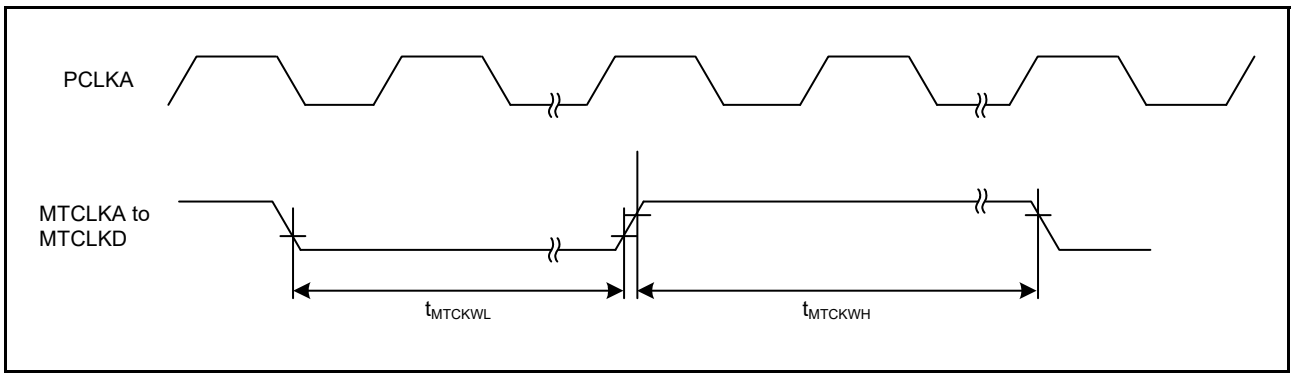



**Figure 5.39 MTU3 Clock Input Timing**

**Table 5.31 POE3 Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| POE | POE# input pulse width | $t_{POEW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.40 |

Note 1. $t_{PBcyc}$: PCLKB cycle

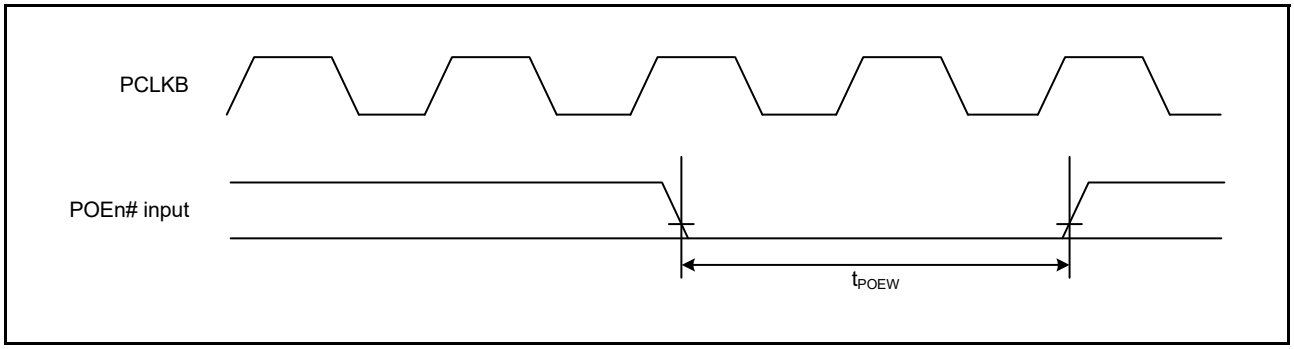



**Figure 5.40 POE# Input Timing**

### Table 5.32 A/D Converter Trigger Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| A/D converter | A/D converter trigger input pulse width | $t_{TRGW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.41 |

Note 1. $t_{PBcyc}$: PCLKB cycle

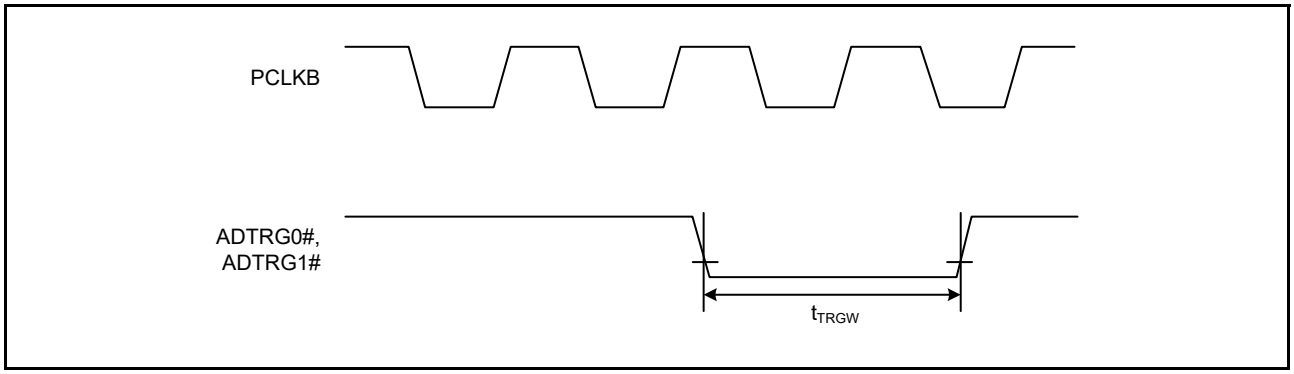



**Figure 5.41 A/D Converter Trigger Input Timing**

### Table 5.33 CAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item*1, *2 | | | Symbol | Min.*1, *2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| CAC | CACREF input pulse width | $t_{PBcyc} \le t_{cac}$ | $t_{CACREF}$ | 4.5 $t_{cac}$ + 3 $t_{PBcyc}$ | — | ns | |
| | | $t_{PBcyc} > t_{cac}$ | | 5 $t_{cac}$ + 6.5 $t_{PBcyc}$ | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle
Note 2. $t_{cac}$: CAC count clock source cycle

### Table 5.34 SCIg, SCIh, and SCIi Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCIg, SCIh | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{PBcyc}$ | Figure 5.42 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous*2 | $t_{Scyc}$ | 8 | — | $t_{PBcyc}$ | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay time | Clock synchronous | $t_{TXD}$ | — | 28 | ns | Figure 5.43 |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 15 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 5 | — | ns | |
| SCIi | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{PAcyc}$ | Figure 5.42 |
| | | Clock synchronous | | 12 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous*2 | $t_{Scyc}$ | 8 | — | $t_{PAcyc}$ | |
| | | Clock synchronous | | 8 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay time | Master | $t_{TXD}$ | — | 15 | ns | Figure 5.43 |
| | | Slave | | — | 28 | | |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 20 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle; $t_{PAcyc}$: PCLKA cycle
Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1

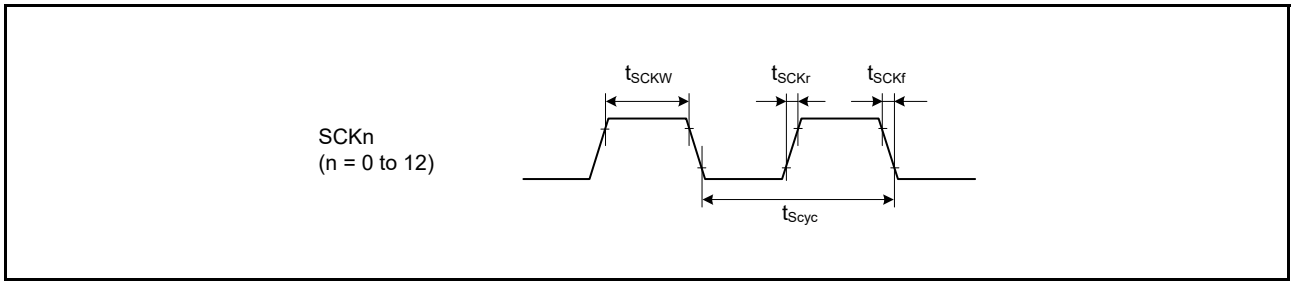



**Figure 5.42 SCK Clock Input Timing**

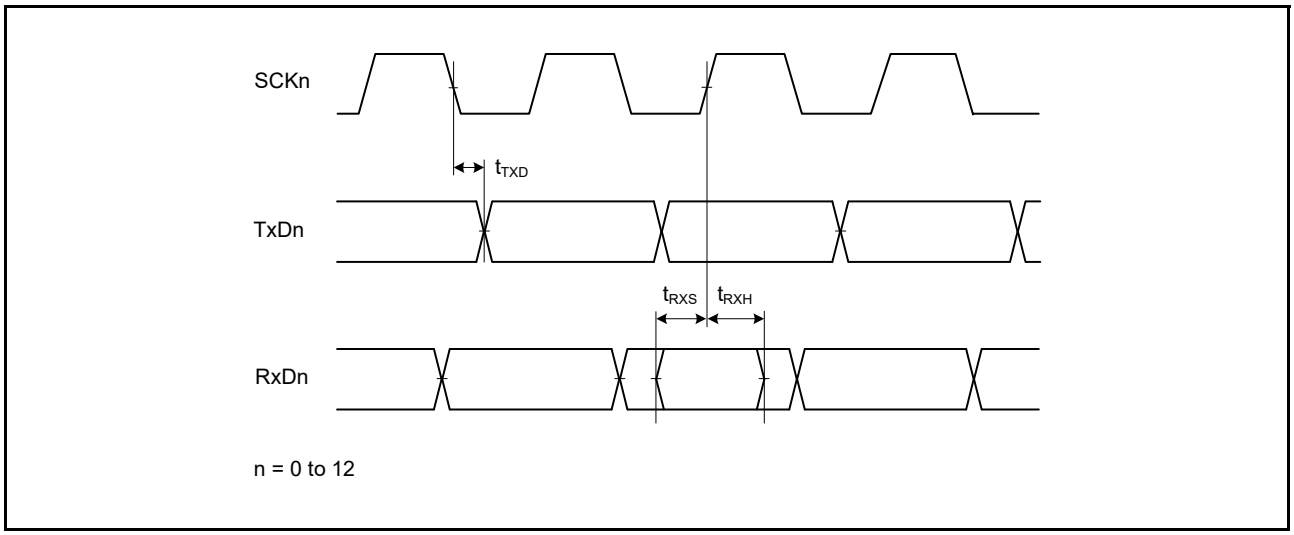



**Figure 5.43 SCI Input/Output Timing: Clock Synchronous Mode**

### Table 5.35 RSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | | | Symbol | Min.*1 | Max.*1 | Unit*1 | Test Conditions*2 |
|---|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | | $t_{SPcyc}$ | 2 | 4096 | $t_{PAcyc}$ | Figure 5.44 |
| | | Slave | | | 4 | 4096 | | |
| | RSPCK clock high pulse width | Master | | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$ | — | | |
| | RSPCK clock low pulse width | Master | | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$ | — | | |
| | RSPCK clock rise/fall time | Output | | $t_{SPCKr}$, $t_{SPCKf}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | Data input setup time | Master | | $t_{SU}$ | 6 | — | ns | Figure 5.45 to Figure 5.50 |
| | | Slave | | | 8.3 | — | | |
| | Data input hold time | Master | PCLKA division ratio set to 1/2 | $t_{HF}$ | 0 | — | ns | |
| | | | PCLKA division ratio set to a value other than 1/2 | $t_H$ | $t_{PAcyc}$ | — | | |
| | | Slave | | | 8.3 | — | | |
| | SSL setup time | Master | | $t_{LEAD}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | | 6 | — | $t_{PAcyc}$ | |
| | SSL hold time | Master | | $t_{LAG}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | | 6 | — | $t_{PAcyc}$ | |
| | Data output delay time | Master | | $t_{OD}$ | — | 6.3 | ns | |
| | | Slave | | | — | 28 | | |
| | Data output hold time | Master | | $t_{OH}$ | 0 | — | ns | |
| | | Slave | | | 0 | — | | |
| | Successive transmission delay time | Master | | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{PAcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{PAcyc}$ | ns | |
| | | Slave | | | $6 \times t_{PAcyc}$ | — | | |
| | MOSI and MISO rise/fall time | Output | | $t_{Dr}$, $t_{Df}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | SSL rise/fall time | Output | | $t_{SSLr}$, $t_{SSLf}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | Slave access time | | | $t_{SA}$ | — | $2 \times t_{PAcyc} + 28$ | ns | Figure 5.49, Figure 5.50 |
| | Slave output release time | | | $t_{REL}$ | — | $2 \times t_{PAcyc} + 28$ | ns | |

Note 1. $t_{PAcyc}$: PCLKA cycle
Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All RSPI AC timings are measured in combination with the pins in the same group.

### Table 5.36 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | $t_{SPcyc}$ | 4 | 65536 | $t_{PAcyc}$ | Figure 5.44 |
| | SCK clock cycle input (slave) | | 8 | 65536 | | |
| | SCK clock high pulse width | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time | $t_{SU}$ | 33.3 | — | ns | Figure 5.45 to Figure 5.50 |
| | Data input hold time | $t_H$ | 33.3 | — | ns | |
| | SS input setup time | $t_{LEAD}$ | 1 | — | $t_{SPcyc}$ | |
| | SS input hold time | $t_{LAG}$ | 1 | — | $t_{SPcyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 33.3 | ns | |
| | Data output hold time | $t_{OH}$ | –10 | — | ns | |
| | Data rise/fall time | $t_{Dr}$, $t_{Df}$ | — | 16.6 | ns | |
| | SS input rise/fall time | $t_{SSLr}$, $t_{SSLf}$ | — | 16.6 | ns | |
| | Slave access time | $t_{SA}$ | — | 5 | $t_{PBcyc}$ | Figure 5.49, Figure 5.50 |
| | Slave output release time | $t_{REL}$ | — | 5 | $t_{PBcyc}$ | |

Note 1. $t_{PAcyc}$: PCLKA cycle, $t_{PBcyc}$: PCLKB cycle

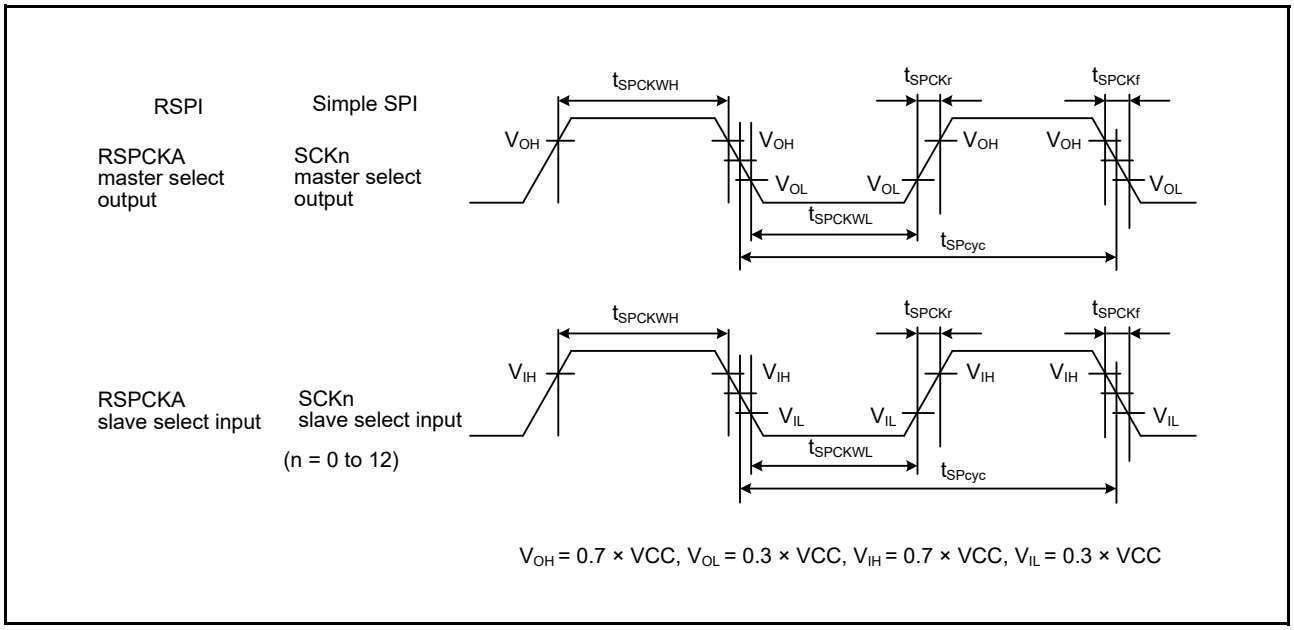



**Figure 5.44 RSPI Clock Timing and Simple SPI Clock Timing**

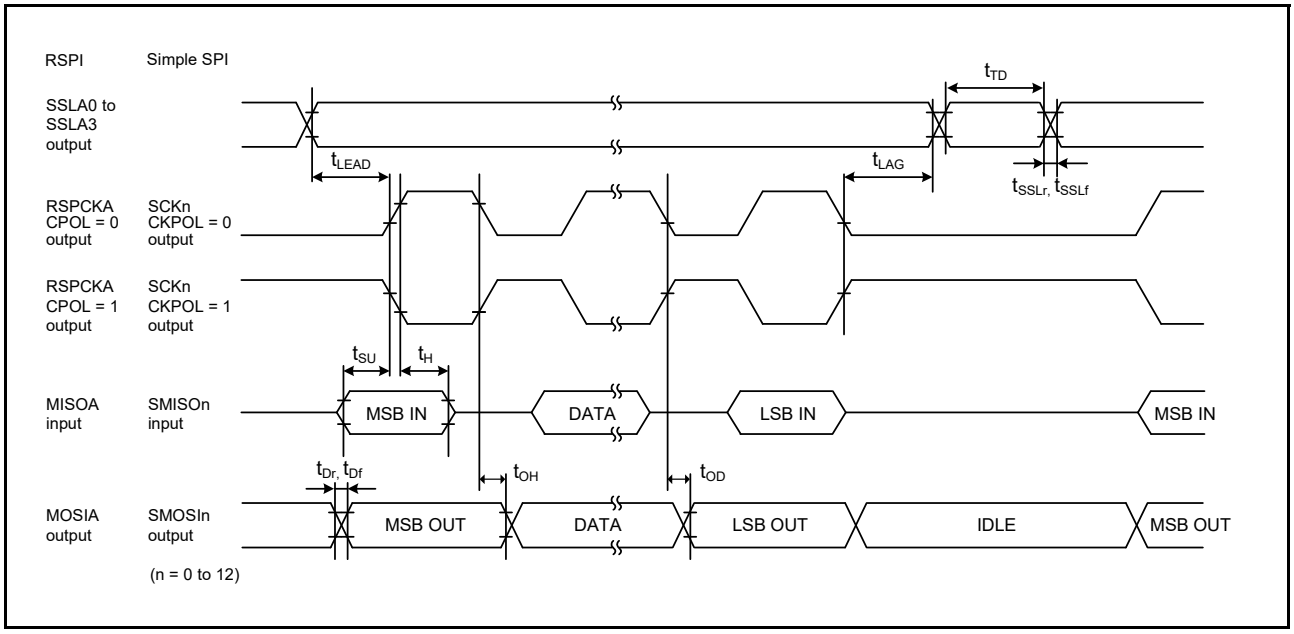



**Figure 5.45 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1)**

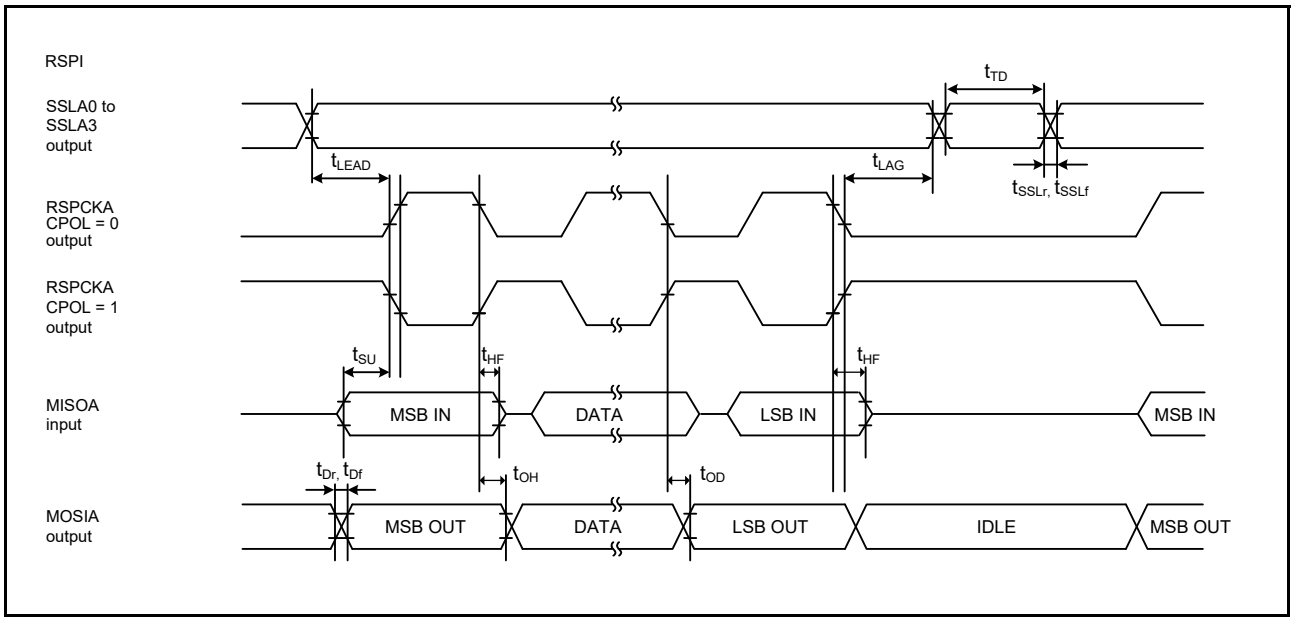



**Figure 5.46 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)**

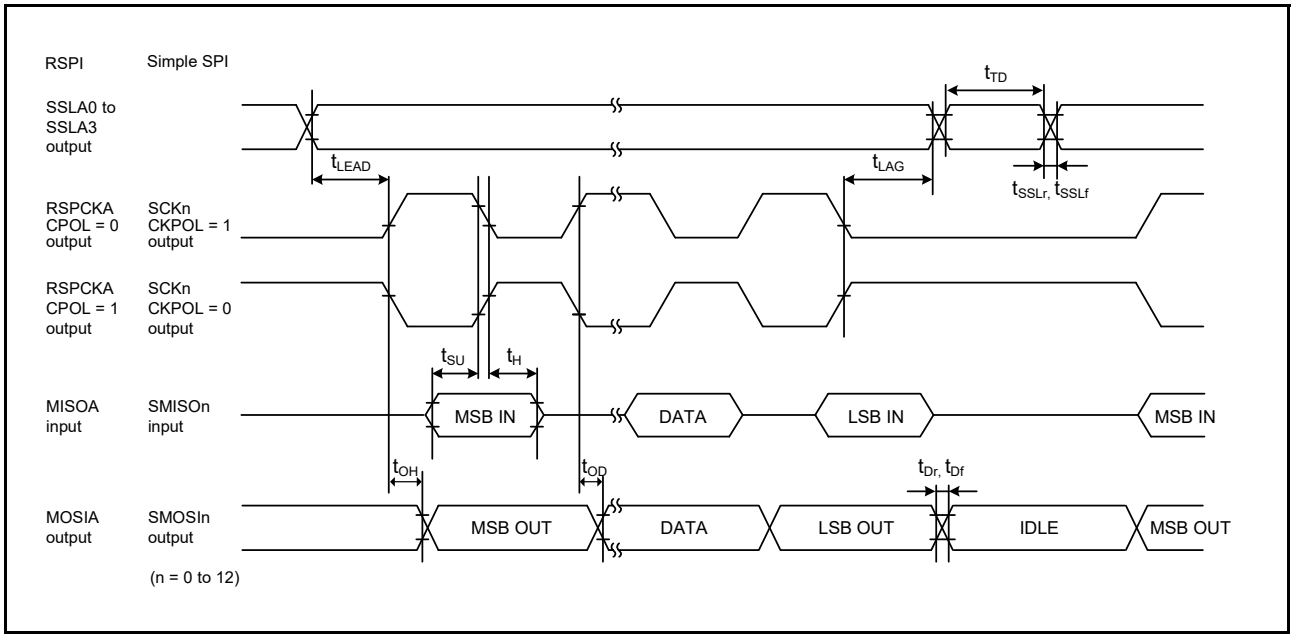



**Figure 5.47 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)**

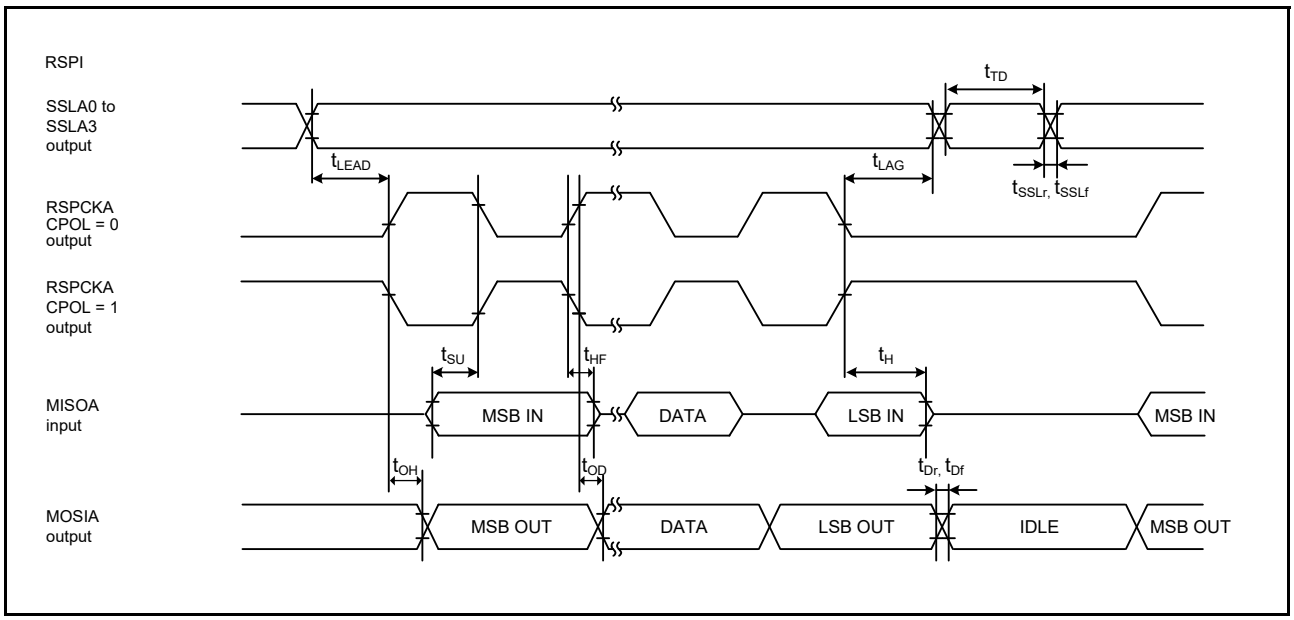



**Figure 5.48 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)**

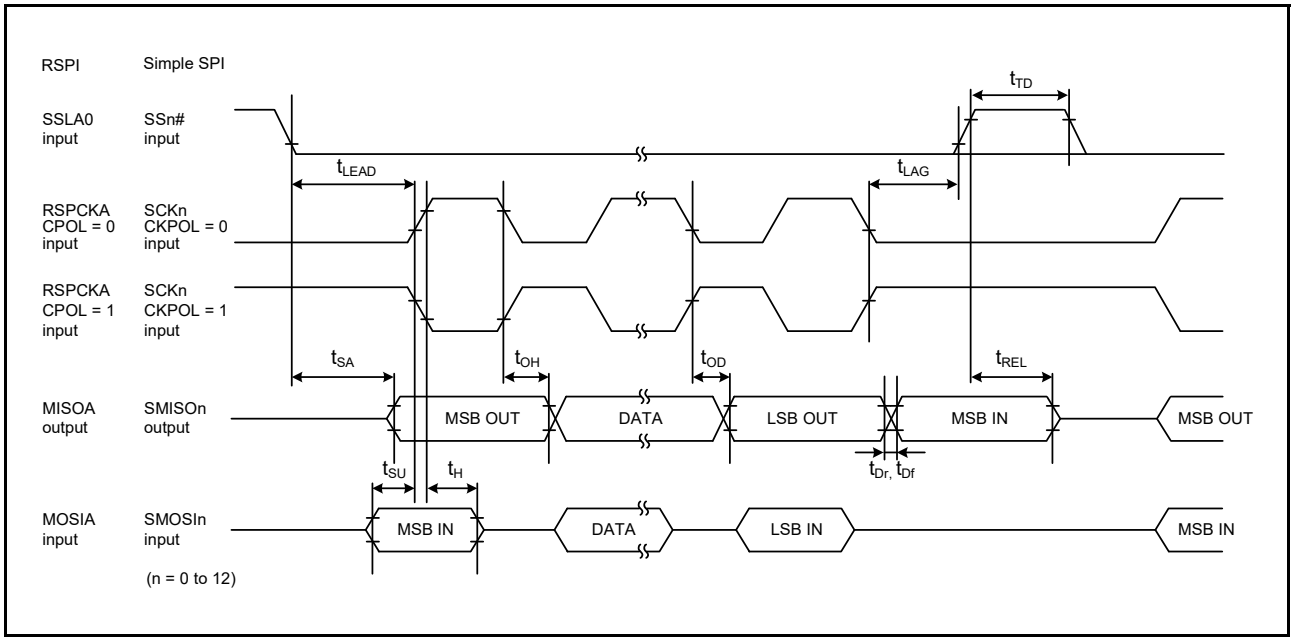



**Figure 5.49 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)**

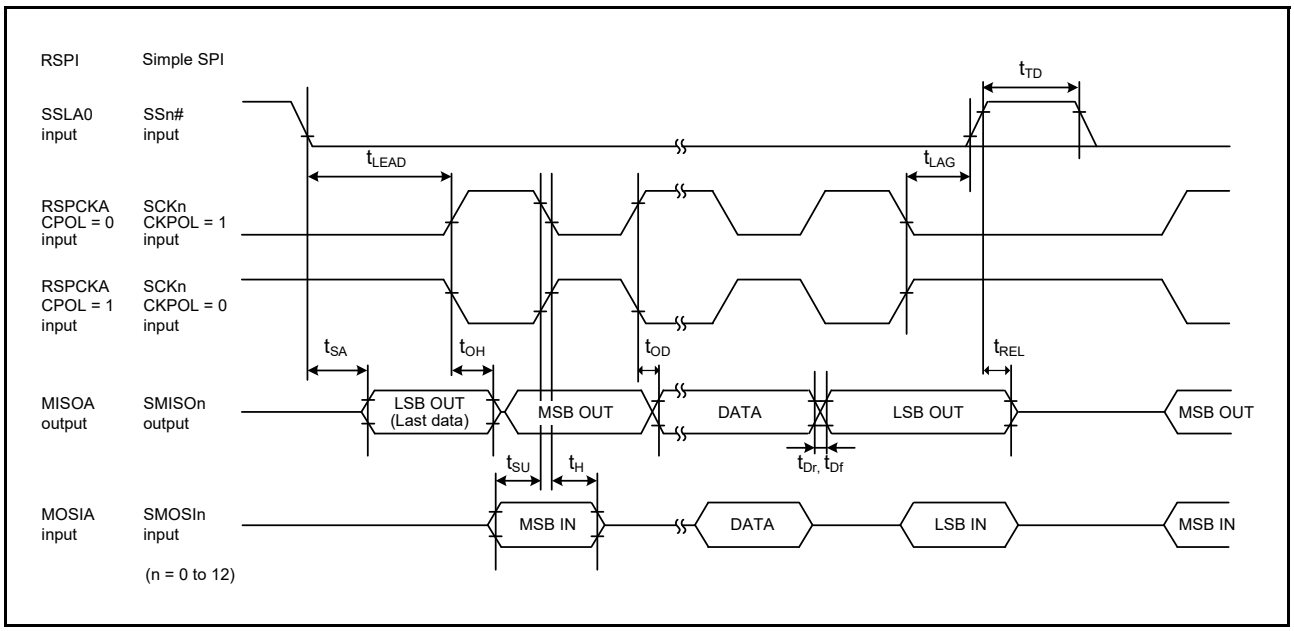



**Figure 5.50 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)**

### Table 5.37 QSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.*3

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions*2 |
|---|---|---|---|---|---|---|
| QSPI | QSPCLK clock cycle | $t_{QScyc}$ | 2 | 4080 | $t_{PBcyc}$ | Figure 5.51 |
| | Data input setup time | $t_{Su}$ | 6.5 | — | ns | Figure 5.52, Figure 5.53 |
| | Data input hold time | $t_{IH}$ | 5 | — | ns | |
| | SS setup time | $t_{LEAD}$ | 1.5 | 8.5 | $t_{QScyc}$ | |
| | SS hold time | $t_{LAG}$ | 1 | 8 | $t_{QScyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 10.0 | ns | |
| | Data output hold time | $t_{OH}$ | –5 | — | ns | |
| | Successive transmission delay time | $t_{TD}$ | 1 | 8 | $t_{QScyc}$ | |

Note 1. $t_{PBcyc}$: PCLKB cycle
Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All QSPI AC timings are measured in combination with the pins in the same group.
Note 3. In the G-version products, the AC characteristics are measured by setting the drive capacity control register 2 corresponding the QSPCLK pin as a high-speed interface high-drive output.

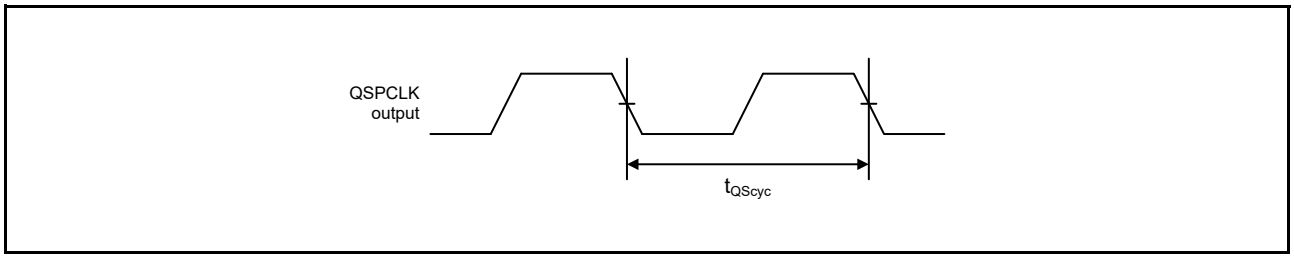



**Figure 5.51 QSPI Clock Timing**

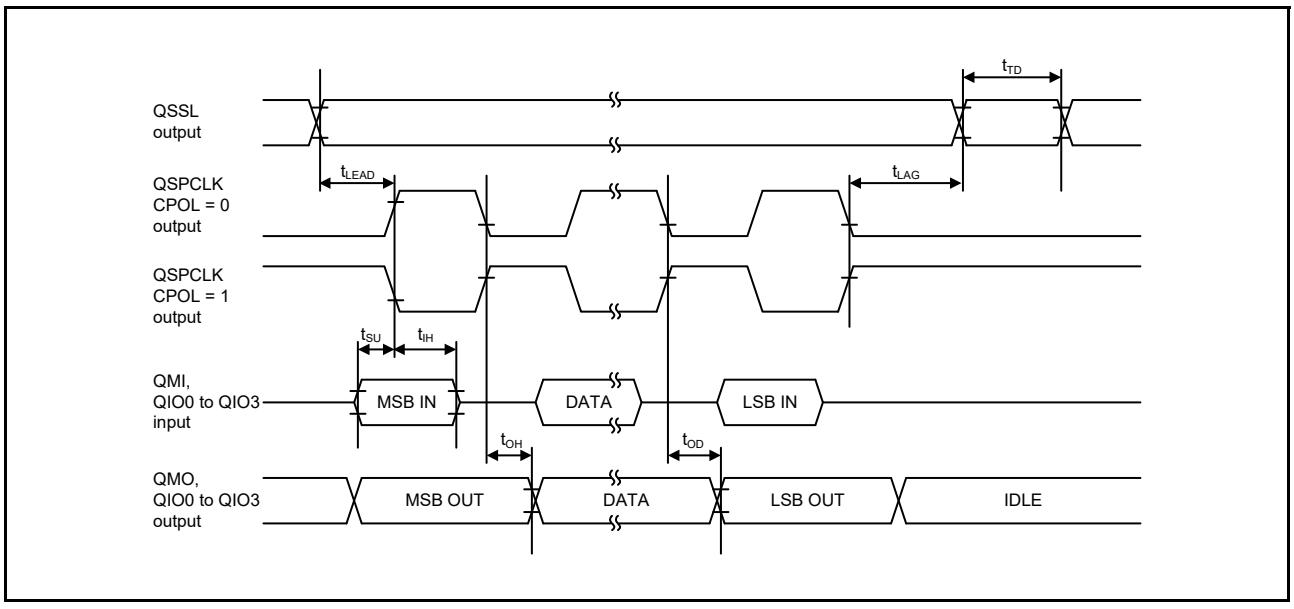



**Figure 5.52 Transmit/Receive Timing (CPHA = 0)**

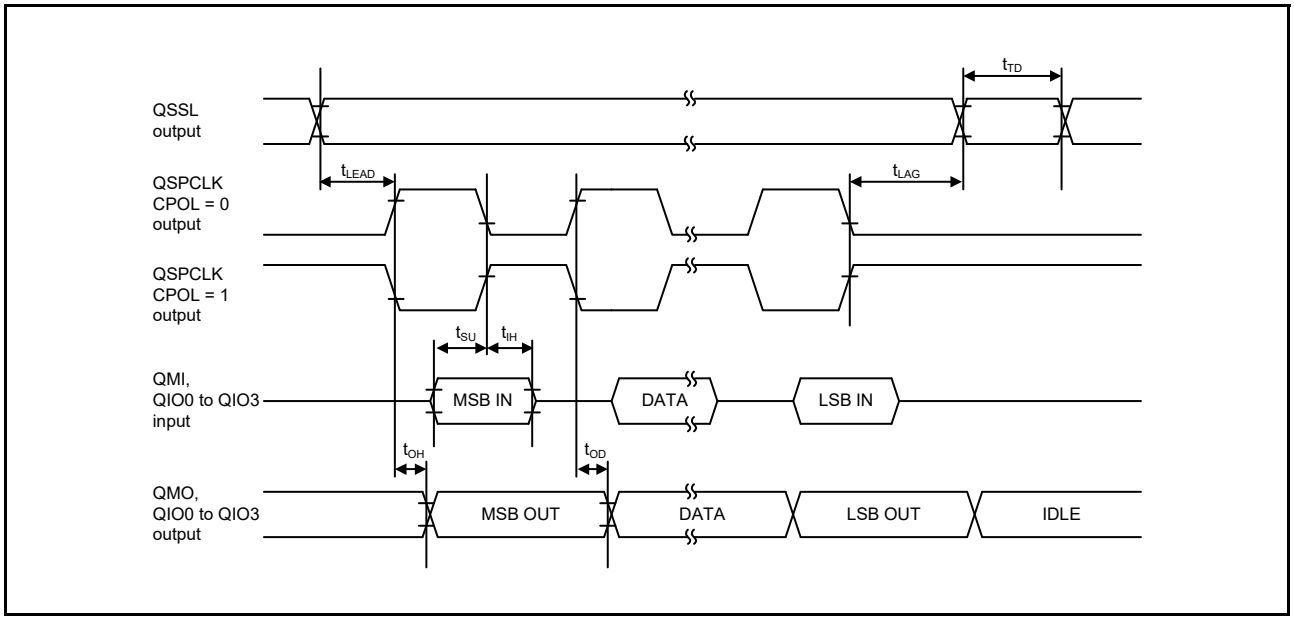



**Figure 5.53 Transmit/Receive Timing (CPHA = 1)**

**Table 5.38 RIIC Timing (1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min.*1, *2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard-mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 1300 | — | ns | Figure 5.54 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast-mode) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 600 | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | 20 × (External pull-up voltage/5.5V) | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 × (External pull-up voltage/5.5V) | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: $t_{IICcyc}$: RIIC internal reference clock (IICϕ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

**Table 5.39 RIIC Timing (2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min.*1, *2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 240 | — | ns | Figure 5.54 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 120 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 120 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 120 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 120 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 120 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 20 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 550 | pF | |
| Simple IIC (Standard-mode) | SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{PBcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| Simple IIC (Fast-mode) | SCL, SDA input rise time | $t_{Sr}$ | — | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{PBcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: $t_{IICcyc}$: RIIC internal reference clock (IICϕ) cycle, $t_{PBcyc}$: PCLKB cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. Cb is the total capacitance of the bus lines.

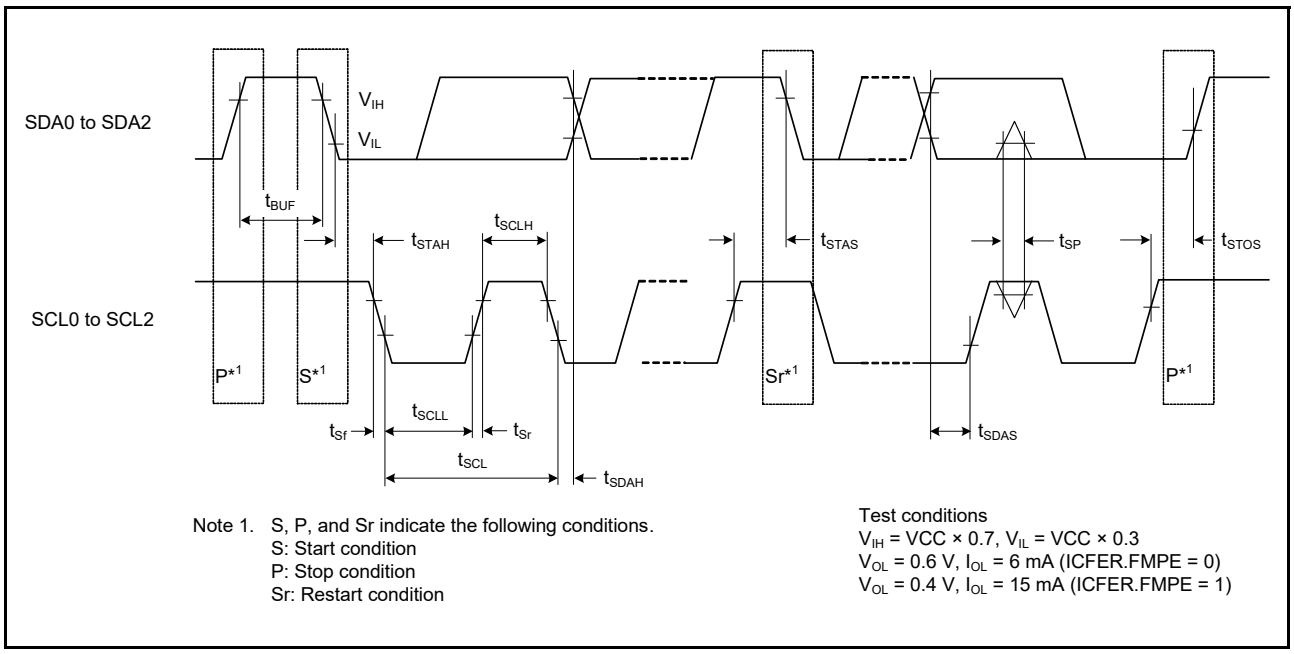



**Figure 5.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing**

### Table 5.40 MMC Host Interface Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min.*1 | Max. | Unit | Test Conditions*2 |
|---|---|---|---|---|---|---|
| MMCIF | MMC_CLK clock cycle | $t_{MMCPP}$ | 2 × $t_{PBcyc}$ | — | ns | Figure 5.55 |
| | MMC_CLK clock high level width | $t_{MMCWH}$ | 6.5 | — | ns | |
| | MMC_CLK clock low level width | $t_{MMCWL}$ | 6.5 | — | ns | |
| | MMC_CLK clock rising time | $t_{MMCLH}$ | — | 3 | ns | |
| | MMC_CLK clock falling time | $t_{MMCHL}$ | — | 3 | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode) | $t_{MMCODLY}$ | –6.6 | 6.6 | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 input data setup | $t_{MMCISU}$ | 8 | — | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 input data hold | $t_{MMCIH}$ | 2.5 | — | ns | |

Note 1. $t_{PBcyc}$: PCLKB cycle
Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All MMC AC timings are measured in combination with the pins in the same group.

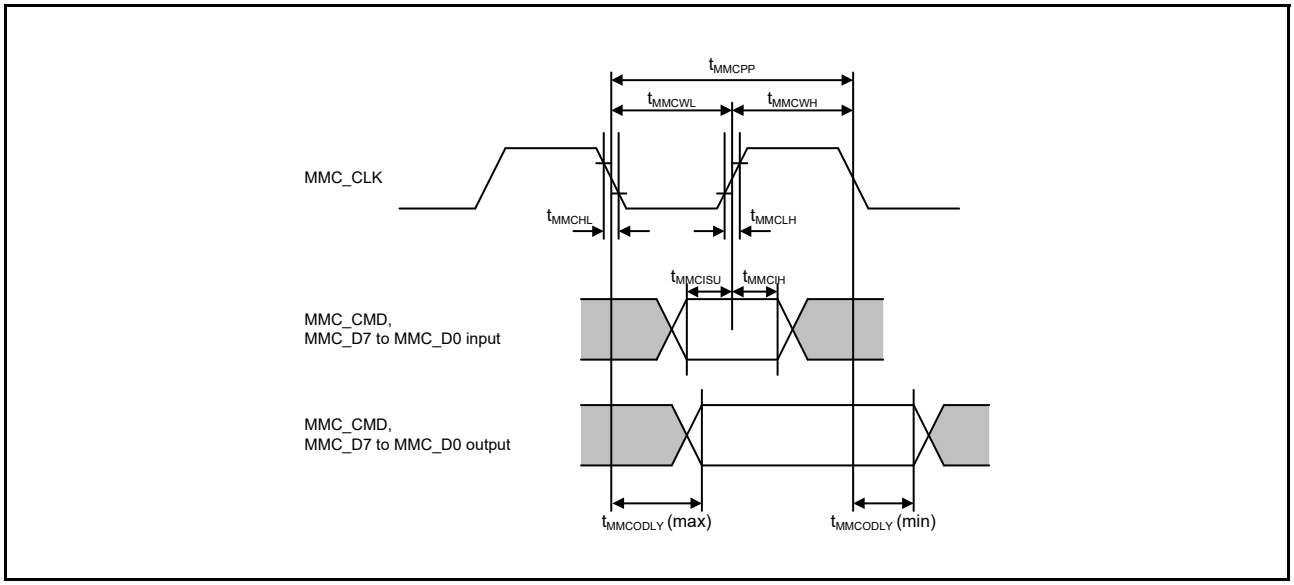


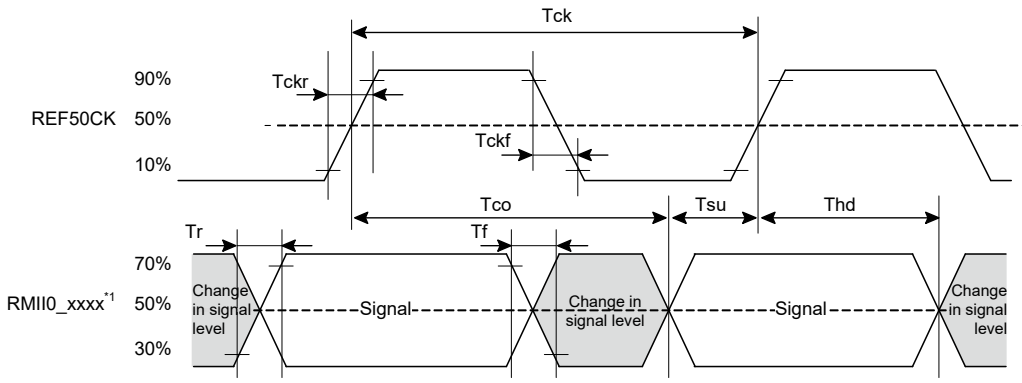

**Figure 5.55 MMC Interface**

### Table 5.41 ETHERC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| ETHERC (RMII) | REF50CK cycle time | $T_{ck}$ | 20 | — | ns | Figure 5.56 to Figure 5.58 |
| | REF50CK frequency Typ. 50 MHz | — | — | 50 + 100 ppm | MHz | |
| | REF50CK duty | — | 35 | 65 | % | |
| | REF50CK rise/fall time | $T_{ckr/ckf}$ | 0.5 | 3.5 | ns | |
| | RMII0_xxxx*1 output delay time | $T_{co}$ | 2.5 | 15.0 | ns | |
| | RMII0_xxxx*2 setup time | $T_{su}$ | 3 | — | ns | |
| | RMII0_xxxx*2 hold time | $T_{hd}$ | 1 | — | ns | |
| | RMII0_xxxx*1, *2 rise/fall time | $T_r/T_f$ | 0.5 | 5 | ns | |
| | ET0_WOL output delay time | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 5.60 |
| ETHERC (MII) | ET0_TX_CLK cycle time | $t_{Tcyc}$ | 40 | — | ns | — |
| | ET0_TX_EN output delay time | $t_{TENd}$ | 1 | 20 | ns | Figure 5.61 |
| | ET0_ETXD0 to ET0_ETXD3 output delay time | $t_{MTDd}$ | 1 | 20 | ns | |
| | ET0_CRS setup time | $t_{CRSs}$ | 10 | — | ns | |
| | ET0_CRS hold time | $t_{CRSh}$ | 10 | — | ns | |
| | ET0_COL setup time | $t_{COLs}$ | 10 | — | ns | Figure 5.62 |
| | ET0_COL hold time | $t_{COLh}$ | 10 | — | ns | |
| | ET0_RX_CLK cycle time | $t_{TRcyc}$ | 40 | — | ns | — |
| | ET0_RX_DV setup time | $t_{RDVs}$ | 10 | — | ns | Figure 5.63 |
| | ET0_RX_DV hold time | $t_{RDVh}$ | 10 | — | ns | |
| | ET0_ERXD0 to ET0_ERXD3 setup time | $t_{MRDs}$ | 10 | — | ns | |
| | ET0_ERXD0 to ET0_ERXD3 hold time | $t_{MRDh}$ | 10 | — | ns | |
| | ET0_RX_ER setup time | $t_{RERs}$ | 10 | — | ns | Figure 5.64 |
| | ET0_RX_ER hold time | $t_{RERh}$ | 10 | — | ns | |
| | ET0_WOL output delay time | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 5.65 |

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER




Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

**Figure 5.56 Timing with the REF50CK and RMII Signals**

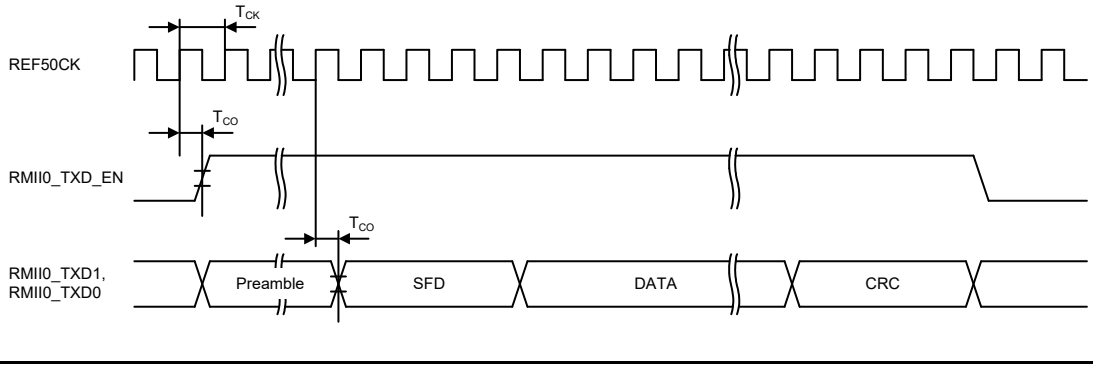



**Figure 5.57 RMII Transmission Timing**

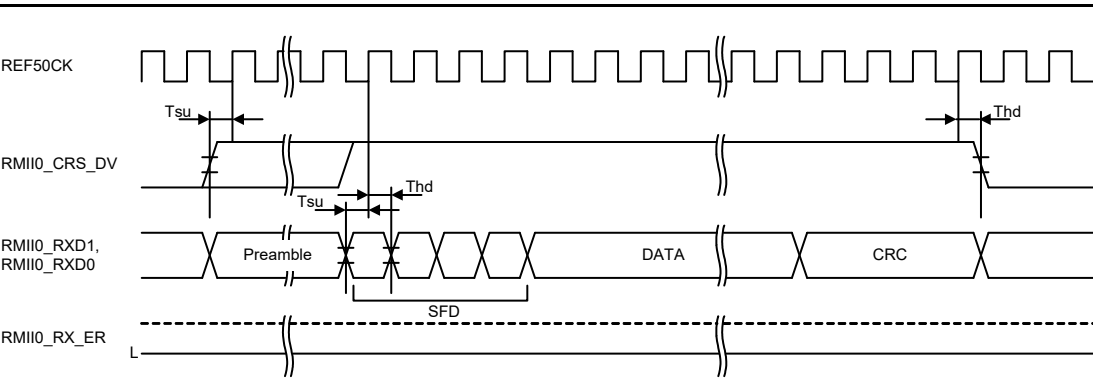



**Figure 5.58 RMII Reception Timing (Normal Operation)**

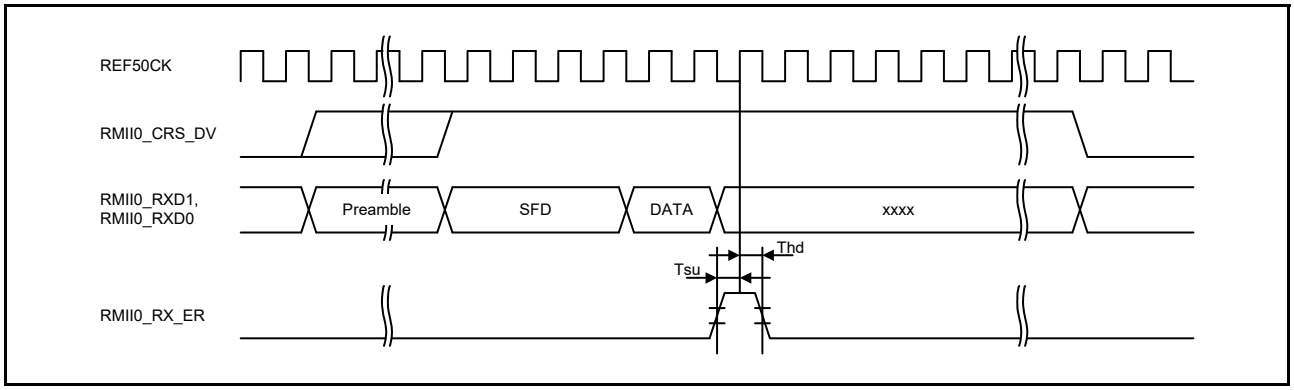



**Figure 5.59 RMII Reception Timing (Error Occurrence)**

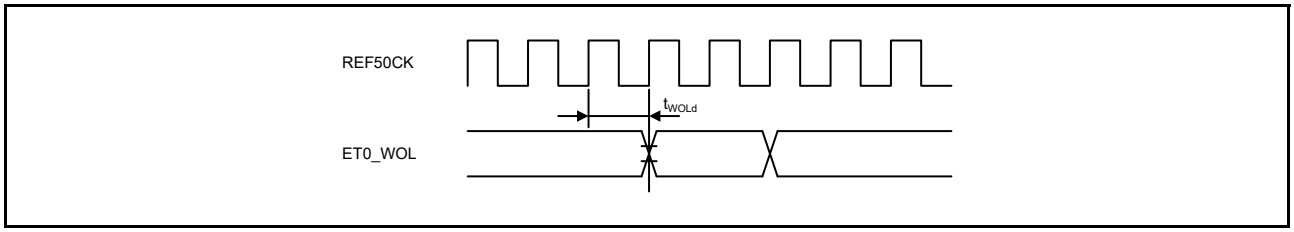



**Figure 5.60 WOL Output Timing (RMII)**

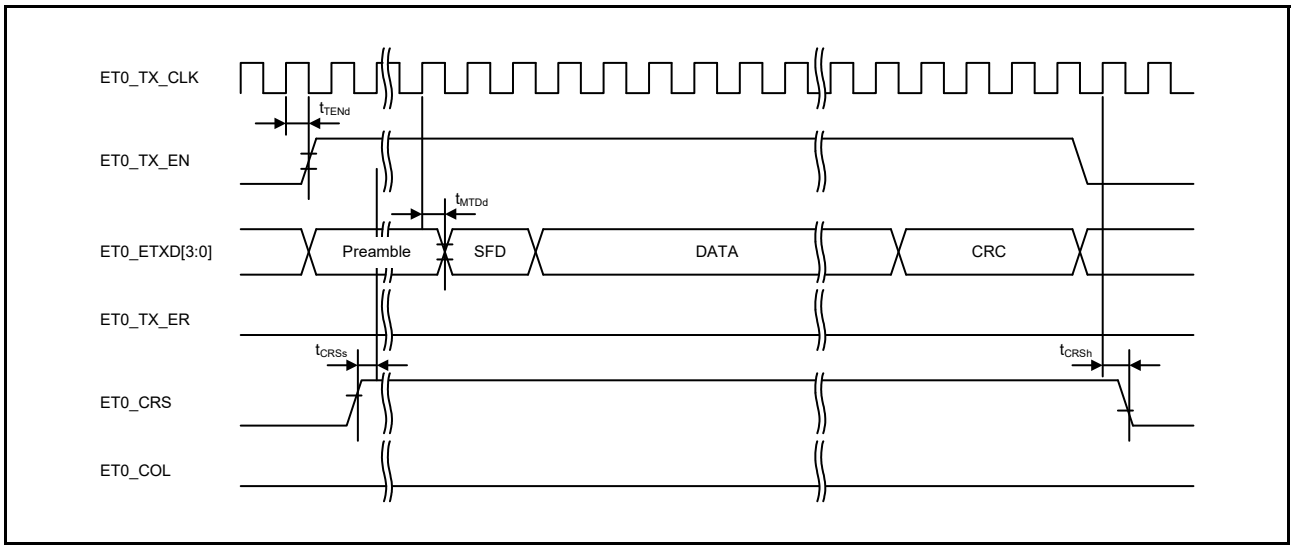



**Figure 5.61 MII Transmission Timing (Normal Operation)**

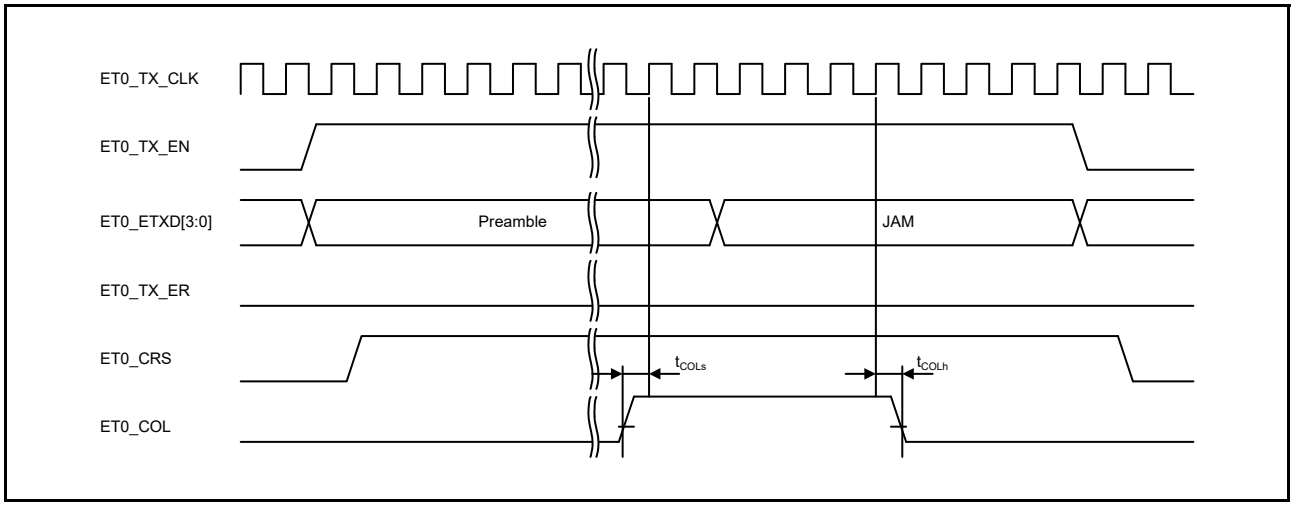



**Figure 5.62 MII Transmission Timing (Conflict Occurrence)**

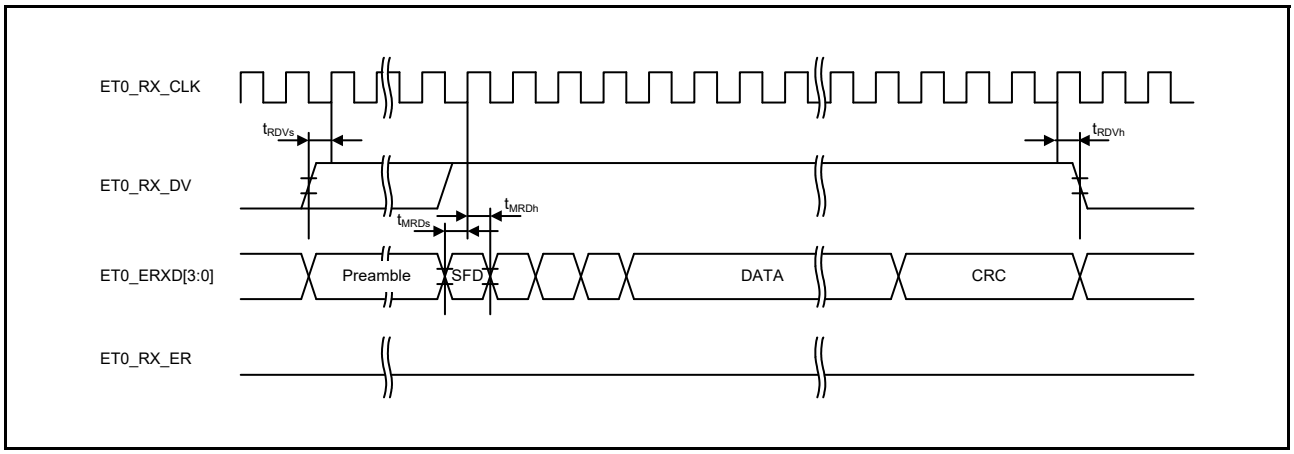



**Figure 5.63 MII Reception Timing (Normal Operation)**

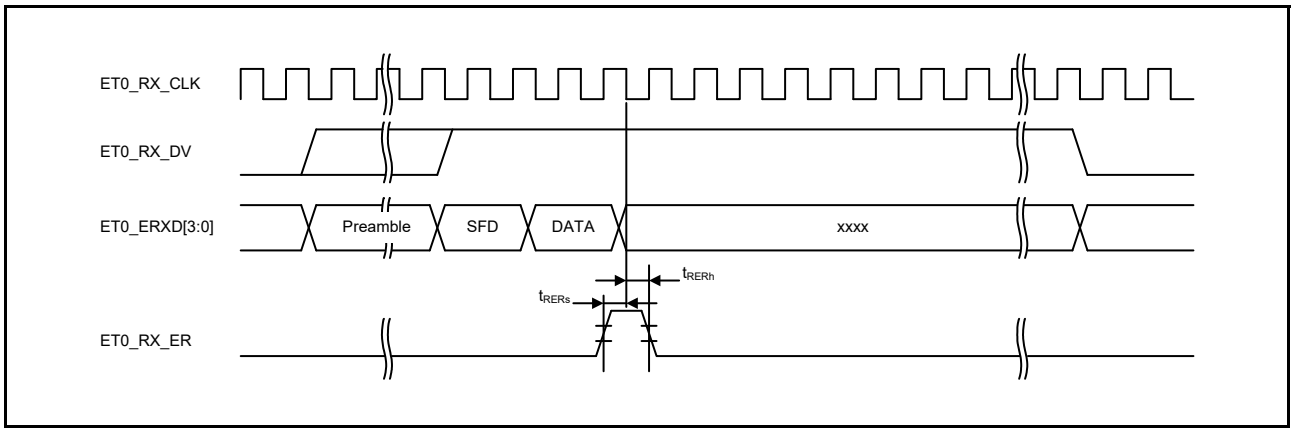



**Figure 5.64 MII Reception Timing (Error Occurrence)**

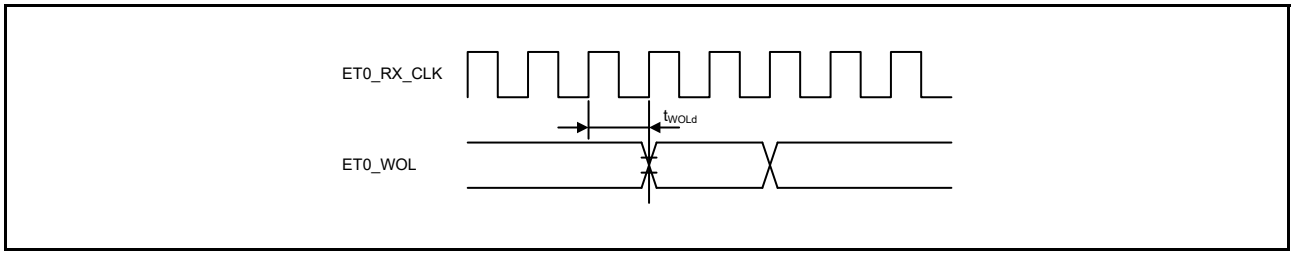



**Figure 5.65 WOL Output Timing (MII)**

### Table 5.42 PDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min.*1 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| PDC | PIXCLK input cycle time | $t_{PIXcyc}$ | 37 | — | ns | Figure 5.66 |
| | PIXCLK input high pulse width | $t_{PIXH}$ | 10 | — | ns | |
| | PIXCLK input low pulse width | $t_{PIXL}$ | 10 | — | ns | |
| | PIXCLK rising time | $t_{PIXr}$ | — | 5 | ns | |
| | PIXCLK falling time | $t_{PIXf}$ | — | 5 | ns | |
| | PCKO output cycle time | $t_{PCKcyc}$ | 2 × $t_{PBcyc}$ | — | ns | Figure 5.67 |
| | PCKO output high pulse width | $t_{PCKH}$ | ($t_{PCKcyc}$ – $t_{PCKr}$ – $t_{PCKf}$)/2 – 3 | — | ns | |
| | PCKO output low pulse width | $t_{PCKL}$ | ($t_{PCKcyc}$ – $t_{PCKr}$ – $t_{PCKf}$)/2 – 3 | — | ns | |
| | PCKO rising time | $t_{PCKr}$ | — | 5 | ns | |
| | PCKO falling time | $t_{PCKf}$ | — | 5 | ns | |
| | VSYNC/HSYNC input setup time | $t_{SYNCS}$ | 10 | — | ns | Figure 5.68 |
| | VSYNC/HSYNC input hold time | $t_{SYNCH}$ | 5 | — | ns | |
| | PIXD input setup time | $t_{PIXDS}$ | 10 | — | ns | |
| | PIXD input hold time | $t_{PIXDH}$ | 5 | — | ns | |

Note 1. $t_{PBcyc}$: PCLKB cycle

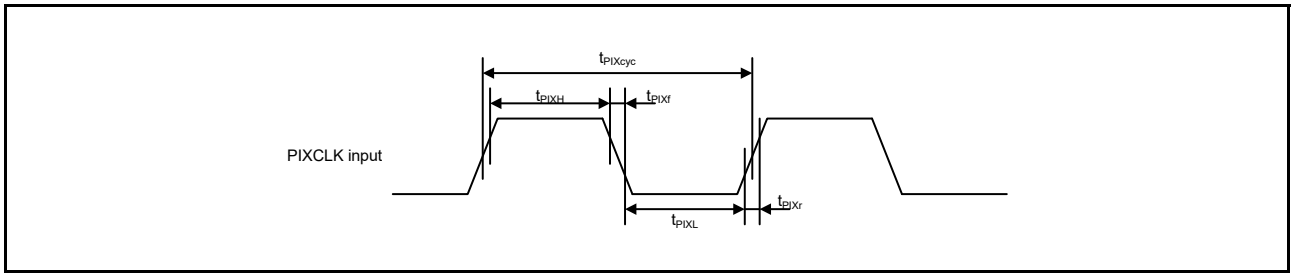



**Figure 5.66 PDC Input Clock Timing**

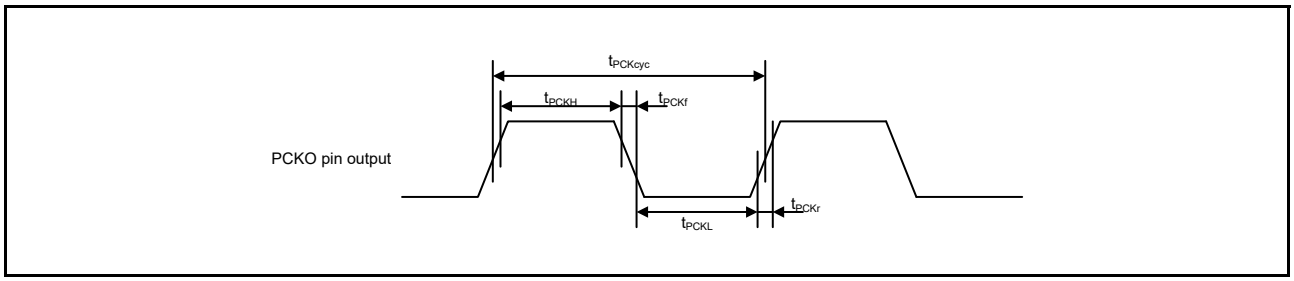



**Figure 5.67 PDC Output Clock Timing**

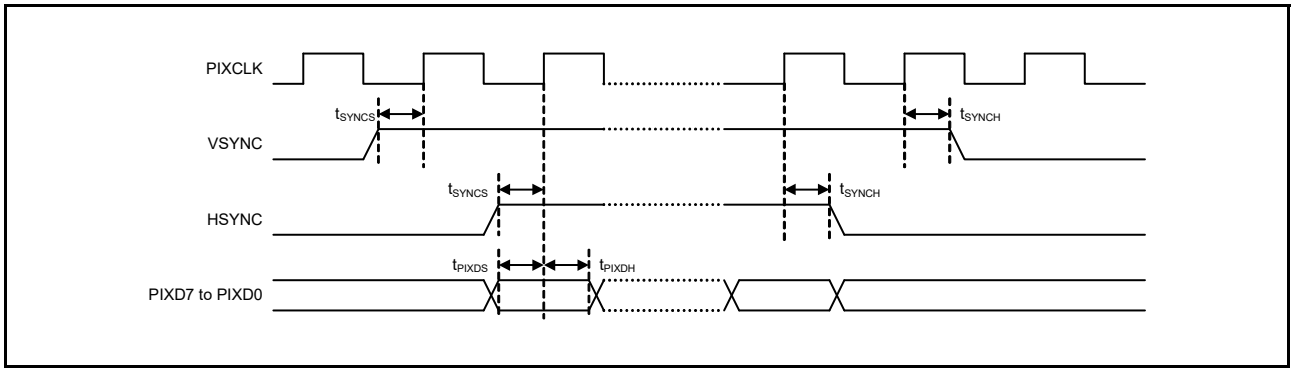



**Figure 5.68 PDC AC Timing**

### Table 5.43 GLCDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| LCD_EXTCLK Input clock frequency | $t_{Ecyc}$ | — | — | 30*1 | MHz | Figure 5.69 |
| LCD_EXTCLK Input clock Low pulse width | $t_{WL}$ | 0.45 | — | 0.55 | $t_{Ecyc}$ | |
| LCD_EXTCLK Input clock High pulse width | $t_{WH}$ | 0.45 | — | 0.55 | | |
| LCD_CLK Output clock frequency | $t_{Lcyc}$ | — | — | 30*1 | MHz | Figure 5.70 |
| LCD_CLK Output clock Low pulse width | $t_{LOL}$ | 0.4 | — | 0.6 | $t_{Lcyc}$ | |
| LCD_CLK Output clock High pulse width | $t_{LOH}$ | 0.4 | — | 0.6 | $t_{Lcyc}$ | |
| LCD data output Delay timing | $t_{DD}$ | –3.5*2 | — | 4*2 | ns | Figure 5.71 |

Note 1. Parallel RGB888,666,565: Max. 27 MHz
Serial RGB888: Max. 30 MHz (4x speed)

Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All GLCDC AC timings are measured in combination with the pins in the same group.
If we use group “-A” and “-B” combination, “LCD data output Delay timing ($t_{DD}$)” is Min = –5.0 ns, Max = 5.5 ns.

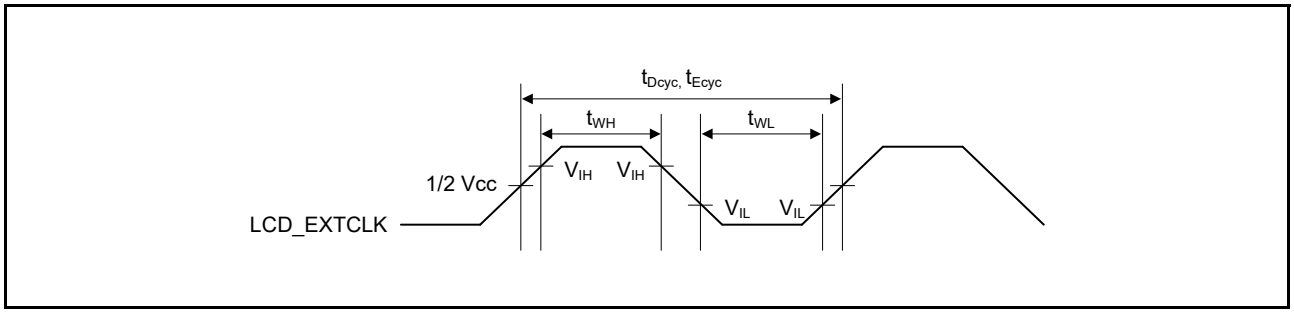



**Figure 5.69 LCD_EXTCLK Clock Input Timing**

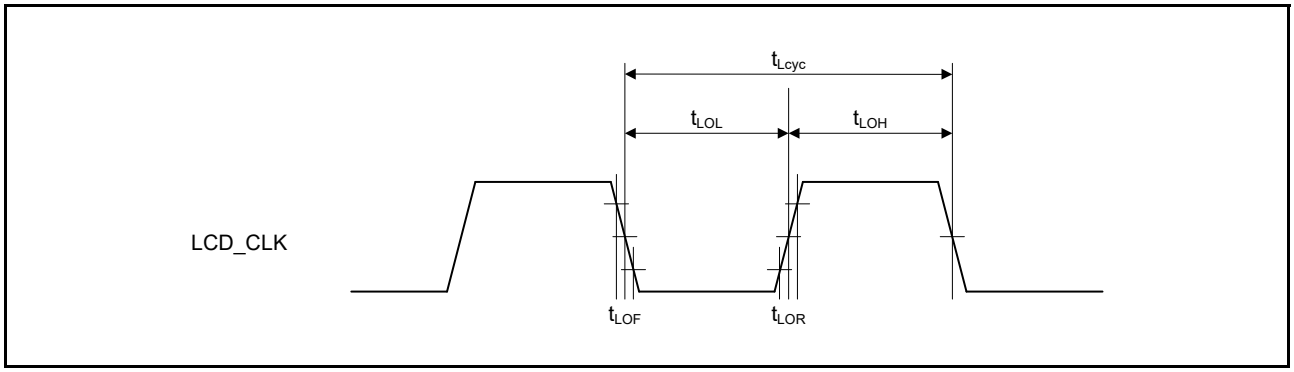



**Figure 5.70 LCD_CLK Clock Output Timing**

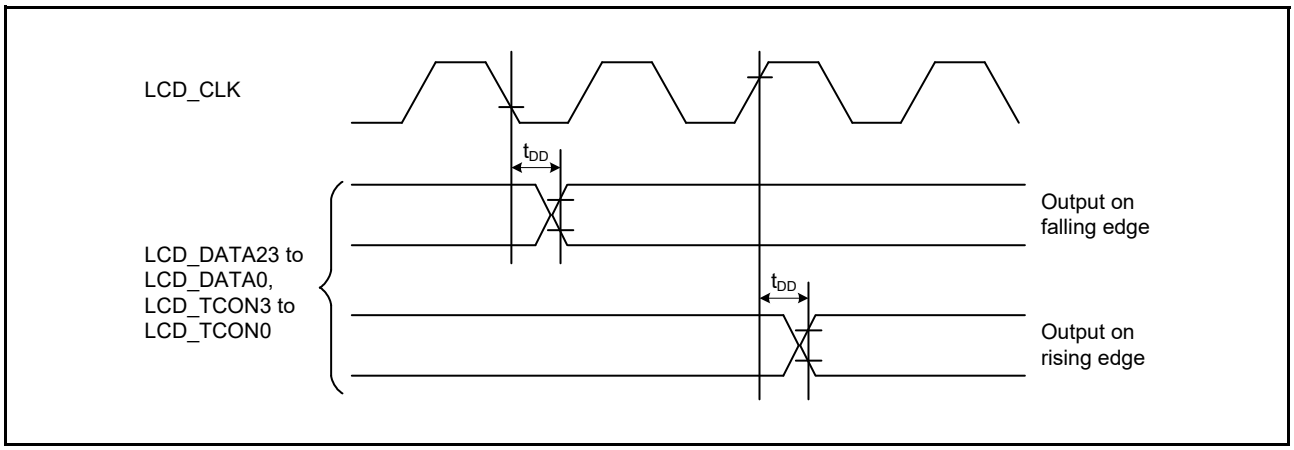



**Figure 5.71 LCD Output Data Timing**

### Table 5.44 SDHI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.*1

| Item | | Symbol | Min. | Max. | Unit | Test Conditions*2 |
|---|---|---|---|---|---|---|
| SDHI | SDHI_CLK pin output cycle time | $t_{PP(SD)}$ | 20 | — | ns | Figure 5.72 |
| | SDHI_CLK pin output high pulse width | $t_{WH(SD)}$ | 0.4 × $t_{PP(SD)}$ | — | ns | |
| | SDHI_CLK pin output low pulse width | $t_{WL(SD)}$ | 0.4 × $t_{PP(SD)}$ | — | ns | |
| | SDHI_CLK pin output rise time | $t_{TLH(SD)}$ | — | 3 | ns | |
| | SDHI_CLK pin output fall time | $t_{THL(SD)}$ | — | 3 | ns | |
| | Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins | $t_{ODLY(SD)}$ | –6.5 | 4 | ns | |
| | Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins | $t_{ISU(SD)}$ | 6 | — | ns | |
| | Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins | $t_{IH(SD)}$ | 2 | — | ns | |

Note 1. In the G-version products, the AC characteristics are measured by setting the drive capacity control register 2 corresponding the SDHI_CLK-C pin as a high-speed interface high-drive output.

Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All SDHI AC timings are measured in combination with the pins in the same group.

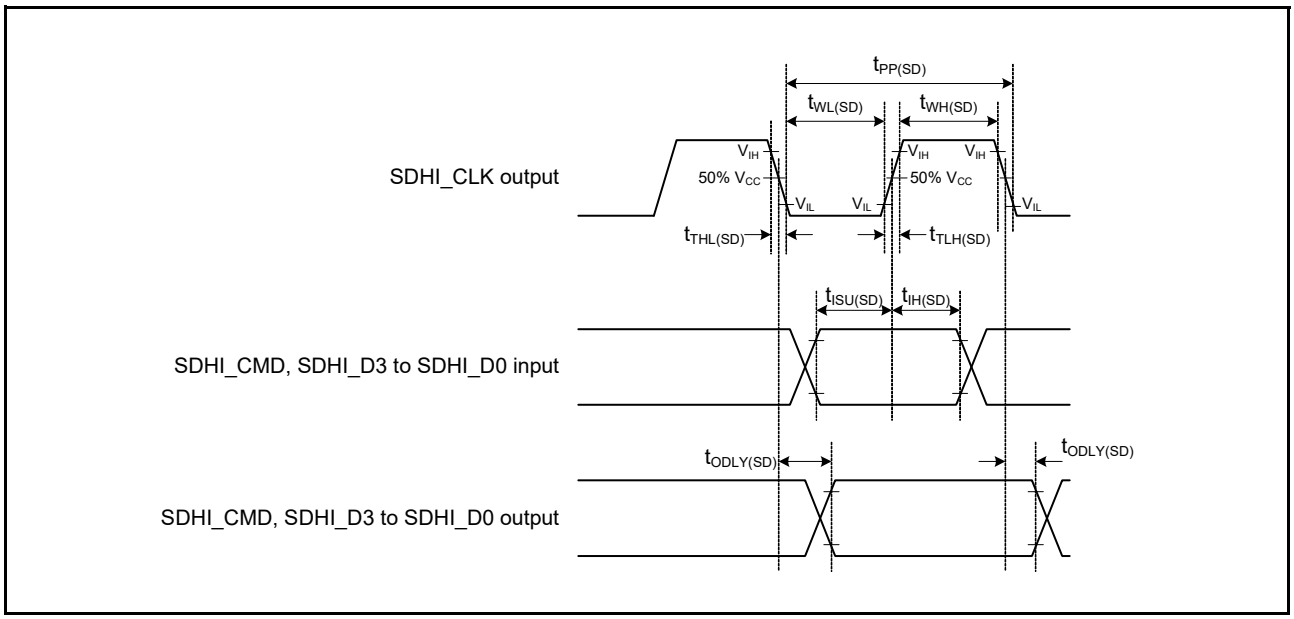



**Figure 5.72 SD Host Interface Input/Output Signal Timing**

**Table 5.45 SDSI Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions*1 |
|---|---|---|---|---|---|---|
| SDSI | SDSI_CLK pin input cycle time | $t_{PP(SDSI)}$ | 20 | — | ns | Figure 5.73 |
| | SDSI_CLK pin input high pulse width | $t_{WH(SDSI)}$ | 0.4 × $t_{PP(SDSI)}$ | — | ns | |
| | SDSI_CLK pin input low pulse width | $t_{WL(SDSI)}$ | 0.4 × $t_{PP(SDSI)}$ | — | ns | |
| | SDSI_CLK pin input rise time | $t_{TLH(SDSI)}$ | — | 3 | ns | |
| | SDSI_CLK pin input fall time | $t_{THL(SDSI)}$ | — | 3 | ns | |
| | Input data setup time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins | $t_{ISU(SDSI)}$ | 5 | — | ns | |
| | Input data hold time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins | $t_{IH(SDSI)}$ | 2 | — | ns | |
| | Output data delay time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins (default speed mode) | $t_{ODLY(SDSI)}$ | 0 | 14 | ns | Figure 5.74 |
| | Output data delay time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins (high speed mode) | | 2.5 | 14 | ns | Figure 5.75 |

Note 1. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All SDSI AC timings are measured in combination with the pins in the same group.

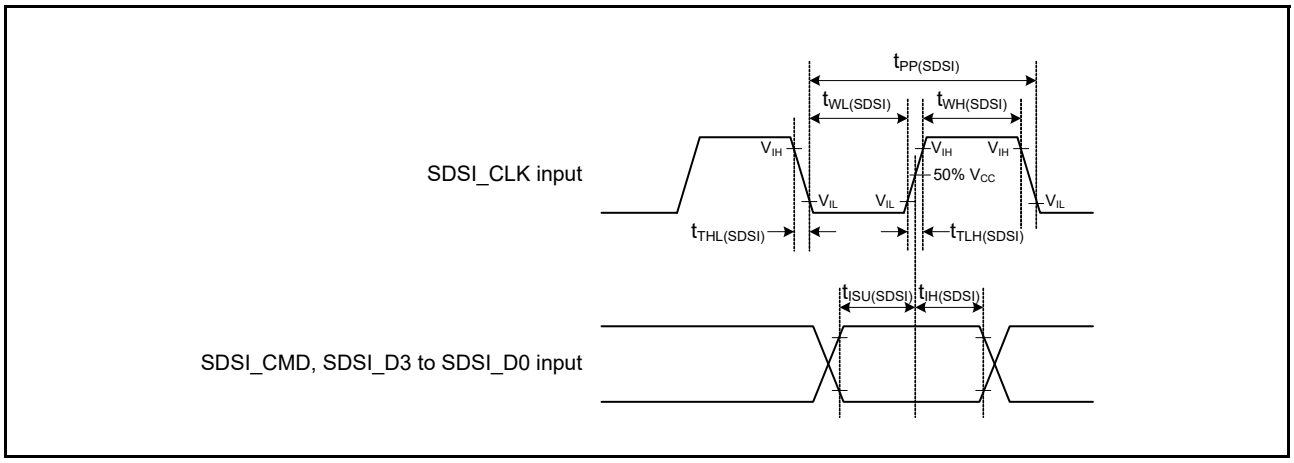



**Figure 5.73 SD Slave Interface Input Signal Timing**

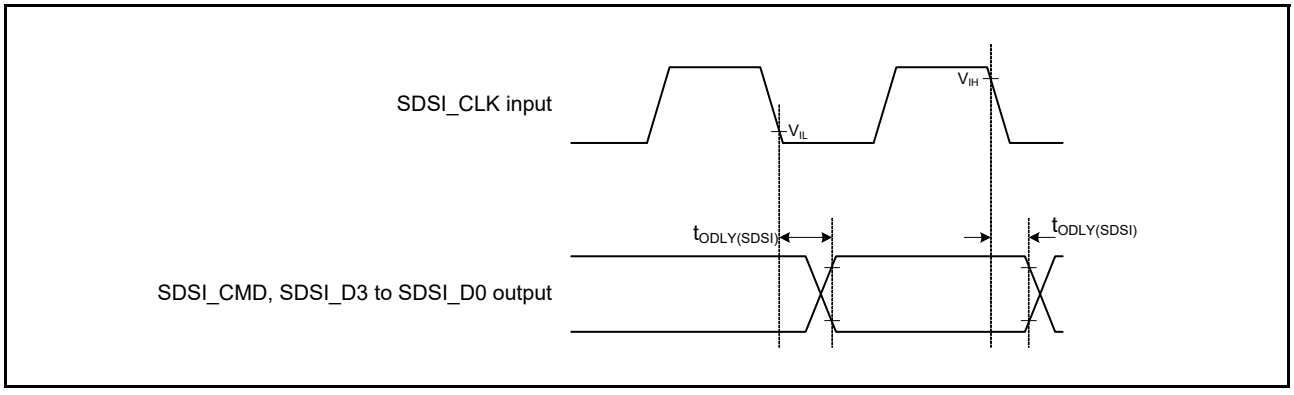



**Figure 5.74 SD Slave Interface Output Signal Timing (Default Speed Mode)**

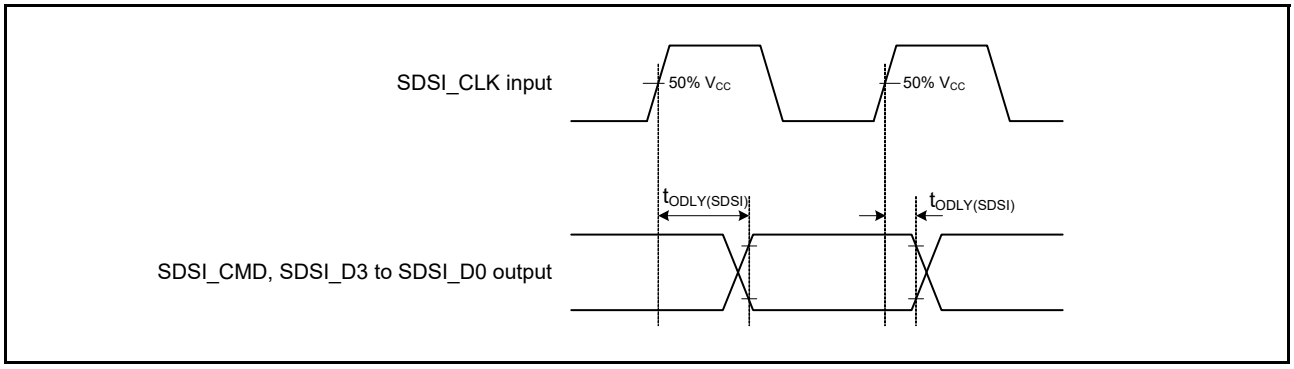



**Figure 5.75 SD Slave Interface Output Signal Timing (High Speed Mode)**

## 5.4 USB Characteristics

**Table 5.46 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high level voltage | $V_{IH}$ | 2.0 | — | — | V | |
| | Input low level voltage | $V_{IL}$ | — | — | 0.8 | V | |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | \| DP – DM \| |
| | Differential common mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | |
| Output characteristics | Output high level voltage | $V_{OH}$ | 2.8 | — | 3.6 | V | $I_{OH}$ = –200 µA |
| | Output low level voltage | $V_{OL}$ | 0.0 | — | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | Figure 5.76 |
| | Rise time | $t_{LR}$ | 75 | — | 300 | ns | |
| | Fall time | $t_{LF}$ | 75 | — | 300 | ns | |
| | Rise/fall time ratio | $t_{LR}$ / $t_{LF}$ | 80 | — | 125 | % | $t_{LR}$/ $t_{LF}$ |
| Pull-down characteristics | DP/DM pull-down resistance (when the host controller function is selected) | $R_{pd}$ | 14.25 | — | 24.80 | kΩ | |

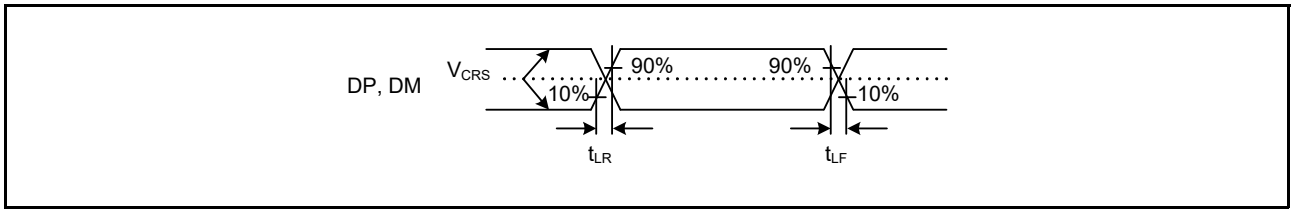



**Figure 5.76 DP and DM Output Timing (Low Speed)**

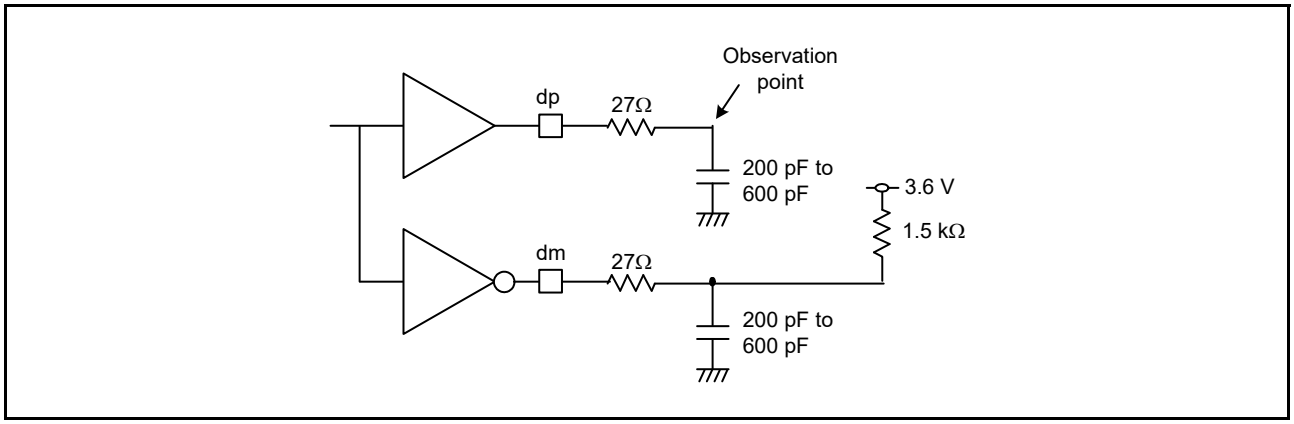



**Figure 5.77 Test Circuit (Low Speed)**

**Table 5.47 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high level voltage | $V_{IH}$ | 2.0 | — | — | V | |
| | Input low level voltage | $V_{IL}$ | — | — | 0.8 | V | |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | \| DP – DM \| |
| | Differential common mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | |
| Output characteristics | Output high level voltage | $V_{OH}$ | 2.8 | — | 3.6 | V | $I_{OH}$ = –200 µA |
| | Output low level voltage | $V_{OL}$ | 0.0 | — | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | Figure 5.78 |
| | Rise time | $t_{FR}$ | 4 | — | 20 | ns | |
| | Fall time | $t_{FF}$ | 4 | — | 20 | ns | |
| | Rise/fall time ratio | $t_{FR}$ / $t_{FF}$ | 90 | — | 111.11 | % | $t_{FR}$/ $t_{FF}$ |
| | Output resistance | $Z_{DRV}$ | 28 | — | 44 | Ω | Rs = 27 Ω included |
| Pull-up and pull-down characteristics | DP pull-up resistance (when the function controller function is selected) | $R_{pu}$ | 0.900 | — | 1.575 | kΩ | Idle state |
| | | | 1.425 | — | 3.090 | kΩ | At transmission and reception |
| | DP/DM pull-down resistance (when the host controller function is selected) | $R_{pd}$ | 14.25 | — | 24.80 | kΩ | |

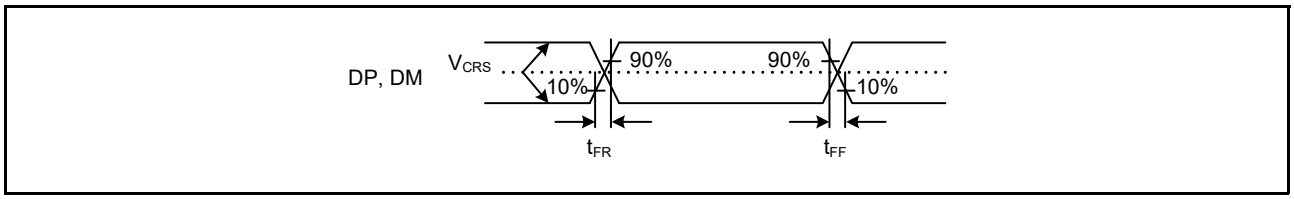



**Figure 5.78 DP and DM Output Timing (Full-Speed)**

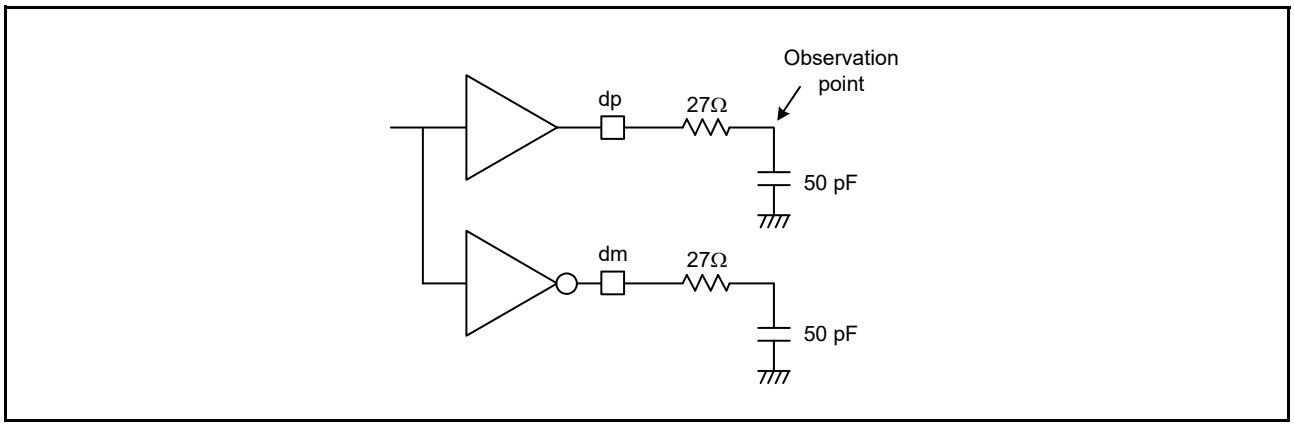



**Figure 5.79 Test Circuit (Full-Speed)**

## 5.5 A/D Conversion Characteristics

**Table 5.48 12-Bit A/D (Unit 0) Conversion Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, $T_a = T_{opr}$,
Source impedance = 1.0 kΩ

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resolution | | 8 | — | 12 | Bit | |
| Analog input capacitance | | — | — | 30 | pF | |
| Channel-dedicated sample-and-hold circuits in use (AN000 to AN002) | Conversion time*1 (Operation at PCLKC = 60 MHz) | 1.06 (0.4 + 0.25) *2 | — | — | µs | • Sampling of channel-dedicated sample-and-hold circuits in 24 states<br>• Sampling in 15 states |
| | Offset error | — | ±1.5 | ±3.5 | LSB | AN000 to AN002 = 0.25 V |
| | Full-scale error | — | ±1.5 | ±3.5 | LSB | AN000 to AN002 = VREFH0 – 0.25 V |
| | Quantization error | — | ±0.5 | — | LSB | |
| | Absolute accuracy | — | ±3.0 | ±5.5 | LSB | |
| | DNL differential nonlinearity error | — | ±1.0 | ±2.0 | LSB | |
| | INL integral nonlinearity error | — | ±1.5 | ±3.0 | LSB | |
| | Holding characteristics of sample-and-hold circuits | — | — | 20 | µs | |
| | Dynamic range | 0.25 | — | VREFH0 – 0.25 | V | |
| Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007) | Conversion time*1 (Operation at PCLKC = 60 MHz) | 0.48 (0.267)*2 | — | — | µs | Sampling in 16 states |
| | Offset error | — | ±1.0 | ±2.5 | LSB | |
| | Full-scale error | — | ±1.0 | ±2.5 | LSB | |
| | Quantization error | — | ±0.5 | — | LSB | |
| | Absolute accuracy | — | ±2.5 | ±4.5 | LSB | |
| | DNL differential nonlinearity error | — | ±0.5 | ±1.5 | LSB | |
| | INL integral nonlinearity error | — | ±1.0 | ±2.5 | LSB | |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

### Table 5.49 12-Bit A/D (Unit 1) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 1 MHz to 60 MHz, $T_a = T_{opr}$,
Source impedance = 1.0 kΩ

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | 8 | — | 12 | Bit | |
| Conversion time*1 (Operation at PCLKD = 60 MHz) | 0.88 (0.633)*2 | — | — | µs | Sampling in 38 states (ADSAM.SAM = 1) |
| Conversion time*1 (Operation at PCLKD = 30 MHz) | 1 (0.500)*2 | — | — | µs | Sampling in 15 states (ADSAM.SAM = 1) |
| Analog input capacitance | — | — | 30 | pF | |
| Offset error | — | ±2.0 | ±3.5 | LSB | |
| Full-scale error | — | ±2.0 | ±3.5 | LSB | |
| Quantization error | — | ±0.5 | — | LSB | |
| Absolute accuracy | — | ±4.0 | ±6.0 | LSB | |
| DNL differential nonlinearity error (Operation at PCLKD = 60 MHz) | — | ±1.5 | ±4.0 | LSB | |
| DNL differential nonlinearity error (Operation at PCLKD = 30 MHz) | — | ±1.5 | ±2.5 | LSB | |
| INL integral nonlinearity error (Operation at PCLKD = 60 MHz) | — | ±2.0 | ±4.0 | LSB | |
| INL integral nonlinearity error (Operation at PCLKD = 30 MHz) | — | ±2.0 | ±3.5 | LSB | |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

### Table 5.50 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 60 MHz, $T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V | |

## 5.6 D/A Conversion Characteristics

**Table 5.51 D/A Conversion Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Resolution | | — | 12 | 12 | 12 | Bit | |
| Unbuffered output | Absolute accuracy | — | — | — | ±6.0 | LSB | 2-MΩ resistive load<br>10-bit conversion |
| | Differential nonlinearity error | DNL | — | ±1.0 | ±2.0 | LSB | 2-MΩ resistive load |
| | Output resistance | $R_O$ | — | 8.6 | — | kΩ | |
| | Setting time | $t_S$ | — | — | 3 | μs | 20-pF capacitive load |
| Buffered output | Load resistance | $R_L$ | 5 | — | — | kΩ | |
| | Load capacitance | $C_L$ | — | — | 50 | pF | |
| | Output voltage | $V_O$ | 0.2 | — | AVCC1 – 0.2 | V | |
| | Differential nonlinearity error | DNL | — | ±1.0 | ±2.0 | LSB | |
| | Integral nonlinearity error | INL | — | ±2.0 | ±4.0 | LSB | |
| | Setting time | $t_S$ | — | — | 4 | μs | |

## 5.7 Temperature Sensor Characteristics

**Table 5.52 Temperature Sensor Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Relative accuracy | — | ±1 | — | °C | |
| Temperature slope | — | 4 | — | mV/°C | |
| Output voltage (at 25°C) | — | 1.21 | — | V | |
| Temperature sensor start time | — | — | 30 | μs | |
| Sampling time*1 | 4.15 | — | — | μs | |

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

## 5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

**Table 5.53 Power-on Reset Circuit and Voltage Detection Circuit Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | Low power consumption function disabled*1 | $V_{POR}$ | 2.5 | 2.6 | 2.7 | V | Figure 5.80 |
| | | Low power consumption function enabled*2 | | 1.8 | 2.25 | 2.7 | | |
| | Voltage detection circuit (LVD0) | | $V_{det0_1}$ | 2.84 | 2.94 | 3.04 | | Figure 5.81 |
| | | | $V_{det0_2}$ | 2.77 | 2.87 | 2.97 | | |
| | | | $V_{det0_3}$ | 2.70 | 2.80 | 2.90 | | |
| | Voltage detection circuit (LVD1) | | $V_{det1_1}$ | 2.89 | 2.99 | 3.09 | | Figure 5.82 |
| | | | $V_{det1_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det1_3}$ | 2.75 | 2.85 | 2.95 | | |
| | Voltage detection circuit (LVD2) | | $V_{det2_1}$ | 2.89 | 2.99 | 3.09 | | Figure 5.83 |
| | | | $V_{det2_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det2_3}$ | 2.75 | 2.85 | 2.95 | | |
| Internal reset time | Power-on reset time | | $t_{POR}$ | — | 4.6 | — | ms | Figure 5.80 |
| | LVD0 reset time | | $t_{LVD0}$ | — | 0.70 | — | | Figure 5.81 |
| | LVD1 reset time | | $t_{LVD1}$ | — | 0.57 | — | | Figure 5.82 |
| | LVD2 reset time | | $t_{LVD2}$ | — | 0.57 | — | | Figure 5.83 |
| Minimum VCC down time | | | $t_{VOFF}$ | 200 | — | — | μs | Figure 5.80, Figure 5.81 |
| Response delay time | | | $t_{det}$ | — | — | 200 | μs | Figure 5.80 to Figure 5.83 |
| LVD operation stabilization time (after LVD is enabled) | | | $T_{d(E-A)}$ | — | — | 10 | μs | Figure 5.82, Figure 5.83 |
| Hysteresis width (LVD1 and LVD2) | | | $V_{LVH}$ | — | 70 | — | mV | |

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det1}$, and $V_{det2}$ for the POR/ LVD.
Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.
Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

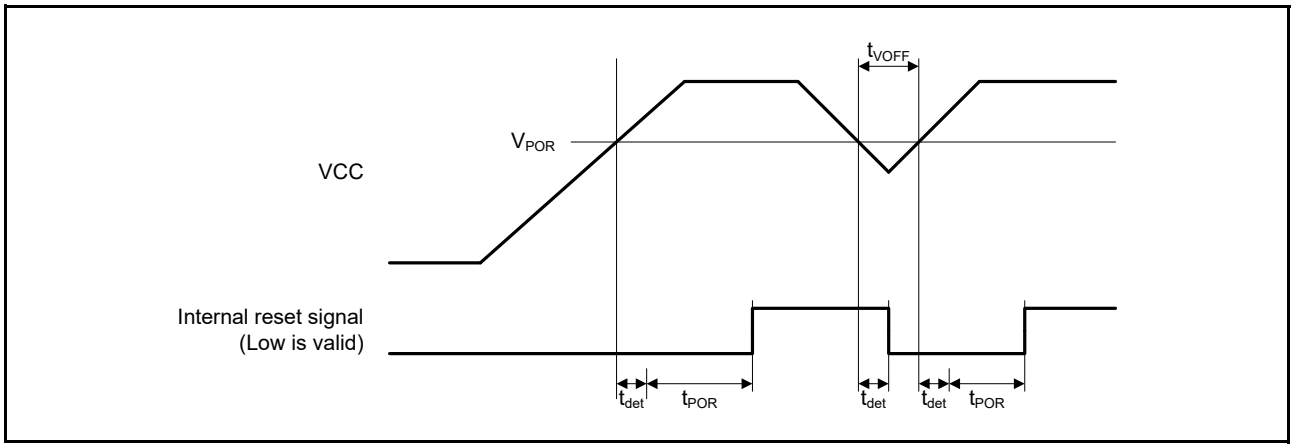



**Figure 5.80 Power-on Reset Timing**

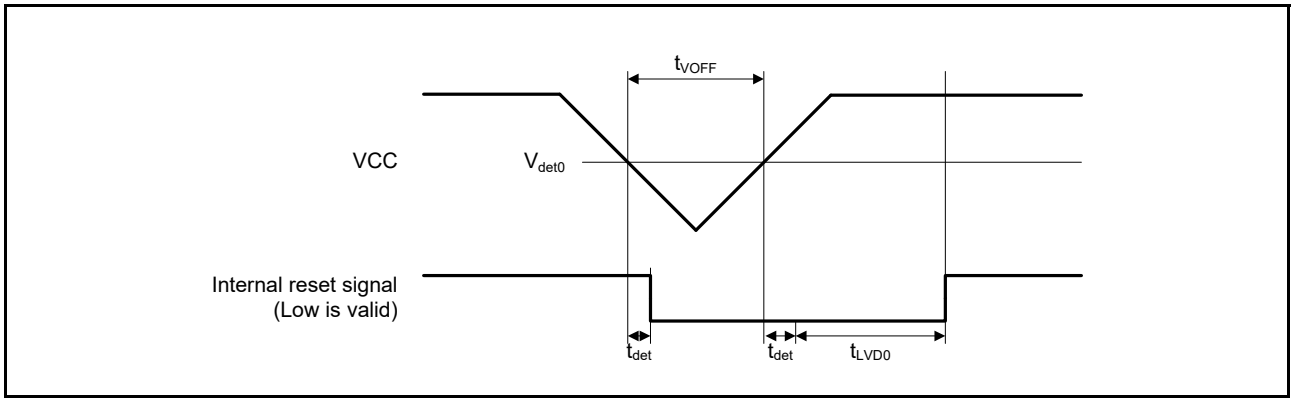



**Figure 5.81 Voltage Detection Circuit Timing ($V_{det0}$)**

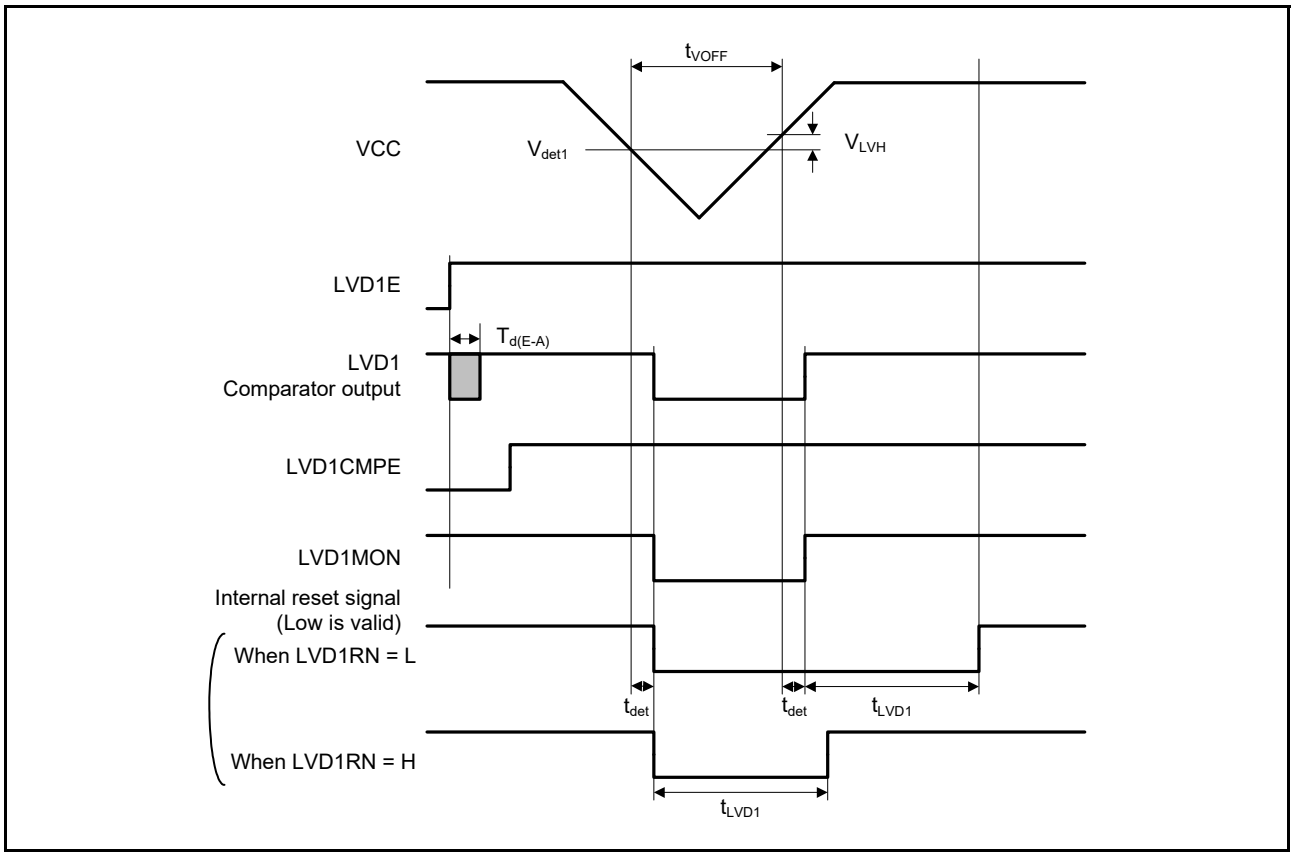



**Figure 5.82 Voltage Detection Circuit Timing ($V_{det1}$)**

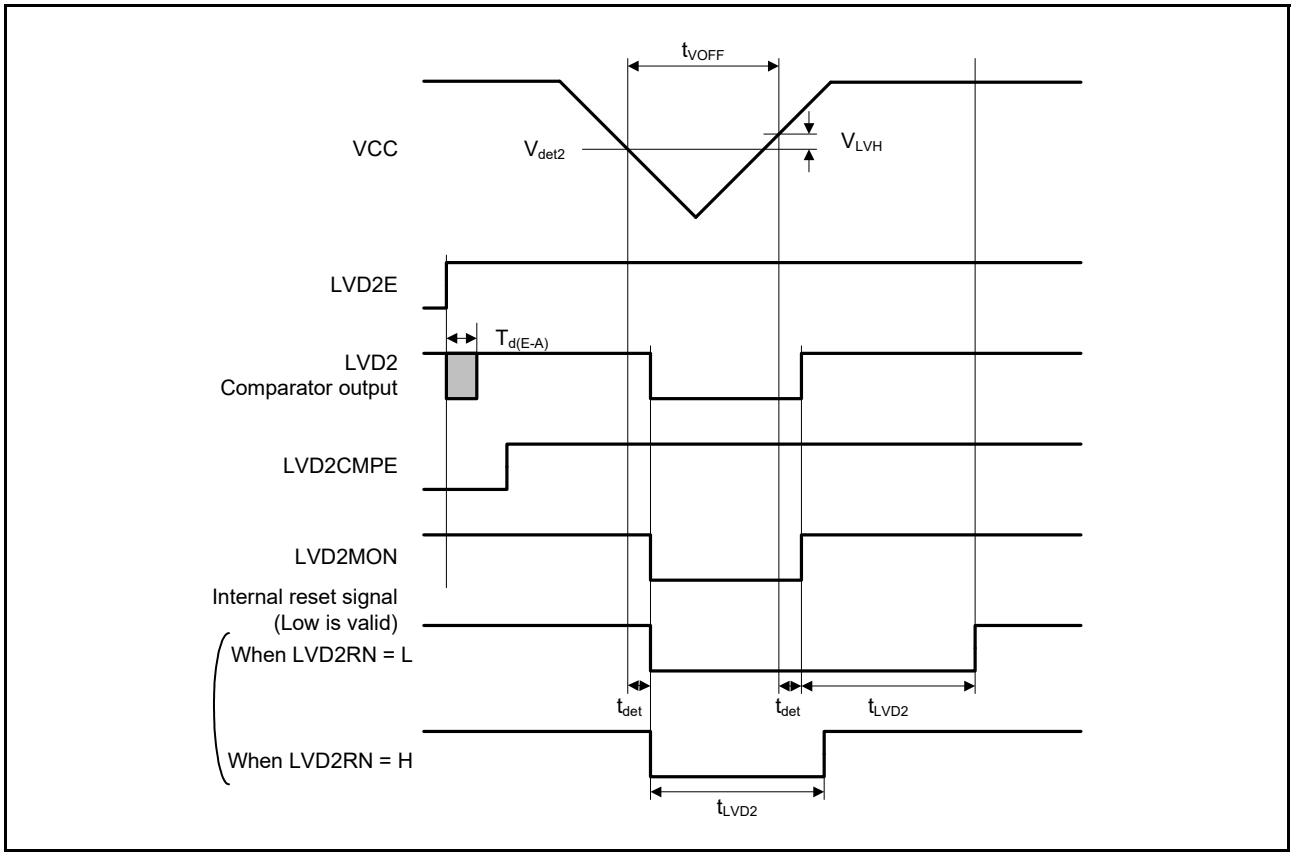



**Figure 5.83 Voltage Detection Circuit Timing ($V_{det2}$)**

## 5.9 Oscillation Stop Detection Timing

**Table 5.54 Oscillation Stop Detection Circuit Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detection time | $t_{dr}$ | — | — | 1 | ms | Figure 5.84 |

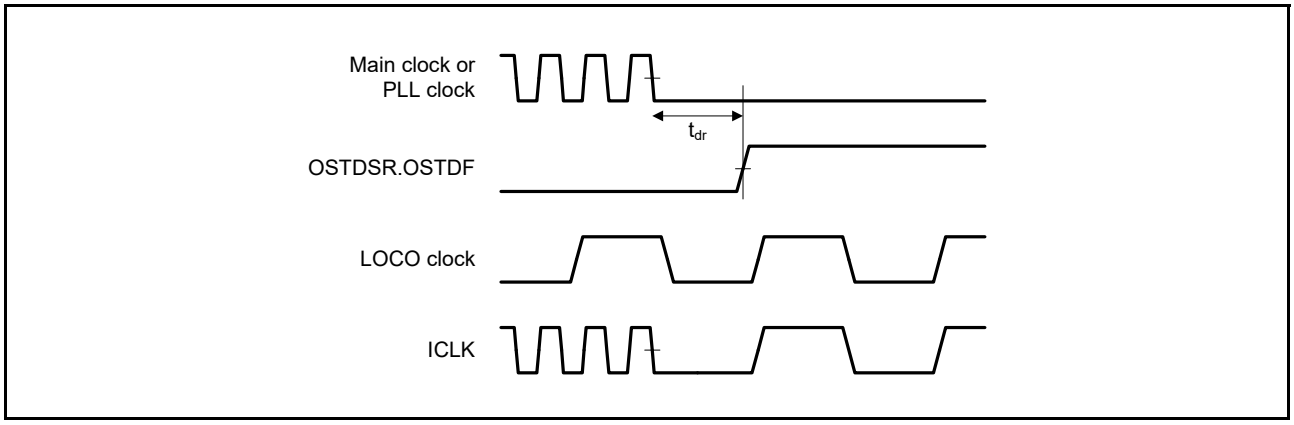



**Figure 5.84 Oscillation Stop Detection Timing**

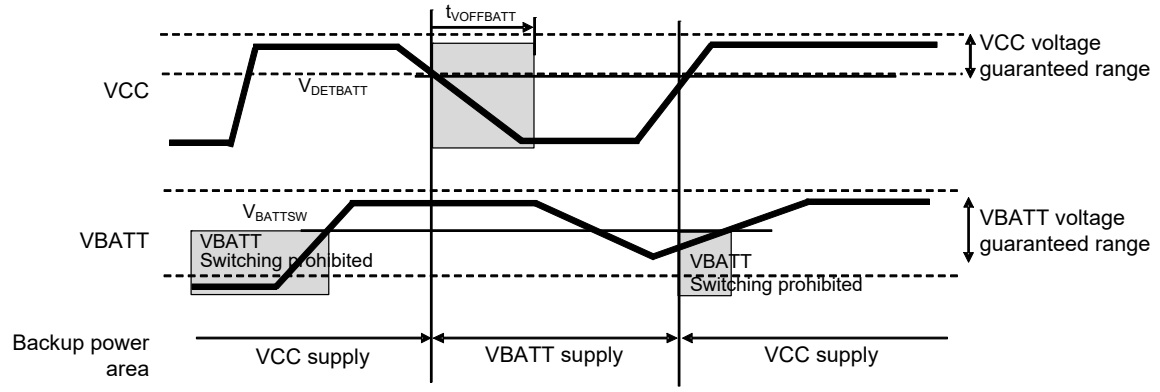
## 5.10 Battery Backup Function Characteristics

**Table 5.55 Battery Backup Function Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$V_{BATT}$ = 2.0 to 3.6 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Voltage level for switching to battery backup | $V_{DETBATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 5.85 |
| Lower-limit $V_{BATT}$ voltage for power supply switching due to VCC voltage drop | $V_{BATTSW}$ | 2.70 | — | — | | |
| VCC-off period for starting power supply switching | $t_{VOFFBATT}$ | 200 | — | — | µs | |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).




Note. The VBATT voltage when the supplied power source switches from Vcc to $V_{BATT}$ should not be lower than $V_{BATTSW}$, the lower-limit VBATT voltage for switching between power supplies due to a drop in the VCC voltage.

**Figure 5.85 Battery Backup Function Characteristics**

## 5.11 Flash Memory Characteristics

**Table 5.56 Code Flash Memory Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 15 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time $N_{PEC}$ ≤ 100 times | 128 bytes | $t_{P128}$ | — | 0.75 | 13.2 | — | 0.38 | 6.6 | — | 0.34 | 6 | ms |
| | 8 Kbytes | $t_{P8K}$ | — | 49 | 176 | — | 25 | 88 | — | 22 | 80 | ms |
| | 32 Kbytes | $t_{P32K}$ | — | 194 | 704 | — | 97 | 352 | — | 88 | 320 | ms |
| Programming time $N_{PEC}$ > 100 times | 128 bytes | $t_{P128}$ | — | 0.91 | 15.8 | — | 0.46 | 8 | — | 0.41 | 7.2 | ms |
| | 8 Kbytes | $t_{P8K}$ | — | 60 | 212 | — | 30 | 106 | — | 27 | 96 | ms |
| | 32 Kbytes | $t_{P32K}$ | — | 234 | 848 | — | 117 | 424 | — | 106 | 384 | ms |
| Erasure time $N_{PEC}$ ≤ 100 times | 8 Kbytes | $t_{E8K}$ | — | 78 | 216 | — | 48 | 132 | — | 43 | 120 | ms |
| | 32 Kbytes | $t_{E32K}$ | — | 283 | 864 | — | 173 | 528 | — | 157 | 480 | ms |
| Erasure time $N_{PEC}$ > 100 times | 8 Kbytes | $t_{E8K}$ | — | 94 | 260 | — | 58 | 158 | — | 52 | 144 | ms |
| | 32 Kbytes | $t_{E32K}$ | — | 341 | 1040 | — | 208 | 632 | — | 189 | 576 | ms |
| Reprogramming/erasure cycle*1 | | $N_{PEC}$ | 10000 *2 | — | — | 10000 *2 | — | — | 10000 *2 | — | — | Times |
| Suspend delay time during programming | | $t_{SPD}$ | — | — | 264 | — | — | 132 | — | — | 120 | µs |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 216 | — | — | 132 | — | — | 120 | µs |
| Second suspend delay time during erasure (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.7 | — | — | 1.7 | ms |
| Suspend delay time during erasure (in erasure priority mode) | | $t_{SEED}$ | — | — | 1.7 | — | — | 1.7 | — | — | 1.7 | ms |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 22 | — | — | 20 | µs |
| Data hold time*3 | | $t_{DRP}$ | 10 | — | — | 10 | — | — | 10 | — | — | Year |

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

### Table 5.57 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 15 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time | 4 bytes | $t_{DP4}$ | — | 0.36 | 3.8 | — | 0.18 | 1.9 | — | 0.16 | 1.7 | ms |
| Erasure time | 64 bytes | $t_{DP64}$ | — | 3.1 | 18 | — | 1.9 | 11 | — | 1.7 | 10 | ms |
| | 128 bytes | $t_{DP128}$ | — | 4.7 | 27 | — | 2.9 | 16 | — | 2.6 | 15 | ms |
| | 256 bytes | $t_{DP256}$ | — | 8.9 | 50 | — | 5.4 | 31 | — | 4.9 | 28 | ms |
| Blank check time | 4 bytes | $t_{DBC4}$ | — | — | 84 | — | — | 33 | — | — | 30 | µs |
| | 64 bytes | $t_{DBC64}$ | — | — | 280 | — | — | 110 | — | — | 100 | µs |
| | 2 Kbytes | $t_{DBC2K}$ | — | — | 6160 | — | — | 2420 | — | — | 2200 | µs |
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 100000 *2 | — | — | 100000 *2 | — | — | 100000 *2 | — | — | Times |
| Suspend delay time during programming | | $t_{DSPD}$ | — | — | 264 | — | — | 132 | — | — | 120 | µs |
| First suspend delay time during erasure (in suspend priority mode) | 64 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs |
| | 128 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs |
| | 256 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs |
| Second suspend delay time during erasure (in suspend priority mode) | 64 bytes | — | — | — | 300 | — | — | 300 | — | — | 300 | µs |
| | 128 bytes | — | — | — | 390 | — | — | 390 | — | — | 390 | µs |
| | 256 bytes | — | — | — | 570 | — | — | 570 | — | — | 570 | µs |
| Suspend delay time during erasing (in suspend priority mode) | 64 bytes | — | — | — | 300 | — | — | 300 | — | — | 300 | µs |
| | 128 bytes | — | — | — | 390 | — | — | 390 | — | — | 390 | µs |
| | 256 bytes | — | — | — | 570 | — | — | 570 | — | — | 570 | µs |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 22 | — | — | 20 | µs |
| Data hold time*3 | | $t_{DDRP}$ | 10 | — | — | 10 | — | — | 10 | — | — | Year |

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

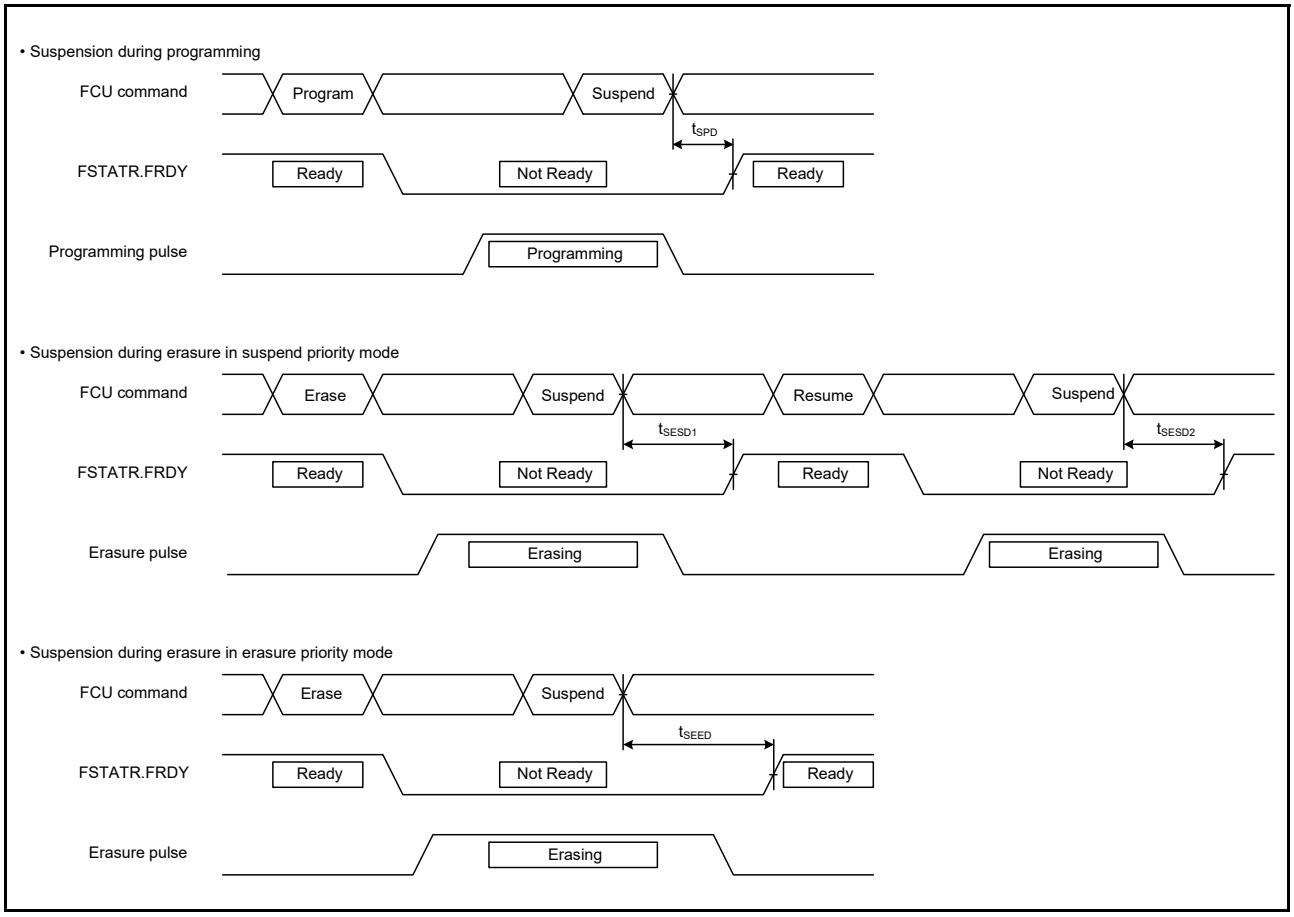



**Figure 5.86 Flash Memory Programming/Erasure Suspension Timing**

## 5.12 Boundary Scan

**Table 5.58 Boundary Scan Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 100 | — | — | ns | Figure 5.87 |
| TCK clock high pulse width | $t_{TCKH}$ | 45 | — | — | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 45 | — | — | ns | |
| TCK clock rise time | $t_{TCKr}$ | — | — | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | — | — | 5 | ns | |
| TRST# pulse width | $t_{TRSTW}$ | 20 | — | — | $t_{TCKcyc}$ | Figure 5.88 |
| TMS setup time | $t_{TMSS}$ | 20 | — | — | ns | Figure 5.89 |
| TMS hold time | $t_{TMSH}$ | 20 | — | — | ns | |
| TDI setup time | $t_{TDIS}$ | 20 | — | — | ns | |
| TDI hold time | $t_{TDIH}$ | 20 | — | — | ns | |
| TDO data delay time | $t_{TDOD}$ | — | — | 40 | ns | |

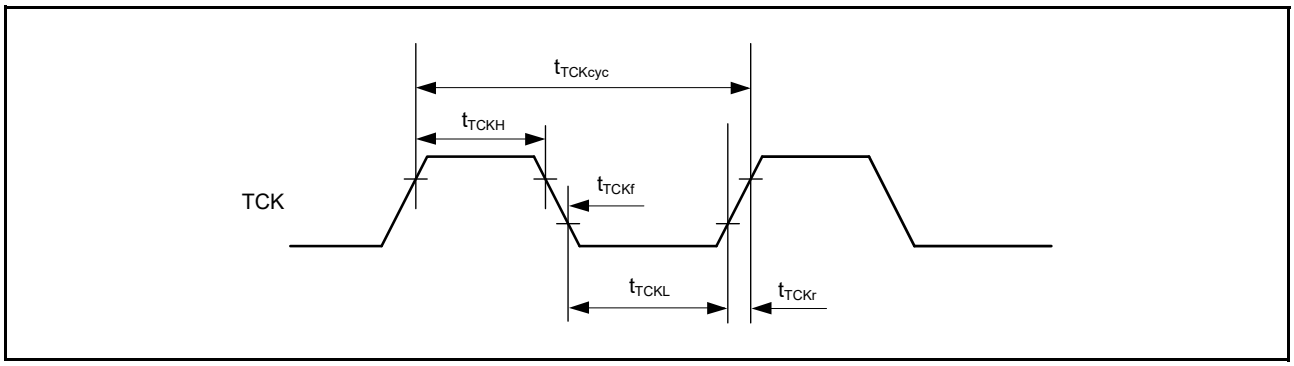



**Figure 5.87 Boundary Scan TCK Timing**

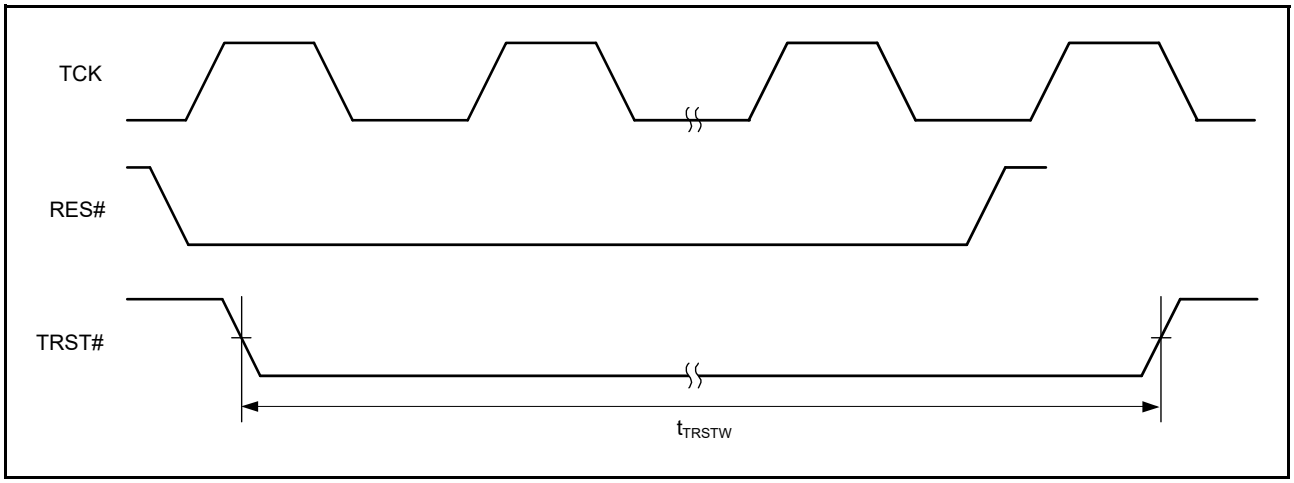



**Figure 5.88 Boundary Scan TRST# Timing**

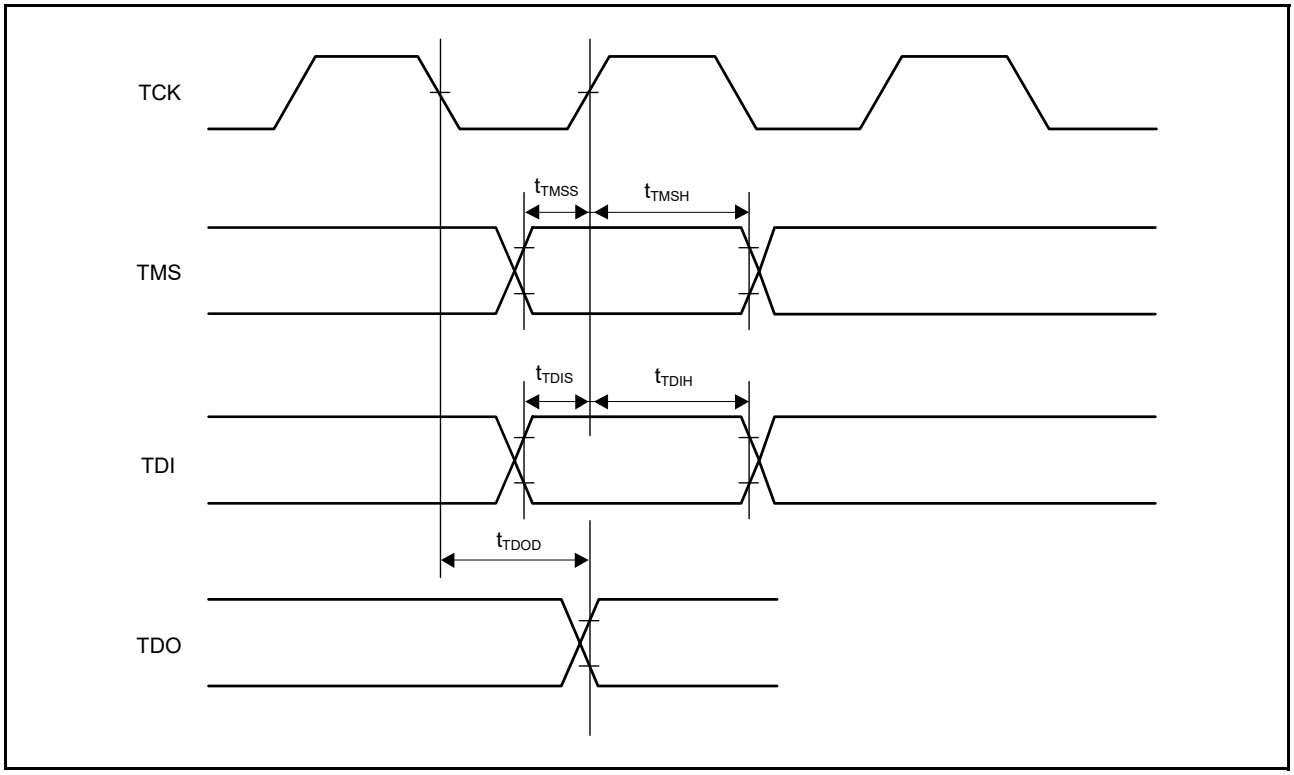
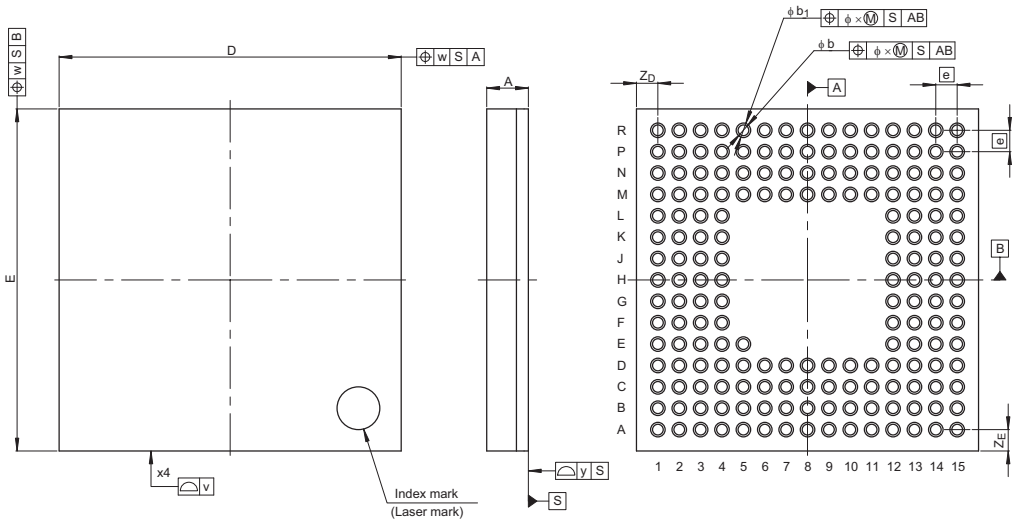



**Figure 5.89 Boundary Scan Input/Output Timing**

# Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

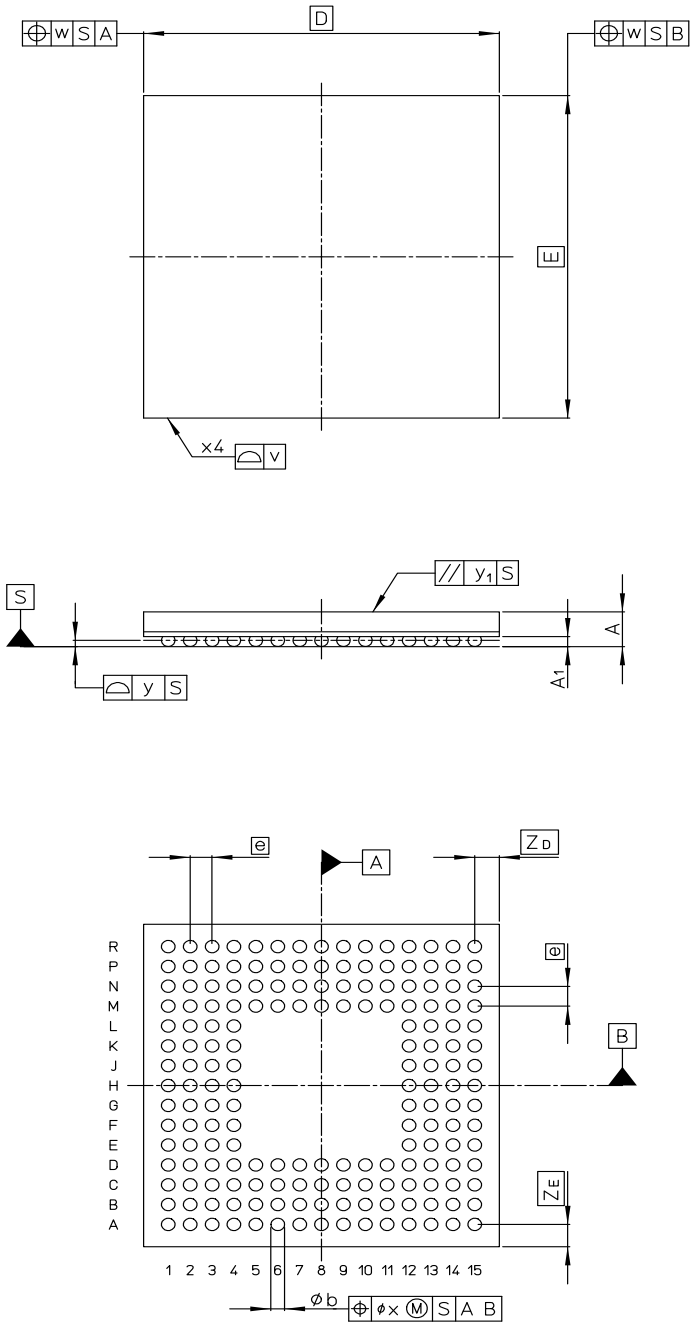
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA177-8x8-0.50 | PTLG0177KA-A | 177F0E-A | 0.2g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 8.0 | — |
| E | — | 8.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.5 | — |
| b | 0.21 | 0.25 | 0.29 |
| $b_1$ | 0.29 | 0.34 | 0.39 |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 0.5 | — |
| $Z_E$ | — | 0.5 | — |

Figure A 177-Pin TFLGA (PTLG0177KA-A)

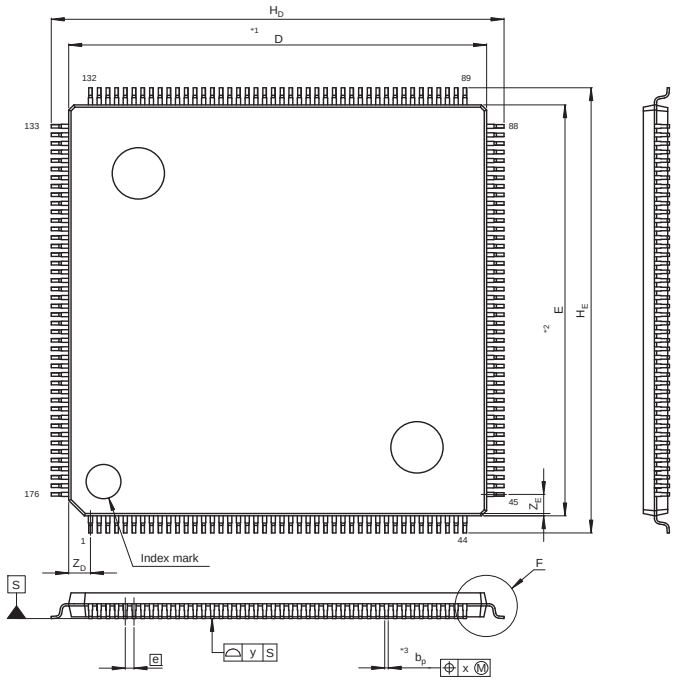
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFBGA176-13x13-0.80 | PLBG0176GA-A | BP-176/BP-176V | 0.45g |

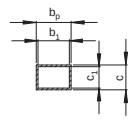



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 13.0 | — |
| E | — | 13.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.40 |
| $A_1$ | 0.35 | 0.40 | 0.45 |
| e | — | 0.80 | — |
| b | 0.45 | 0.50 | 0.55 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $y_1$ | — | — | 0.2 |
| $S_D$ | — | — | — |
| $S_E$ | — | — | — |
| $Z_D$ | — | 0.90 | — |
| $Z_E$ | — | 0.90 | — |

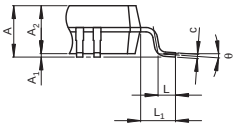
Figure B 176-Pin LFBGA (PLBG0176GA-A)

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP176-24x24-0.50 | PLQP0176KB-A | 176P6Q-A/FP-176E/FP-176EV | 1.8g |




Terminal cross section



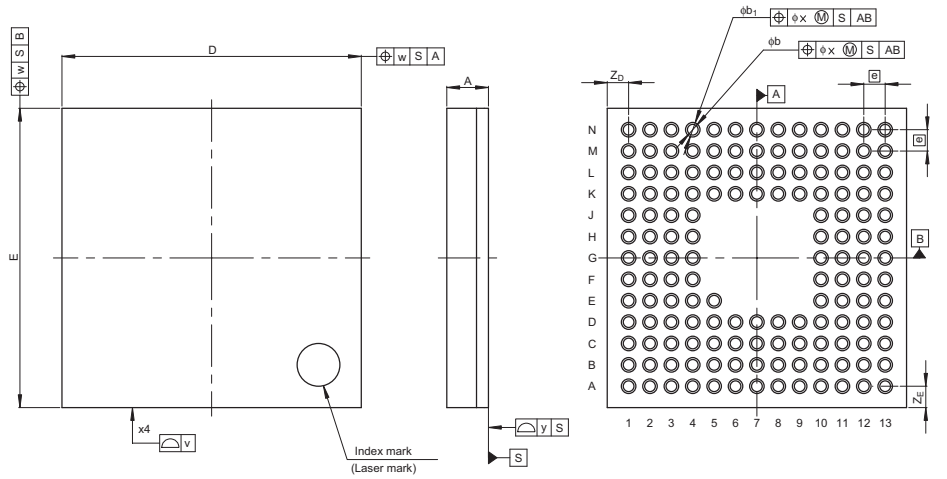

Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 23.9 | 24.0 | 24.1 |
| E | 23.9 | 24.0 | 24.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 25.8 | 26.0 | 26.2 |
| $H_E$ | 25.8 | 26.0 | 26.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure C 176-Pin LFQFP (PLQP0176KB-A)

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA145-7x7-0.50 | PTLG0145KA-A | 145F0G | 0.1g |

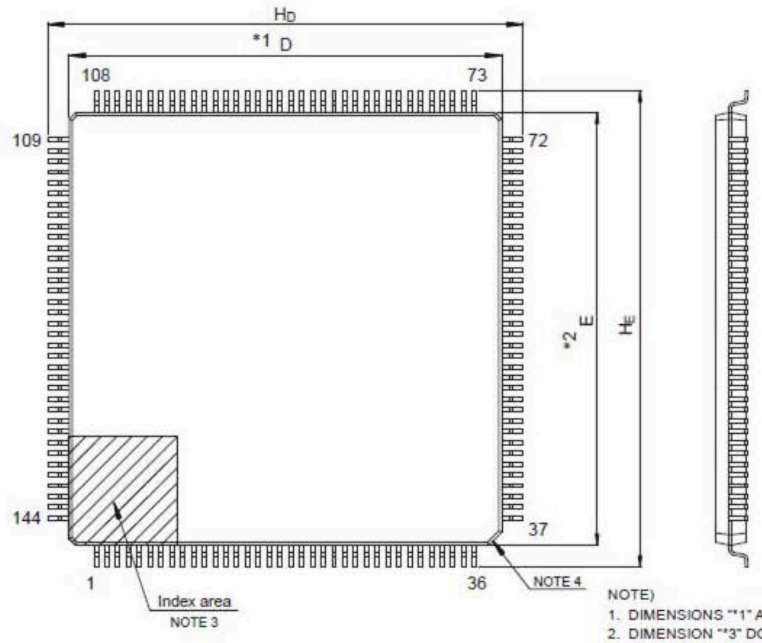


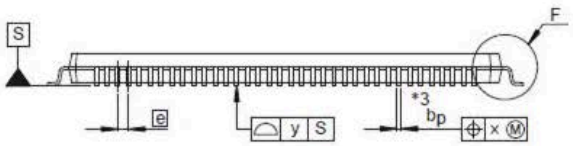

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.5 | — |
| b | 0.21 | 0.25 | 0.29 |
| $b_1$ | 0.29 | 0.34 | 0.39 |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 0.5 | — |
| $Z_E$ | — | 0.5 | — |

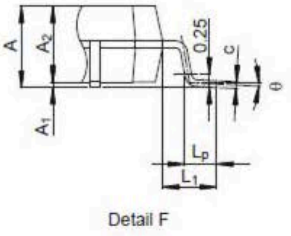
Figure D 145-Pin TFLGA (PTLG0145KA-A)

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP144-20x20-0.50 | PLQP0144KA-B | — | 1.2 |

Unit: mm



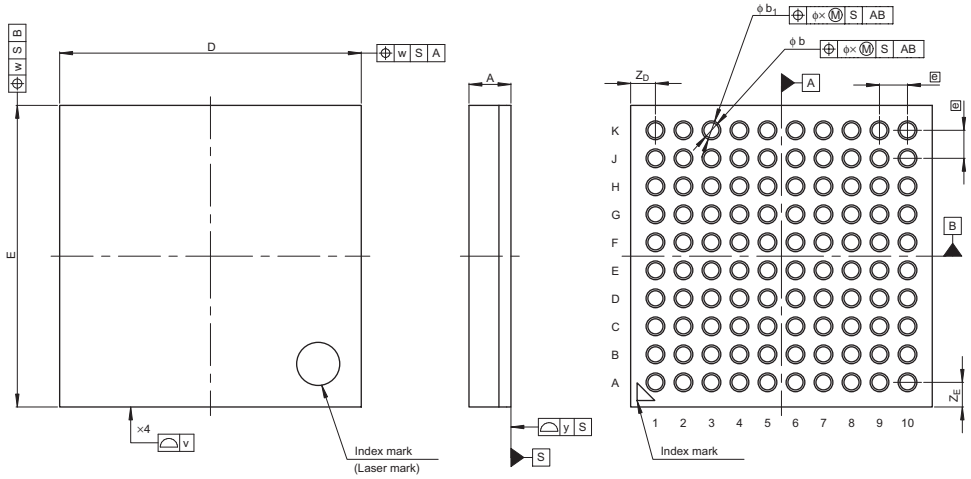

Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 21.8 | 22.0 | 22.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

Figure E 144-Pin LFQFP (PLQP0144KA-B)

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA100-7x7-0.65 | PTLG0100JA-A | 100F0G | 0.1g |

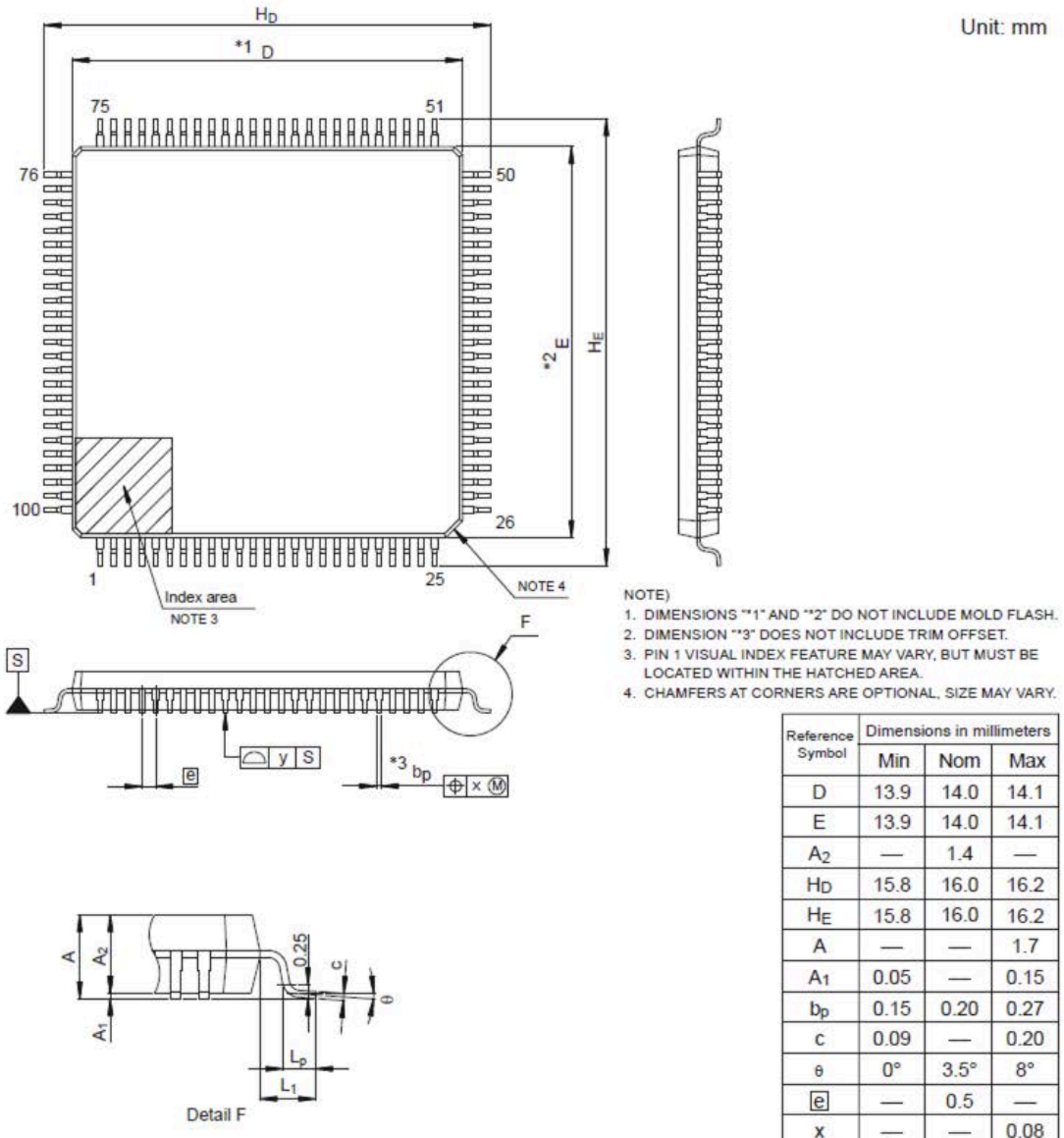



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.385 | 0.435 | 0.485 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.575 | — |

Figure F 100-Pin TFLGA (PTLG0100JA-A)

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |

Unit: mm

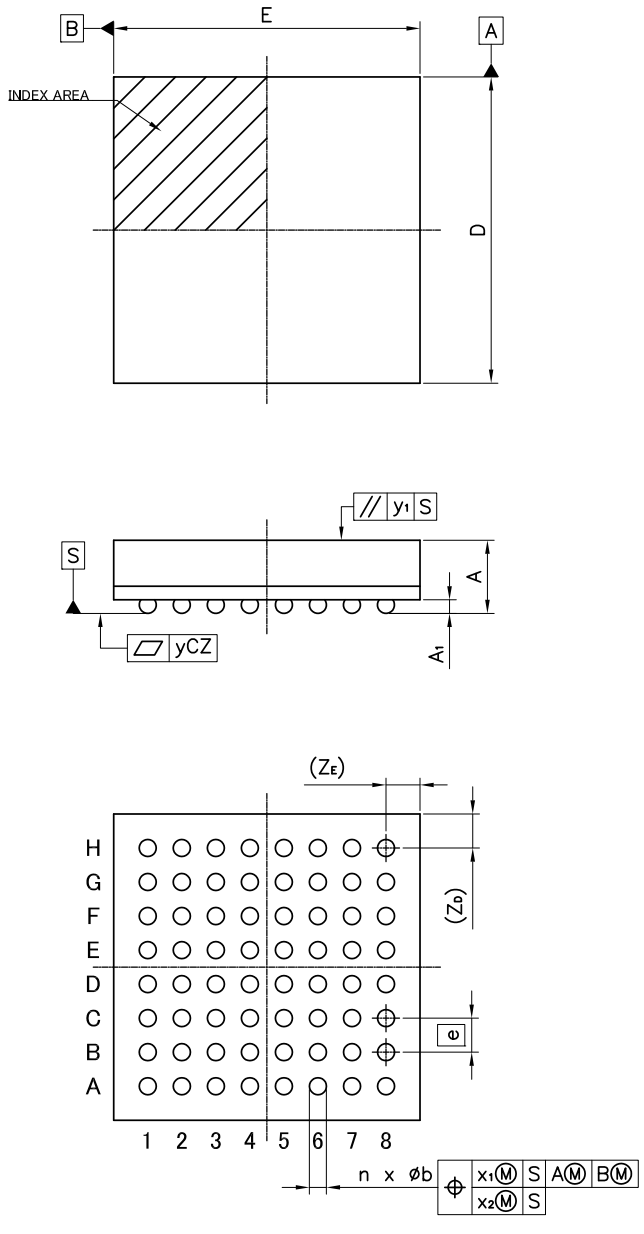



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

Figure G 100-Pin LFQFP (PLQP0100KB-B)

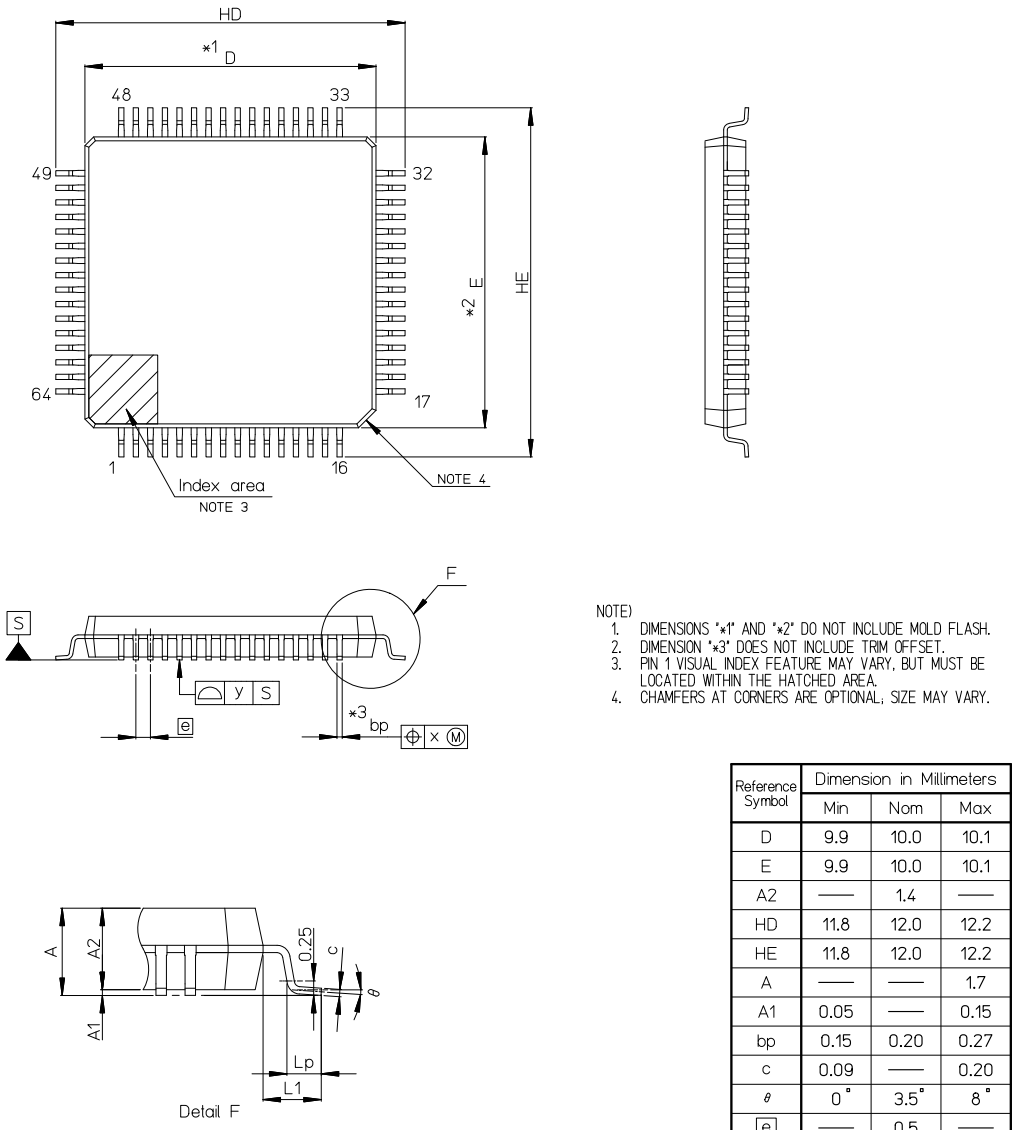
| JEITA Package Code | RENESAS Code | MASS(Typ.)[g] |
|---|---|---|
| P-TFBGA64-4.5×4.5-0.50 | PTBG0064KB-A | 0.04 |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| D | 4.42 | 4.50 | 4.58 |
| E | 4.42 | 4.50 | 4.58 |
| A | — | — | 1.20 |
| $A_1$ | 0.15 | 0.20 | 0.25 |
| e | — | 0.50 | — |
| b | 0.20 | 0.25 | 0.30 |
| $x_1$ | — | — | 0.15 |
| $x_2$ | — | — | 0.05 |
| y | — | — | 0.08 |
| $y_1$ | — | — | 0.20 |
| n | — | 64 | — |
| $Z_D$ | — | 0.50 | — |
| $Z_E$ | — | 0.50 | — |

Figure H 64-Pin TFBGA (PTBG0064KB-A)

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | —— | 0.3g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| A2 | —— | 1.4 | —— |
| HD | 11.8 | 12.0 | 12.2 |
| HE | 11.8 | 12.0 | 12.2 |
| A | —— | —— | 1.7 |
| A1 | 0.05 | —— | 0.15 |
| bp | 0.15 | 0.20 | 0.27 |
| c | 0.09 | —— | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | —— | 0.5 | —— |
| x | —— | —— | 0.08 |
| y | —— | —— | 0.08 |
| Lp | 0.45 | 0.6 | 0.75 |
| L1 | —— | 1.0 | —— |

Figure I 64-Pin LFQFP (PLQP0064KB-C)

| REVISION HISTORY | RX65N Group, RX651 Group Datasheet |
|---|---|

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|---|---|---|---|---|
| | | Page | Summary | |
| 1.00 | Aug 24, 2016 | — | First edition, issued | |
| 2.10 | Oct 02, 2017 | — | Products with at least 1.5 Mbytes of code flash memory added<br>The conventional products indicated as “products with 1 Mbyte of code flash memory or less” | |
| | | 1. Overview | | |
| | | 6, 9 | Table 1.1 Outline of Specifications (5/9), Note added | TN-RX*-A164B/E |
| | | 8 | Table 1.1 Outline of Specifications (8/9)<br>Description of the 12-bit D/A converter (R12DA) changed | TN-RX*-A165A/E |
| | | 4. I/O Registers | | |
| | | 131 | Table 4.1 List of I/O Registers (Address Order) (46 / 61), changed | TN-RX*-A176A/E |
| | | 5. Electrical Characteristics | | |
| | | 147 | Table 5.1 Absolute Maximum Rating, changed | |
| | | 150 | Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less), changed | TN-RX*-A164B/E |
| | | 152 | Table 5.7 DC Characteristics (4), changed | TN-RX*-A164B/E<br>TN-RX*-A176A/E |
| | | 153 | Table 5.9 Heat Resistance Value (Reference), added | |
| | | 162 | Table 5.21 Timing of Recovery from Low Power Consumption Modes (1), changed | TN-RX*-A176A/E |
| | | 189 | Table 5.35 RSPI Timing, changed | |
| | | 212 | Table 5.49 D/A Conversion Characteristics, changed | TN-RX*-A165A/E |
| | | 218 | Table 5.54 Code Flash Memory Characteristics, changed | |
| | | 219 | Table 5.55 Data Flash Memory Characteristics, changed | |
| 2.30 | Jun 20, 2019 | — | 64-pin Package Products added<br>Terms unified:<br>pull-up MOS → pull-up resistors<br>pull-down MOS → pull-down resistors | |
| | | 1. Overview | | |
| | | 14 to 22 | Table 1.3 List of Products, changed | TN-RX*-A204A/E |
| | | 30 | Table 1.4 Pin Functions (6/8), changed | TN-RX*-A0211A/E |
| | | 47 to 49 | Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA), changed | TN-RX*-A182A/E |
| | | 52 | Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP), changed | |
| | | 4. I/O Registers | | |
| | | 136 to 138 | Table 4.1 List of I/O Registers (Address Order), changed | TN-RX*-A0211A/E |
| | | 5. Electrical Characteristics | | |
| | | 157 | Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less), changed | TN-RX*-A0211A/E |
| | | 158, 159 | Table 5.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory), changed | |
| | | 159 | Table 5.7 DC Characteristics (4), changed | |
| | | 161 | Table 5.9 Thermal Resistance Value (Reference), changed | TN-RX*-A182A/E |
| | | 164 | Table 5.13 Reset Timing, Unit changed | TN-RX*-A202A/E |
| | | 206 | Figure 5.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing, changed | |
| | | 216 | Table 5.44 SDHI Timing, added<br>Figure 5.72 SD Host Interface Input/Output Signal Timing, added | TN-RX*-A196A/E |
| | | 217, 218 | Table 5.45 SDSI Timing, added<br>Figure 5.73 SD Slave Interface Input Signal Timing to<br>Figure 5.75 SD Slave Interface Output Signal Timing (High Speed Mode), added | |
| | | 221 | Table 5.48 12-Bit A/D (Unit 0) Conversion Characteristics, changed | TN-RX*-A182A/E |

| Rev. | Date | Description | | Classification |
|---|---|---|---|---|
| | | Page | Summary | |
| 2.30 | Jun 20, 2019 | 230 | Table 5.57 Data Flash Memory Characteristics, changed (64-bytes and 2-Kbytes blank check time added) | |

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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