ISL78424, ISL78434, ISL78444

100V Boot, 4A Peak, Half-Bridge Driver with Single PWM Input and Adaptive Dead Time Control

FN9357
Rev.0.00
Sep 10, 2018

The ISL78424, ISL78434, and ISL78444 are Automotive Grade (AEC-Q100 Grade 1) high voltage, high frequency, half-bridge NMOS FET drivers for driving the gates of up to 70V half-bridge topologies.

The family of half-bridge drivers feature 3A sourcing, 4A sinking peak gate drive current. The ISL78424 and ISL78444 feature a single tri-level PWM input for controlling both gate drivers. The ISL78434 has dual independent inputs for controlling the high-side and low-side driver separately. The ISL78424 and ISL78434 have independent sourcing and sinking pins for each gate driver while ISL78444 has a single combined sourcing/sinking output for each gate driver.

Strong gate drive strength and the Adaptive Dead Time (ADT) feature allow this family of drivers to switch high voltage, low $r_{DS(ON)}$ power FETs in half-bridge topologies at high operating frequencies while providing shoot-through protection and minimizing dead time switching losses.

The ISL78424, ISL78434, and ISL78444 are offered in a 14 Ld HTSSOP package that complies with 100V conductor spacing per IPC-2221B. The ISL78444 is pin compatible with the ISL78420. All devices are specified across a wide ambient temperature range of -40°C to +140°C.

Related Literature

For a full list of related documents, visit our website:

- ISL78424, ISL78434, ISL78444 product pages

Features

- Patented gate-sensed adaptive dead time control provides shoot-through protection and mimized dead time
- Unique tri-level PWM input for integration with Renesas multiphase controllers (for example, ISL78225 and ISL78226)
- 3A sourcing and 4A sinking output current
- On-chip 3Ω bootsrap FET switch
- Programmable dead time delay with single resistor
- Tri-level PWM input (ISL78424, ISL78444)
- Independent HI/LI inputs (ISL78434)
- Separate source/sink pins at driver outputs (ISL78424, ISL78434)
- Bootstrap and VDD Undervoltage Lockout (UVLO)
- Wide supply range: 8V to 18V
- Bootstrap supply maximum voltage: 100V
- Maximum phase voltage: 86V
- Minimum phase voltage: -10V

Applications

- Automotive half-bridge and 3-phase motor driver
- 12V to 24V and 12V to 48V bidirectional DC/DC (with ISL78226, ISL78224 controllers)
- Multi-phase boost (with ISL78220 and ISL78225 controllers)

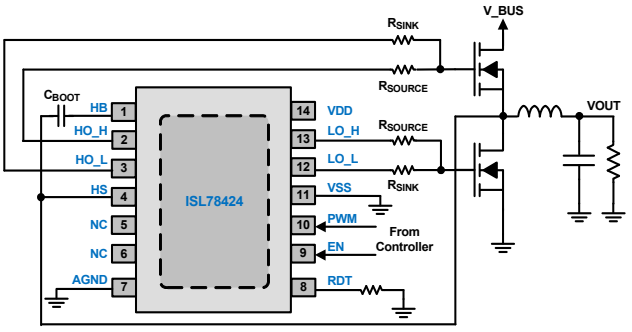


Figure 1. Independent Source and Sink Outputs for Optimizing Gate Drive Current and Adaptive Dead Time Sensing

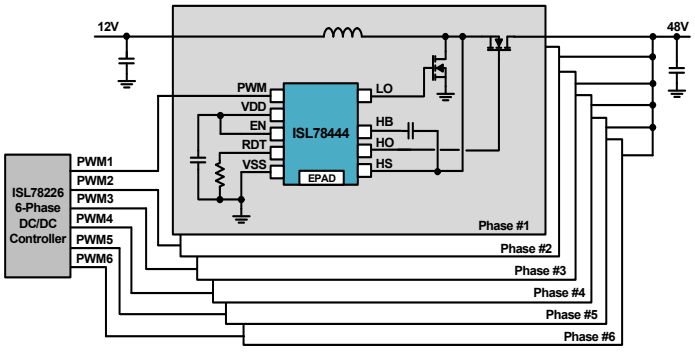


Figure 2. NMOS Half-Bridge Driver for 12V-48V Bi-Directional DC/DC Controller

Contents

1. Overview

1.1 Block Diagrams

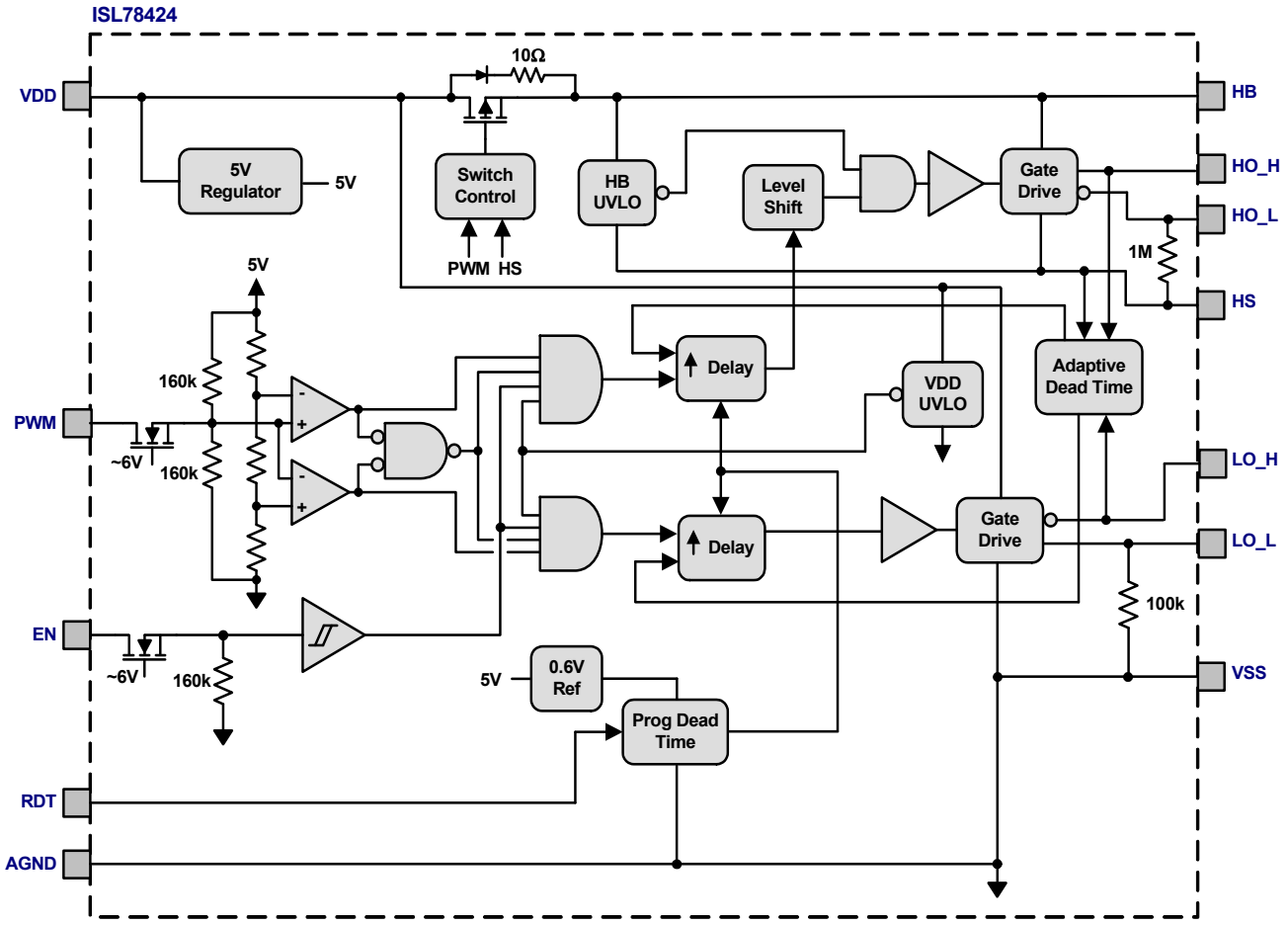


Figure 3. ISL78424 Block Diagram

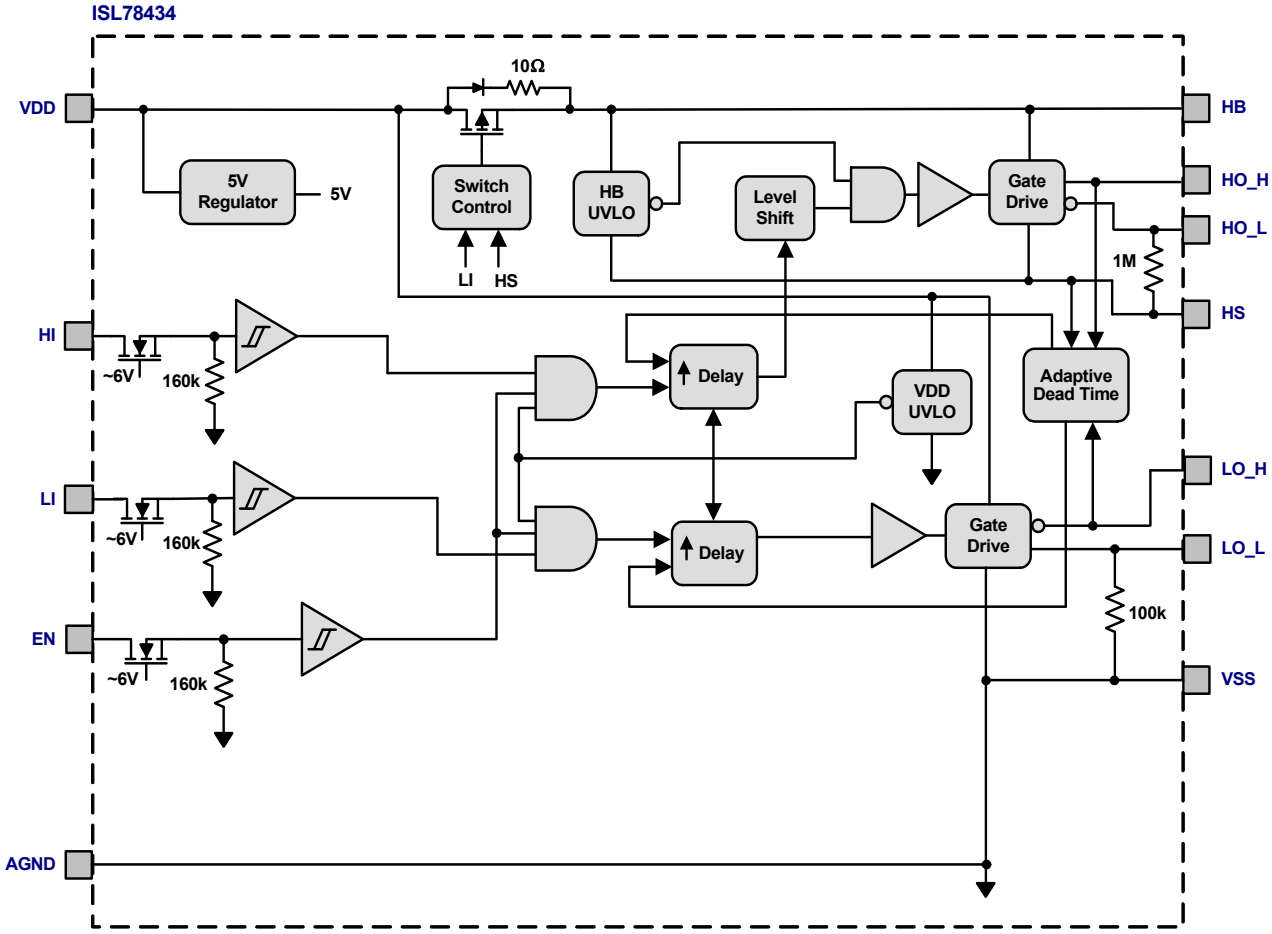


Figure 4. ISL78434 Block Diagram

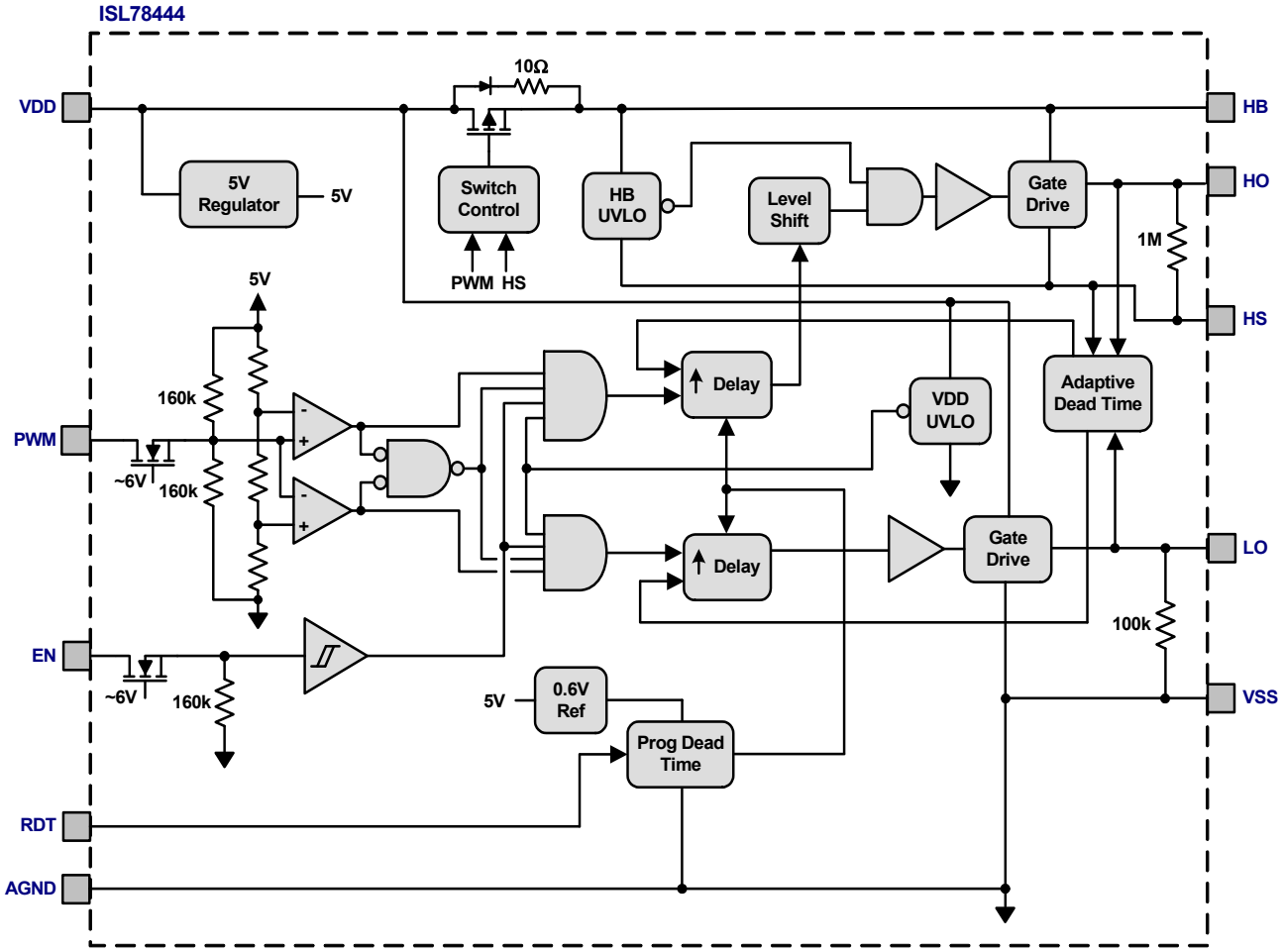


Figure 5. ISL78444 Block Diagram

1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL78424AVEZ	78424 AVEZ	-40 to +125	-	14 Ld HTSSOP	M14.173B
ISL78424AVEZ-T	78424 AVEZ	-40 to +125	2.5k	14 Ld HTSSOP	M14.173B
ISL78424AVEZ-T7A	78424 AVEZ	-40 to +125	250	14 Ld HTSSOP	M14.173B
ISL78434AVEZ	78434 AVEZ	-40 to +125	-	14 Ld HTSSOP	M14.173B
ISL78434AVEZ-T	78434 AVEZ	-40 to +125	2.5k	14 Ld HTSSOP	M14.173B
ISL78434AVEZ-T7A	78434 AVEZ	-40 to +125	250	14 Ld HTSSOP	M14.173B
ISL78444AVEZ	78444 AVEZ	-40 to +125	-	14 Ld HTSSOP	M14.173B
ISL78444AVEZ-T	78444 AVEZ	-40 to +125	2.5k	14 Ld HTSSOP	M14.173B
ISL78444AVEZ-T7A	78444 AVEZ	-40 to +125	250	14 Ld HTSSOP	M14.173B

Notes:

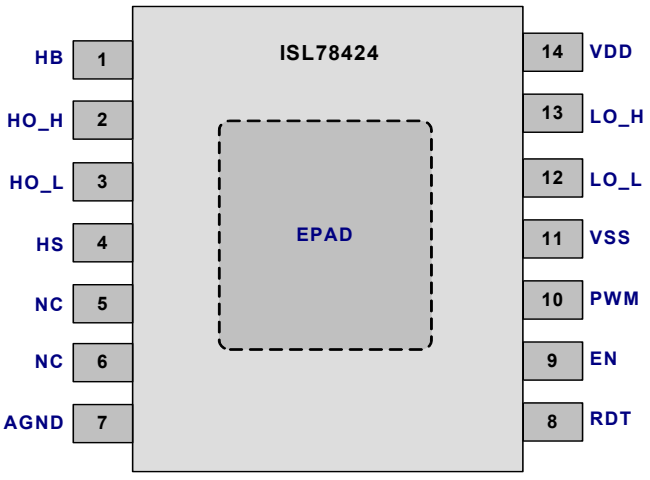
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL78424, ISL78434, and ISL78444 product information pages. For more information about MSL, refer to TB363.
4. These packages are in compliance with 100V conductor spacing guidelines per IPC-2221.

Table 1. Key Differences Between Family of Parts

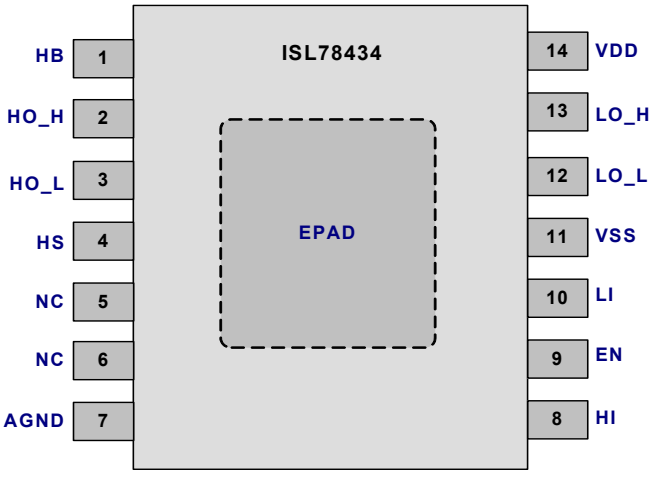
Part Number	Input	Driver Output Pins	Adaptive Dead Time Control
ISL78424	PWM	HO_H: High-Side Source HO_L: High-side Sink LO_H: Low-Side Source LO_L: Low-Side Sink	Yes
ISL78434	HI/LI		Yes
ISL78444	PWM	HO: High-Side Source and Sink LO: Low-Side Source and Sink	Yes

1.3 Pin Configurations

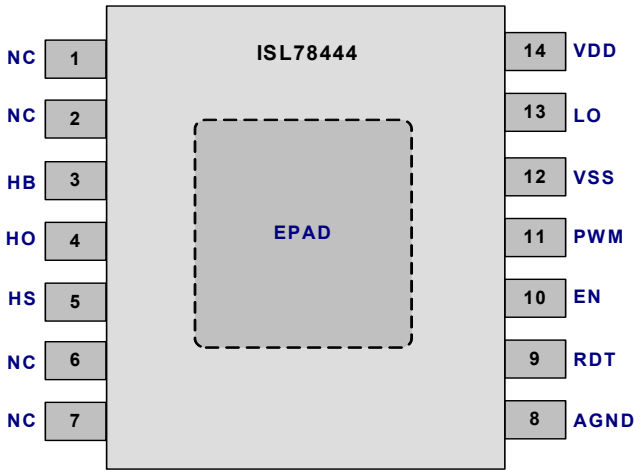
ISL78424 (14 Ld HTSSOP)
Top View



ISL78434 (14 Ld HTSSOP)
Top View



ISL78444 (14 Ld HTSSOP)
Top View



1.4 Pin Descriptions

ISL78424	ISL78434	ISL78444	Symbol	Description
1	1	3	HB	High-side bootstrap supply voltage referenced to HS. Connect boot cap from HB to HS.
-	-	4	HO	High-side driver output. Connect to gate of high-side NFET.
2	2	-	HO_H	High-side driver source output. Connect to gate of high-side NFET. This pin is also the sense input for high-side adaptive dead time control.
3	3	-	HO_L	High-side driver sink output. Connect to gate of high-side NFET.
4	4	5	HS	High-side driver reference. Connect to source of high-side NFET.
7	7	8	AGND	Analog ground pin. Connect to VSS through EPAD.
-	8	-	HI	High-side gate driver logic input. 3V and 5V logic compatible.
8	-	9	RDT	Adjustable dead time delay pin. Connect a resistor to ground to increase the dead time delay in addition to the adaptive dead time control. See "Adjustable Dead Time Delay (RDT Pin)" on page 25 for more information.
9	9	10	EN	Driver enable. When high, the driver outputs respond to input logic control. When low, the low-side driver sink output is active and the high-side driver sink output has a 1MΩ impedance to HS to keep the half bridge NFETs off.
-	10	-	LI	Low-side gate driver logic input. 3V and 5V logic compatible.
10	-	11	PWM	Tri-Level PWM input for controlling the driver outputs.
11	11	12	VSS	Low-side driver reference. Connect to AGND through EPAD. Connect to source of low-side NFET.
-	-	13	LO	Low-side driver output. Connect to gate of low-side NFET.
12	12	-	LO_L	Low-side driver sink output. Connect to gate of low-side NFET.
13	13	-	LO_H	Low-side driver source output. Connect to gate of low-side NFET. This pin is also the sense input for the low-side adaptive dead time control.
14	14	14	VDD	Supply voltage for internal bias circuitry and low-side driver source output.
5, 6	5, 6	1, 2, 6, 7	NC	No connect. This pin is not internally connected.
EPAD				Bottom side thermal pad is not electrically connected internally. Connect VSS and AGND pins together with EPAD on PCB. Connect EPAD PCB to ground plane with as many vias as possible for optimum thermal performance. See "PCB Layout Guidelines" on page 31 for more information.

2. Specifications

2.1 Absolute Maximum Ratings

All voltages referenced to V_{SS} unless otherwise specified.

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}, HB-HS	-0.3	20	V
PWM, HI, LI and EN Voltage	-0.3	V_{DD} + 0.3	V
RDT Voltage	-0.3	5	V
Voltage on LO	-0.3	V_{DD} + 0.3	V
Voltage on HO (Referenced to HS)	V_{HS} - 0.3	V_{HB} + 0.3	V
Voltage on HB		100	V
Voltage on HS	-1	86	V
Average Current in VDD to HB FET		100	mA
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per AEC-Q100-002)	2.5		kV
Charged Device Model (Tested per AEC-Q100-011)	1		kV
Latch-Up (Tested per AEC-A100-004)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld HTSSOP Package (Notes 5, 6)	35	2.5

Notes:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Power Dissipation at +25°C in Free Air		3.5	W
Storage Temperature Range	-65	+150	°C
Junction Temperature Range	-55	+150	°C
Pb-Free Reflow Profile	Refer to TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}	8	18	V
Voltage on HS	-0.7	70	V
Voltage on HS (Negative repetitive transient <100ns)		-10	V
Voltage on HB (Referenced to HS)	8	18	V
Voltage on HB (Referenced to VSS)		86	V
HS Slew Rate		<50	V/ns
Junction Temperature	-40	+140	°C

2.4 Electrical Specifications

Unless otherwise specified: V_{DD} = 12V, V_{SS} = AGND = HS = 0V, HB = HS+VDD, EN = 5V, PWM = 2.5V, HI = LI = 0V, 10kΩ resistor on RDT pin to AGND. No load on LO or HO. Typical parameters for T_J = +25°C. **Boldface limits apply across the ambient operating temperature range, -40°C to +140°C.**

Parameters	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Supply Currents						
V_{DD} Quiescent Current	I_{DD1}	R_{DT} = 0Ω to AGND	-	500	**800**	µA
	I_{DD2}	R_{DT} = 10kΩ to AGND, ISL78424 and ISL78444 only	-	650	**830**	µA
V_{DD} Operating Current	I_{DDO1}	PWM 0V to 5V HI and LI 0V to 5V f_{PWM} = 500kHz, 50% duty cycle R_{DT} = 0Ω to AGND; V_{HS} = 5V	-	6.6	**11.8**	mA
	I_{DDO2}	PWM 0V to 5V ISL78424 and ISL78444 only f_{PWM} = 500kHz, 50% duty cycle R_{DT} = 10kΩ to AGND; V_{HS} = 5V	-	6.8	**11.9**	mA
V_{DD} Disabled Current	I_{DDSD}	EN = 0V	-	170	**360**	µA
HB to HS Quiescent Current	I_{HBQ}	PWM = 12V; HI = 12V	-	250	**320**	µA
HB to HS Operating Current	I_{HBO}	f_{PWM} = 500kHz, 50% duty cycle PWM = 2.5V to 5V HI 0V to 5V; V_{HS} = 5V	-	5.4	**10**	mA
HB to V_{SS} Leakage Current	$I_{HBSLeak}$	V_{HB} = V_{HS} = 70V	-	50	**80**	µA
HB to V_{SS} Bias Current	$I_{HBSBias}$	$I_{HBSBias}$ = I_{HB} - I_{HS} V_{DD} = 16V; V_{HB} = 86V; V_{HS} = 70V; PWM = 5V; HI = 5V	-	125	**150**	µA
Tri-Level PWM Input						
High Level Rising Threshold	V_{PWMH}		-	3.5	**3.8**	V
Middle Level Range	V_{MIDH}	Middle level upper limit	**3.0**	3.3	-	V
	V_{MIDL}	Middle level lower limit	-	1.5	**1.65**	V
Middle Level Hysteresis			-	200	-	mV
Low Level Falling Threshold	V_{PWML}		**0.8**	1.2	-	V
Logic High and Low Input Current	I_{PWM_IH}	V_{PWM} = 5V; Sourcing	**20**	30	**45**	µA
	I_{PWM_IL}	V_{PWM} = 0V; Sinking	**10**	24	**35**	µA
Open Circuit Voltage	V_{float}	No load on PWM pin	**2.35**	2.5	**2.55**	V
PWM Middle Level Resistors	R_{mid}	Pull-up resistor to internal reference and pull-down resistor to AGND	-	165	-	kΩ
HI/LI Input						
High Level Threshold	V_{IH}		-	1.7	**2.1**	V
Low Level Threshold	V_{IL}		**1.0**	1.3	-	V
Input Hysteresis			-	400	-	mV
HI/LI Pin Pull-Down Resistance	R_{HI_LI}	HI = LI = 5V	**100**	175	**320**	kΩ
EN Input						
High Level Threshold	V_{ENH}		-	1.7	**2.1**	V
Low Level Threshold	V_{ENL}		**1.0**	1.3	-	V
EN Input Hysteresis			-	400	-	mV

Unless otherwise specified: V_{DD} = 12V, V_{SS} = AGND = HS = 0V, HB = HS+VDD, EN = 5V, PWM = 2.5V, HI = LI = 0V, 10kΩ resistor on RDT pin to AGND. No load on LO or HO. Typical parameters for T_J = +25°C. **Boldface limits apply across the ambient operating temperature range, -40°C to +140°C. (Continued)**

Parameters	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
EN Pin Pull-Down Resistor	R_{EN}	EN = 5V	**100**	175	**260**	kΩ
Enable High Delay	$t_{EN\_H\_LO}$	From V_{ENH} to transition at LO; PWM = 0V, ISL78424 and ISL78444; LI = 5V, HI = 0V, for ISL78434	-	3	**5.275**	µs
	$t_{EN\_H\_HO}$	From V_{ENH} to transition at HO; PWM = 5V, ISL78424 and ISL78444; LI = 0V, HI = 5V, for ISL78434	-	3		µs
Enable Low Delay	$t_{EN\_L\_HO}$	From V_{ENL} to transition at HO; PWM = 5V, ISL78424 and ISL78444; LI = 0V, HI = 5V, for ISL78434	-	0.8		µs
	$t_{EN\_L\_LO}$	From V_{ENL} to transition at LO; PWM = 0V, ISL78424 and ISL78444; LI = 5V, HI = 0V, for ISL78434	-	0.8	**1.7**	µs
V_{DD} Start-Up Delay	t_{VDD}	EN = V_{DD}; ISL78424, ISL78444 PWM = 0V; ISL78434 HI = 0V, LI = V_{DD}; V_{DD} crossing V_{DDR} to LO rising	-	20	-	µs
Undervoltage Protection						
V_{DD} Rising Threshold	V_{DDR}		**6.8**	7.2	**7.7**	V
V_{DD} UVLO Hysteresis	V_{DDH}		-	0.7	-	V
HB Rising Threshold	V_{HBR}		**6**	7	**7.8**	V
HB UVLO Hysteresis	V_{HBH}		-	0.5	-	V
Bootstrap FET Switch						
Low Current Forward Voltage	V_{DL}	I_{VDD-HB} = 100µA	-	1	-	mV
High Current Forward Voltage	V_{DH}	I_{VDD-HB} = 100mA	-	0.3	**1**	V
VDD to HB Resistance	R_{BOOT}	I_{BOOT} out of HB pin = 100mA	**1**	3	**6**	Ω
LO Gate Driver						
Output Low Voltage	V_{LOL}	I_{LO} = 100mA sink	-	100	**225**	mV
Output High Voltage	V_{LOH}	I_{LO} = 100mA source; Voltage below V_{DD} rail: $V_{OHL} = V_{DD} - V_{LO}$	-	170	**325**	mV
Peak Pull-Up Current	I_{LOH}	V_{LO} = 0V; T = +25°C	-	4	-	A
		V_{LO} = 0V; T = +85°C	-	3.75	-	A
		V_{LO} = 0V; T = +140°C	-	3.5	-	A
Peak Pull-Down Current	I_{LOL}	V_{LO} = 12V; T = +25°C	-	4.5	-	A
		V_{LO} = 12V; T = +85°C	-	4	-	A
		V_{LO} = 12V; T = +140°C	-	3.5	-	A
HO Gate Driver						
Output Low Voltage	V_{HOH}	I_{HO} = 100mA sink	-	100	**225**	mV
Output High Voltage	V_{HOL}	I_{HO} = 100mA source Voltage below V_{HB} rail: $V_{OHH} = V_{HB} - V_{HO}$	-	170	**325**	mV

Unless otherwise specified: V_{DD} = 12V, V_{SS} = AGND = HS = 0V, HB = HS+VDD, EN = 5V, PWM = 2.5V, HI = LI = 0V, 10kΩ resistor on RDT pin to AGND. No load on LO or HO. Typical parameters for T_J = +25°C. **Boldface limits apply across the ambient operating temperature range, -40°C to +140°C. (Continued)**

Parameters	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Peak Pull-Up Current	I_{HOH}	V_{LO} = 0V; T = +25°C	-	3.75	-	A
		V_{LO} = 0V; T = +85°C	-	3.5	-	A
		V_{LO} = 0V; T = +140°C	-	3.25	-	A
Peak Pull-Down Current	I_{HOL}	V_{LO} = 12V; T = +25°C	-	4.5	-	A
		V_{LO} = 12V; T = +85°C	-	4	-	A
		V_{LO} = 12V; T = +140°C	-	3.5	-	A
Adaptive Dead Time Control Threshold Voltage						
LO or LO_H Threshold Voltage Relative to V_{SS}	V_{ADTC_LO}	Falling edge on LO	-	1.3	-	V
HO or HO_H Threshold Voltage Relative to HS (Gate Sense Threshold)	V_{ADTC_HO}	Falling edge on HO	-	1.0	-	V
HS Threshold Voltage Relative to V_{SS} (Phase Sense Threshold)	V_{ADTC_HS}	Falling edge on HS; HO-HS > V_{ADTC_HO}	-	0.5	-	V

2.5 Switching Specifications

Unless otherwise specified: V_{DD} = 12V, V_{SS} = AGND = HS = 0V, HB = HS+VDD, PWM = 0V to 5V or HI/LI = 0V to 5V switching. No load on LO or HO. Typical parameters for T_J = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +140°C.**

Parameters	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
HO Turn-Off Propagation Delay	t_{PDHO}	PWM falling to HO falling	**29**	45	**75**	ns
LO Turn-Off Propagation Delay	t_{PDLO}	PWM rising to LO falling	**35**	45	**66**	ns
PWM Propagation Delay Matching		t_{PDHO} - t_{PDLO}	**-10**	0	**10**	ns
HO Turn-Off Propagation Delay	t_{PDHO1}	PWM entering mid-level state to HO falling PWM = 5V to 2.5V R_{DT} = 0Ω to AGND	**45**	55	**75**	ns
HO Turn-On Propagation Delay	t_{PDHO2}	PWM exiting mid-level state to HO rising PWM = 2.5V to 5V; R_{DT} = 0Ω to AGND	**25**	40	**60**	ns
LO Turn-Off Propagation Delay	t_{PDLO1}	PWM entering mid-level state to LO falling PWM = 0V to 2.5V R_{DT} = 0Ω to AGND	**50**	65	**80**	ns
LO Turn-On Propagation Delay	t_{PDLO2}	PWM exiting mid-level state to LO rising PWM = 2.5V to 0V R_{DT} = 0Ω to AGND	**34**	45	**61**	ns
HO Turn-Off Propagation Delay	t_{PDHI1}	HI falling to HO falling LI = 0V	**27**	45	**60**	ns
LO Turn-Off Propagation Delay	t_{PDLI1}	LI Falling to LO Falling HI = 0V	**34**	45	**56**	ns
HI and LI Falling Propagation Delay Matching		t_{PDHI1} - t_{PDLI1}	**-10**	0	**10**	ns
HO Turn-On Propagation Delay	t_{PDHI2}	HI rising to HO rising LI = 0V	**18**	28	**47**	ns
LO Turn-On Propagation Delay	t_{PDLI2}	LI rising to LO rising HI = 0V	**27**	35	**51**	ns
HI and LI Rising Propagation Delay Matching		t_{PDHI2} - t_{PDLI2}	**-15**	-7	**-1**	ns

Unless otherwise specified: V_{DD} = 12V, V_{SS} = AGND = HS = 0V, HB = HS+VDD, PWM = 0V to 5V or HI/LI = 0V to 5V switching. No load on LO or HO. Typical parameters for T_J = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +140°C. (Continued)**

Parameters	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Minimum Dead Time Delay (Note 8) Includes ISL78434	$t_{DTLHmin}$ (LO Sense)	LO falling to HO rising R_{DT} = 0Ω to AGND	**50**	70	**100**	ns
	$t_{DTHLmin}$ (HO Sense)	HO falling to LO rising HS = 5V, R_{DT} = 0Ω to AGND	**60**	85	**130**	ns
	$t_{DTHSmin}$ (HS Sense)	ISL78424 and ISL78434 only HS falling to LO rising HO_H-HS > V_{ADTC_HO} R_{DT} = 0Ω to AGND	**150**	210	**325**	ns
Low Range Resistor Delay (Note 8) (ISL78424 and ISL78444 only)	t_{DTLH_10k} (LO Sense)	LO falling to HO rising R_{DT} = 10kΩ to AGND	**89**	110	**142**	ns
	t_{DTHL_10k} (HO Sense)	HO falling to LO rising HS = 5V R_{DT} = 10kΩ to AGND	**108**	125	**150**	ns
	t_{DTHS_10k} (HS Sense)	ISL78424 only HS falling to LO Rising HO_H-HS > V_{ADTC_HO} R_{DT} = 10kΩ to AGND	**190**	250	**350**	ns
Mid Range Resistor Delay (Note 8) (ISL78424 and ISL78444 only)	t_{DTLH_65k} (LO Sense)	LO falling to HO rising R_{DT} = 100kΩ to AGND	**250**	290	**335**	ns
	t_{DTHL_65k} (HO Sense)	HO falling to LO rising HS = 5V R_{DT} = 100kΩ to AGND	**265**	300	**340**	ns
	t_{DTHS_65k} (HS Sense)	ISL78424 only HS falling to LO rising HO_H-HS > V_{ADTC_HO} R_{DT} = 100kΩ to AGND	**385**	440	**542**	ns
High Range Resistor Delay (Note 8) (ISL78424 and ISL78444 only)	t_{DTLH_100k} (LO Sense)	LO falling to HO rising R_{DT} = 100kΩ to AGND	-	405	-	ns
	t_{DTHL_100k} (HO Sense)	HO falling to LO rising HS = 5V R_{DT} = 100kΩ to AGND	-	430	-	ns
	t_{DTHS_100k} (HS Sense)	ISL78424 only HS falling to LO rising HO_H-HS > V_{ADTC_HO} R_{DT} = 100kΩ to AGND	-	550	-	ns
Dead Time Delay Matching (Note 8) LO Gate Sense to HO Gate Sense Delay Matching	$t_{MATCHmin}$	R_{DT} = 0Ω to AGND ($t_{DTHLmin}$ - $t_{DTLHmin}$)	**-38**	-15	**15**	ns
	t_{MATCH_10k}	R_{DT} = 10kΩ to AGND (t_{DTHL_10k} - t_{DTLH_10k}) ISL78424 and ISL78444 only	**-38**	-12	**13**	ns
	t_{MATCH_65k}	R_{DT} = 65kΩ to AGND (t_{DTHL_65k} - t_{DTLH_65k}) ISL78424 and ISL78444 only	**-38**	-13	**10**	ns
Either Output Rise/Fall Time (10% to 90%/90% to 10%)	t_{RC},t_{FC}	C_L = 1nF	-	10	-	ns
Minimum Input Pulse Width for Output to Respond	t_{min}	ISL78424, ISL78444	-	50	-	ns
		ISL78434	-	50	-	ns

Notes:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
8. Dead Time is defined as the period of time between LO falling and HO rising or between HO falling and LO rising.

2.6 Timing Diagrams

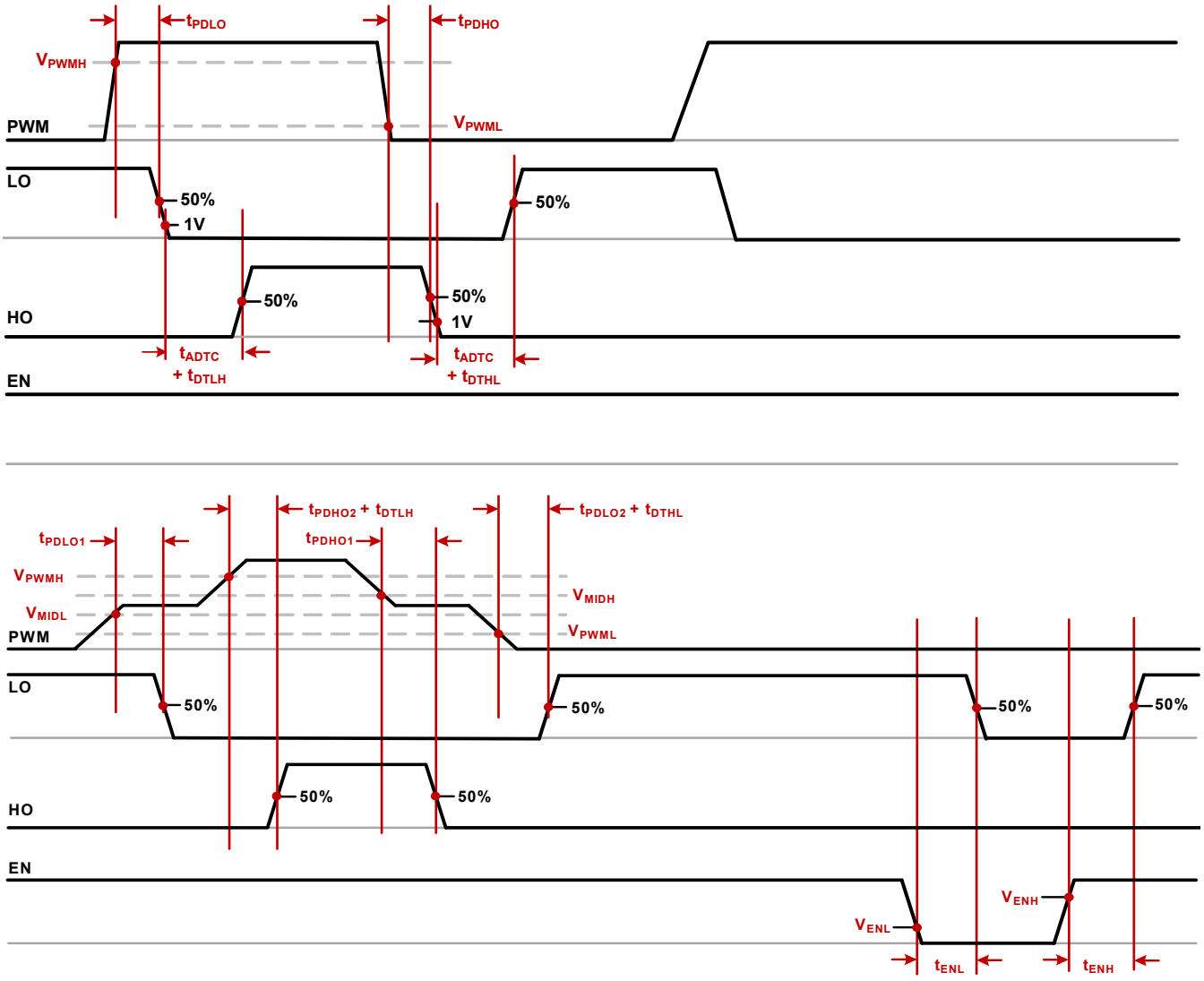


Figure 6. ISL78424, ISL78444

Notes:

9. Rise and Fall Times on PWM signal are shown exaggerated.
10. Timing Diagrams are with HS = V_{SS} = 0V
11. For ISL78424, HO_H shorted to HO_L and represented as HO; LO_H shorted to LO_L and represented as LO
12. t_{ADTC}: Adaptive dead time control delay from LO or HO falling below V_{ADTC}
13. t_{DTLH} and t_{DTHL} is adjustable dead time delay. See "Adjustable Dead Time Delay (RDT Pin)" on page 25 for more information.
14. For R_{DT} = 0V the adjustable dead time control is disabled and t_{DTLH} = t_{DTHL} = 0ns
15. t_{ADTC} + t_{DTLH}: Dead time delay from LO falling to HO rising. Measured from 1V on LO to 50% of HO.
16. t_{ADTC} + t_{DTHL}: Dead time delay from HO falling to LO rising. Measured from 1V on HO to 50% of LO.
17. t_{PDLO}: Propagation delay from PWM rising to LO falling. Measured from PWM = 3.8V to 50% of LO.
18. t_{PDHO}: Propagation delay from PWM falling to HO falling. Measured from PWM = 0.8V to 50% of HO.
19. t_{PDLO1}: Propagation delay from PWM entering tri-level state to LO falling. Measured from PWM = 1.6V to 50% of LO.
20. t_{PDLO2}: Propagation delay from PWM exiting tri-level state to LO rising. Measured from PWM = 0.8V to 50% of LO.
21. t_{PDHO1}: Propagation delay from PWM entering tri-level state to HO falling. Measured from PWM = 3.0V to 50% of HO.
22. t_{PDHO2}: Propagation delay from PWM exiting tri-level state to HO rising. Measured from PWM = 3.8V to 50% of HO.
23. t_{ENL}: Disable delay time from EN falling. Measured from V_{ENL} to 50% falling on LO with PWM = 0V.
24. t_{ENH}: Enable delay time from EN rising. Measured from V_{ENH} to 50% rising on LO with PWM = 0V.

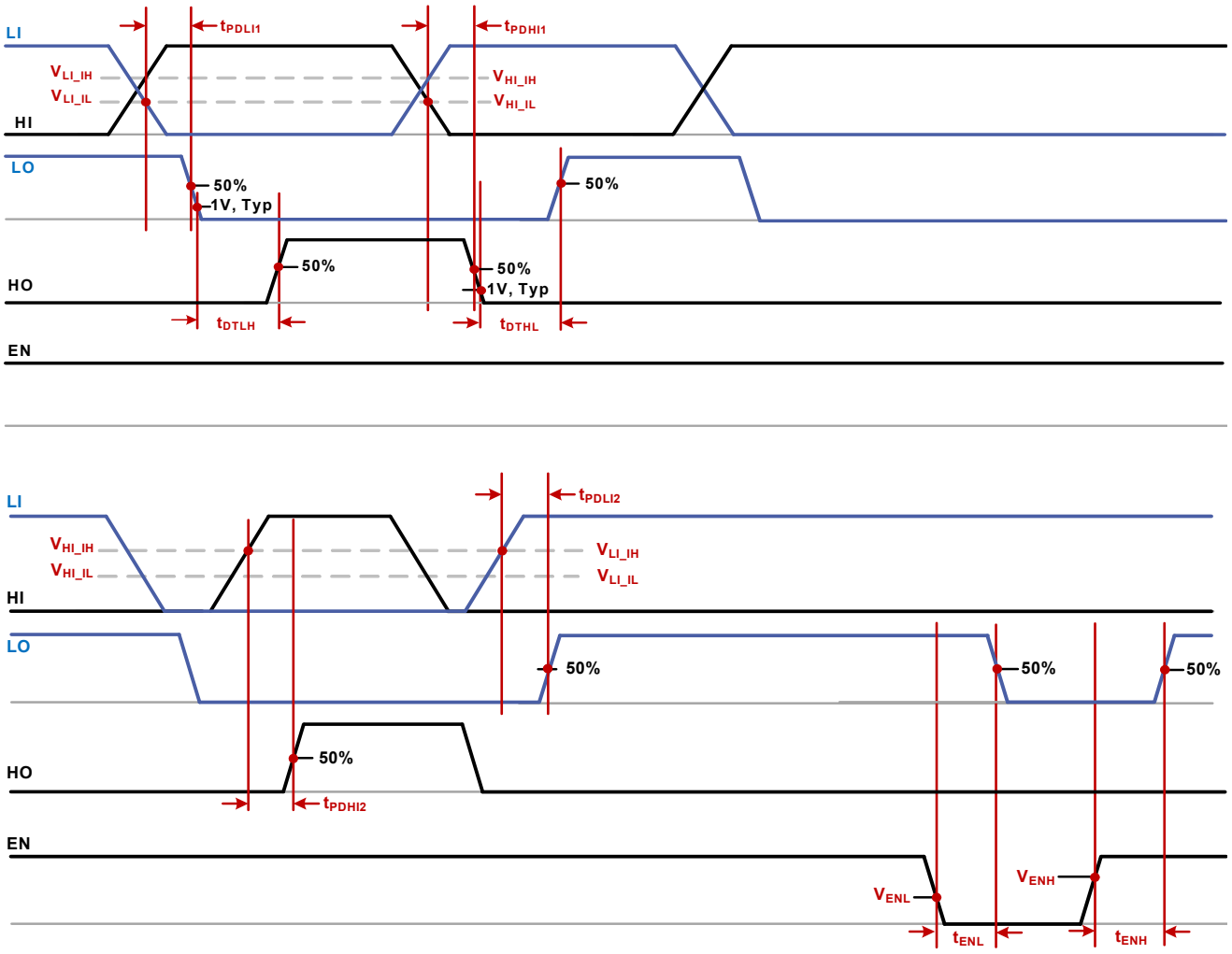


Figure 7. ISL78434

Notes:

25. Rise and fall times on HI and LI signal are shown exaggerated.
26. Timing diagrams are with HS = V_{SS} = 0V
27. For ISL78434, HO_H shorted to HO_L and represented as HO; LO_H shorted to LO_L and represented as LO
28. t_{DTLH}: Adaptive dead time delay from LO falling to HO rising. Measured from 1V on LO to 50% of HO.
29. t_{DTHL}: Adaptive dead time delay from HO falling to LO rising. Measured from 1V on HO to 50% of LO.
30. t_{PDLI1}: Propagation delay from LI falling to LO falling. Measured from LI = 1.0V to 50% of LO.
31. t_{PDHI1}: Propagation delay from HI falling to HO falling. Measured from HI = 1.0V to 50% of HO.
32. t_{PDLI2}: Propagation delay from LI rising to LO rising. Measured from LI = 2.1V to 50% of LO with HI = 0 for >1µs before LI rising.
33. t_{PDHI2}: Propagation delay from HI rising to HO rising. Measured from HI = 2.1V to 50% of HO with LI = 0 for >1µs before HI rising.
34. t_{ENL}: Disable delay time from EN falling. Measured from V_{ENL} to 50% falling on LO with LI = 5V.
35. t_{ENH}: Enable delay time from EN rising. Measured from V_{ENH} to 50% rising on LO with LI = 5V.

3. Typical Performance Curves

Unless otherwise stated, typical performance curves are taken with conditions with respect to its corresponding parameter in the Electrical Specifications table.

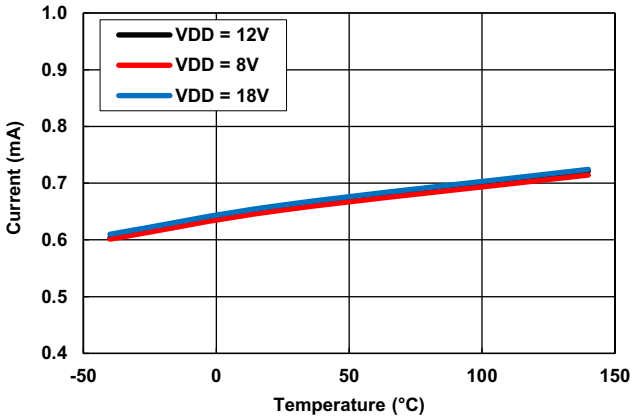


Figure 8. Quiescent Current vs Temperature

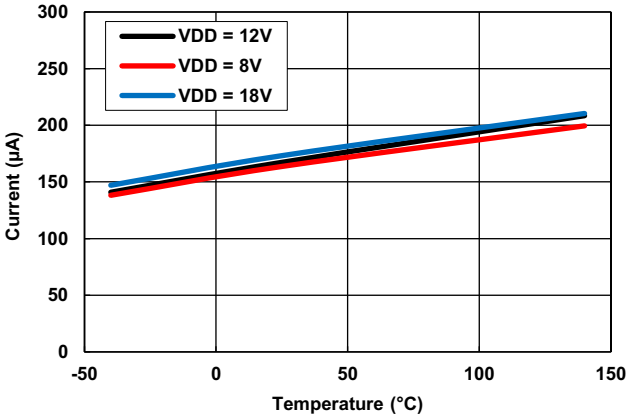


Figure 9. Shutdown Current vs Temperature (ISL78424 and ISL78444)

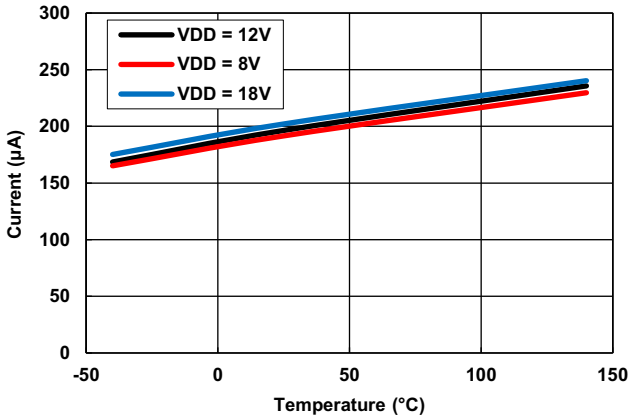


Figure 10. Shutdown Current vs Temperature (ISL78434)

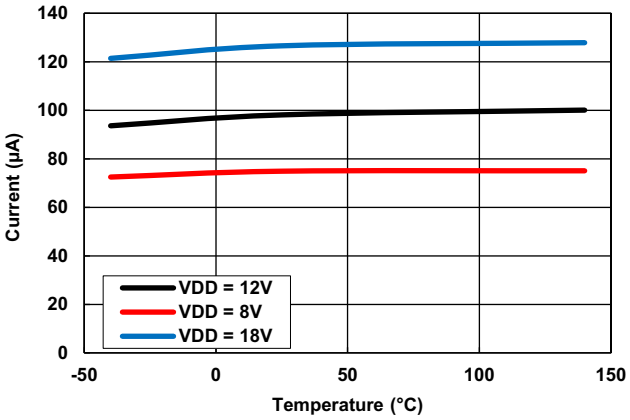


Figure 11. HB to VSS Bias Current vs Temperature

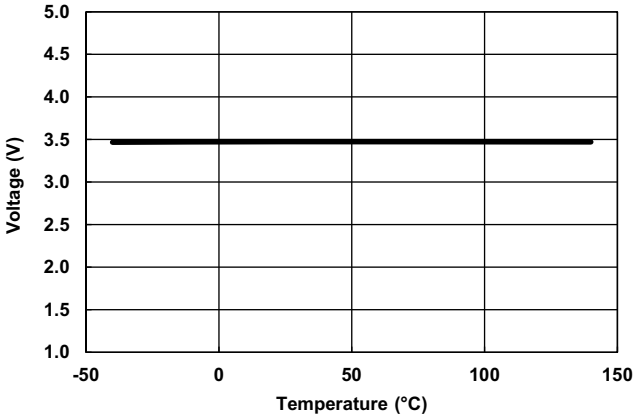


Figure 12. PWM High Rising Threshold Voltage vs Temperature

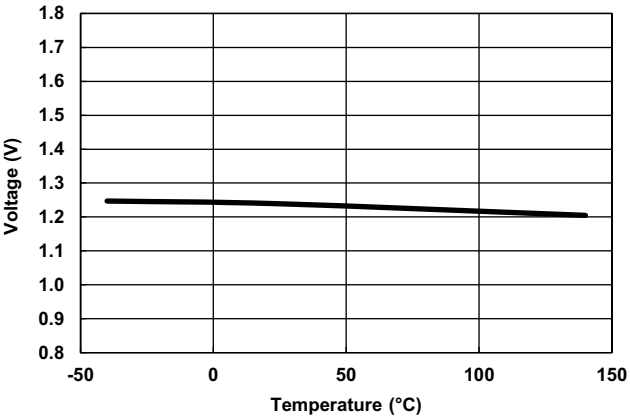


Figure 13. PWM Low Falling Threshold Voltage vs Temperature

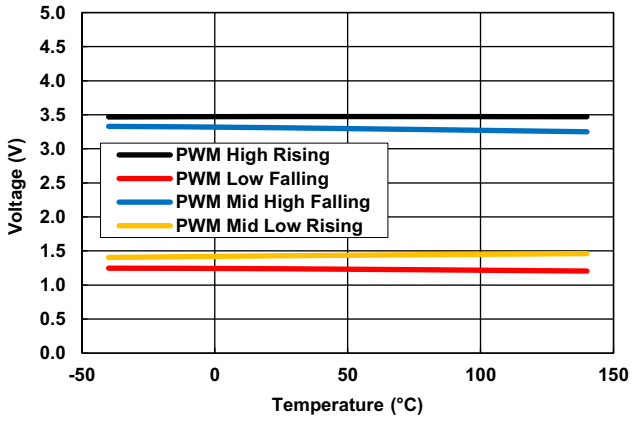


Figure 14. PWM Threshold Voltage vs Temperature

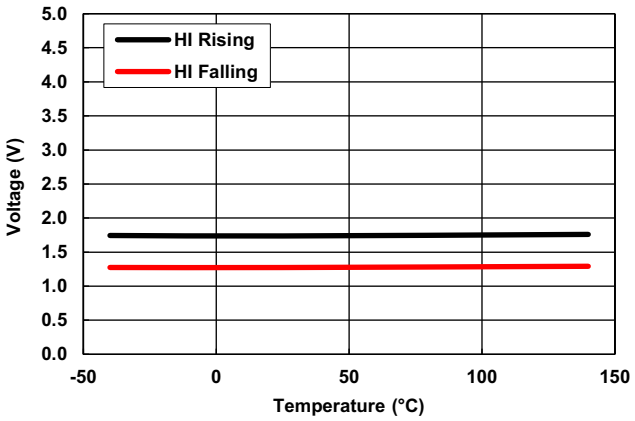


Figure 15. HI Threshold Voltage vs Temperature

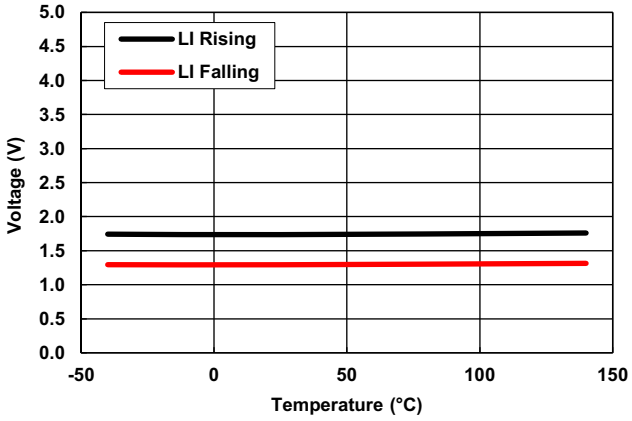


Figure 16. LI Threshold Voltage vs Temperature

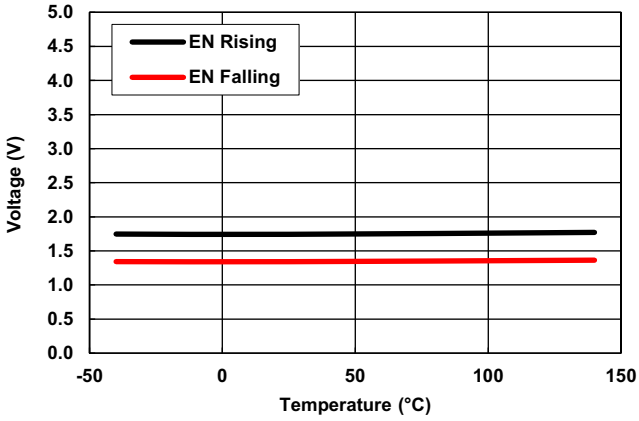


Figure 17. EN Threshold Voltage vs Temperature

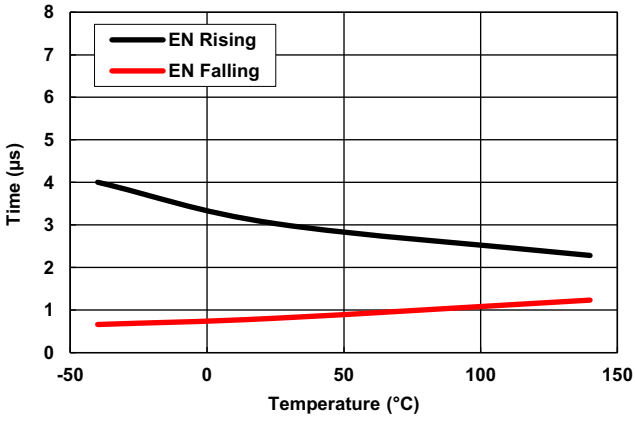


Figure 18. EN Delay Time vs Temperature

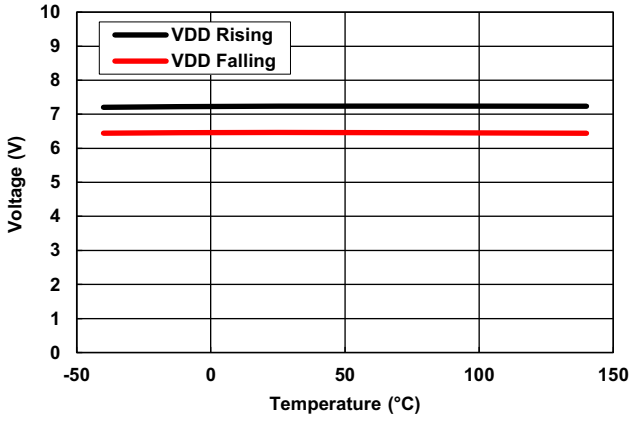


Figure 19. UVLO Threshold Voltage vs Temperature

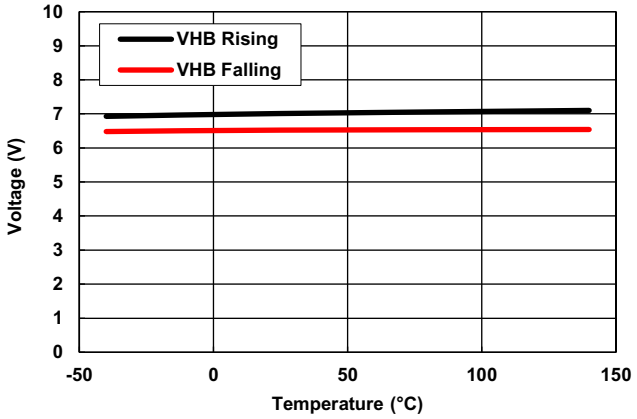


Figure 20. Boot UVLO Threshold Voltage vs Temperature

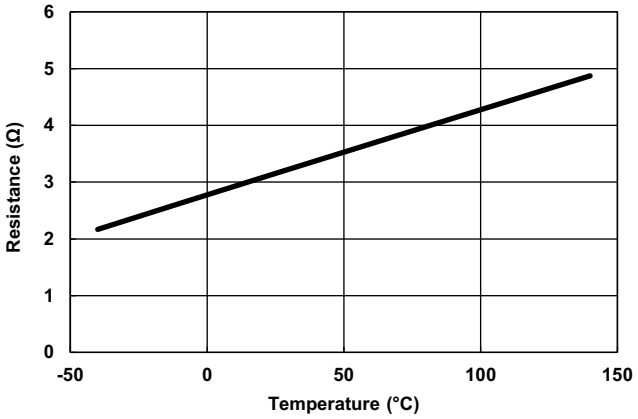


Figure 21. Boot Switch Resistance vs Temperature

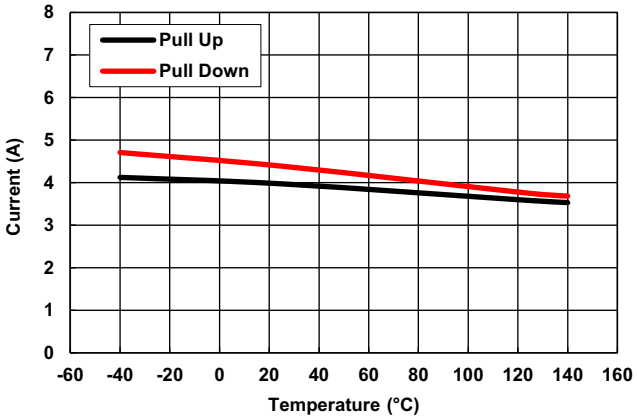


Figure 22. Low-Side Peak Current vs Temperature

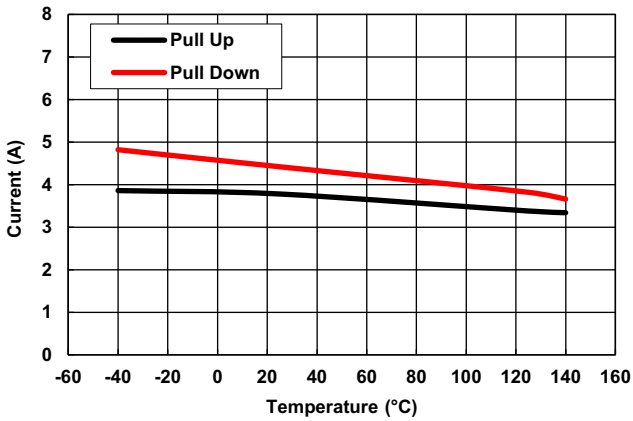


Figure 23. High-Side Peak Current vs Temperature

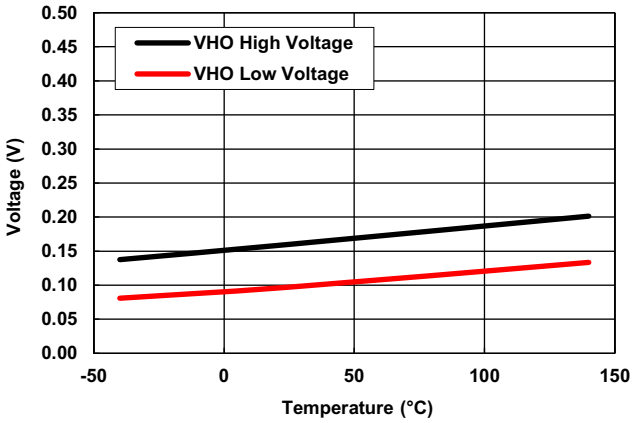


Figure 24. HO Gate Driver Voltage vs Temperature

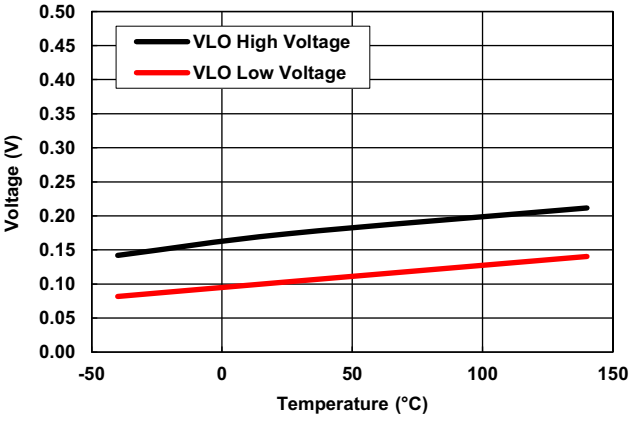


Figure 25. LO Gate Driver Voltage vs Temperature

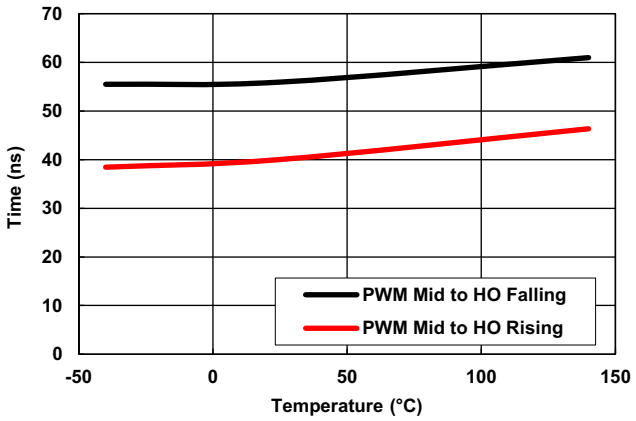


Figure 26. PWM to HO Propagation Delay vs Temperature

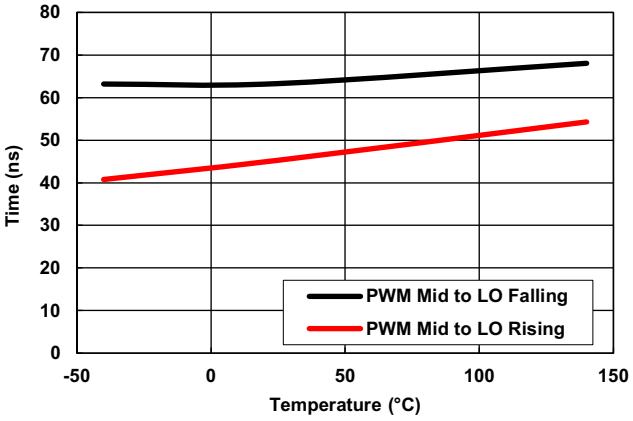


Figure 27. PWM to LO Propagation Delay vs Temperature

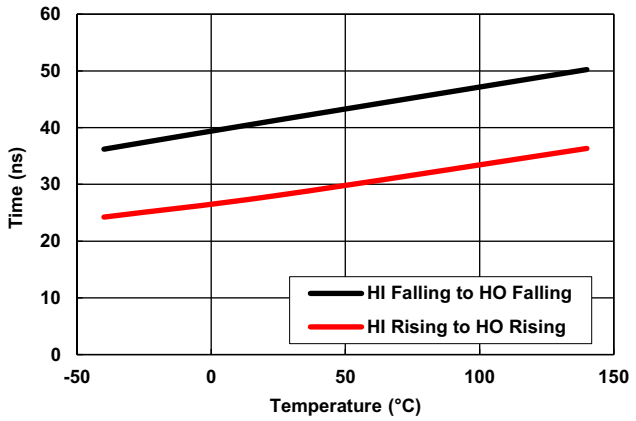


Figure 28. HI Propagation Delay vs Temperature

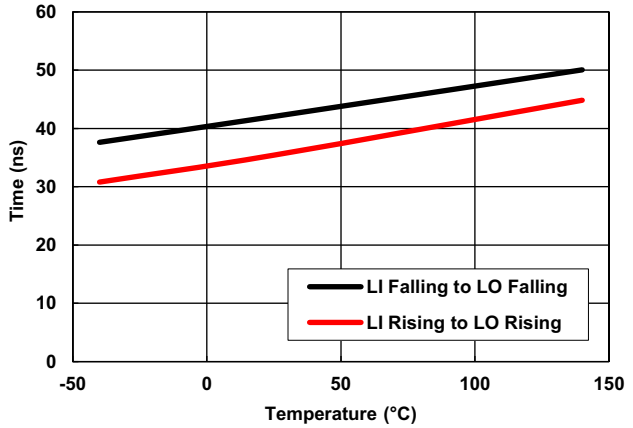


Figure 29. LI Propagation Delay vs Temperature

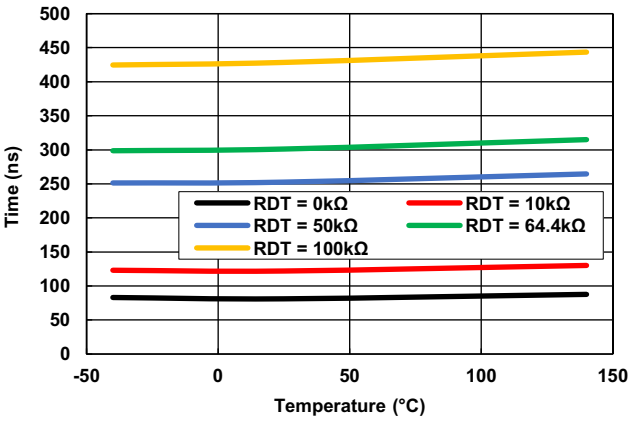


Figure 30. Dead Time HO Falling to LO Rising vs Temperature (ISL78424 and ISL78444 only)

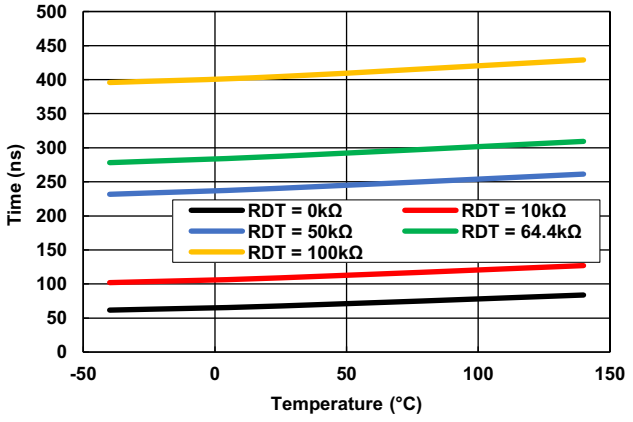


Figure 31. Dead Time LO Falling to HO Rising vs Temperature (ISL78424 and ISL78444 only)

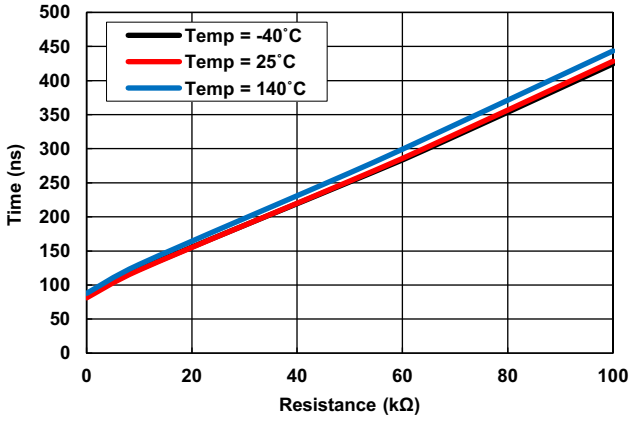


Figure 32. Dead Time HO Falling to LO Rising vs R_{DT} Resistance (ISL78424 and ISL78444 only)

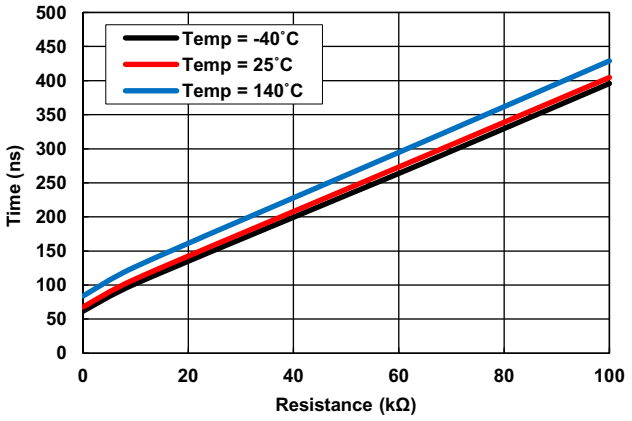


Figure 33. Dead Time LO Falling to HO Rising vs R_{DT} Resistance (ISL78424 and ISL78444 only)

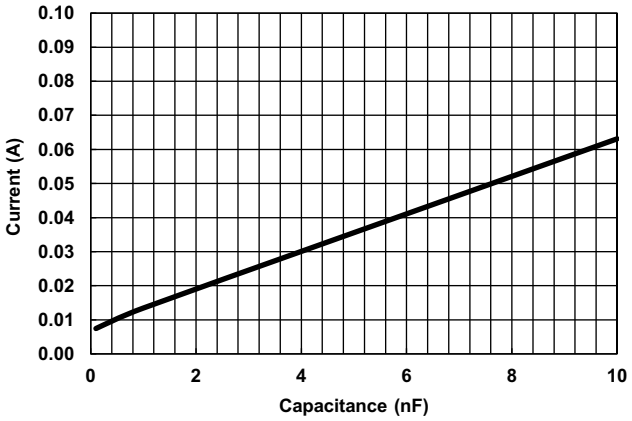


Figure 34. V_{DD} Current vs Capacitance on HO, LO

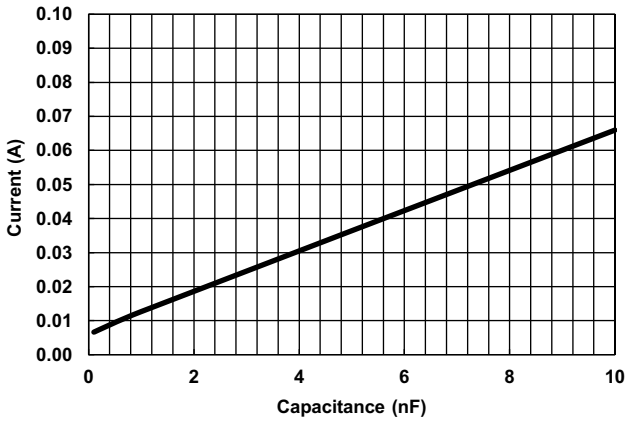


Figure 35. HB to HS Current vs Capacitance on HO, LO

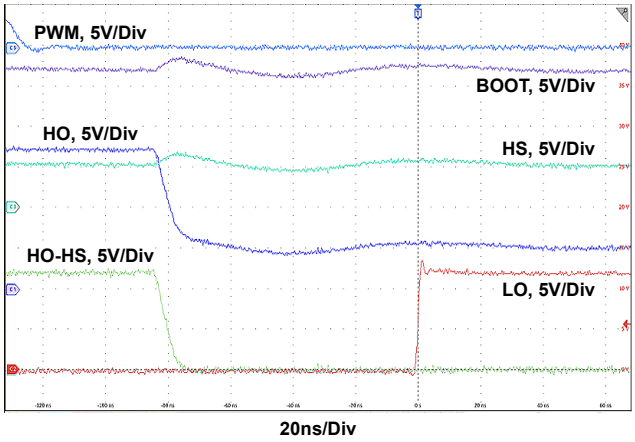


Figure 36. Dead Time HO Falling to LO Rising

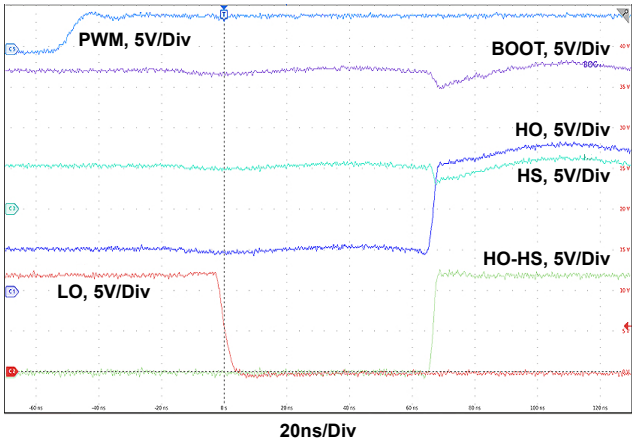


Figure 37. Dead Time LO Falling to HO Rising

4. Product Description

The ISL78424, ISL78434, and ISL78444 are Automotive Grade (AEC-Q100 Grade 1) high voltage, high frequency, half-bridge N-MOSFET gate drivers for up to 70V half-bridge topologies. The family of half bridge drivers feature 3A sourcing, 4A sinking peak gate drive current. The ISL78424 and ISL78444 feature a single tri-level PWM input for controlling both gate drivers. The ISL78434 has dual independent inputs for controlling the high and low-side driver separately. Strong gate drive strength and the adaptive dead time feature allow this family of drivers to switch high voltage, low r_{ON} power MOSFETs in half bridge topologies at high operating frequencies while providing shoot-through protection and minimizing dead time switching losses. For drivers with single PWM inputs (ISL78424 and ISL78444), when the input is logic high, the high-side driver is on and the low-side driver is off. When the input is a logic low, the low-side driver is on and the high-side driver is off. When the input voltage is mid-level, both the high and low-side drivers are low to keep the bridge off. The tri-level single PWM input allows the half-bridge to be phase dropped in multi-phase applications. When the enable pin (EN) is low, it takes the bridge driver outputs to a low state to turn off the FETs. When used with the Renesas Multiphase PWM Controllers (ISL78220, ISL78225, ISL78224, and ISL78226) with driver enable output logic, the EN pin prevents false bridge operation during controller start up.

4.1 Single PWM or Independent HI/LI Inputs

The ISL78424 and ISL78444 feature a single tri-level PWM input pin to control both the high-side and low-side driver outputs. When PWM is logic high on the ISL78424, the high-side source driver is active and the low-side sink driver is active. When PWM is logic low on the ISL78424, the low-side source driver is active and the high-side sink driver is active. The ISL78444 combines the sinking and sourcing drivers to make one gate drive signal (LO or HO). The gate drive signal is high when the sourcing driver is active, and conversely, the gate drive is low when the sinking driver is active. If the PWM pin is left floating, internal pull-up and pull down resistors bias the PWM pin to the mid-level state. The mid-level state has both high-side and low-side sink drivers active. Alternatively, the PWM pin can be actively driven to the mid-level state.

The single tri-level PWM input is ideal for multi-phase DC/DC converter applications that require phase dropping in light-load conditions. With a single input controlling the high and low-side driver, this reduces the number of controller signals needed by half and simplifies the PCB design, especially in six phase or greater DC/DC converters. The mid-level state puts the half-bridge in high impedance state for phase dropping.

The ISL78434 features independent inputs HI and LI that drive the HO and LO outputs, respectively. The PWM pin is replaced with HI and LI pins. Separate inputs are used in controllers that need to control the upper and lower FET with independent signals.

4.2 ISL78424 and ISL78444 PWM Input

The ISL78424 and ISL78444 single PWM input controls both high and low-side driver with one control signal. When the PWM input is switching between logic high and logic low, the high-side driver output is in phase with the PWM input while the low-side driver is logic inverted from the PWM input. If the PWM is in mid-level (that is, 2.5V) both driver outputs are low. By design, the PWM input prevents a controller from turning both drivers on, providing shoot-through protection against faulted input logic that can occur from a two input driver inadvertently turning both drivers on.

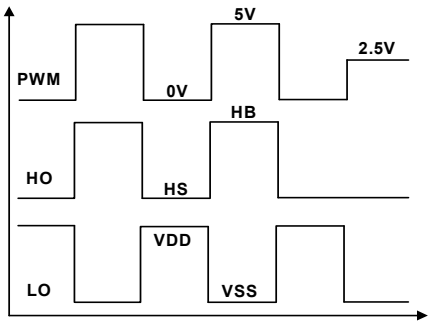


Figure 38. Single PWM Tri-Level Input Control

4.3 ISL78434 HI/LI Lockout Protection

With independent HI and LI inputs being driven by two control signals, dead time is set with the controller by ensuring one control signal is off prior to turning on the other one. There is a possibility the controller outputs are damaged, faulted or from improper dead time programming, causing logic high to both inputs to the driver. The ISL78434 features an input lockout protection to prevent both driver outputs going active high at the same time. Internal logic in the IC senses the HI and LI inputs. The driver locks out any input logic from propagating to that driver output if the other input is already logic high. For example, if HI = 1, LO output does not respond to LI input logic high. If LI = 1, HO output does not respond to HI input logic high. The lockout function is disabled when the first high input goes low, allowing the second input logic to propagate to the output. As a further protection against shoot-through, adaptive dead time is enforced when recovering from the lockout function.

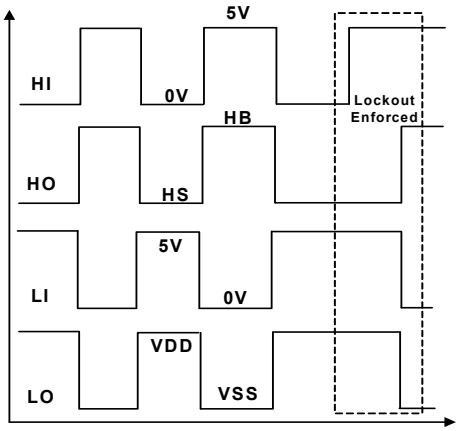


Figure 39. HI/LI Input with Lockout Protection

4.4 Separate Source and Sink Outputs

The ISL78424 and ISL78434 feature separate pins for the sourcing and sinking driver outputs. The HO_H and HO_L are the high-side sourcing and sinking drivers, respectively. The LO_H and LO_L are the low-side sourcing and sinking drivers, respectively. Separate source and sink output pins allow optimizing the FET turn on/off times using gate drive limiting resistors.

The half bridge MOSFET drain-to-source switching dv/dt and di/dt can cause problems when the turn on or turn off occurs too fast (transient overshoot, ringing, and EMI). Many half bridge circuit designs commonly place gate drive limiting resistors in series with the driver output to limit the gate drive current and effectively slow down the turn on and/or turn off of the MOSFET. The turn on and turn off times are typically independently optimized.

A cumbersome solution for single output drivers is to use a series diode + resistor in parallel of a second gate resistor to provide isolation of the sourcing and sinking driver currents (see Figure 40 on page 22). With the diode solution, the gate drive limiting impedance is the parallel resistance in the sinking path and the resistance without the diode in the sourcing path. The drawback of the diode solution is the extra component cost and the parallel resistance requires tuning of both resistors for slew rate control.

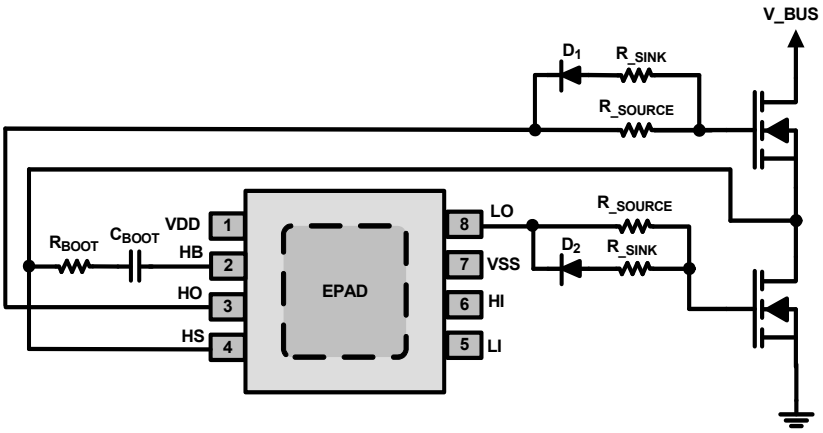


Figure 40. Gate Resistors in Standard Bridge Driver

A solution to eliminate the diode and simplify the gate resistance tuning is to provide independent high (sourcing) and low (sinking) driver outputs. This gives flexibility of tuning the source and sink driver impedance to the MOSFET gate without the need of a blocking diode. To separate each output into independent source and sink paths, the half bridge requires an additional pin per driver output (see Figure 41).

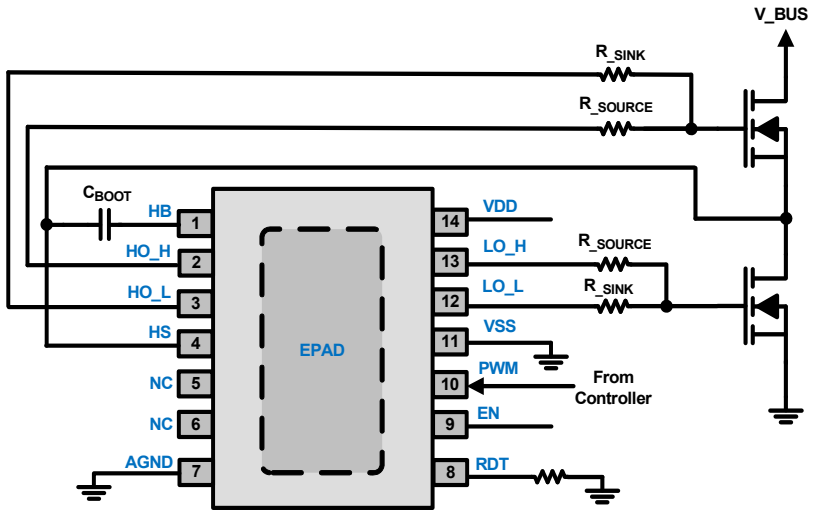


Figure 41. Independent Source and Sink Driver Outputs

4.5 Peak Gate Drive Currents

The high-side and low-side drivers feature 3A peak sourcing and 4A peak sinking drive capability. Strong gate drive allows fast switching times when low $r_{DS(ON)}$, high voltage power MOSFETs are used. The switching time of the MOSFET translates to the total gate charge of the MOSFET divided by the peak current of the driver.

Example:

$Q_{GS} = 50nC = 50nA \bullet s$
$I_{SOURCING} = 3A$
$I_{SINKING} = 4A$

(EQ. 1) $$t_{FET\_ON} = \frac{Q_{GS}}{I_{SOURCING}} = \frac{50nA \bullet s}{3A} = 16.7ns$$

(EQ. 2) $$t_{FET\_OFF} = \frac{Q_{GS}}{I_{SINKING}} = \frac{50nA \bullet s}{4A} = 12.5ns$$

As we can see with the high sourcing and sinking currents of the ISL78424, ISL78434, and ISL78444, the switching times of the MOSFETs are 16.7ns (turn on) and 12.5ns (turn off) for a MOSFET with about 5nF of gate capacitance (V_{GS} = 0V to 10V). Some bridge drivers offer gate drive capability as low as 500mA, resulting in switching times in the 100ns range for the MOSFET in the example above.

4.6 Shoot-Through Protection

The ISL78424, ISL78434, and ISL78444 feature shoot-through protection of the half bridge by preventing the driver from turning on both FETs at the same time. These drivers integrate Adaptive Dead Time Control (ADTC) that prevents a MOSFET in the bridge from being switched on until the complementary MOSFET has been switched off. The ADTC function seeks to minimize dead time, the time when both MOSFETs are off, while preventing the possibility that both MOSFETs are on at the same time, a condition that could result in shoot-through. ADTC prevents shoot-through while minimizing the higher conduction losses that occur during long dead times.

4.7 Shoot-Through and Dead Time

Shoot-through occurs when both FETs in the half bridge are on at the same time, creating a short-circuit path of the bridge. In a buck regulator, the bus voltage would see a short-circuit to ground causing large current to flow through both FETs. This leads to high power dissipation and can result in FET damage. Dead time is the time when both FETs are off at the same time. Before a FET in the half bridge is turned on, the complementary FET is first switched off, purposefully creating a period of dead time that prevents shoot-through. However, if care is not taken, under some conditions one FET may not be completely off before the complementary FET is turned on. In such a condition, there is no dead time and a transient shoot though condition occurs that results in a momentary short-circuit of the bridge. This fault becomes very serious as the duration when both FETs are on simultaneously is extended and can quickly result in damage of the power FETs due to high power dissipation. ISL78424, ISL78434, and ISL78444 driver includes shoot-through protection to prevent such a condition.

4.8 Adaptive Dead Time Control (ADTC)

With proper design, shoot-through caused by faulted inputs turning both drivers on are avoided. Other shoot-through conditions occur when there is no dead time on the driver outputs causing a momentary overlap when both FETs are still on. This kind of shoot-through occurs when the gate to source voltage for the top and bottom FET are above the gate threshold voltages, turning both FETs on. Even with proper input logic control, anything that causes the turning off FET to overlap with the turning on FET without dead time causes a transient shoot-through. To prevent against transient shoot-through faults, the ISL78424, ISL78434, and ISL78444 family of drivers implement Adaptive Dead Time Control circuit that prevents a driver output from turning ON until a satisfactory condition is sensed at the turning OFF driver. To turn on a FET, the associated driver output does not go high until the driver output of the turning off FET crosses a falling threshold. This ensures that one FET is completely off before the other FET is turned on with a minimum dead time, minimizing switching losses, and increasing converter efficiency.

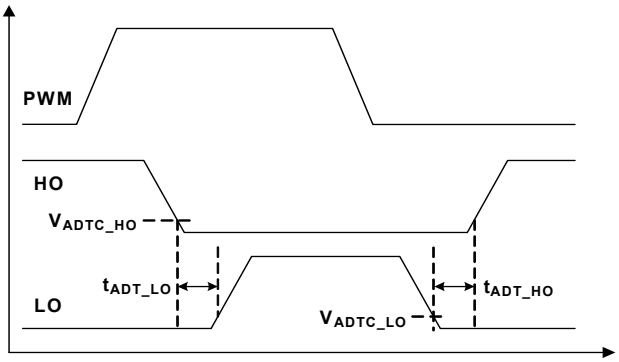


Figure 42. Adaptive Dead Time Control

4.9 Adaptive Dead Time and Gate Resistors

To prevent shoot-through, adaptive dead time control senses the voltage at the driver output pins for crossing a falling threshold, at which point the driver considers the FET to be off, before turning the other driver on. With single driver outputs HO and LO, the accuracy of the sense circuit is disrupted when gate resistors are used in series with the driver outputs to slow down the FET turn on/off time because the resistor isolates the driver output from the FET gate. The resistor and FET gate capacitance form an RC low pass filter of the driver output to the FET gate. With the gate voltage lagging behind the driver output voltage, the adaptive dead time control could sense a falling threshold at the driver output but the slower falling gate voltage could still be higher than the gate threshold, resulting in no dead time and causing a momentary shoot-through condition of the bridge.

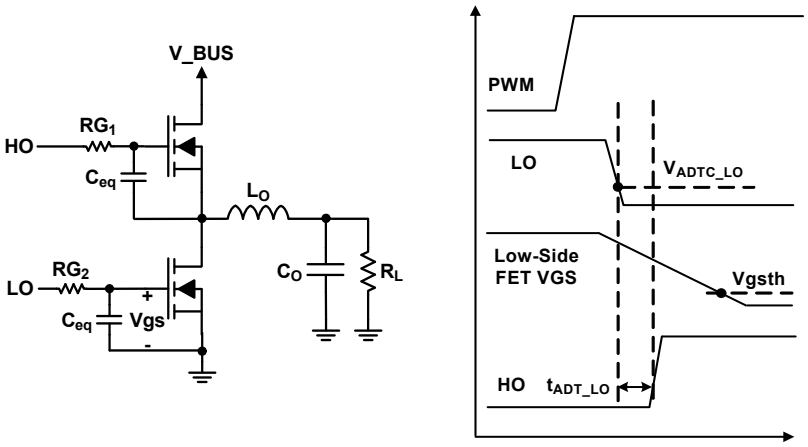


Figure 43. Adaptive Dead Time Problem with Gate Resistors

The ISL78424 and ISL78434 drivers include a means of using independent source/sink driver outputs to overcome the error that gate resistors typically introduce to adaptive dead time implementations. The driver output sourcing pins (LO_H and HO_H) are used as a Kelvin sense when not actively sourcing. When the sinking pins (LO_L or HO_L) are active during FET turn off, even with gate resistors between driver output and FET gate, the gate voltage (and not the driver output) is sensed by the LO_H or HO_H pin. Adaptive Dead Time Control combined with the gate sensing from separate driver output source and sink pins eliminates the error of inaccurate adaptive dead time sensing when combined with gate resistors.

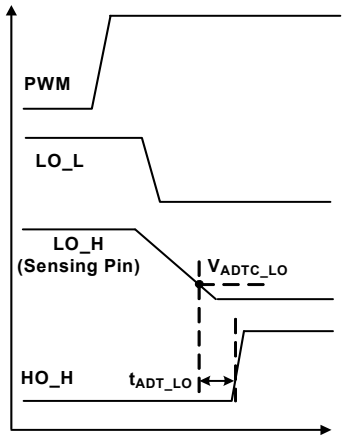


Figure 44. Adaptive Dead Time with Gate Sensing

Adaptive dead time control minimizes dead time needed to prevent bridge shoot-through. During dead time, the body diode of the synchronous FET conducts, generating conduction losses that exceed those that would occur if the MOSFET itself was conducting. Because conduction losses are higher during dead time than they otherwise would be if the MOSFET were conducting, conversion efficiency is improved as dead time is decreased, so long as

shoot-through does not occur. The lowest adaptive dead time achieved is limited by the propagation delay of the sense circuitry inside the driver. If more dead time is required, the adjustable dead time delay function (ISL78424 and ISL78444 only) further increases the minimum dead time set by the Adaptive dead time control by adjusting the resistor value on RDT pin.

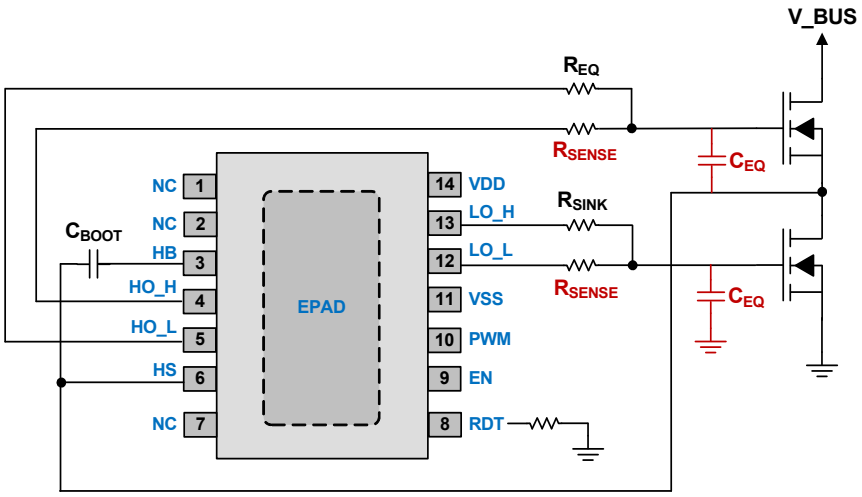


Figure 45. Adaptive Dead Time with Independent Source/Sink for Gate Sensing

4.10 Falling Thresholds for ADTC

The three thresholds for the falling edge detection for Adaptive Dead Time Control - two for the high-side and one for the low-side are summarized in Table 2. For ISL78424 and ISL78434, the detection is sensed at the driver source pins LO_H (low side) and HO_H (high side). For ISL78444 where the source and sink driver outputs are on one pin, the detection is done at LO and HO directly, losing the gate sense capability. Additionally, there is a falling edge HS phase sense detector on the high-side driver that turns on the LO output when the high-side gate sense is not detected. This occurs when a large gate resistor slows down the turn off of the high-side FET such that gate voltage is below the Miller voltage but still above the ADTC detection threshold. Here the changing of the HS phase node voltage detects that the high-side FET has turned off.

Table 2. Adaptive Dead Time Falling Edge Thresholds (Note)

Sense Pin	Name	Threshold Voltage (Typical)
LO_H	Low-Side Gate Sense	1.0V from LO_H to VSS
HO_H	High-Side Gate Sense	1.3V from HO_H to HS
HS	High-Side Phase Sense	0.5V from HS to VSS

Note: This information only applies to the ISL78424 and ISL78434. The ISL78444 uses LO and HO as sense pins.

4.11 Adjustable Dead Time Delay (RDT Pin)

The minimum dead time due to propagation delays of the adaptive dead time control circuit on this family of bridge drivers can be increased with the adjustable dead time delay feature (ISL78424 and ISL78444). Connect a resistor from the RDT pin to AGND to further increase the dead time set by the ADTC circuit. The adaptive dead time range due to the additional programmed dead time is 30ns to 240ns, from the allowable R_{DT} resistance values of 10kΩ to 100kΩ. This function is useful if the minimum dead time from the adaptive dead time control requires extra margin in the system to prevent shoot-through from occurring.

If adjustable dead time delay is not needed, connect the RDT pin to ground.

A 0.6V reference voltage combined with the resistor on the RDT pin generates a current for an internal oscillator; the current being proportional to the additional dead time delay. The relationship of resistor value on the RDT pin to dead time is shown in Figure 46 on page 26.

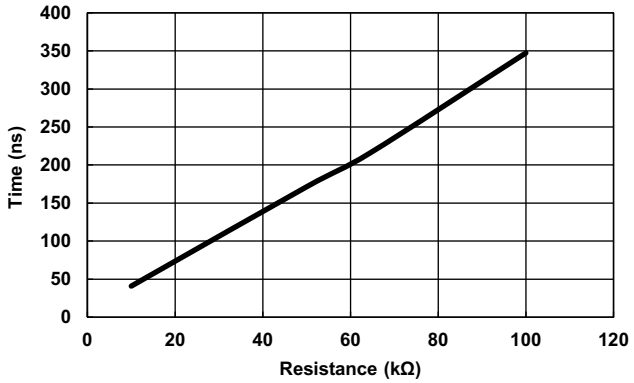


Figure 46. Dead Time HO Falling to LO Rising vs R_{DT} Resistance ($V_{DD} = V_{HB} - V_{HS} = 12V$; $V_{HS} = 0V$)

4.12 Integrated Bootstrap Switch

The ISL78424, ISL78434, and ISL78444 family integrates a bootstrap switch internal to the IC. No external boot diode is necessary for the high-side driver bootstrap operation. The advantage of a boot switch compared to a boot diode is that a switch has less voltage drop across it. With a switch the bootstrap voltage at HB can be charged to ~VDD while a boot diode has ~0.7V drop at HB. With the boot switch implementation, the low-side and high-side driver outputs can turn on FETs at the V_{DD} voltage across gate to source. The boot switch r_{ON} is 3Ω typical which provides the proper impedance to refresh the boot capacitor in applications up to 500kHz when the proper boot capacitor is selected.

Upon initial enabling of driver, the boot switch is turned on when PWM is logic low for the ISL78424 and ISL78444 (LI is logic high and HI is logic low for the ISL78434) and the HS pin is below 2V. After a subsequent turning on of the high-side driver, PWM is logic high for the ISL78424 and ISL78444 (LI is logic low and HI is logic high for the ISL78434), whenever PWM (HI for the ISL78434) is not logic high and the HS pin is below 2V the boot switch is turned on. When the boot switch FET is not turned on, there is a parallel path of the FET body diode with a 10Ω series impedance (see Figure 47).

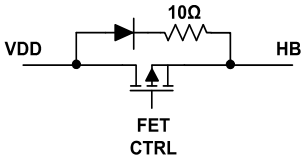


Figure 47. Bootstrap Switch

4.13 Bootstrap Capacitor

To provide the proper gate drive to the high-side FET, the high-side driver bias on this family of drivers is handled with a bootstrap capacitor across the HB and HS pins. The boot bias is recharged whenever the HS pin voltage goes below 2V and the high-side source driver is not commanded by PWM or HI. The internal boot switch from VDD to HB turns on and the bootstrap capacitor is charged by VDD. To maintain operation of the high-side gate drive and at the same time be adequately charged during initial boot up and refreshed in operation requires choosing an appropriate capacitor value. In general, for most applications a 0.1µF to 0.33µF bootstrap capacitor is a good starting point. For more information on choosing the right bootstrap capacitor, see "Bootstrap Capacitor Design" on page 28.

4.14 EN Pin

The EN pin when placed in logic 0 state places the driver into a low power shutdown state. In shutdown, the driver outputs do not respond to PWM inputs (for ISL78424 and ISL78444) and HI/LI inputs (for ISL78434). The low-side driver sink output is active and the high-side driver sink output has a 1MΩ impedance to HS to keep the bridge FETs off. The EN pin is used with Renesas analog DC/DC controllers (that is, ISL78220, ISL78225, and ISL78226) to provide a state of non-operation before soft-start of the converter. The Renesas controllers have a driver enable pin that asserts high when soft-start begins to ensure the half bridge is not switching before the controller is properly biased.

The EN pin has an internal 160kΩ pull-down resistor that disables the driver when the pin is left floating.

4.15 UVLO Protection - VDD and Boot

The driver implements UVLO on both the VDD and HB-HS bootstrap supply. When the voltage on VDD and HB (referenced to HS) is below the UVLO threshold, UVLO protection is active. For the VDD UVLO, both driver sourcing outputs are disabled and the low-side sinking output is active. For boot UVLO, only the high-side driver sourcing output is disable and there is a 1MΩ impedance on the HO pin relative to HS. The low-side driver continues to respond to driver inputs in Boot UVLO.

When coming out of VDD UVLO, the high-side sourcing driver does not respond to input commands until the low-side sourcing driver is active first. This ensures a boot refresh cycle occurs first to charge the bootstrap capacitor to provide proper bias for the high-side driver.

5. Applications Information

5.1 Supply Voltage Operating Range

The recommended operating voltage range on VDD is 8V to 18V. Renesas recommends placing a 0.1µF high frequency decoupling capacitor close to the VDD and VSS pin of the IC. A decoupling capacitor of at least 10 times the value of the boot capacitor is recommended to be placed in parallel with the 0.1µF at VDD and VSS.

5.2 Bootstrap Capacitor Design

ISL78424, ISL78434, and ISL78444 family has an integrated bootstrap switch that charges the external bootstrap capacitor required on the HB to HS pins. To ensure that proper value of the bootstrap capacitance is selected, the minimum V_{GS} of the FET which is being driven needs to take into account, along with the voltage drop across the bootstrap switch, typically 0.4V.

(EQ. 3) $$\Delta V_{BOOT} = V_{DD} - V_{DH} - V_{GS\_MIN}$$

- ΔV_{BOOT} = Maximum allowable voltage dip to ensure proper function
- V_{DD} = V_{BOOT} charging supply
- V_{DH} = High current forward voltage
- V_{GS_MIN} = Minimum V_{GS} voltage of FET required to keep FET on

The minimum C_{BOOT} capacitance required to ensure proper functionality becomes dependent on the total charge required during the on state of the high side when the C_{BOOT} is not charging, along with the allowable change in voltage of the boot.

(EQ. 4) $$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}}$$

where:

(EQ. 5) $$Q_{TOTAL} = Q_{G\_MAX} + (I_{GS\_LKG} + I_{HBQ} + I_{HBSLEAK}) \times t_{ON}$$

- Q_{G_MAX} = Maximum gate charge, from FET datasheet
- I_{GS_LKG} = Maximum FET gate-body leakage current, from FET datasheet
- I_{HBQ} = Boot quiescent current
- $I_{HBSLEAK}$ = Boot leakage current

5.3 Gate Drive Limiting Resistors

Gate limiting resistors are generally used for two purposes. One is to slow down the NMOS FET turn on and turn off by limiting drive current to the gate. The ISL78424 and ISL78434 has separate sourcing and sinking pins on the driver outputs which allow independent control of the gate drive limiting.

A second reason for adding gate drive limiting resistors is to control the transient ringing voltage on the MOSFET gate-source pins. This occurs when there is excessive trace inductance in the layout of the driver output to the MOSFET gate, combined with a low impedance high current driver output producing very fast edges with large transient voltages at the FET gate. Gate drive limiting resistors reduce the peak voltage to safe levels to the gate.

5.4 Adaptive Dead Time Control

The ISL78424 and ISL78434 use gate sensing adaptive dead time control for turning on a NMOS FET gate with a minimum dead time after a valid detection of turning off the other NMOS FET gate in a half bridge configuration. The gate sense pins accurately monitor the FET gate-to-source voltage for crossing the internal detection thresholds on the driver.

A low-side gate sense (1.3V typical) and two detectors on the high side (gate sense (1.0V typical to HS) and phase sense (0.5V to VSS typical)), determine when the FET gate voltage is sufficiently low enough to turn a FET off before allowing the other gate driver to turn on. Some bridge drivers with adaptive dead time control only offer a high-side phase sense. The high-side gate sense is necessary for boost converter applications because the HS phase node is clamped to the synchronous FET body diode voltage above VOUT and only falls when the low-side FET is turned on.

In Buck Converter applications, the turn off of the high-side control FET causes the HS phase node to fall until clamped by a body diode voltage below GND of the low-side FET. The falling edge HS dv/dt is proportional to the peak inductor current at high-side FET turn off. A fast dv/dt on HS couples current into the high-side gate sense detection circuitry that triggers the HO_H gate sense circuitry, even though the high-side gate sense (HO_H-HS) is still above the gate sense threshold. In this situation, the Adaptive Dead Time is determined by the falling edge of HS to LO rising. The high-side gate sense detection circuitry is only active on falling edges of HO from PWM or HI going low, therefore ringing on rising edges of phase/HS does not cause false detection of the gate sense.

5.5 Adjustable Dead Time Control

When the minimum dead times from the adaptive dead time control is insufficient, the ISL78424 and ISL78444 provides adjustable dead time control on the RDT pin. A resistor on the RDT pin to AGND adds an additional delay in addition to the adaptive dead time delay.

The recommended range of resistor values is 10kΩ to 100kΩ which provides an additional 40ns to 340ns dead time delay in addition to the ADTC. Place the resistor as close as possible to the RDT and AGND pins. If additional delay is not needed, short the RDT pin to AGND.

5.6 Power Dissipation Calculation

The ISL78424, ISL78434, and ISL78444 family power dissipation loss is comprised of the DC loss (P_{LOSS_DC}) and the losses due to switching (P_{LOSS_SW}).

(EQ. 6) $$P_{LOSS\_TOTAL} = P_{LOSS\_DC} + P_Q$$

The DC power loss is proportional to the input voltage (V_{DD}) of the driver and the quiescent current, 500µA typical.

(EQ. 7) $$P_{LOSS\_DC} = V_{DD} \times I_Q$$

The switching power loss accounts for the larger portion of the power loss and is directly proportional to the frequency (f_{SW}) at which the drivers (HO and LO) are turning on/off their respective transistors, the gate charge of the transistor being driven (Q_{G_MAX}), and the input voltage of the drivers (V_{DD}) which is the drive voltage for the FETs.

Separate source and sink output pins allow for optimized FET turn on/off times using different value resistors. These gate resistors also help to allow calculation of the energy required to charge the gate (C_{GATE}) of the FETs, and the energy dissipated in this gate resistor is equal to the energy stored in the capacitor. The energy dissipation of the resistor does not depend on the gate resistance, but solely on the gate charge of the transistor.

(EQ. 8) $$C_{GATE} = \frac{Q_{G\_MAX}}{V_{DD}}$$

(EQ. 9) $$E_{CGATE} = \frac{1}{2} \times (V_{DD})^2 = \frac{1}{2} \times Q_{G\_MAX} \times V_{DD}$$

As the transistor is being switched on/off, the power loss is doubled as the user is charging up the gate to V_{DD} with a finite amount of energy, ECGATE, and then it is discharging that finite amount of energy when the gate is brought back to GND.

(EQ. 10) $$P_{LOSS\_SW} = 2 \times E_{CGATE} \times f_{SW} = C_{GATE} \times (V_{DD})^2 \times f_{SW} = Q_{G\_MAX} \times V_{DD} \times f_{SW}$$

where:

- Q_{G_MAX} = Maximum gate charge, from FET datasheet
- E_{CGATE} = Energy required to charge the drive transistor gate voltage to V_{DD}; energy stored in capacitor
- V_{DD} = Driver input voltage
- f_{SW} = Switching frequency operation of driver

6. PCB Layout Guidelines

For best thermal performance, connect the driver EPAD to a low thermal impedance ground plane. Use as many vias as possible to connect the top layer PCB thermal land to ground planes on other PCB layers. For best electrical performance, connect the VSS and AGND pins together through the EPAD to maintain a low impedance connection between the two pins.

When adjustable dead time is used (ISL78424 and ISL78444 only), connect the resistor to the RDT pin and GND plane close to the IC to minimize ground noise from disrupting the timing performance.

Place the VDD decoupling capacitors and bootstrap capacitors close to the VDD-VSS and HB-HS pins, respectively. Use decoupling capacitors to reduce the influence of parasitic inductors. To be effective, these capacitors must also have the shortest possible lead lengths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.

(1) Keep power loops as short as possible by paralleling the source and return traces.

(2) Adding resistance might be necessary to dampen resonating parasitic circuits. In PCB designs with long leads on the LO and HO outputs, add series gate resistors on the bridge FETs to dampen the oscillations.

(3) Large power components (power FETs, electrolytic capacitors, power resistors, etc.) have internal parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.

(4) If you simulate your circuits, consider including parasitic components.

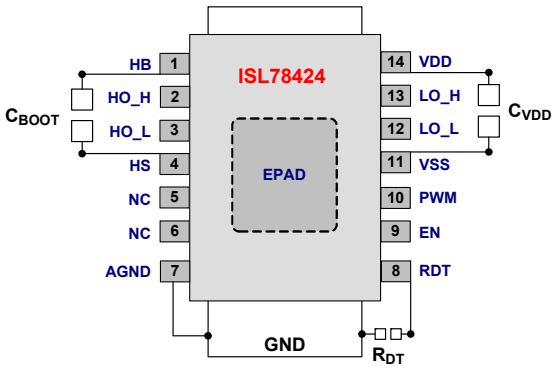


Figure 48. Component Placement

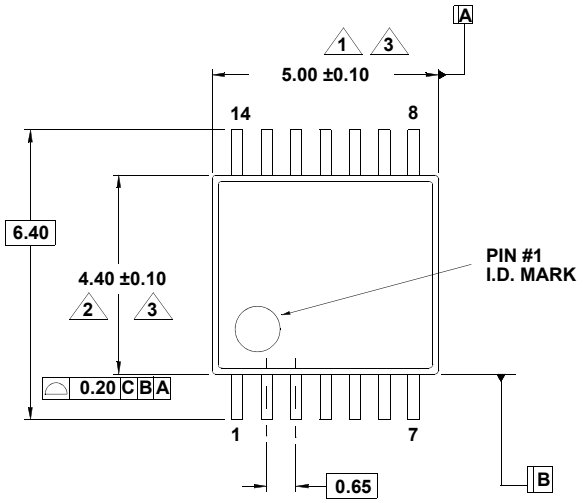
7. Revision History

Rev.	Date	Description
0.00	Sep 10, 2018	Initial release

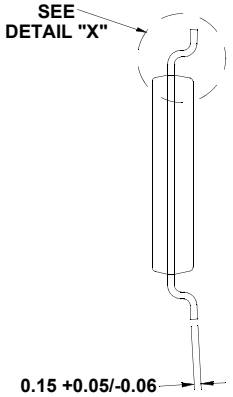
8. Package Outline Drawing

For the most recent package outline drawing, see M14.173B.

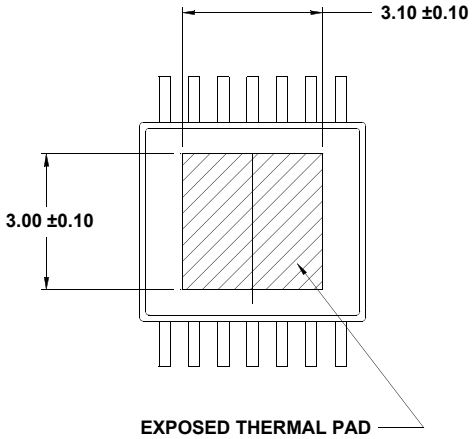
M14.173B
14 LEAD HEATSINK THIN SHRINK SMALL OUTLINE PACKAGE (HTSSOP)
Rev 1, 1/10



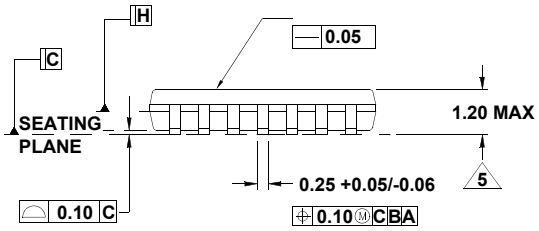
TOP VIEW



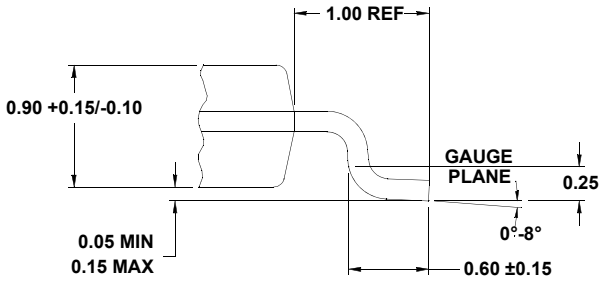
END VIEW



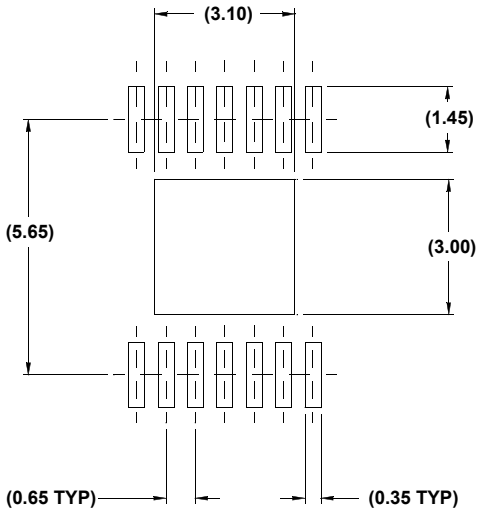
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion.
   Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition.
   Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation ABT-1.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

California Eastern Laboratories, Inc.
4590 Patrick Henry Drive, Santa Clara, California 95054-1817, U.S.A.
Tel: +1-408-919-2500, Fax: +1-408-988-0279

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.1