RX130 Group

Renesas MCUs

R01DS0273EJ0300
Rev.3.00
Aug 09, 2018

32-MHz, 32-bit RX MCUs, 50 DMIPS, up to 512-KB flash memory, up to 36 pins capacitive touch sensing unit, up to 6 comms channels, 12-bit A/D, D/A, RTC, IEC60730 compliance, 1.8-V to 5.5-V single supply

Features

■ 32-bit RX CPU core

- Max. operating frequency: 32 MHz
  Capable of 50 DMIPS in operation at 32 MHz
- Accumulator handles 64-bit results (for a single instruction) from 32-bit × 32-bit operations
- Multiplication and division unit handles 32-bit × 32-bit operations (multiplication instructions take one CPU clock cycle)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit

■ Low power design and architecture

- Operation from a single 1.8-V to 5.5-V supply
- Three low power consumption modes
- Low power timer (LPT) that operates during the software standby state
- Supply current
  High-speed operating mode: 96 µA/MHz
  Supply current in software standby mode: 0.37 µA
- Recovery time from software standby mode: 4.8 µs

■ On-chip flash memory for code, no wait states

- 64 K/128 K/256 K/383 K/512 Kbytes
- Operation at 32 MHz, read cycle of 31.25 ns
- No wait states for reading at full CPU speed
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory

- 8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states

- 10 K/16 K/32 K/48 Kbytes size capacities

■ DTC

- Four transfer modes
- Transfer can be set for each interrupt source.

■ ELC

- Module operation can be initiated by event signals without using interrupts.
- Linked operation between modules is possible while the CPU is sleeping.

■ Reset and supply management

- Eight types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- External clock input frequency: Up to 20 MHz
- Main clock oscillator frequency: 1 to 20 MHz
- Sub clock oscillator frequency: 32.768 kHz
- PLL circuit input: 4 MHz to 8 MHz
- Low-speed on-chip oscillator: 4 MHz
- High-speed on-chip oscillator: 32 MHz ± 1 %
- IWDT-dedicated on-chip oscillator: 15 kHz
- Generate a 32.768 kHz clock for the real-time clock
- On-chip clock frequency accuracy measurement circuit (CAC)

■ Realtime clock

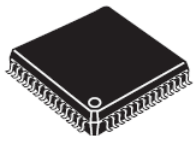
- Adjustment functions (30 seconds, leap year, and error)
- Calendar count mode or binary count mode selectable

■ Independent watchdog timer

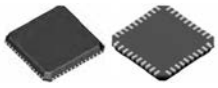
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance

- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.



PLQP0100KB-B 14 × 14mm, 0.5mm pitch
PLQP0080KB-B 12 × 12mm, 0.5mm pitch
PLQP0064GA-A 14 × 14mm, 0.8mm pitch
PLQP0064KB-C 10 × 10mm, 0.5mm pitch
PLQP0048KB-B 7 × 7mm, 0.5mm pitch



PWQN0048KB-A 7 × 7mm, 0.5mm pitch

■ MPC

- Input/output functions selectable from multiple pins

■ Up to 6 communication functions

- SCI with many useful functions (up to 4 channels)
  Asynchronous mode (Fine adjustable baud rate: 0 to 255/255), clock synchronous mode, smart card interface mode
- I^2C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPI (one channel): Transfer at up to 16 Mbps

■ Remote control signal reception

- Two units integrated
- Four pattern waveform matching supported

■ Up to 12 extended-function timersMPC

- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (two channels)

■ 12-bit A/D converter

- Capable of conversion within 1.4 µs
- 17 channels
- Sampling time can be set for each channel
- Conversion results compare features
- Self-diagnostic function and analog input disconnection detection assistance function
- Double trigger (data duplication) function for motor control

■ D/A converter

- Two channels

■ Capacitive touch sensing unit

- Self-capacitance method: A single pin configures a single key, supporting up to 36 keys
- Mutual capacitance method: Matrix configuration with 36pins, supporting up to 324 keys

■ Comparator B

- Two channels

■ General I/O ports

- 5-V tolerant, open drain, input pull-up, switching of driving capacity

■ Temperature sensor

■ Unique ID

- 32-byte ID code for the MCU

■ Operating temperature range

- –40 to +85°C
- –40 to +105°C

■ Applications

- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages in the RX130 Group.

Table 1.1 Outline of Specifications (1/3)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit registers • Basic instructions: 73 (variable-length instruction format) • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits
Memory	ROM	• Capacity: 64 K/128 K/256 K/383 K/512 Kbytes • No-wait memory access • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 10 K/16 K/32 K/48 Kbytes • No-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 32 MHz (at max.) Peripheral modules run in synchronization with the PCLKB: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.) • The ICLK frequency can only be set to FCLK, PCLKB, or PCLKD multiplied by n (n: 1,2,4,8,16,32,64)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 14 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 115 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (The NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority

Table 1.1 Outline of Specifications (2/3)

Classification	Module/Function	Description
DMA	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	100-pin /80-pin /64-pin /48-pin • I/O: 88/68/52/38 • Input: 1/1/1/1 • Pull-up resistors: 88/68/52/38 • Open-drain outputs: 67/47/35/26 • 5-V tolerance: 4/4/2/2
Event link controller (ELC)		• Event signals of 47 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 1 unit • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCc)*1	• Clock source: Sub-clock • Calendar count mode or binary count mode selectable • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt
	Low power timer (LPT)	• 16 bits × 1 channel • Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIg, SCIh)	• 7 channels (channel 0, 1, 5, 6, 8, 9: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Event linking by the ELC (only on channel 5) • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Communication functions	Serial peripheral interface (RSPIa)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	Remote control signal receiver (REMC)	• 2 channels • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLK, sub-clock, HOCO, IWDTCLK, and TMR.
12-bit A/D converter (S12ADE)		• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.4 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Conversion results compare features • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
D/A converter (DA)		• 2 channels • 8-bit resolution • Output voltage: 0V to AVCC0
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSUa)		Detection pin: 36 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 32 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 80-pin LFQFP (PLQP0080KB-B) 12 × 12 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch
Debugging interfaces		FINE interface

Note 1. When the realtime clock is not to be used, refer to section 24.5.7, Initialization Procedure When the Realtime Clock is Not to be Used.

Table 1.2 Comparison of Functions for Different Packages in the RX130 Group

Module/Functions		RX130 Group			
		100 Pins	80 Pins	64 Pins	48 Pins
Interrupts	External interrupts	NMI, IRQ0 to IRQ7		NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7
DMA	Data transfer controller	Available			
Timers	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)			
	Port output enable 2	POE0# to POE3#, POE8#			
	8-bit timer	2 channels × 2 units			
	Compare match timer	2 channels × 1 unit			
	Low power timer	1 channel			
	Realtime clock	Available			Not supported
	Independent watchdog timer	Available			
Communication functions	Serial communications interfaces (SCIg)	6 channels (SCI0, 1, 5, 6, 8, 9)	3 channels (SCI1, 5, 6)		
	Serial communications interfaces (SCIh)	1 channel (SCI12)			
	I²C bus interface	1 channel			
	Serial peripheral interface	1 channel			
	Remote control signal receiver (REMC)	2 channels	Not supported		
Capacitive touch sensing unit		36 channels	36 channels	32 channels	24 channels
12-bit A/D converter		24 channels	17 channels	14 channels	10 channels
Temperature sensor		Available			
D/A converter		2 channels			Not supported
CRC calculator		Available			
Event link controller		Available			
Comparator B		2 channels			
Packages		100-pin LFQFP (0.5 mm)	80-pin LFQFP (0.5 mm)	64-pin LQFP (0.8 mm) 64-pin LFQFP (0.5 mm)	48-pin LFQFP (0.5 mm) 48-pin HWQFN (0.5 mm)

1.2 List of Products

Table 1.3 is a lists of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX130	R5F51308ADFP	R5F51308ADFP#30	PLQP0100KB-B	512 Kbytes	48 Kbytes	8 Kbytes	32 MHz	–40 to +85°C
	R5F51308ADFN	R5F51308ADFN#30	PLQP0080KB-B					
	R5F51308ADFM	R5F51308ADFM#30	PLQP0064KB-C					
	R5F51308ADFK	R5F51308ADFK#30	PLQP0064GA-A					
	R5F51308ADFL	R5F51308ADFL#30	PLQP0048KB-B					
	R5F51308ADNE	R5F51308ADNE#U0	PWQN0048KB-A					
	R5F51307ADFP	R5F51307ADFP#30	PLQP0100KB-B	384 Kbytes				
	R5F51307ADFN	R5F51307ADFN#30	PLQP0080KB-B					
	R5F51307ADFM	R5F51307ADFM#30	PLQP0064KB-C					
	R5F51307ADFK	R5F51307ADFK#30	PLQP0064GA-A					
	R5F51307ADFL	R5F51307ADFL#30	PLQP0048KB-B					
	R5F51307ADNE	R5F51307ADNE#U0	PWQN0048KB-A					
	R5F51306BDFP*1	R5F51306BDFP#30*1	PLQP0100KB-B	256 Kbytes	32 Kbytes			
	R5F51306BDFN*1	R5F51306BDFN#30*1	PLQP0080KB-B					
	R5F51306BDFM*1	R5F51306BDFM#30*1	PLQP0064KB-C					
	R5F51306BDFK*1	R5F51306BDFK#30*1	PLQP0064GA-A					
	R5F51306BDFL*1	R5F51306BDFL#30*1	PLQP0048KB-B					
	R5F51306BDNE*1	R5F51306BDNE#U0*1	PWQN0048KB-A					
	R5F51305BDFP*1	R5F51305BDFP#30*1	PLQP0100KB-B	128 Kbytes	16 Kbytes			
	R5F51305ADFN	R5F51305ADFN#30	PLQP0080KB-B					
	R5F51305ADFM	R5F51305ADFM#30	PLQP0064KB-C					
	R5F51305ADFK	R5F51305ADFK#30	PLQP0064GA-A					
	R5F51305ADFL	R5F51305ADFL#30	PLQP0048KB-B					
	R5F51305ADNE	R5F51305ADNE#U0	PWQN0048KB-A					
	R5F51303ADFN	R5F51303ADFN#30	PLQP0080KB-B	64 Kbytes	10 Kbytes			
	R5F51303ADFM	R5F51303ADFM#30	PLQP0064KB-C					
	R5F51303ADFK	R5F51303ADFK#30	PLQP0064GA-A					
	R5F51303ADFL	R5F51303ADFL#30	PLQP0048KB-B					
	R5F51303ADNE	R5F51303ADNE#U0	PWQN0048KB-A					

Table 1.3 List of Products (2/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX130	R5F51308AGFP	R5F51308AGFP#30	PLQP0100KB-B	512 Kbytes	48 Kbytes	8 Kbytes	32 MHz	–40 to +105°C
	R5F51308AGFN	R5F51308AGFN#30	PLQP0080KB-B					
	R5F51308AGFM	R5F51308AGFM#30	PLQP0064KB-C					
	R5F51308AGFK	R5F51308AGFK#30	PLQP0064GA-A					
	R5F51308AGFL	R5F51308AGFL#30	PLQP0048KB-B					
	R5F51308AGNE	R5F51308AGNE#U0	PWQN0048KB-A					
	R5F51307AGFP	R5F51307AGFP#30	PLQP0100KB-B	384 Kbytes				
	R5F51307AGFN	R5F51307AGFN#30	PLQP0080KB-B					
	R5F51307AGFM	R5F51307AGFM#30	PLQP0064KB-C					
	R5F51307AGFK	R5F51307AGFK#30	PLQP0064GA-A					
	R5F51307AGFL	R5F51307AGFL#30	PLQP0048KB-B					
	R5F51307AGNE	R5F51307AGNE#U0	PWQN0048KB-A					
	R5F51306BGFP*1	R5F51306BGFP#30*1	PLQP0100KB-B	256 Kbytes	32 Kbytes			
	R5F51306BGFN*1	R5F51306BGFN#30*1	PLQP0080KB-B					
	R5F51306BGFM*1	R5F51306BGFM#30*1	PLQP0064KB-C					
	R5F51306BGFK*1	R5F51306BGFK#30*1	PLQP0064GA-A					
	R5F51306BGFL*1	R5F51306BGFL#30*1	PLQP0048KB-B					
	R5F51306BGNE*1	R5F51306BGNE#U0*1	PWQN0048KB-A					
	R5F51305BGFP*1	R5F51305BGFP#30*1	PLQP0100KB-B	128 Kbytes	16 Kbytes			
	R5F51305AGFN	R5F51305AGFN#30	PLQP0080KB-B					
	R5F51305AGFM	R5F51305AGFM#30	PLQP0064KB-C					
	R5F51305AGFK	R5F51305AGFK#30	PLQP0064GA-A					
	R5F51305AGFL	R5F51305AGFL#30	PLQP0048KB-B					
	R5F51305AGNE	R5F51305AGNE#U0	PWQN0048KB-A					
	R5F51303AGFN	R5F51303AGFN#30	PLQP0080KB-B	64 Kbytes	10 Kbytes			
	R5F51303AGFM	R5F51303AGFM#30	PLQP0064KB-C					
	R5F51303AGFK	R5F51303AGFK#30	PLQP0064GA-A					
	R5F51303AGFL	R5F51303AGFL#30	PLQP0048KB-B					
	R5F51303AGNE	R5F51303AGNE#U0	PWQN0048KB-A					

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.

Note 1. The chip version portion of the part number of this product has been changed to B from A. There are no differences between the specifications of chip versions A and B. We are not accepting new orders for chip version A.

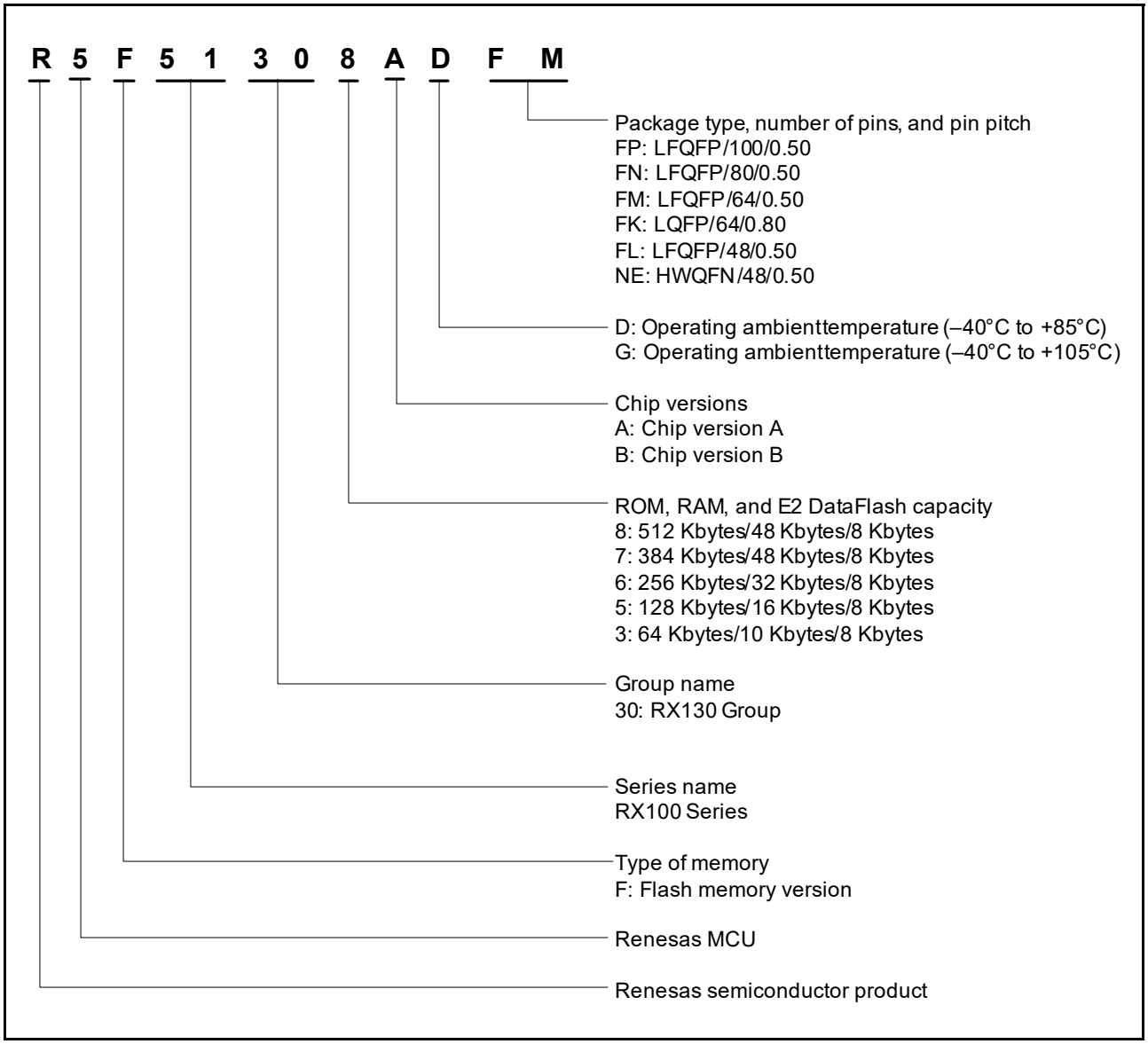


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

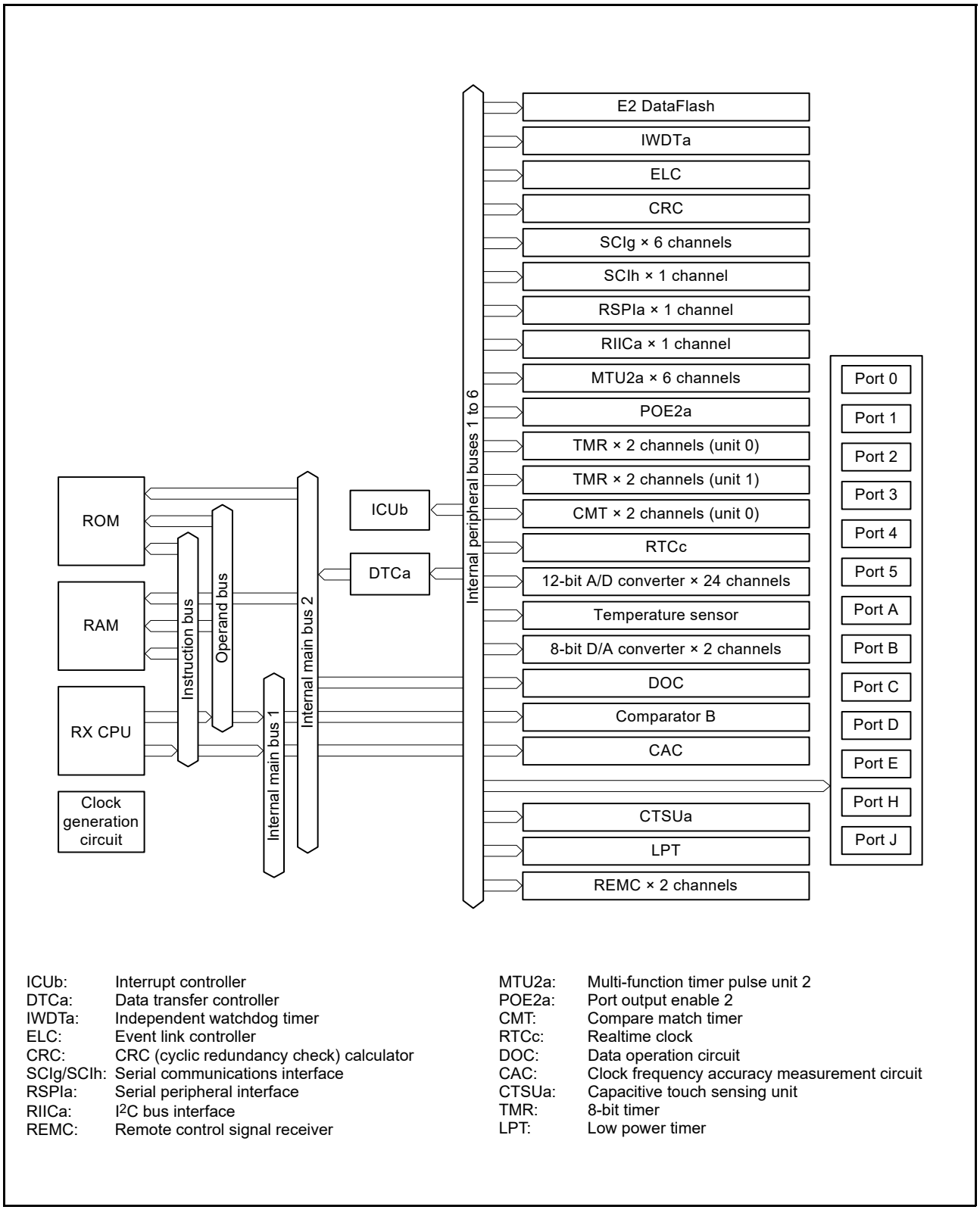


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.

Table 1.4 Pin Functions (2/3)

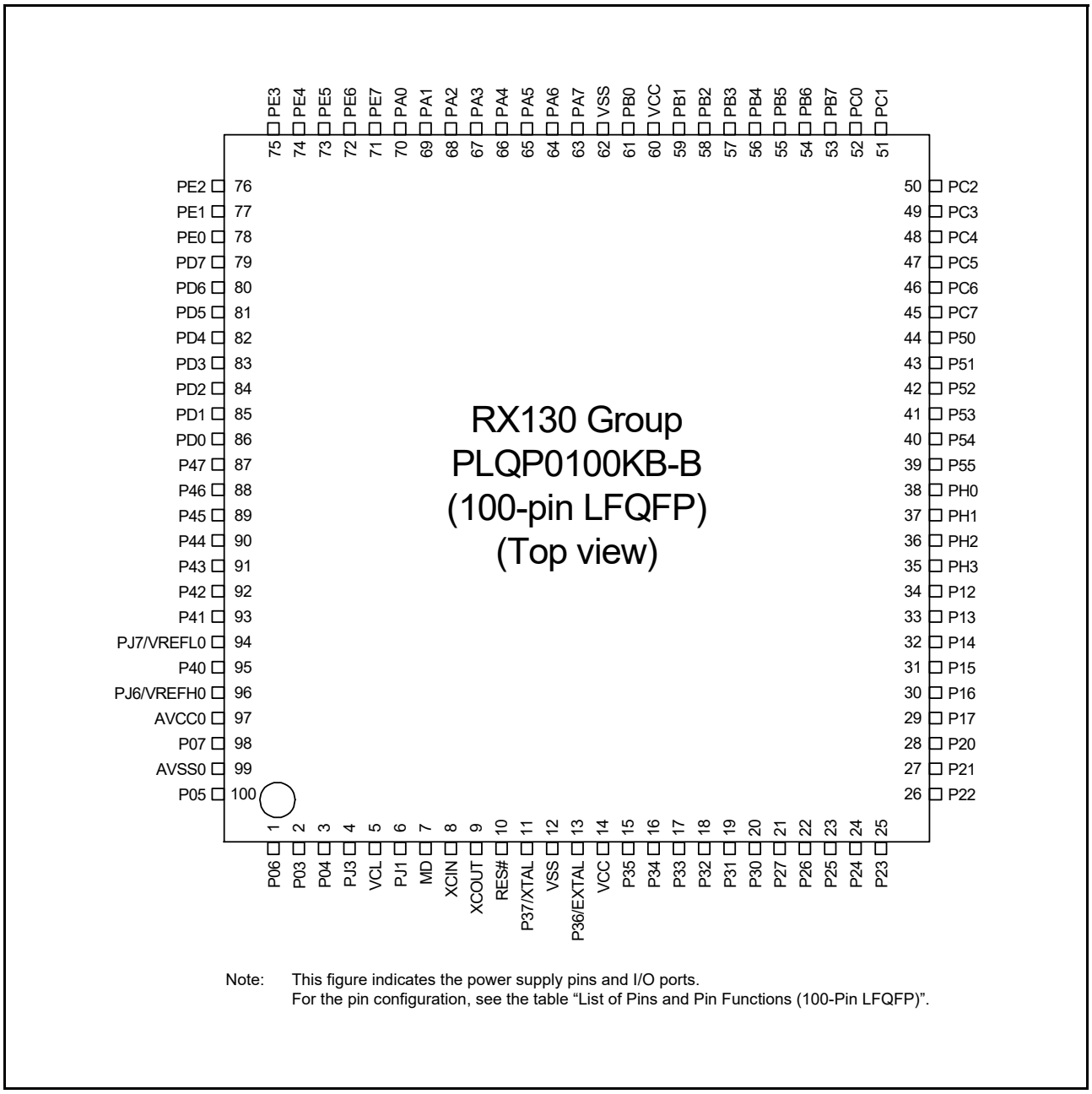
Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock.
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	SMISO0, SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS5#, SS6#, SS8#, SS9#	Input	Slave-select input pins.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock.
	SSDA12	I/O	Input/output pin for the I^2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
I^2C bus interface	SCL0	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
Remote control signal receiver (REMC)	PMC0	Input	Input pin for external pulse signal
	PMC1	Input	Input pin for external pulse signal
12-bit A/D converter	AN000 to AN007, AN016 to AN031	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB0, CMPB1	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB0, CVREFB1	Input	Analog reference voltage supply pin for comparator B.
	CMPOB0, CMPOB1	Output	Output pin for comparator B.
CTSU	TS0 to TS35	I/O	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	—	Connect to the VSS via a decoupling capacitor (10 nF) for stabilizing the internal voltage
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
I/O ports	P03 to P07	I/O	5-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3, PJ6, PJ7	I/O	4-bit input/output pins.

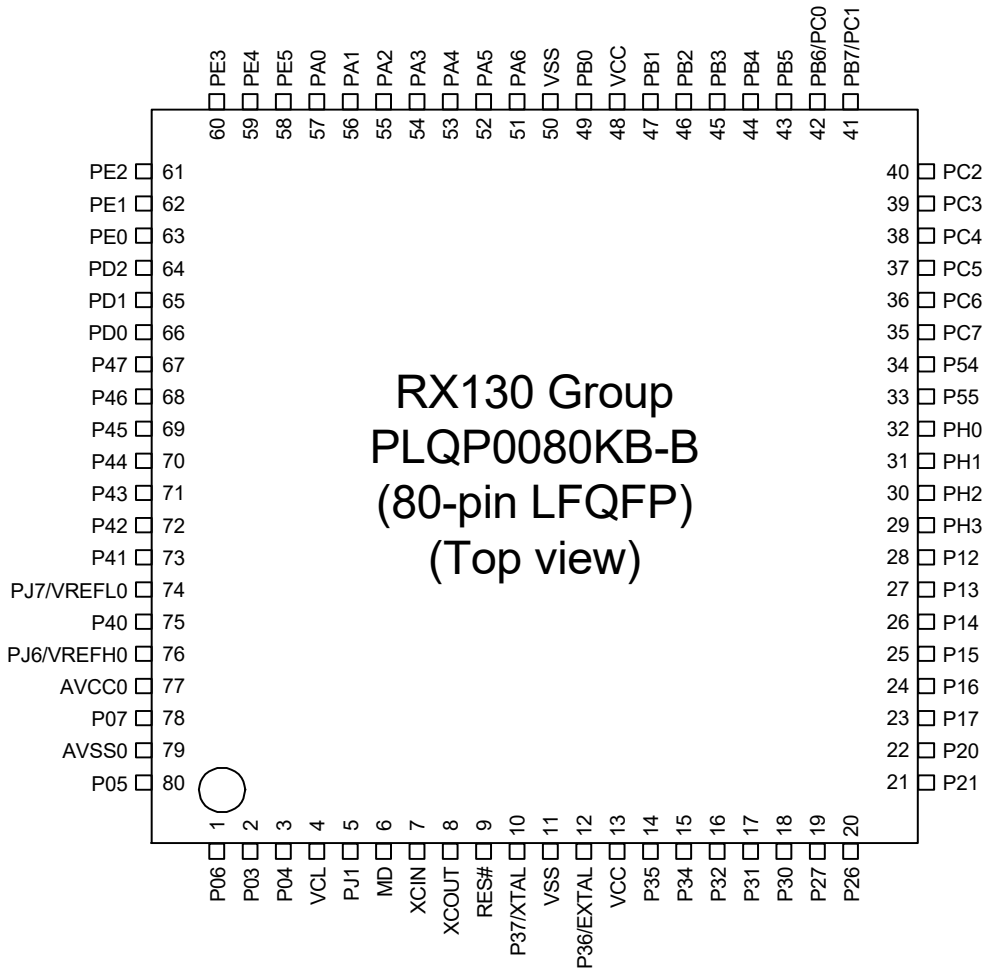
1.5 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments. Table 1.5 to Table 1.8 show the lists of pins and pin functions.



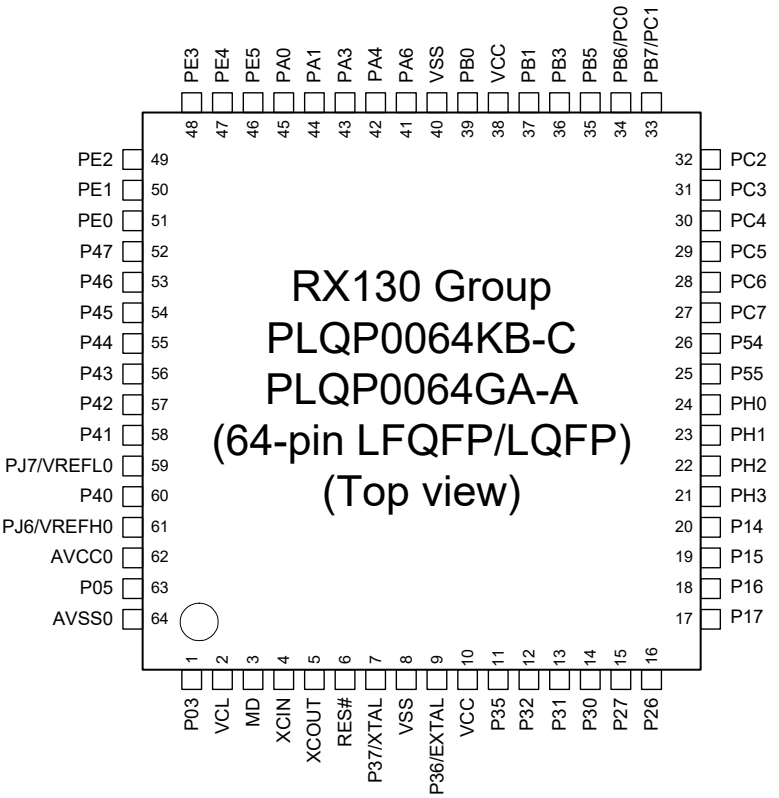
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LFQFP)”.

Figure 1.3 Pin Assignments of the 100-Pin LFQFP



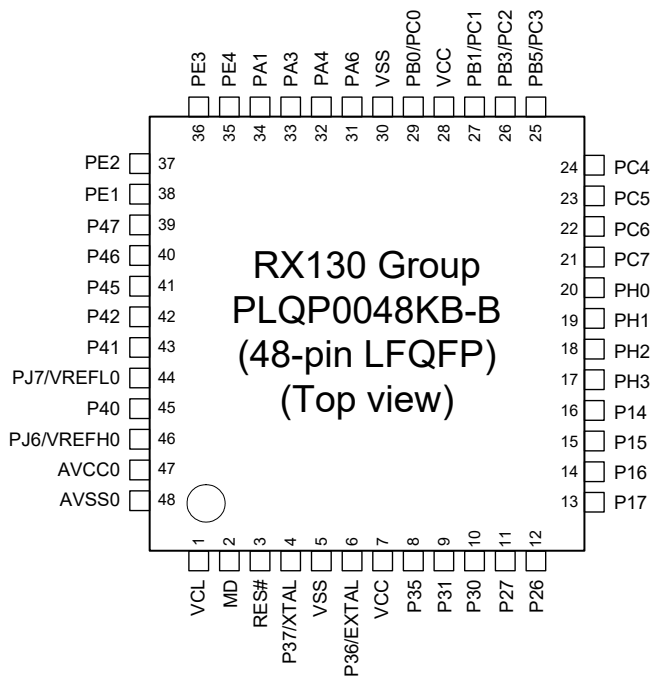
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LFQFP)”.

Figure 1.4 Pin Assignments of the 80-Pin LFQFP



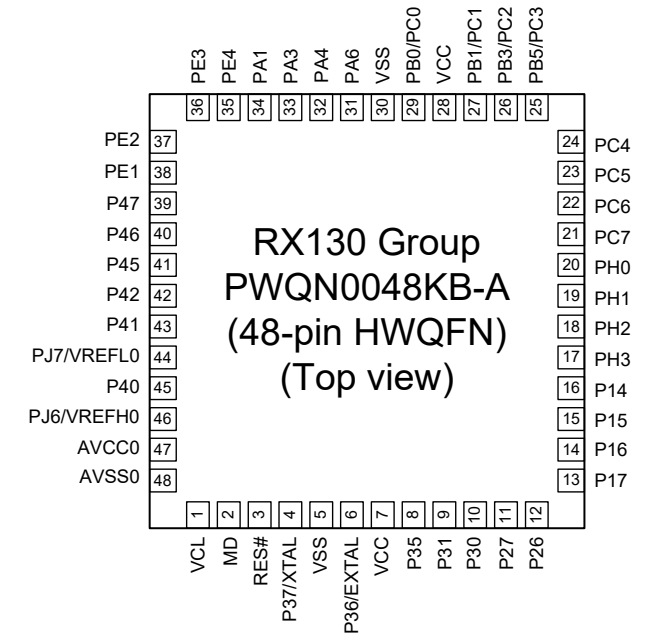
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/LQFP)”.

Figure 1.5 Pin Assignments of the 64-Pin LFQFP/LQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/ HWQFN)”.

Figure 1.6 Pin Assignments of the 48-Pin LQFP



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/ HWQFN)”.

Figure 1.7 Pin Assignments of the 48-Pin HWQFN

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC, REMC)	Touch sensing	Others
1		P06*1				
2		P03*1				DA0
3		P04*1				
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#		
5	VCL					
6		PJ1	MTIOC3A			
7	MD					FINED
8	XCIN					
9	XCOUT					
10	RES#					
11	XTAL	P37				
12	VSS					
13	EXTAL	P36				
14	VCC					
15		P35				NMI
16		P34	MTIOC0A/TMCI3/POE2#	SCK6		IRQ4
17		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6		IRQ3
18		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
19		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
20		P30	MTIOC4B/POE8#/TMRI3	RXD1/SMISO1/SSCL1	TS2	IRQ0
21		P27	MTIOC2B/TMCI3	SCK1	TS3	
22		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
23		P25	MTIOC4C/MTCLKB			ADTRG0#
24		P24	MTIOC4A/MTCLKA/TMRI1			
25		P23	MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#		
26		P22	MTIOC3B/MTCLKC/TMO0	SCK0		
27		P21	MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0		
28		P20	MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0		
29	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0		IRQ7
30	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL0		IRQ6/RTCOUT/ ADTRG0#
31		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
32		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
33	(5V tolerant)	P13	MTIOC0B/TMO3	SDA0		IRQ3
34	(5V tolerant)	P12	TMCI1	SCL0		IRQ2
35		PH3	TMCI0		TS7	
36		PH2	TMRI0		TS8	IRQ1
37		PH1	TMO0		TS9	IRQ0
38		PH0			TS10	CACREF
39		P55	MTIOC4D/TMO3		TS11	
40		P54	MTIOC4B/TMCI1		TS12	
41		P53				
42		P52		PMC1		
43		P51		PMC0		
44		P50				
45		PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA	TS13	CACREF
46		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	TS14	
47		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	TS15	
48		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	TSCAP	
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
51		PC1	MTIOC3A	SCK5/SSLA2		
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1		

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC, REMC)	Touch sensing	Others
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	TS18	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	TS19	
55		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	TS20	
56		PB4		CTS9#/RTS9#/SS9#	TS21	
57		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
58		PB2		CTS6#/RTS6#/SS6#	TS23	
59		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
60	VCC					
61		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	
62	VSS					
63		PA7		MISOA		
64		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
65		PA5		RSPCKA	TS27	
66		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
67		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
68		PA2		RXD5/SMISO5/SSCL5/SSLA3	TS30	
69		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
70		PA0	MTIOC4A	SSLA1	TS32	CACREF
71		PE7				IRQ7/AN023
72		PE6				IRQ6/AN022
73		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
74		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/ CLKOUT
75		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT
76		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
77		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
78		PE0		SCK12		AN016
79		PD7	MTIC5U/POE0#			IRQ7/AN031
80		PD6	MTIC5V/POE1#			IRQ6/AN030
81		PD5	MTIC5W/POE2#			IRQ5/AN029
82		PD4	POE3#			IRQ4/AN028
83		PD3	POE8#			IRQ3/AN027
84		PD2	MTIOC4D	SCK6		IRQ2/AN026
85		PD1	MTIOC4B	RXD6/SMISO6/SSCL6		IRQ1/AN025
86		PD0		TXD6/SMOSI6/SSDA6		IRQ0/AN024
87		P47*1				AN007
88		P46*1				AN006
89		P45*1				AN005
90		P44*1				AN004
91		P43*1				AN003
92		P42*1				AN002
93		P41*1				AN001
94	VREFL0	PJ7*1				
95		P40*1				AN000
96	VREFH0	PJ6*1				
97	AVCC0					
98		P07*1				ADTRG0#
99	AVSS0					
100		P05*1				DA1

Note 1. The power source of the I/O buffer for these pins is AVCC0.

Table 1.6 List of Pins and Pin Functions (80-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
1		P06*1				
2		P03*1				DA0
3		P04*1				
4	VCL					
5		PJ1	MTIOC3A			
6	MD					FINED
7	XCIN					
8	XCOUT					
9	RES#					
10	XTAL	P37				
11	VSS					
12	EXTAL	P36				
13	VCC					
14		P35				NMI
15		P34	MTIOC0A/TMCI3/POE2#	SCK6		IRQ4
16		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
17		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
18		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2	IRQ0
19		P27	MTIOC2B/TMCI3	SCK1	TS3	
20		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
21		P21	MTIOC1B/TMCI0			
22		P20	MTIOC1A/TMRI0			
23	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0		IRQ7
24	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL0		IRQ6/RTCOUT/ ADTRG0#
25		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
26		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
27	(5V tolerant)	P13	MTIOC0B/TMO3	SDA0		IRQ3
28	(5V tolerant)	P12	TMCI1	SCL0		IRQ2
29		PH3	TMCI0		TS7	
30		PH2	TMRI0		TS8	IRQ1
31		PH1	TMO0		TS9	IRQ0
32		PH0			TS10	CACREF
33		P55	MTIOC4D/TMO3		TS11	
34		P54	MTIOC4B/TMCI1		TS12	
35		PC7	MTIOC3A/TMO2/MTCLKB	MISOA	TS13	CACREF
36		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	TS14	
37		PC5	MTIOC3B/MTCLKD/TMRI2	RSPCKA	TS15	
38		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	TSCAP	
39		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
40		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
41		PB7/ PC1*2	MTIOC3B		TS18	
42		PB6/ PC0*2	MTIOC3D		TS19	
43		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#		TS20	
44		PB4			TS21	
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
46		PB2		CTS6#/RTS6#/SS6#	TS23	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
48	VCC					
49		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	

Table 1.6 List of Pins and Pin Functions (80-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
50	VSS					
51		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
52		PA5		RSPCKA	TS27	
53		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
54		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
55		PA2		RXD5/SMISO5/SSCL5/SSLA3	TS30	
56		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
57		PA0	MTIOC4A	SSLA1	TS32	CACREF
58		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
59		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/ CLKOUT
60		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT
61		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
62		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
63		PE0		SCK12		AN016
64		PD2	MTIOC4D	SCK6		IRQ2/AN026
65		PD1	MTIOC4B	RXD6/SMISO6/SSCL6		IRQ1/AN025
66		PD0		TXD6/SMOSI6/SSDA6		IRQ0/AN024
67		P47*1				AN007
68		P46*1				AN006
69		P45*1				AN005
70		P44*1				AN004
71		P43*1				AN003
72		P42*1				AN002
73		P41*1				AN001
74	VREFL0	PJ7*1				
75		P40*1				AN000
76	VREFH0	PJ6*1				
77	AVCC0					
78		P07*1				ADTRG0#
79	AVSS0					
80		P05*1				DA1

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. PC0 and PC1 are valid only when the port switching function is selected.

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
1		P03*1				DA0
2	VCL					
3	MD					FINED
4	XCIN					
5	XCOUT					
6	RES#					
7	XTAL	P37				
8	VSS					
9	EXTAL	P36				
10	VCC					
11		P35				NMI
12		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
13		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
14		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2	IRQ0
15		P27	MTIOC2B/TMCI3	SCK1	TS3	
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
17	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0		IRQ7
18	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL0		IRQ6/RTCOUT/ ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
20		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
21		PH3	TMCI0		TS7	
22		PH2	TMRI0		TS8	IRQ1
23		PH1	TMO0		TS9	IRQ0
24		PH0			TS10	CACREF
25		P55	MTIOC4D/TMO3		TS11	
26		P54	MTIOC4B/TMCI1		TS12	
27		PC7	MTIOC3A/TMO2/MTCLKB	MISOA	TS13	CACREF
28		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	TS14	
29		PC5	MTIOC3B/MTCLKD/TMRI2	RSPCKA	TS15	
30		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	TSCAP	
31		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
32		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
33		PB7/ PC1*2	MTIOC3B		TS18	
34		PB6/ PC0*2	MTIOC3D		TS19	
35		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#		TS20	
36		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
37		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
38	VCC					
39		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	
40	VSS					
41		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
42		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
43		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
45		PA0	MTIOC4A	SSLA1	TS32	CACREF
46		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
47		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/ CLKOUT
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
51		PE0		SCK12		AN016
52		P47*1				AN007
53		P46*1				AN006
54		P45*1				AN005
55		P44*1				AN004
56		P43*1				AN003
57		P42*1				AN002
58		P41*1				AN001
59	VREFL0	PJ7*1				
60		P40*1				AN000
61	VREFH0	PJ6*1				
62	AVCC0					
63		P05*1				DA1
64	AVSS0					

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. PC0 and PC1 are valid only when the port switching function is selected.

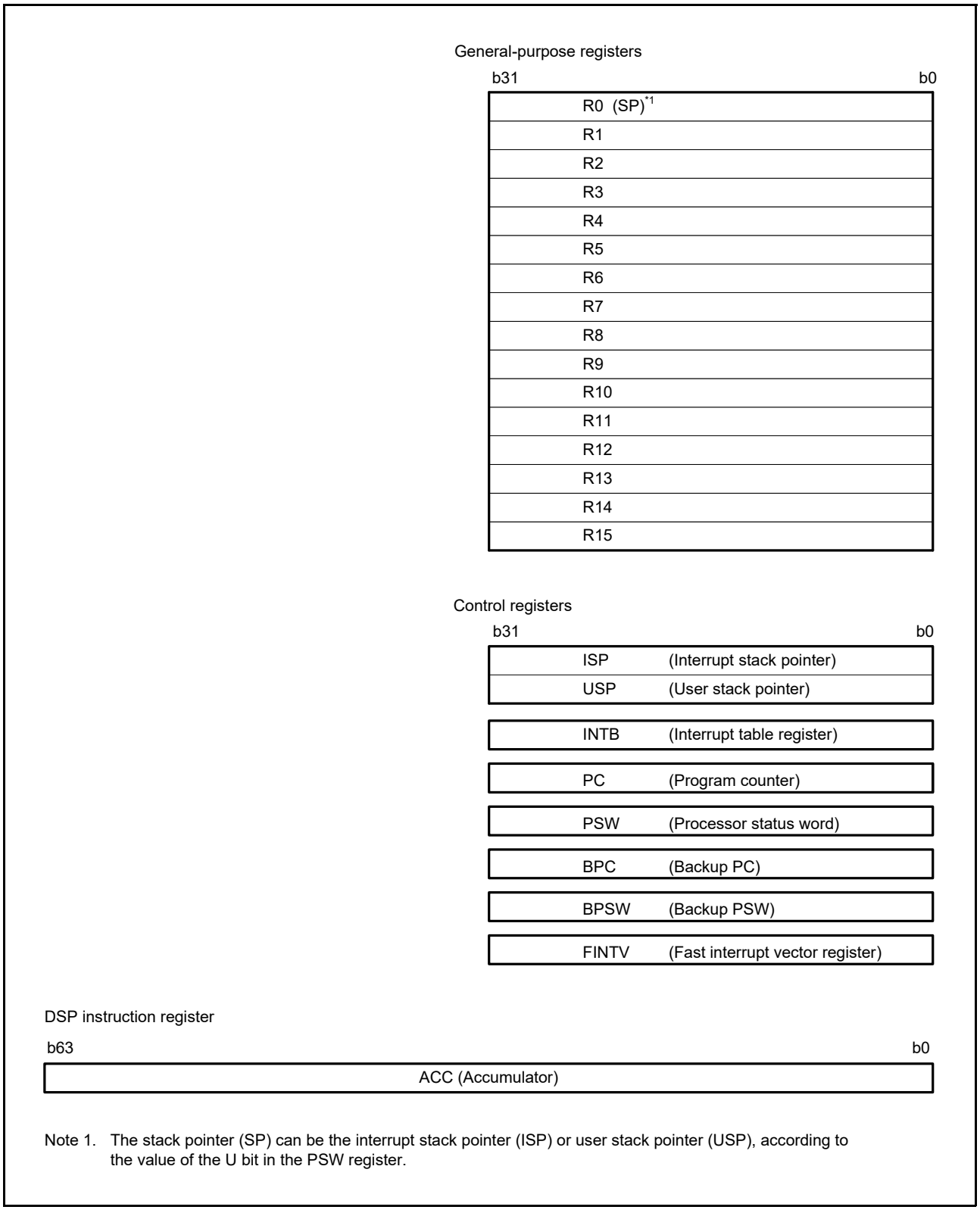
Table 1.8 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
1	VCL					
2	MD					FINED
3	RES#					
4	XTAL	P37				
5	VSS					
6	EXTAL	P36				
7	VCC					
8		P35				NMI
9		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
10		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2	IRQ0
11		P27	MTIOC2B/TMCI3	SCK1	TS3	
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
13	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0		IRQ7
14	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0		IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
16		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
17		PH3	TMCI0		TS7	
18		PH2	TMRI0		TS8	IRQ1
19		PH1	TMO0		TS9	IRQ0
20		PH0			TS10	CACREF
21		PC7	MTIOC3A/TMO2/MTCLKB	MISOA	TS13	CACREF
22		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	TS14	
23		PC5	MTIOC3B/MTCLKD/TMRI2	RSPCKA	TS15	
24		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	TSCAP	
25		PB5/PC3*1	MTIOC2A/MTIOC1B/TMRI1/ POE1#		TS20	
26		PB3/PC2*1	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
27		PB1/PC1*1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
28	VCC					
29		PB0/PC0*1	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	
30	VSS					
31		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
32		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
33		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
34		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
35		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/ CLKOUT
36		PE3	MTIOC4B/POE8#	CTS12#/RTS12#	TS34	AN019/CLKOUT
37		PE2	MTIOC4A	RXD12/RXDX12/SSCL12	TS35	IRQ7/AN018/CVREFB0
38		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SSDA12		AN017/CMPB0
39		P47*2				AN007
40		P46*2				AN006
41		P45*2				AN005
42		P42*2				AN002
43		P41*2				AN001
44	VREFL0	PJ7*2				
45		P40*2				AN000
46	VREFH0	PJ6*2				
47	AVCC0					
48	AVSS0					

Note 1. PC0 to PC3 are valid only when the port switching function is selected.
Note 2. The power source of the I/O buffer for these pins is AVCC0.

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has 16 general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

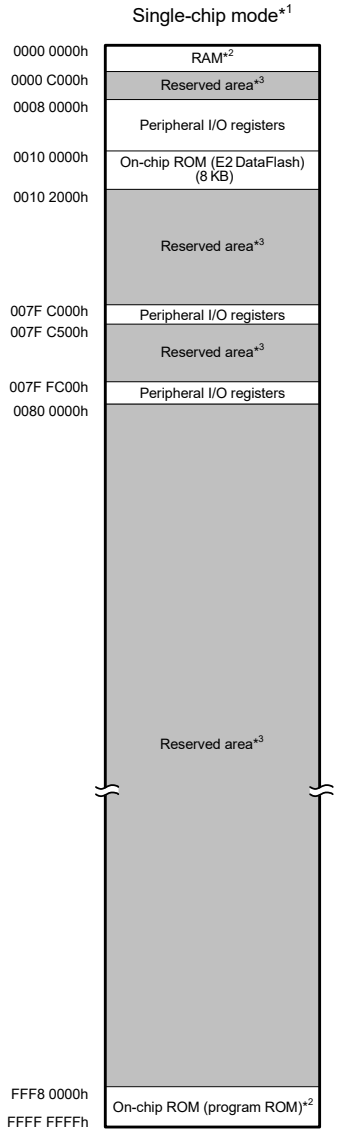
(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps.



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 Kbytes	FFF8 0000h to FFFF FFFFh	48 Kbytes	0000 0000h to 0000 BFFFh
384 Kbytes	FFFA 8000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh	16 Kbytes	0000 0000h to 0000 3FFFh
64 Kbytes	FFFF 0000h to FFFF FFFFh	10 Kbytes	0000 0000h to 0000 27FFh

Note: See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral buses 1 to 3, and 6

The number of bus cycles of internal peripheral buses 1 to 3, and 6 differs according to the register to be accessed.
When the registers for peripheral functions connected to internal peripheral buses 2, 3, and 6 (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(5) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 003Dh	SYSTEM	High-Speed On-Chip Oscillator Forced Oscillation Control Register	HOFCR	8	8	3 ICLK
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 0060h	SYSTEM	Low-Speed On-Chip Oscillator Trimming Register	LOCOTRR	8	8	3 ICLK
0008 0064h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Trimming Register	ILOCOTRR	8	8	3 ICLK
0008 0068h	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 0	HOCOTRR0	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK
0008 00B0h	LPT	Low-Power Timer Control Register 1	LPTCR1	8	8	3 ICLK
0008 00B1h	LPT	Low-Power Timer Control Register 2	LPTCR2	8	8	3 ICLK
0008 00B2h	LPT	Low-Power Timer Control Register 3	LPTCR3	8	8	3 ICLK
0008 00B4h	LPT	Low-Power Timer Cycle Setting Register	LPTPRD	16	16	3 ICLK
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK
0008 00BCh	LPT	Low-Power Timer Standby Wakeup Enable Register	LPWUCR	16	16	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (2 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 7010h to 0008 70FFh	ICU	Interrupt Request Register 016 to 255	IRn	8	8	2 ICLK
0008 711Bh to 0008 71FFh	ICU	DTC Activation Enable Register 027 to 255	DTCERn	8	8	2 ICLK
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Register 02 to 1F	IERm	8	8	2 ICLK
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Register 000 to 255	IPRn	8	8	2 ICLK
0008 7500h to 0008 7507h	ICU	IRQ Control Register 0 to 7	IRQCRi	8	8	2 ICLK
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 or 3 PCLKB
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2 or 3 PCLKB
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2 or 3 PCLKB
0008 80C4h	DA	D/A Control Register	DACR	8	8	2 or 3 PCLKB
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2 or 3 PCLKB
0008 80C6h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2 or 3 PCLKB
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8204h	TMR01	Time Constant Register A	TCORA	16	16	2 or 3 PCLKB
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8206h	TMR01	Time Constant Register B	TCORB	16	16	2 or 3 PCLKB
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8208h	TMR01	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8209h	TMR1	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Ah	TMR01	Timer Counter Control Register	TCCR	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (3 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Ch	TMR0	Timer Counter Start Register	TCSTR	8	8	2 or 3 PCLKB
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8214h	TMR23	Time Constant Register A	TCORA	16	16	2 or 3 PCLKB
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8216h	TMR23	Time Constant Register B	TCORB	16	16	2 or 3 PCLKB
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8218h	TMR23	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8219h	TMR3	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Ah	TMR23	Timer Counter Control Register	TCCR	16	16	2 or 3 PCLKB
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Ch	TMR2	Timer Counter Start Register	TCSTR	8	8	2 or 3 PCLKB
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB
0008 8300h	RIIC0	I^2C Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB
0008 8301h	RIIC0	I^2C Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB
0008 8302h	RIIC0	I^2C Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB
0008 8303h	RIIC0	I^2C Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB
0008 8304h	RIIC0	I^2C Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I^2C Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I^2C Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I^2C Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I^2C Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I^2C Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB
0008 8310h	RIIC0	I^2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB
0008 8311h	RIIC0	I^2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB
0008 8312h	RIIC0	I^2C Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB
0008 8313h	RIIC0	I^2C Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB/2 ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (4 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 8600h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8601h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8602h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8603h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8604h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8605h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8606h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8607h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8608h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8609h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 860Ah	MTU	Timer Output Master Enable Registers	TOER	8	8	2 or 3 PCLKB
0008 860Dh	MTU	Timer Gate Control Registers	TGCR	8	8	2 or 3 PCLKB
0008 860Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKB
0008 860Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKB
0008 8610h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8612h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8614h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKB
0008 8616h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKB
0008 8618h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 861Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8620h	MTU	Timer Subcounter	TCNTS	16	16	2 or 3 PCLKB
0008 8622h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKB
0008 8624h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 8626h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8628h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 862Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 862Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 862Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8630h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKB
0008 8631h	MTU	Timer Interrupt Skipping Counter	TITCNT	8	8	2 or 3 PCLKB
0008 8632h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKB
0008 8634h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKB
0008 8636h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKB
0008 8638h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8639h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8640h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKB
0008 8644h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKB
0008 8646h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKB
0008 8648h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (5 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 864Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	2 or 3 PCLKB
0008 8660h	MTU	Timer Waveform Control Register	TWCR	8	8, 16	2 or 3 PCLKB
0008 8680h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKB
0008 8681h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKB
0008 8684h	MTU	Timer Read/Write Enable Register	TRWER	8	8, 16	2 or 3 PCLKB
0008 8690h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8691h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8692h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8693h	MTU3	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8694h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8695h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8700h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8701h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8702h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8703h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8704h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8705h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8706h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8708h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 870Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 870Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 870Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8720h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKB
0008 8722h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKB
0008 8724h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKB
0008 8726h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8780h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8781h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8782h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8784h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8785h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8786h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8788h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 878Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8790h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKB
0008 8800h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8801h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8802h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8804h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8805h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8806h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8808h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 880Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8880h	MTU5	Timer Counter U	TCNTU	16	16	2 or 3 PCLKB
0008 8882h	MTU5	Timer General Register U	TGRU	16	16	2 or 3 PCLKB
0008 8884h	MTU5	Timer Control Register U	TCRU	8	8	2 or 3 PCLKB
0008 8886h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 or 3 PCLKB
0008 8890h	MTU5	Timer Counter V	TCNTV	16	16	2 or 3 PCLKB
0008 8892h	MTU5	Timer General Register V	TGRV	16	16	2 or 3 PCLKB
0008 8894h	MTU5	Timer Control Register V	TCRV	8	8	2 or 3 PCLKB
0008 8896h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 or 3 PCLKB
0008 88A0h	MTU5	Timer Counter W	TCNTW	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (6 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB
0008 904Ch	S12AD	A/D Data Register 22	ADDR22	16	16	2 or 3 PCLKB
0008 904Eh	S12AD	A/D Data Register 23	ADDR23	16	16	2 or 3 PCLKB
0008 9050h	S12AD	A/D Data Register 24	ADDR24	16	16	2 or 3 PCLKB
0008 9052h	S12AD	A/D Data Register 25	ADDR25	16	16	2 or 3 PCLKB
0008 9054h	S12AD	A/D Data Register 26	ADDR26	16	16	2 or 3 PCLKB
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB
0008 9058h	S12AD	A/D Data Register 28	ADDR28	16	16	2 or 3 PCLKB
0008 905Ah	S12AD	A/D Data Register 29	ADDR29	16	16	2 or 3 PCLKB
0008 905Ch	S12AD	A/D Data Register 30	ADDR30	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (7 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 905Eh	S12AD	A/D Data Register 31	ADDR31	16	16	2 or 3 PCLKB
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 908Ah	S12AD	A/D High-Potential/Low-Potential Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPANSER	8	8	2 or 3 PCLKB
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPANSR0	16	16	2 or 3 PCLKB
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPANSR1	16	16	2 or 3 PCLKB
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPDR0	16	16	2 or 3 PCLKB
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPDR1	16	16	2 or 3 PCLKB
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	8	8	2 or 3 PCLKB
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPBNSR	8	8	2 or 3 PCLKB
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB
0008 90AAh	S12AD	A/D Compare Function Window B Upper-Side Level Setting Register	ADWINULB	16	16	2 or 3 PCLKB
0008 90ACh	S12AD	A/D Compare Function Window B Status Register	ADCMPBSR	8	8	2 or 3 PCLKB
0008 90B0h	S12AD	A/D Data Storage Buffer Register 0	ADBUF0	16	16	2 or 3 PCLKB
0008 90B2h	S12AD	A/D Data Storage Buffer Register 1	ADBUF1	16	16	2 or 3 PCLKB
0008 90B4h	S12AD	A/D Data Storage Buffer Register 2	ADBUF2	16	16	2 or 3 PCLKB
0008 90B6h	S12AD	A/D Data Storage Buffer Register 3	ADBUF3	16	16	2 or 3 PCLKB
0008 90B8h	S12AD	A/D Data Storage Buffer Register 4	ADBUF4	16	16	2 or 3 PCLKB
0008 90BAh	S12AD	A/D Data Storage Buffer Register 5	ADBUF5	16	16	2 or 3 PCLKB
0008 90BCh	S12AD	A/D Data Storage Buffer Register 6	ADBUF6	16	16	2 or 3 PCLKB
0008 90BEh	S12AD	A/D Data Storage Buffer Register 7	ADBUF7	16	16	2 or 3 PCLKB
0008 90C0h	S12AD	A/D Data Storage Buffer Register 8	ADBUF8	16	16	2 or 3 PCLKB
0008 90C2h	S12AD	A/D Data Storage Buffer Register 9	ADBUF9	16	16	2 or 3 PCLKB
0008 90C4h	S12AD	A/D Data Storage Buffer Register 10	ADBUF10	16	16	2 or 3 PCLKB
0008 90C6h	S12AD	A/D Data Storage Buffer Register 11	ADBUF11	16	16	2 or 3 PCLKB
0008 90C8h	S12AD	A/D Data Storage Buffer Register 12	ADBUF12	16	16	2 or 3 PCLKB
0008 90CAh	S12AD	A/D Data Storage Buffer Register 13	ADBUF13	16	16	2 or 3 PCLKB
0008 90CCh	S12AD	A/D Data Storage Buffer Register 14	ADBUF14	16	16	2 or 3 PCLKB
0008 90CEh	S12AD	A/D Data Storage Buffer Register 15	ADBUF15	16	16	2 or 3 PCLKB
0008 90D0h	S12AD	A/D Data Storage Buffer Enable Register	ADBUFEN	8	8	2 or 3 PCLKB
0008 90D2h	S12AD	A/D Data Storage Buffer Pointer Register	ADBUFPTR	8	8	2 or 3 PCLKB
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 90DEh	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (8 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A006h	SMCI0	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A012h	SCI0	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A026h	SMCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (9 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0A9h	SCI5	I2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0AAh	SCI5	I2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0ABh	SCI5	I2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0ACh	SCI5	I2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0C9h	SCI6	I2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0CAh	SCI6	I2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0CBh	SCI6	I2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0CCh	SCI6	I2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A106h	SMCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A109h	SCI8	I2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A10Ah	SCI8	I2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A10Bh	SCI8	I2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A10Ch	SCI8	I2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (10 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A126h	SMCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A129h	SCI9	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A12Ah	SCI9	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A12Bh	SCI9	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A12Ch	SCI9	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A131h	SCI9	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A132h	SCI9	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB
0008 B109h	ELC	Event Link Setting Register 8	ELSR8	8	8	2 or 3 PCLKB
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 or 3 PCLKB
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 or 3 PCLKB
0008 B10Fh	ELC	Event Link Setting Register 14	ELSR14	8	8	2 or 3 PCLKB
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 or 3 PCLKB
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (11 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 or 3 PCLKB
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SMCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (12 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C011h	PORTH	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C031h	PORTH	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (13 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C0A4h	PORTJ	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0D1h	PORTH	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0D2h	PORTJ	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0F1h	PORTH	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C120h	PORT	Port Switching Register B	PSRB	8	8	2 or 3 PCLKB
0008 C121h	PORT	Port Switching Register A	PSRA	8	8	2 or 3 PCLKB
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2 or 3 PCLKB
0008 C145h	MPC	P05 Pin Function Control Register	P05PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 C147h	MPC	P07 Pin Function Control Register	P07PFS	8	8	2 or 3 PCLKB
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2 or 3 PCLKB
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2 or 3 PCLKB
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 or 3 PCLKB
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2 or 3 PCLKB
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2 or 3 PCLKB
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2 or 3 PCLKB
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (15 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2 or 3 PCLKB
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2 or 3 PCLKB
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2 or 3 PCLKB
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2 or 3 PCLKB
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2 or 3 PCLKB
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2 or 3 PCLKB
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2 or 3 PCLKB
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2 or 3 PCLKB
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB
0008 C1D1h	MPC	PJ1 Pin Function Control Register	PJ1PFS	8	8	2 or 3 PCLKB
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB
0008 C1D6h	MPC	PJ6 Pin Function Control Register	PJ6PFS	8	8	2 or 3 PCLKB
0008 C1D7h	MPC	PJ7 Pin Function Control Register	PJ7PFS	8	8	2 or 3 PCLKB
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 or 5 PCLKB
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (16 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB
0008 C580h	CMPB	Comparator B Control Register 1	CPBCNT1	8	8	2 or 3 PCLKB
0008 C581h	CMPB	Comparator B Control Register 2	CPBCNT2	8	8	2 or 3 PCLKB
0008 C582h	CMPB	Comparator B Flag Register	CPBFLG	8	8	2 or 3 PCLKB
0008 C583h	CMPB	Comparator B Interrupt Control Register	CPBINT	8	8	2 or 3 PCLKB
0008 C584h	CMPB	Comparator B Filter Select Register	CPBF	8	8	2 or 3 PCLKB
0008 C585h	CMPB	Comparator B Mode Select Register	CPBMD	8	8	2 or 3 PCLKB
0008 C586h	CMPB	Comparator B Reference Input Voltage Select Register	CPBREF	8	8	2 or 3 PCLKB
0008 C587h	CMPB	Comparator B Output Control Register	CPBOCR	8	8	2 or 3 PCLKB
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	1 or 2 PCLKB
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	1 or 2 PCLKB
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	1 or 2 PCLKB
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	1 or 2 PCLKB
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	1 or 2 PCLKB
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	1 or 2 PCLKB
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	1 or 2 PCLKB
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	1 or 2 PCLKB
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	1 or 2 PCLKB
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	1 or 2 PCLKB
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	1 or 2 PCLKB
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	1 or 2 PCLKB
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	1 or 2 PCLKB
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	1 or 2 PCLKB
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	1 or 2 PCLKB
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	1 or 2 PCLKB
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	1 or 2 PCLKB
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	1 or 2 PCLKB
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	1 or 2 PCLKB
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	1 or 2 PCLKB
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	1 or 2 PCLKB
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	1 or 2 PCLKB
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	1 or 2 PCLKB
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	1 or 2 PCLKB
000A 0B00h	REMC0	Function Select Register 0	REMCON0	8	8	1 or 2 PCLKB
000A 0B01h	REMC0	Function Select Register 1	REMCON1	8	8	1 or 2 PCLKB
000A 0B02h	REMC0	Status Register	REMSTS	8	8	1 or 2 PCLKB
000A 0B03h	REMC0	Interrupt Control Register	REMINT	8	8	1 or 2 PCLKB
000A 0B04h	REMC0	Compare Control Register	REMCPC	8	8	1 or 2 PCLKB

Table 4.1 List of I/O Registers (Address Order) (17 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
000A 0B05h	REMC0	Compare Value Setting Register	REMCPD	8	8	1 or 2 PCLKB
000A 0B06h	REMC0	Header Pattern Minimum Width Setting Register	HDPMIN	16	16	1 or 2 PCLKB
000A 0B08h	REMC0	Header Pattern Maximum Width Setting Register	HDPMAX	16	16	1 or 2 PCLKB
000A 0B0Ah	REMC0	Data '0' Pattern Minimum Width Setting Register	D0PMIN	8	8	1 or 2 PCLKB
000A 0B0Bh	REMC0	Data '0' Pattern Maximum Width Setting Register	D0PMAX	8	8	1 or 2 PCLKB
000A 0B0Ch	REMC0	Data '1' Pattern Minimum Width Setting Register	D1PMIN	8	8	1 or 2 PCLKB
000A 0B0Dh	REMC0	Data '1' Pattern Maximum Width Setting Register	D1PMAX	8	8	1 or 2 PCLKB
000A 0B0Eh	REMC0	Special Data Pattern Minimum Width Setting Register	SDPMIN	16	16	1 or 2 PCLKB
000A 0B10h	REMC0	Special Data Pattern Maximum Width Setting Register	SDPMAX	16	16	1 or 2 PCLKB
000A 0B12h	REMC0	Pattern End Setting Register	REMPE	16	16	1 or 2 PCLKB
000A 0B14h	REMC0	Reception Standby Control Register	REMSTC	8	8	1 or 2 PCLKB
000A 0B15h	REMC0	Receive Bit Count Register	REMRBIT	8	8	1 or 2 PCLKB
000A 0B16h	REMC0	Receive Data 0 Register	REMDAT0	8	8	1 or 2 PCLKB
000A 0B17h	REMC0	Receive Data 1 Register	REMDAT1	8	8	1 or 2 PCLKB
000A 0B18h	REMC0	Receive Data 2 Register	REMDAT2	8	8	1 or 2 PCLKB
000A 0B19h	REMC0	Receive Data 3 Register	REMDAT3	8	8	1 or 2 PCLKB
000A 0B1Ah	REMC0	Receive Data 4 Register	REMDAT4	8	8	1 or 2 PCLKB
000A 0B1Bh	REMC0	Receive Data 5 Register	REMDAT5	8	8	1 or 2 PCLKB
000A 0B1Ch	REMC0	Receive Data 6 Register	REMDAT6	8	8	1 or 2 PCLKB
000A 0B1Dh	REMC0	Receive Data 7 Register	REMDAT7	8	8	1 or 2 PCLKB
000A 0B1Eh	REMC0	Measurement Result Register	REMTIM	16	16	1 or 2 PCLKB
000A 0B80h	REMC1	Function Select Register 0	REMCON0	8	8	1 or 2 PCLKB
000A 0B81h	REMC1	Function Select Register 1	REMCON1	8	8	1 or 2 PCLKB
000A 0B82h	REMC1	Status Register	REMSTS	8	8	1 or 2 PCLKB
000A 0B83h	REMC1	Interrupt Control Register	REMINT	8	8	1 or 2 PCLKB
000A 0B84h	REMC1	Compare Control Register	REMCPC	8	8	1 or 2 PCLKB
000A 0B85h	REMC1	Compare Value Setting Register	REMCPD	8	8	1 or 2 PCLKB
000A 0B86h	REMC1	Header Pattern Minimum Width Setting Register	HDPMIN	16	16	1 or 2 PCLKB
000A 0B88h	REMC1	Header Pattern Maximum Width Setting Register	HDPMAX	16	16	1 or 2 PCLKB
000A 0B8Ah	REMC1	Data '0' Pattern Minimum Width Setting Register	D0PMIN	8	8	1 or 2 PCLKB
000A 0B8Bh	REMC1	Data '0' Pattern Maximum Width Setting Register	D0PMAX	8	8	1 or 2 PCLKB
000A 0B8Ch	REMC1	Data '1' Pattern Minimum Width Setting Register	D1PMIN	8	8	1 or 2 PCLKB
000A 0B8Dh	REMC1	Data '1' Pattern Maximum Width Setting Register	D1PMAX	8	8	1 or 2 PCLKB
000A 0B8Eh	REMC1	Special Data Pattern Minimum Width Setting Register	SDPMIN	16	16	1 or 2 PCLKB
000A 0B90h	REMC1	Special Data Pattern Maximum Width Setting Register	SDPMAX	16	16	1 or 2 PCLKB
000A 0B92h	REMC1	Pattern End Setting Register	REMPE	16	16	1 or 2 PCLKB
000A 0B94h	REMC1	Reception Standby Control Register	REMSTC	8	8	1 or 2 PCLKB
000A 0B95h	REMC1	Receive Bit Count Register	REMRBIT	8	8	1 or 2 PCLKB
000A 0B96h	REMC1	Receive Data 0 Register	REMDAT0	8	8	1 or 2 PCLKB
000A 0B97h	REMC1	Receive Data 1 Register	REMDAT1	8	8	1 or 2 PCLKB
000A 0B98h	REMC1	Receive Data 2 Register	REMDAT2	8	8	1 or 2 PCLKB
000A 0B99h	REMC1	Receive Data 3 Register	REMDAT3	8	8	1 or 2 PCLKB
000A 0B9Ah	REMC1	Receive Data 4 Register	REMDAT4	8	8	1 or 2 PCLKB
000A 0B9Bh	REMC1	Receive Data 5 Register	REMDAT5	8	8	1 or 2 PCLKB
000A 0B9Ch	REMC1	Receive Data 6 Register	REMDAT6	8	8	1 or 2 PCLKB
000A 0B9Dh	REMC1	Receive Data 7 Register	REMDAT7	8	8	1 or 2 PCLKB
000A 0B9Eh	REMC1	Measurement Result Register	REMTIM	16	16	1 or 2 PCLKB
000A 0C00h	REMCOM	HOCO Clock Supply Control Register	HOSCR	8	8	1 or 2 PCLKB
007F C090h	FLASH	E2 DataFlash Control Register	DFLCTL	8	8	2 or 3 FCLK
007F C0ACh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRL	8	8	2 or 3 FCLK
007F C0ADh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRH	8	8	2 or 3 FCLK
007F C0B0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK

Table 4.1 List of I/O Registers (Address Order) (18 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
007F C0B2h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 FCLK
007F C0B4h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C0B6h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C0B7h	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C0B8h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C0BAh	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK
007F C0C0h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C0C1h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C0C2h	FLASH	Flash Read Buffer Register L	FRBL	16	16	2 or 3 FCLK
007F C0C4h	FLASH	Flash Read Buffer Register H	FRBH	16	16	2 or 3 FCLK
007F FF80h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F FF81h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F FF82h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F FF84h	FLASH	Flash Processing Start Address Register H	FSARH	8	8	2 or 3 FCLK
007F FF85h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F FF86h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F FF88h	FLASH	Flash Processing End Address Register H	FEARH	8	8	2 or 3 FCLK
007F FF89h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F FF8Ah	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F FF8Bh	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F FF8Ch	FLASH	Flash Write Buffer Register L	FWBL	16	16	2 or 3 FCLK
007F FF8Eh	FLASH	Flash Write Buffer Register H	FWBH	16	16	2 or 3 FCLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK
007F FFBEh	CTSU	CTSU Reference Current Calibration Register	CTSUTRMR	8	8	2 or 3 FCLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		–0.3 to AVCC0 + 0.3	V
	Ports other than above		–0.3 to VCC + 0.3	
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3	V
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN007 used	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN016 to AN031 used		–0.3 to VCC + 0.3	
Operating temperature*2		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin, refer to section 5.13.1, Connecting VCL Capacitor and Bypass Capacitors

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.

The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports P12, P13, P16, and P17 are 5 V tolerant.

Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2, *3		1.8	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0*1, *2		1.8	—	5.5	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V
AVCC0 = VCC when VCC < 2.0 V

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Note 3. When VCC < 2.4 V, some functions of the REMC and CTSU are restricted. For details, refer to section 28, Remote Control Signal Receiver (REMC) and section 32, Capacitive Touch Sensing Unit (CTSUa) in the User's Manual: Hardware.

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports P12, P13, P16, P17 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports P14, P15, Ports P20 to P27, Ports P30 to P37, Ports P50 to P55, Ports PA0 to PA7, Ports PB0 to PB7, Ports PC0 to PC7, Ports PD0 to PD7, Ports PE0 to PE7, Ports PH0 to PH3, Ports PJ1, PJ3, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		AVCC0 × 0.8	—	AVCC0 + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		–0.3	—	AVCC0 × 0.2		
	Ports other than above		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Ports P12, P13, P16, P17 (5 V tolerant)		VCC × 0.05	—	—		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		AVCC0 × 0.1	—	—		
	Ports other than above		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Table 5.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC < 2.7 V, 2.0 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports P12, P13, P16, P17 (5 V tolerant)	V_{IH}	VCC × 0.8	—	5.8	V	
	Ports P14, P15, Ports P20 to P27, Ports P30 to P37, Ports P50 to P55, Ports PA0 to PA7, Ports PB0 to PB7, Ports PC0 to PC7, Ports PD0 to PD7, Ports PE0 to PE7, Ports PH0 to PH3, Ports PJ1, PJ3, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7	V_{IL}	–0.3	—	AVCC0 × 0.2		
	Ports other than above		–0.3	—	VCC × 0.2		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7	ΔV_T	AVCC0 × 0.01	—	—		
	Ports other than above		VCC × 0.01	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		

Table 5.5 DC Characteristics (3)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port P35	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0V, VCC
Three-state leakage current (off-state)	Ports for 5-V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0V, 5.8V
	Ports except for 5 V tolerant		—	—	0.2		V_{in} = 0V, VCC
Input capacitance	All input pins (except for port P35)	C_{in}	—	—	15	pF	V_{in} = 0mV, f = 1MHz, T_a = 25°C
	port P35		—	—	30		

Table 5.6 DC Characteristics (4)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC < 5.5 V, 2.0 V ≤ AVCC0 < 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for port P35)	R_U	10	20	50	kΩ	V_{in} = 0 V

[Products with 128 Kbytes of flash memory or less (except for 100-pin packages)]

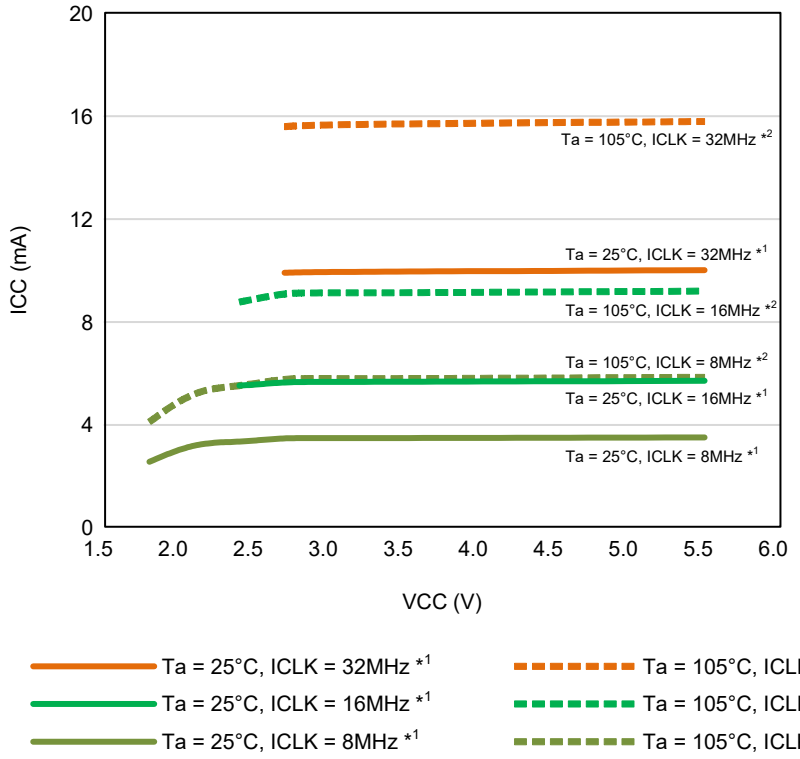
Table 5.7 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32MHz	I_{CC}	3.1	—	mA	
				ICLK = 16MHz		2.1	—		
				ICLK = 8MHz		1.6	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		10.0	—		
				ICLK = 16MHz		5.7	—		
				ICLK = 8MHz		3.5	—		
			All peripheral operation: Max.*3	ICLK = 32MHz		—	17.5		
		Sleep mode	No peripheral operation*2	ICLK = 32MHz		1.6	—		
				ICLK = 16MHz		1.2	—		
				ICLK = 8MHz		1.1	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		5.3	—		
				ICLK = 16MHz		3.2	—		
				ICLK = 8MHz		2.0	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32MHz		1.0	—		
				ICLK = 16MHz		0.9	—		
				ICLK = 8MHz		0.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		4.2	—		
				ICLK = 16MHz		2.5	—		
				ICLK = 8MHz		1.7	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.9	—	mA	
				ICLK = 8MHz		1.2	—		
				ICLK = 4MHz		0.6	—		
				ICLK = 1MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		4.6	—		
				ICLK = 8MHz		3.2	—		
				ICLK = 4MHz		2.0	—		
				ICLK = 1MHz		0.9	—		
			All peripheral operation: Max.*7	ICLK = 12MHz		—	8.2		
		Sleep mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.2	—	mA	
				ICLK = 8MHz		0.8	—		
				ICLK = 4MHz		0.3	—		
				ICLK = 1MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		2.7	—		
				ICLK = 8MHz		1.9	—		
				ICLK = 4MHz		1.2	—		
				ICLK = 1MHz		0.7	—		

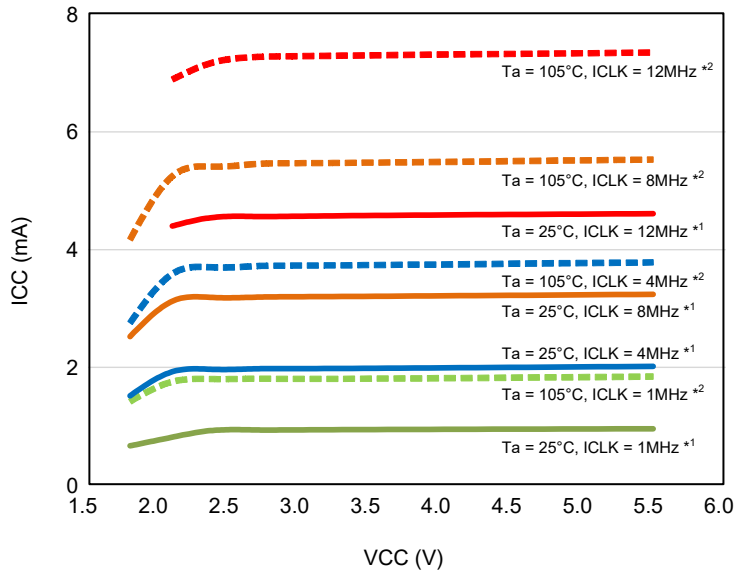
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes	Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	1.0	—	mA	
				ICLK = 8 MHz		0.7	—		
				ICLK = 4 MHz		0.2	—		
				ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.3	—		
				ICLK = 8 MHz		1.6	—		
				ICLK = 4 MHz		1.0	—		
				ICLK = 1 MHz		0.7	—		
		Increase during flash rewrite*5				2.5	—		
	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32.768 kHz	I_{CC}	3.8	—	μA	
			All peripheral operation: Normal*10	ICLK = 32.768 kHz		10.9	—		
			All peripheral operation: Max.*10	ICLK = 32.768 kHz		—	29.2		
		Sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		2.1	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		6.0	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		1.6	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		5.0	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.
Note 4. Values when VCC = 3.3 V.
Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.
Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.
Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.



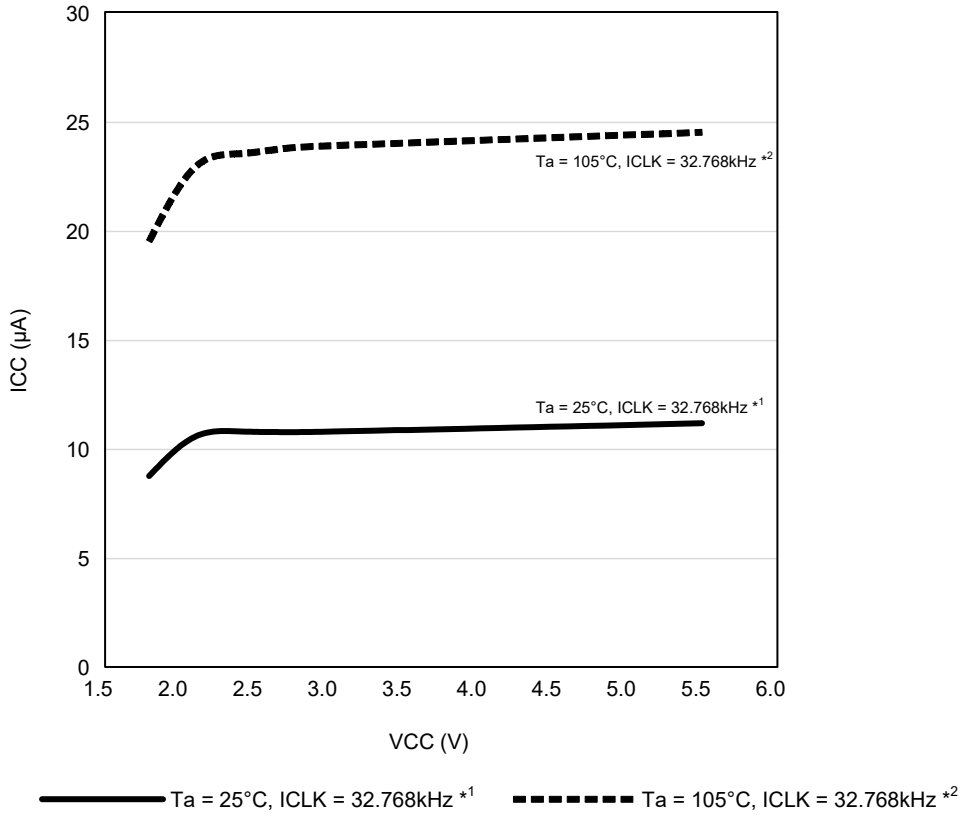
Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

[Products with at least 256 Kbytes of flash memory or 100-pin packages]

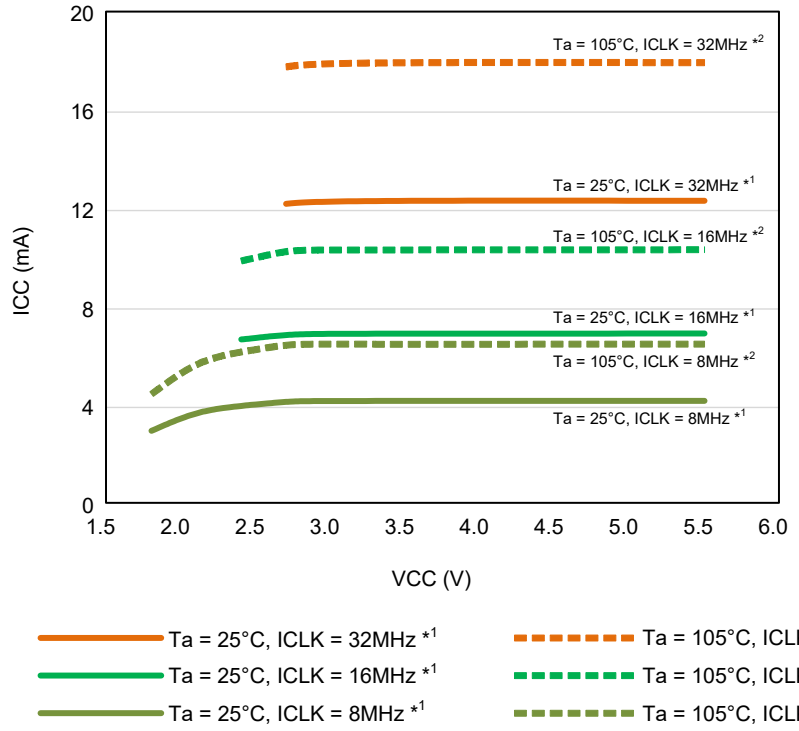
Table 5.8 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32MHz	I_{CC}	3.5	—	mA	
				ICLK = 16MHz		2.4	—		
				ICLK = 8MHz		1.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		12.4	—		
				ICLK = 16MHz		7.0	—		
				ICLK = 8MHz		4.3	—		
			All peripheral operation: Max.*3	ICLK = 32MHz		—	25.4		
		Sleep mode	No peripheral operation*2	ICLK = 32MHz		1.8	—		
				ICLK = 16MHz		1.4	—		
				ICLK = 8MHz		1.2	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		6.5	—		
				ICLK = 16MHz		3.8	—		
				ICLK = 8MHz		2.5	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32MHz		1.1	—		
				ICLK = 16MHz		0.9	—		
				ICLK = 8MHz		0.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		5.2	—		
				ICLK = 16MHz		3.0	—		
				ICLK = 8MHz		1.9	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	2.1	—	mA	
				ICLK = 8MHz		1.4	—		
				ICLK = 4MHz		0.7	—		
				ICLK = 1MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		5.5	—		
				ICLK = 8MHz		3.9	—		
				ICLK = 4MHz		2.4	—		
				ICLK = 1MHz		1.1	—		
			All peripheral operation: Max.*7	ICLK = 12MHz		—	11.6		
		Sleep mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.4	—	mA	
				ICLK = 8MHz		0.8	—		
				ICLK = 4MHz		0.3	—		
				ICLK = 1MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		3.2	—		
				ICLK = 8MHz		2.2	—		
				ICLK = 4MHz		1.4	—		
				ICLK = 1MHz		0.8	—		

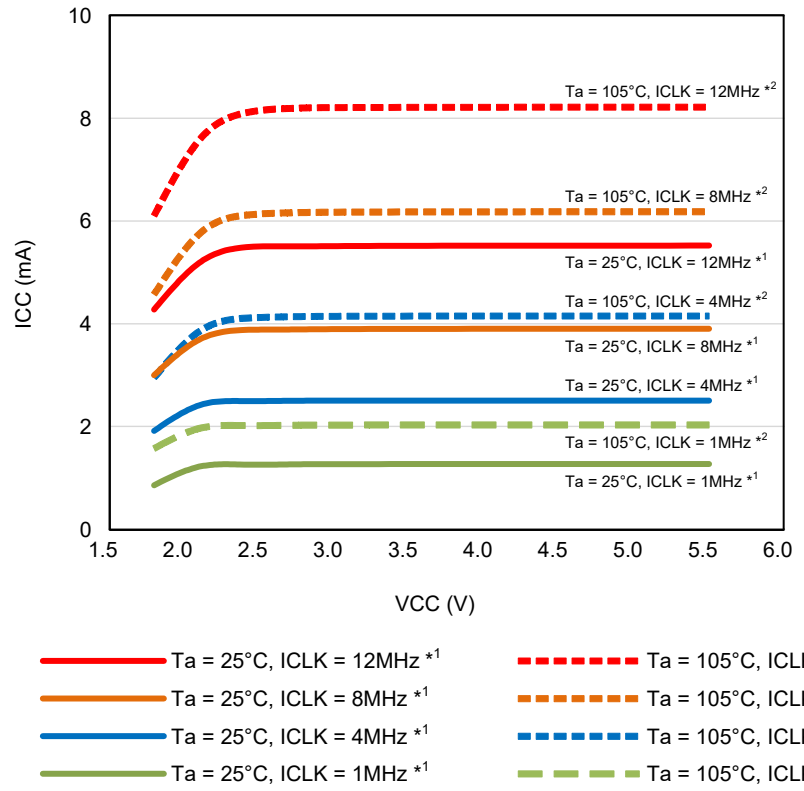
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes	Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	1.1	—	mA	
				ICLK = 8 MHz		0.7	—		
				ICLK = 4 MHz		0.2	—		
				ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.6	—		
				ICLK = 8 MHz		1.8	—		
				ICLK = 4 MHz		1.1	—		
				ICLK = 1 MHz		0.7	—		
		Increase during flash rewrite*5				2.5	—		
	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32.768 kHz	I_{CC}	4.3	—	μA	
			All peripheral operation: Normal*10	ICLK = 32.768 kHz		13.4	—		
			All peripheral operation: Max.*10	ICLK = 32.768 kHz		—	51.3		
		Sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		2.2	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		7.2	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		1.7	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		6.0	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.
Note 4. Values when VCC = 3.3 V.
Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.
Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.
Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.



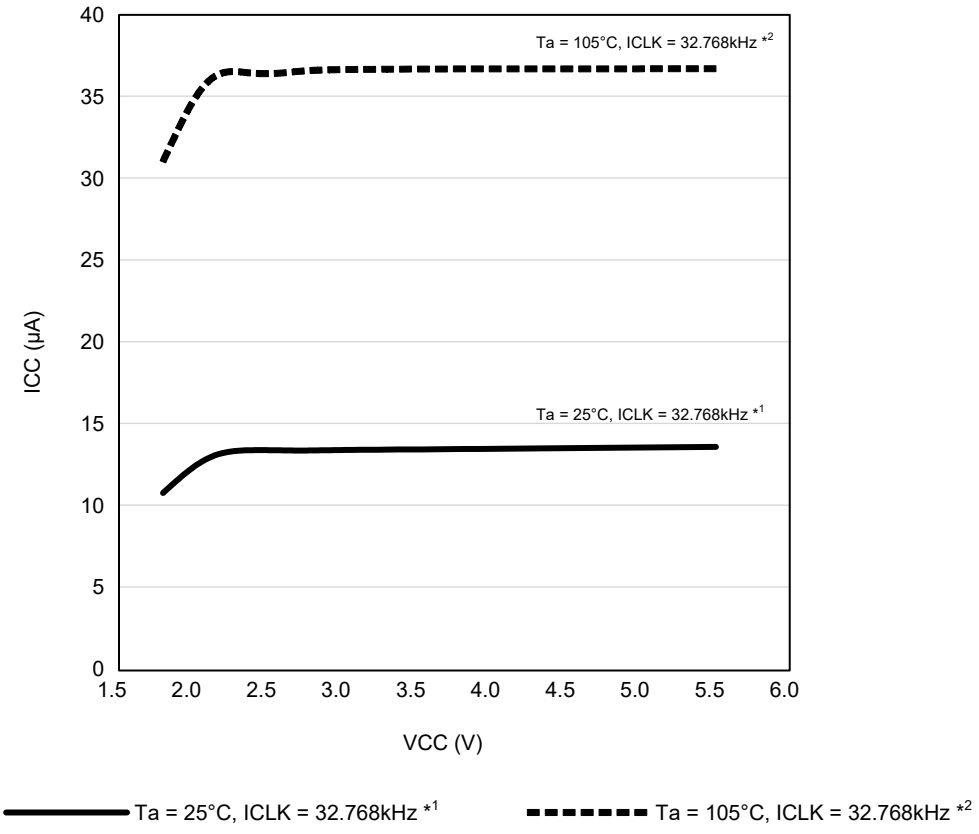
Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.6 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

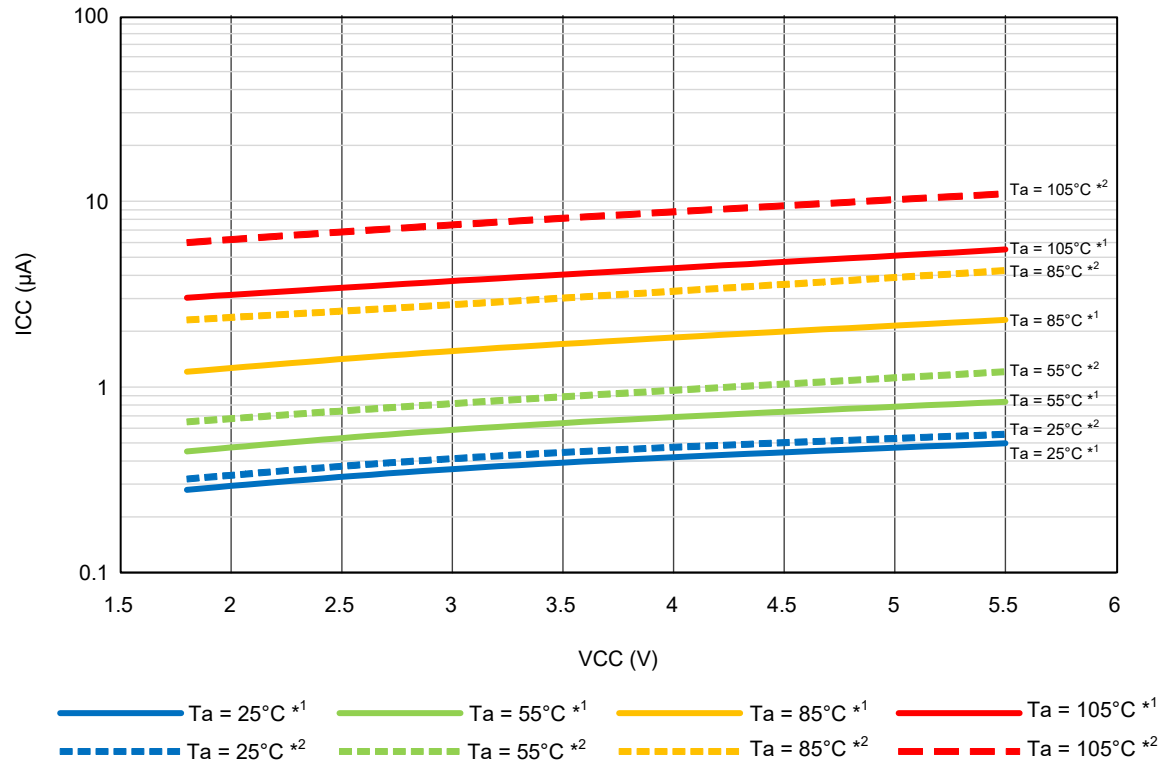
[Products with 128 Kbytes of flash memory or less (except for 100-pin packages)]

Table 5.9 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

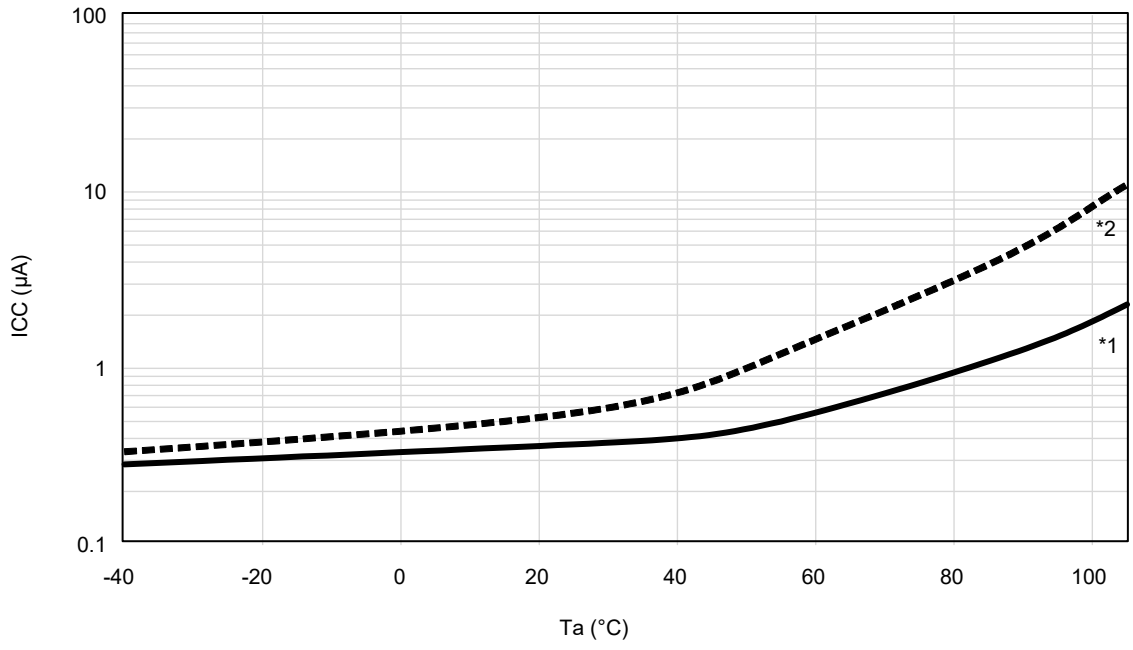
Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.37	0.71	μA	
		T_a = 55°C		0.50	1.70		
		T_a = 85°C		1.20	8.00		
		T_a = 105°C		2.30	19.60		
	Increment for RTC operation*4			0.40	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.21	—		RCR3.RTCDV[2:0] set to normal drive capacity
	Increment for low-power timer operation			0.37	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
	Increment for Independent Watchdog Timer operation			0.37	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.7 Voltage Dependency in Software Standby Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.8 Temperature Dependency in Software Standby Mode (Reference Data)

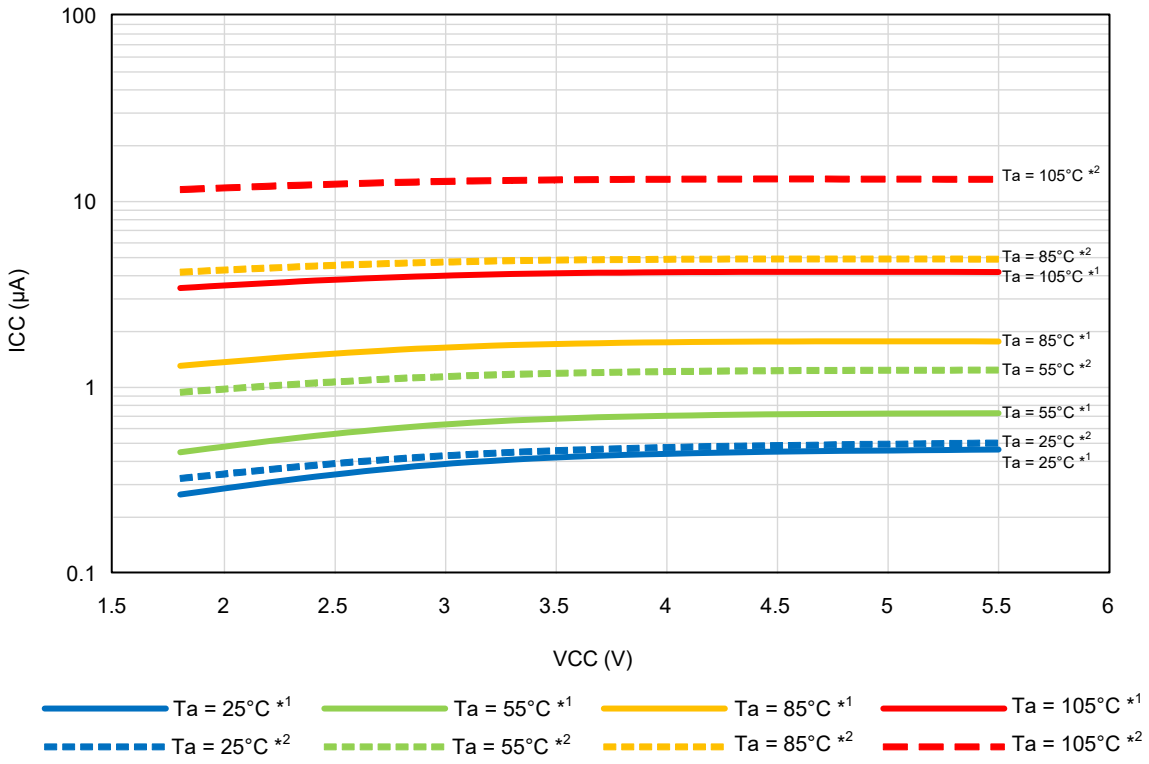
[Products with at least 256 Kbytes of flash memory or 100-pin packages]

Table 5.10 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

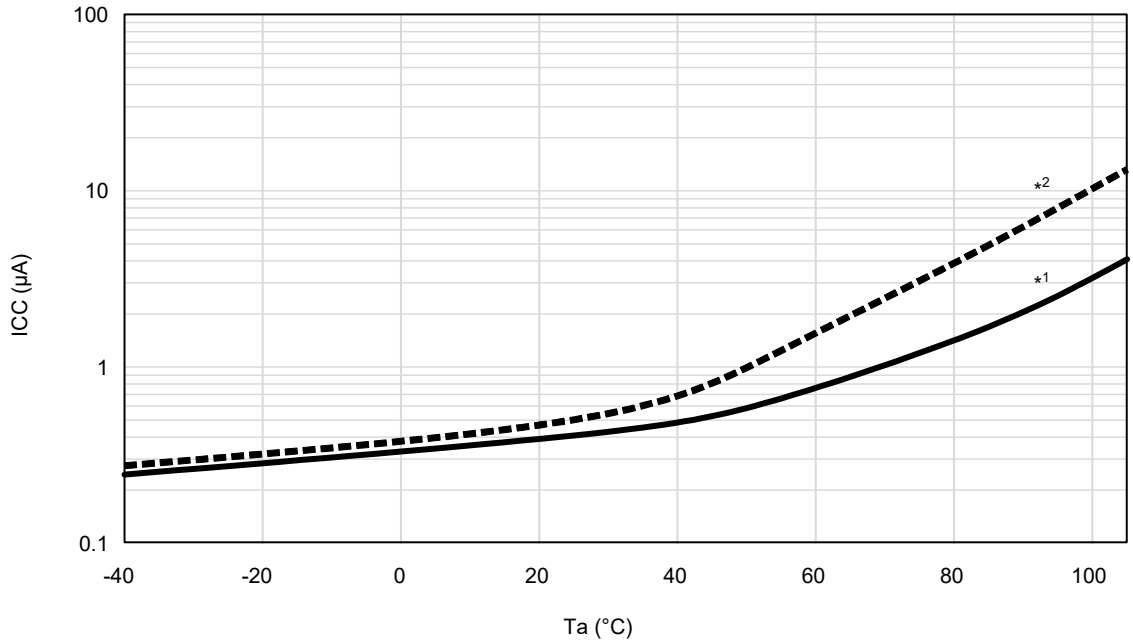
Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.41	0.98	μA	
		T_a = 55°C		0.66	2.78		
		T_a = 85°C		1.69	9.65		
		T_a = 105°C		4.08	25.04		
	Increment for RTC operation*4			0.40	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.21	—		RCR3.RTCDV[2:0] set to normal drive capacity
	Increment for low-power timer operation			0.37	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
	Increment for Independent Watchdog Timer operation			0.37	—		
	Increment for REMC operation			0.44*4	—		REMCON1.CSRC[3:0] set to Sub-clock RCR3.RTCDV[2:0] set to low drive capacity
				1.34*4	—		REMCON1.CSRC[3:0] set to Sub-clock RCR3.RTCDV[2:0] set to normal drive capacity
				235	—		REMCON1.CSRC[3:0] set to HOCO clock/512

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.11 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	P_d	—	300	mW	D version
		—	105		G version

Note: Please contact a Renesas Electronics sales office for information on the derating of the G-version product. Derating is the systematic reduction of load to improve reliability.
Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.12 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.*4	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.7	mA	
	During A/D conversion (at low-speed conversion)		—	0.6	1.0		
	During D/A conversion (per channel)*1		—	—	1.5		
	Waiting for A/D and D/A conversion (all units)		—	—	0.4	µA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	25	150	µA	
	Waiting for A/D conversion (all units)		—	—	60	nA	
LVD0	—	I_{LVD}	—	0.1	—	µA	
LVD1, 2	Per channel		—	0.15	—	µA	
Temperature sensor*3	—	I_{TEMP}	—	75	—	µA	
Comparator B operating current*3	Window function enabled	I_{CMP}*2	—	12.5	28.6	µA	
	Comparator high-speed mode (per channel)		—	3.2	16.2	µA	
	Comparator low-speed mode (per channel)		—	1.7	4.4	µA	
CUSU operating current	During measurement (CPU is in sleep mode) Base clock: 2 MHz Pin capacity: 50 pF	I_{CTSU}	—	150	—	µA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. Current consumed only by the comparator B module.
Note 3. ICurrent consumed by the power supply (VCC).
Note 4. When VCC = AVCC0 = 3.3 V.

Table 5.13 DC Characteristics (9)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 5.14 DC Characteristics (10)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) = 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) = 01b.
Note 3. When OFS1.LVDAS = 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

Table 5.15 DC Characteristics (11)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit and lower limit. When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 5.11 $V_{r\,(VCC)}$ ≤ VCC × 0.2
		—	—	1	MHz	Figure 5.11 $V_{r\,(VCC)}$ ≤ VCC × 0.08
		—	—	10	MHz	Figure 5.11 $V_{r\,(VCC)}$ ≤ VCC × 0.06
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

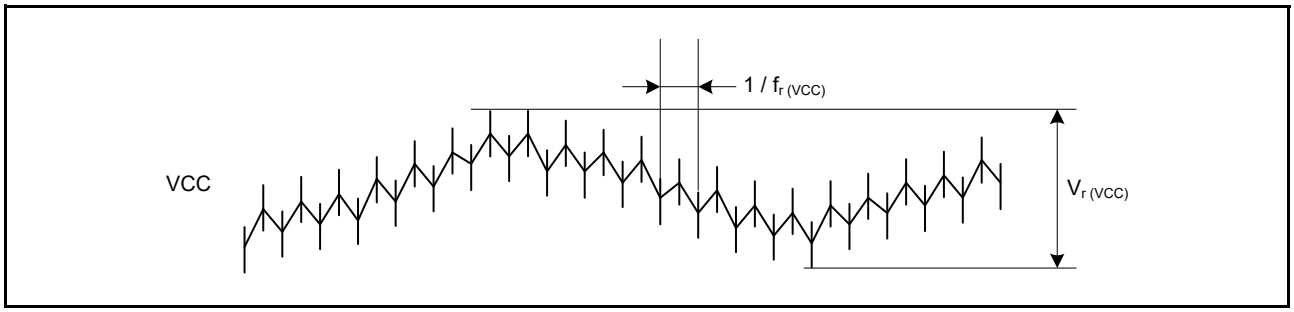


Figure 5.11 Ripple Waveform

Table 5.16 DC Characteristics (12)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	1.4	4.7	7.0	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

Table 5.17 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		ΣI_{OL}	40	
	Total of Ports P12 to P17, Ports P20 to P27, Ports P30 to P37, Ports PH2, PH3, Ports PJ1, PJ3			40	
	Total of Ports P50 to P55, Ports PB0 to PB7, Ports PC0 to PC7, Ports PH0, PH1			40	
	Total of Ports PA0 to PA7, Ports PD0 to PD7, Ports PE0 to PE7			40	
	Total of all output pins			80	
Permissible output high current (average value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		ΣI_{OH}	–40	
	Total of Ports P12 to P17, Ports P20 to P27, Ports P30 to P37, Ports PH2, PH3, Ports PJ1, PJ3			–40	
	Total of Ports P50 to P55, Ports PB0 to PB7, Ports PC0 to PC7, Ports PH0, PH1			–40	
	Total of Ports PA0 to PA7, Ports PD0 to PD7, Ports PE0 to PE7			–40	
	Total of all output pins			–80	

Note: Do not exceed the permissible total supply current.

Table 5.18 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		ΣI_{OL}	30	
	Total of Ports P12 to P17, Ports P20 to P27, Ports P30 to P37, Ports PH2, PH3, Ports PJ1, PJ3			30	
	Total of Ports P50 to P55, Ports PB0 to PB7, Ports PC0 to PC7, Ports PH0, PH1			30	
	Total of Ports PA0 to PA7, Ports PD0 to PD7, Ports PE0 to PE7			30	
	Total of all output pins			60	
Permissible output high current (average value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		ΣI_{OH}	–30	
	Total of Ports P12 to P17, Ports P20 to P27, Ports P30 to P37, Ports PH2, PH3, Ports PJ1, PJ3			–30	
	Total of Ports P50 to P55, Ports PB0 to PB7, Ports PC0 to PC7, Ports PH0, PH1			–30	
	Total of Ports PA0 to PA7, Ports PD0 to PD7, Ports PE0 to PE7			–30	
	Total of all output pins			–60	

Note: Do not exceed the permissible total supply current.

Table 5.19 Output Values of Voltage (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC < 2.7 V, 2.0 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 0.5 mA
		High-drive output mode			—	0.8		I_{OL} = 1.0 mA
Output high	All output ports	Normal output mode	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.5	—	V	I_{OH} = –0.5 mA
			Ports other than above		VCC – 0.5	—		
		High-drive output mode			VCC – 0.5	—		I_{OH} = –1.0 mA

Table 5.20 Output Values of Voltage (2)

Conditions: 2.7 V ≤ VCC < 4.0 V, 2.7 V ≤ AVCC0 < 4.0 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 1.0 mA
		High-drive output mode			—	0.8		I_{OL} = 2.0 mA
	RIIC pins	Standard mode (Normal output mode)			—	0.4		I_{OL} = 3.0 mA
		Fast mode (High-drive output mode)			—	0.4		I_{OL} = 6.0 mA
Output high	All output ports	Normal output mode	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = –1.0 mA
			Ports other than above		VCC – 0.8	—		
		High-drive output mode			VCC – 0.8	—		I_{OH} = –2.0 mA

Table 5.21 Output Values of Voltage (3)

Conditions: 4.0 V ≤ VCC ≤ 5.5 V, 4.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode			—	0.8		I_{OL} = 4.0 mA
	RIIC pins	Standard mode (Normal output mode)			—	0.4		I_{OL} = 3.0 mA
		Fast mode (High-drive output mode)			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports	Normal output mode	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = –2.0 mA
			Ports other than above		VCC – 0.8	—		
		High-drive output mode			VCC – 0.8	—		I_{OH} = –4.0 mA

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.12 to Figure 5.16 show the characteristics when normal output is selected by the drive capacity control register.

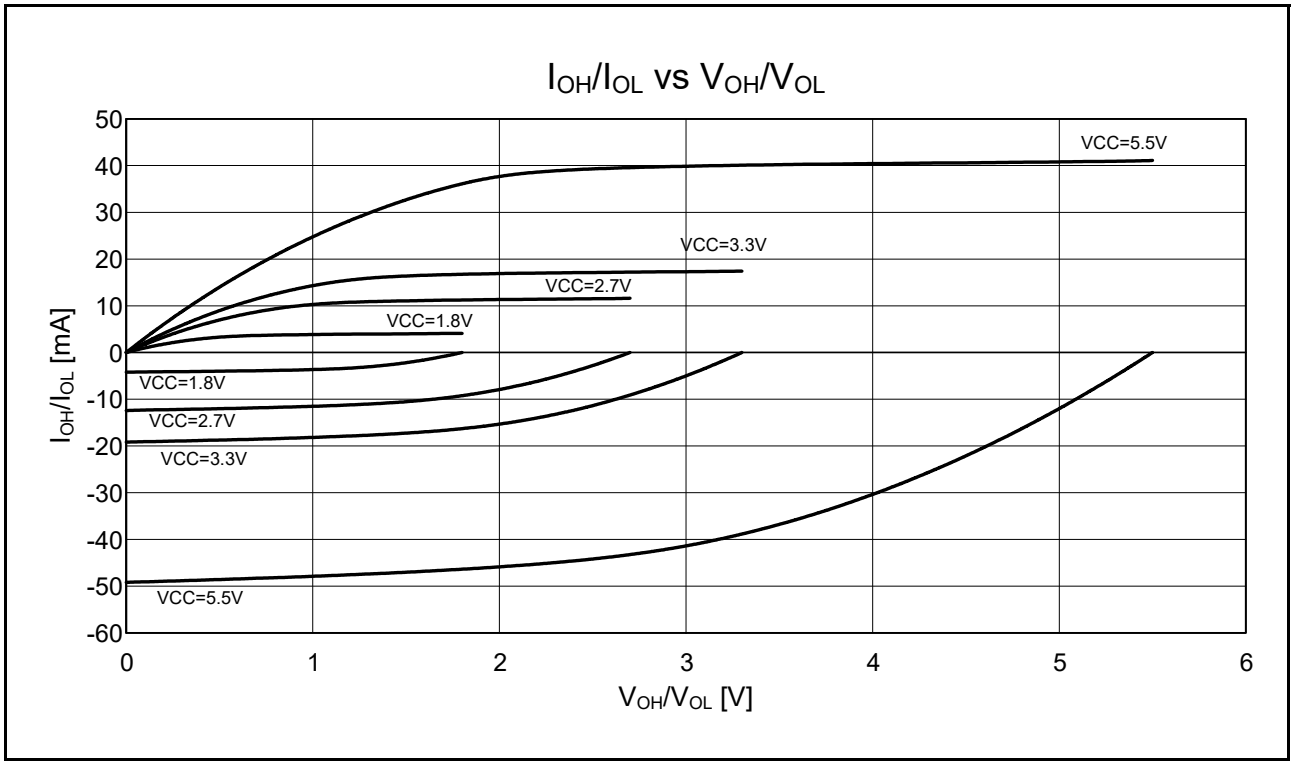


Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

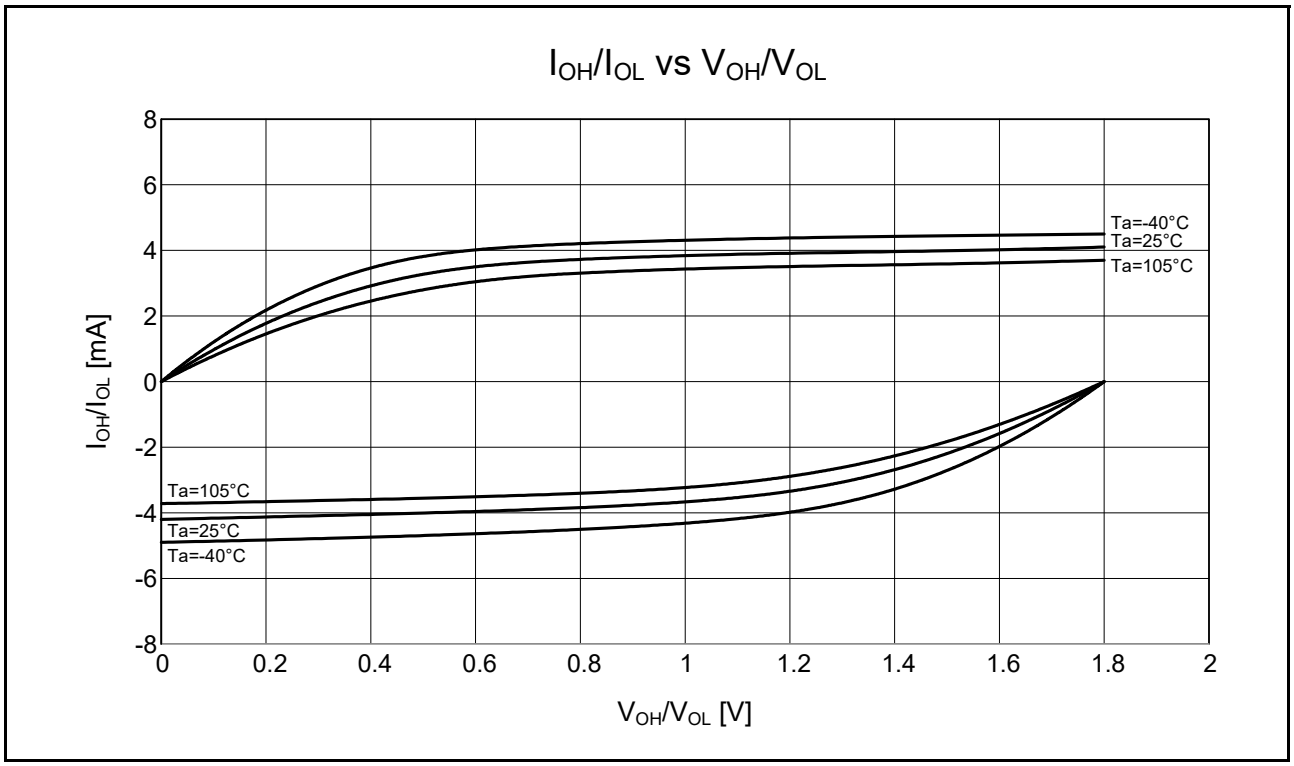


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When Normal Output is Selected (Reference Data)

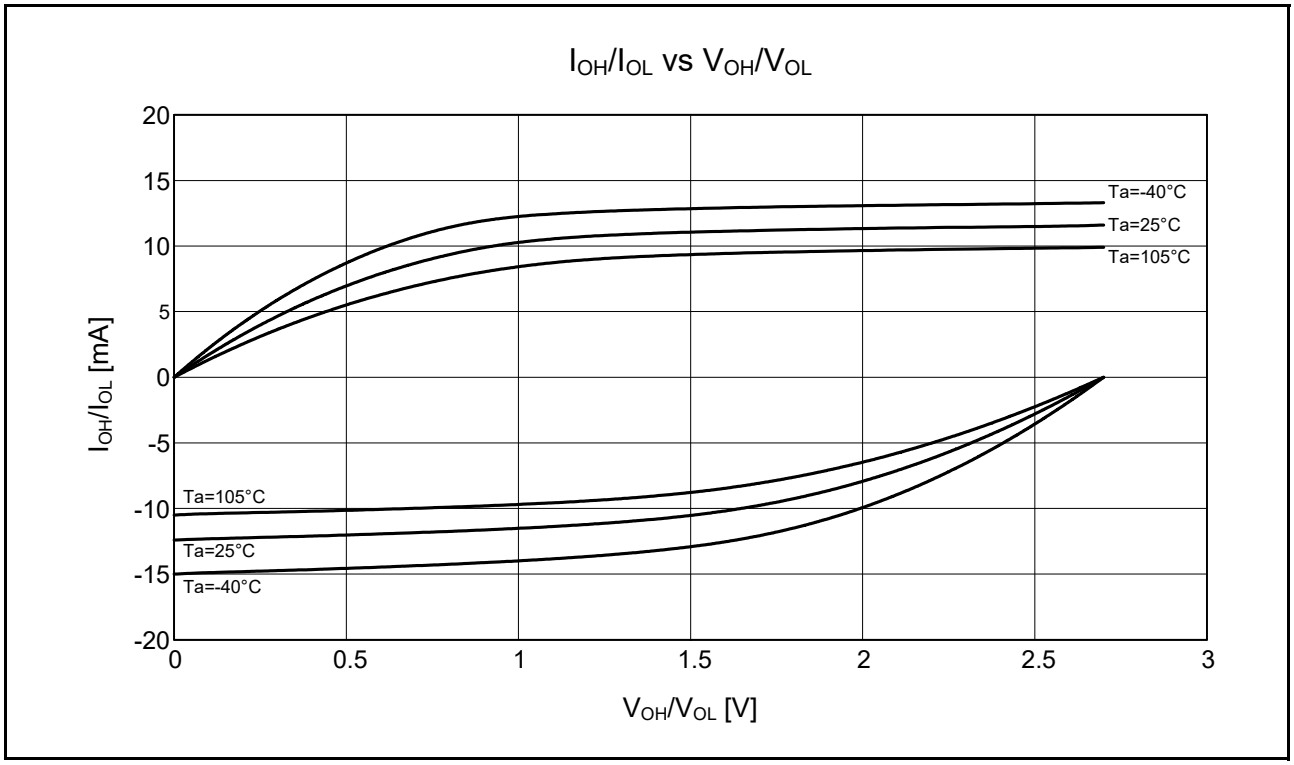


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Normal Output is Selected (Reference Data)

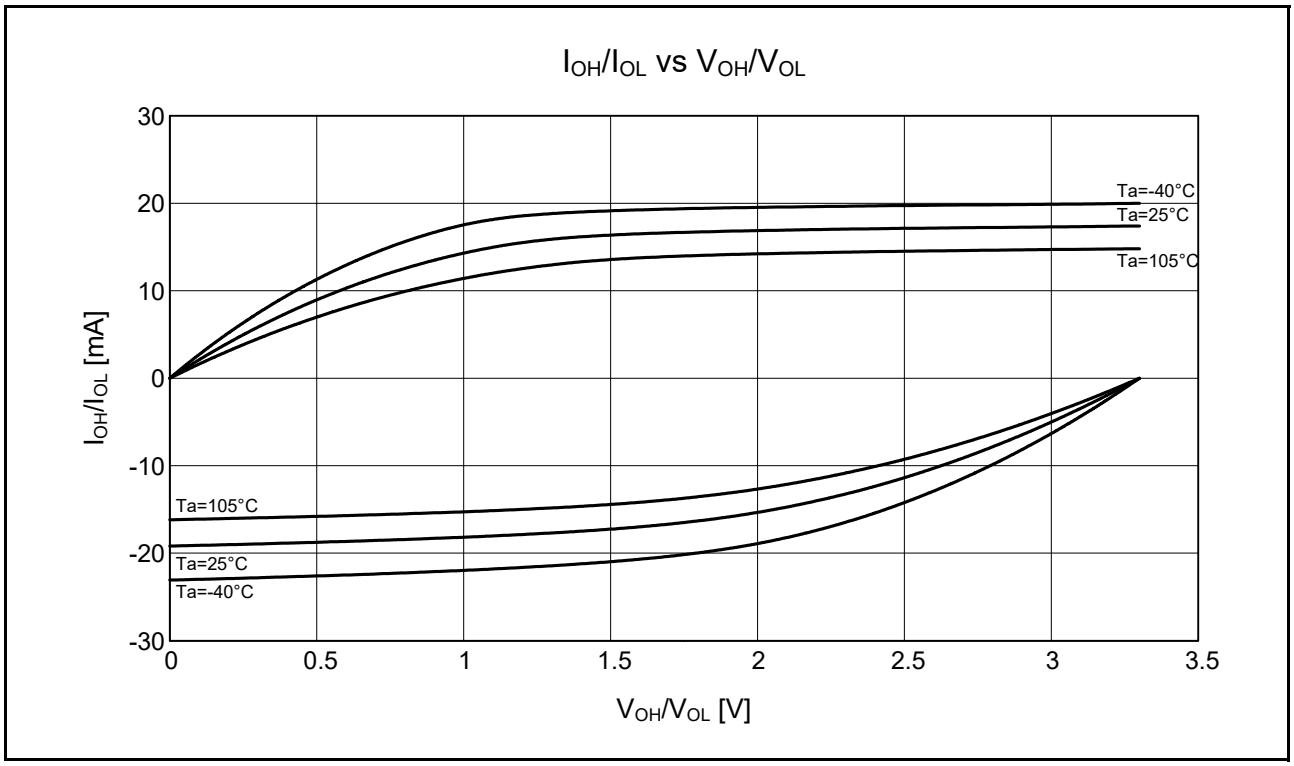


Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Normal Output is Selected (Reference Data)

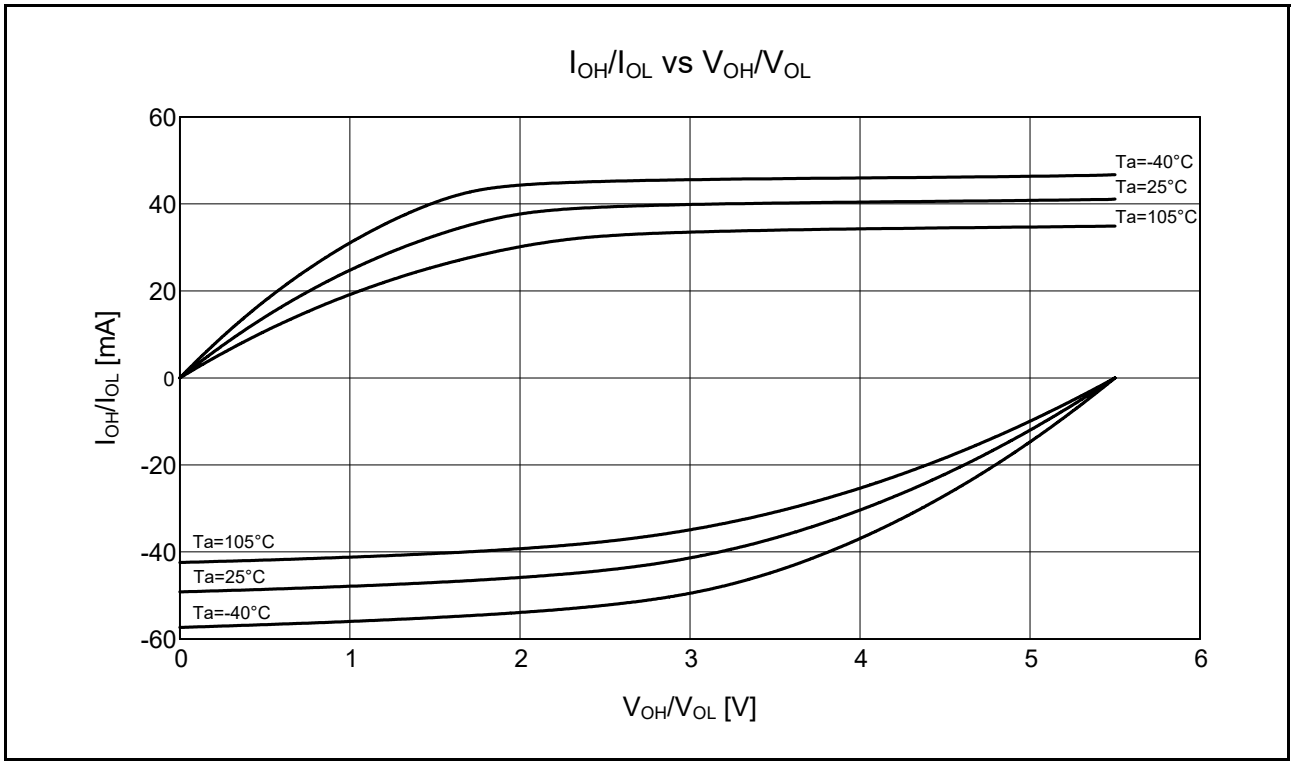


Figure 5.16 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data)**

5.2.2 Normal I/O Pin Output Characteristics (2)

Figure 5.17 to Figure 5.21 show the characteristics when high-drive output is selected by the drive capacity control register.

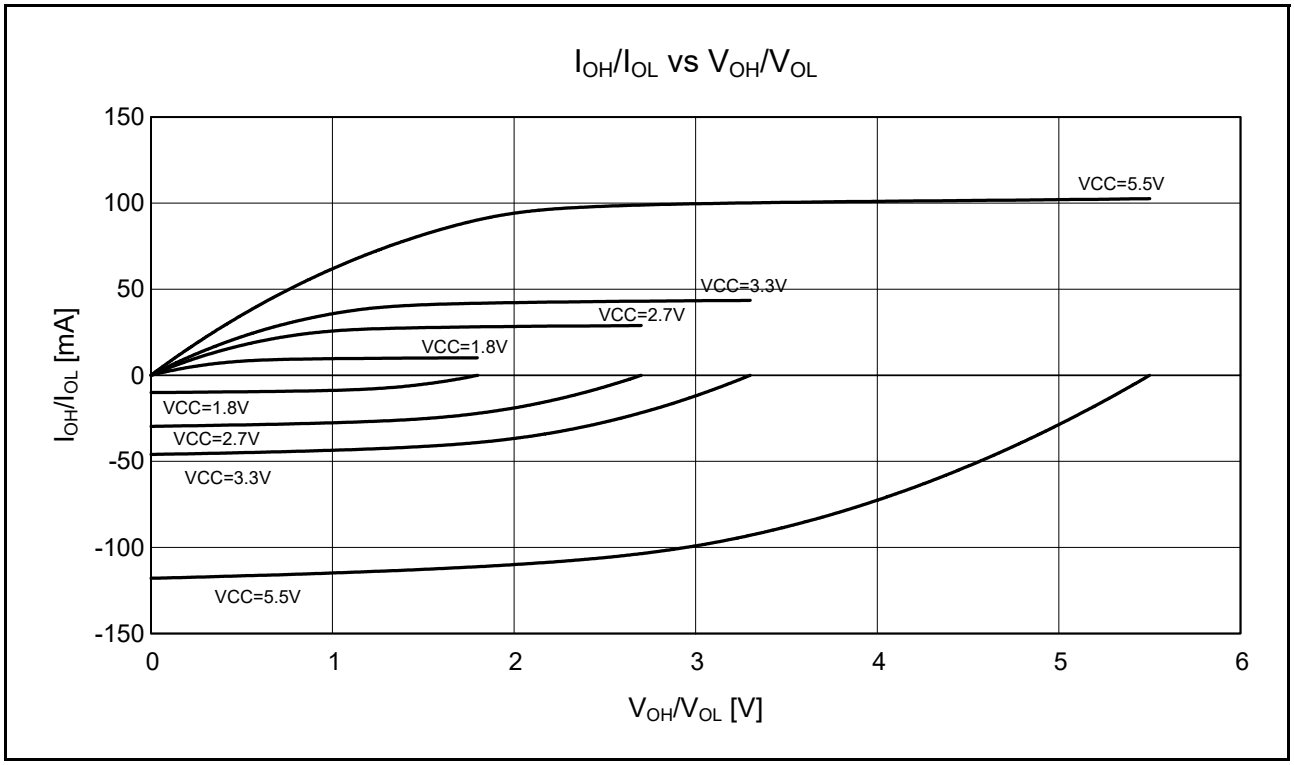


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When High-Drive Output is Selected (Reference Data)

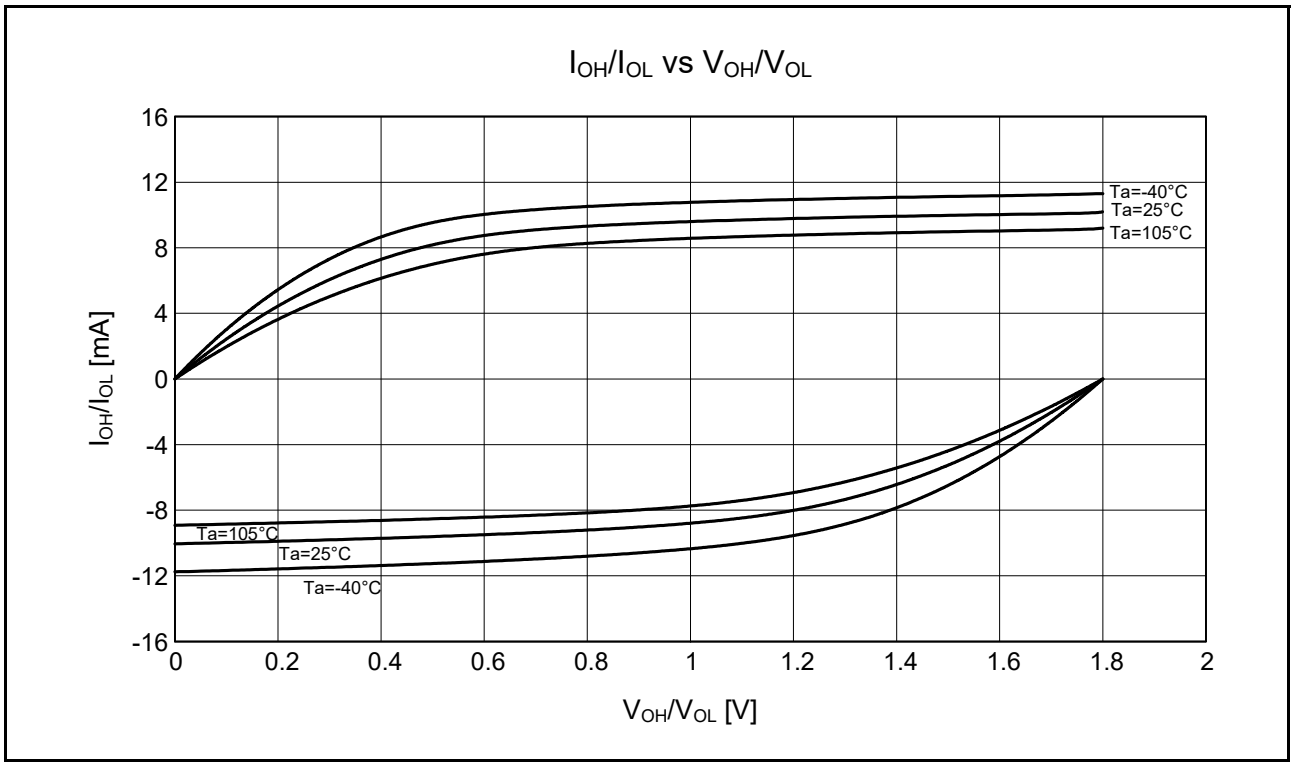


Figure 5.18 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When High-Drive Output is Selected (Reference Data)

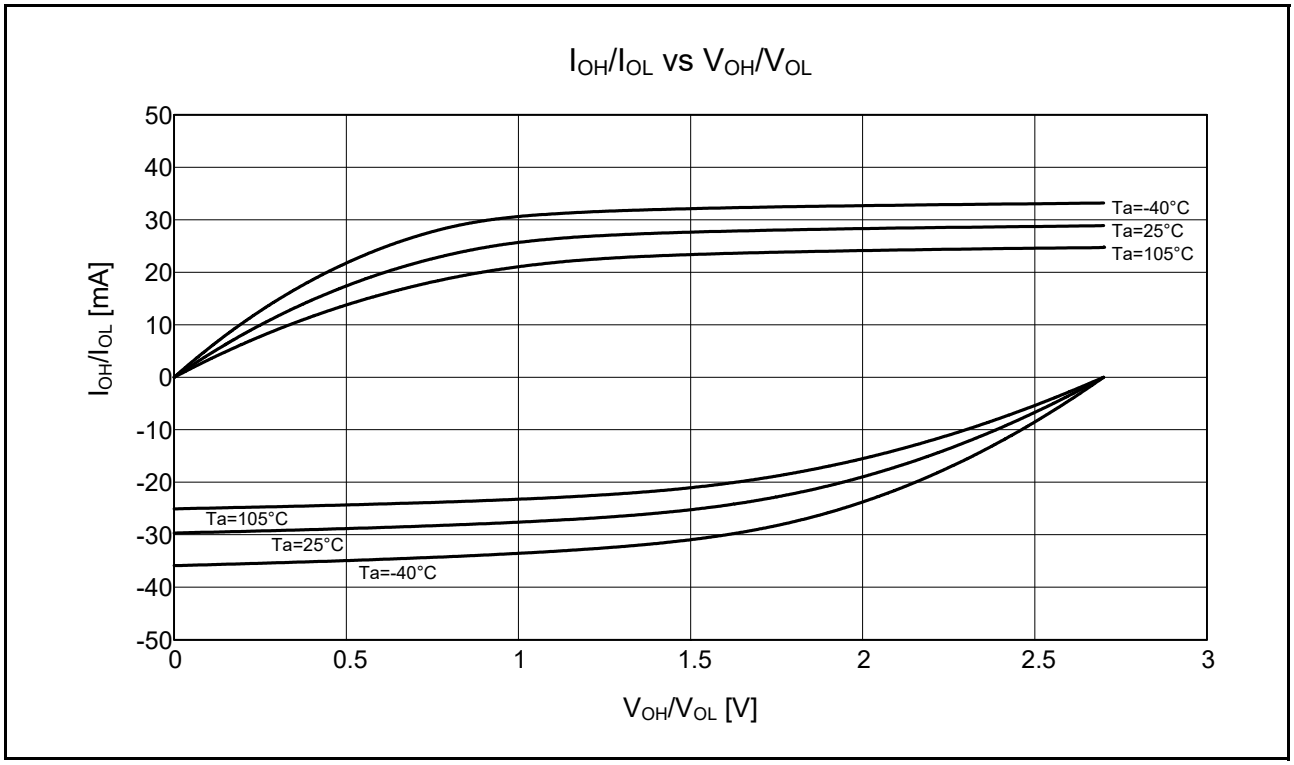


Figure 5.19 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When High-Drive Output is Selected (Reference Data)

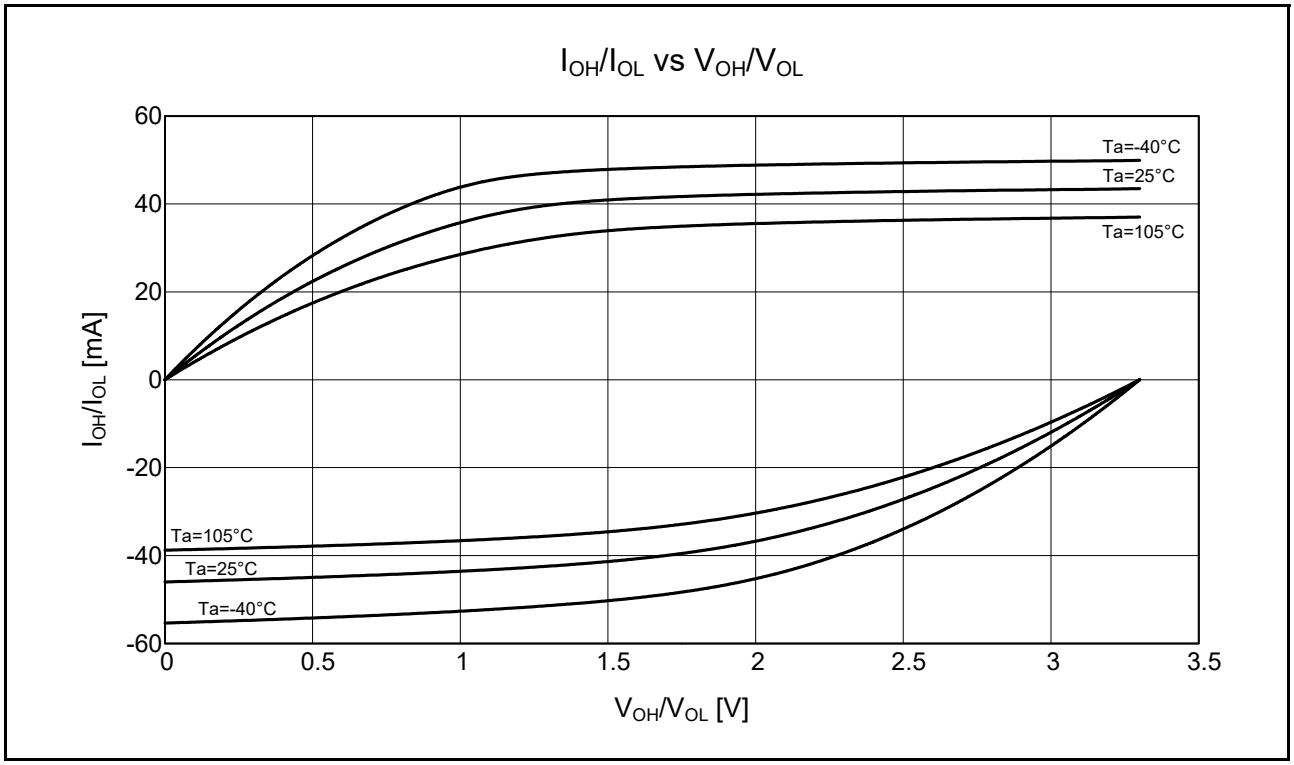


Figure 5.20 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When High-Drive Output is Selected (Reference Data)

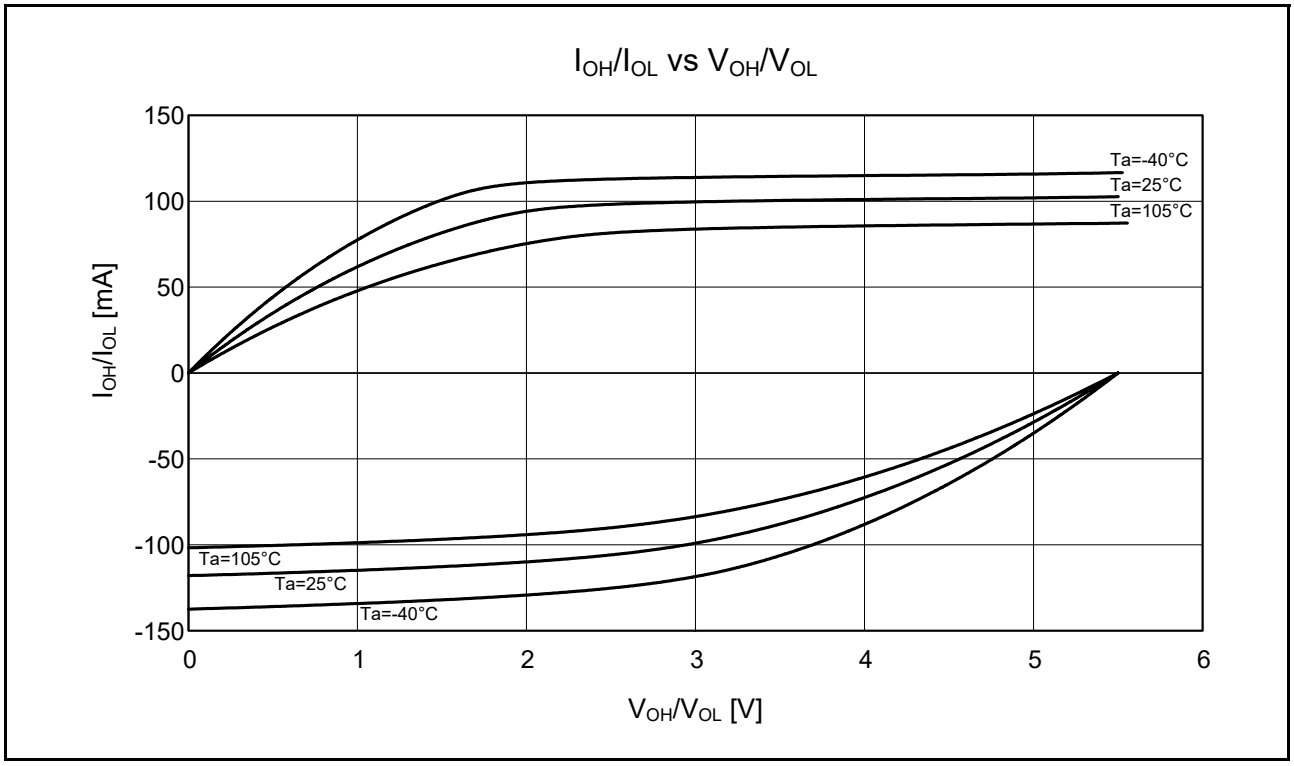


Figure 5.21 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When High-Drive Output is Selected (Reference Data)**

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.22 to Figure 5.25 show the characteristics of the RIIC output pin.

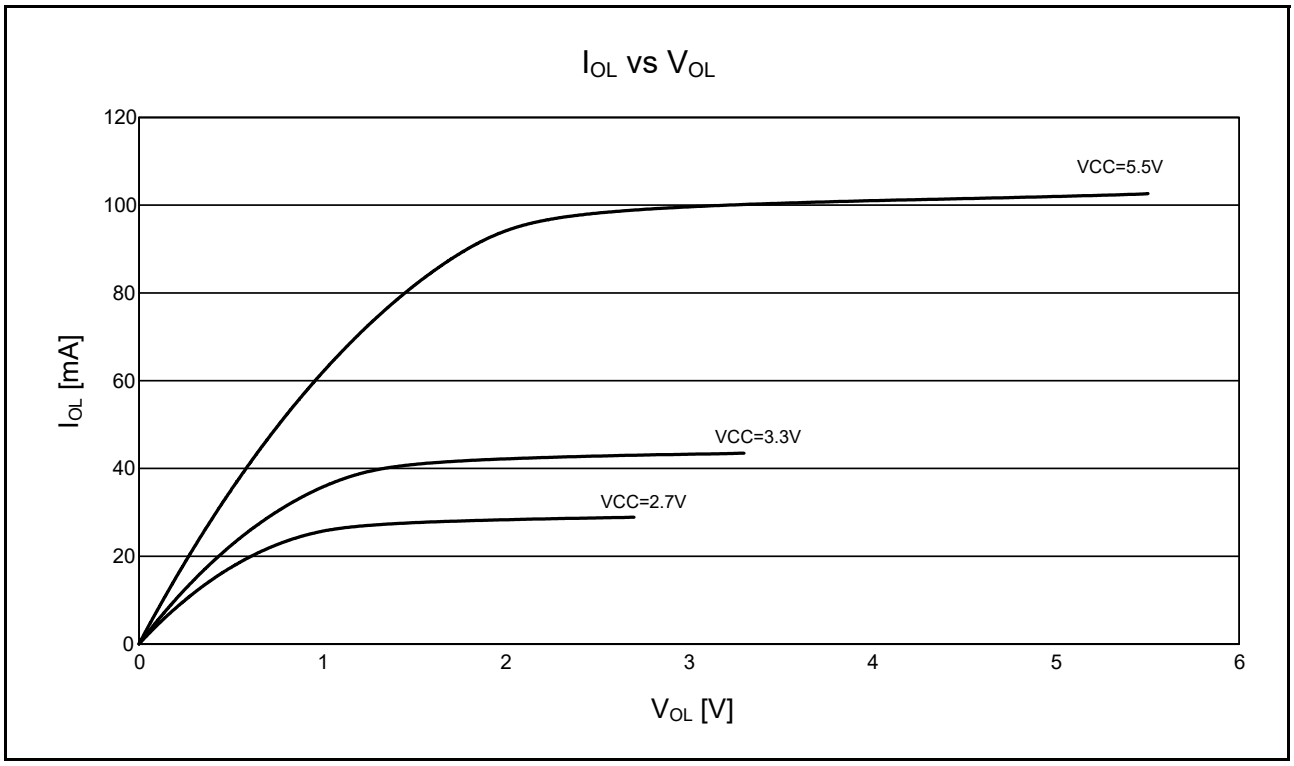


Figure 5.22 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

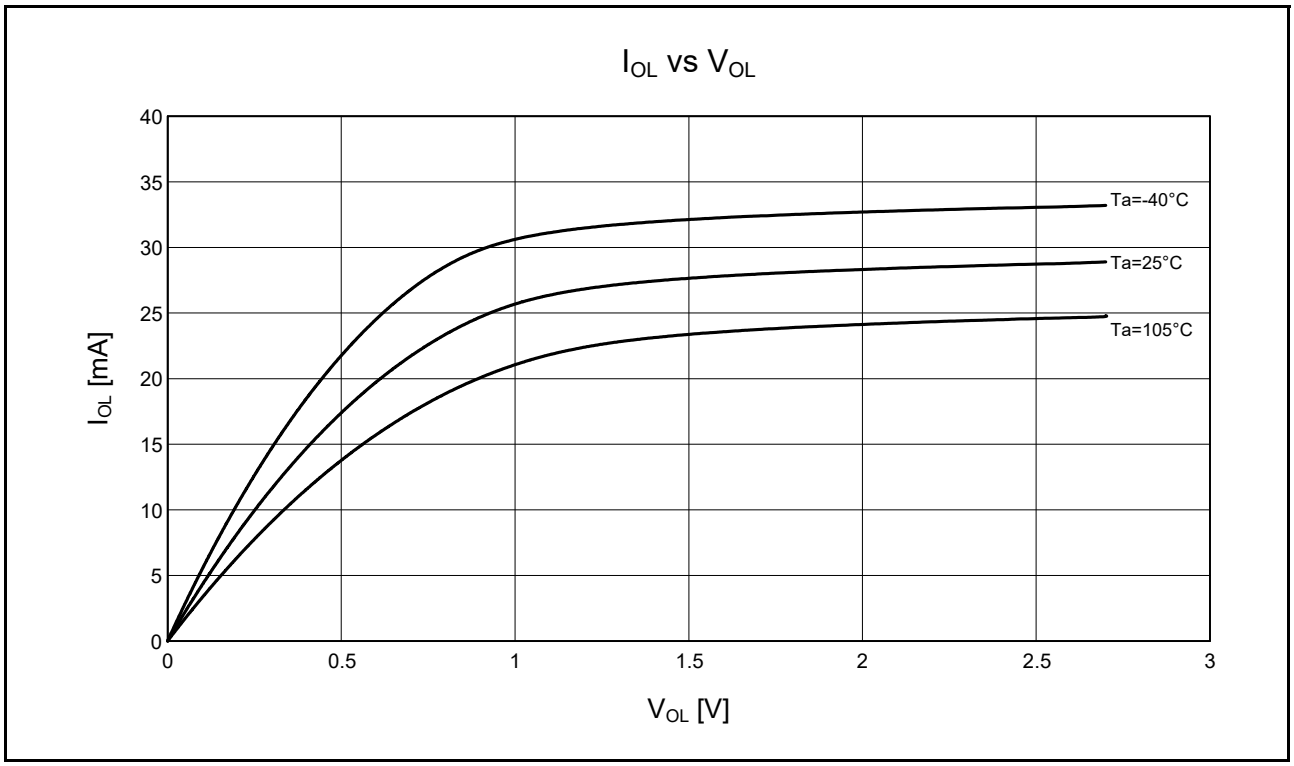


Figure 5.23 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

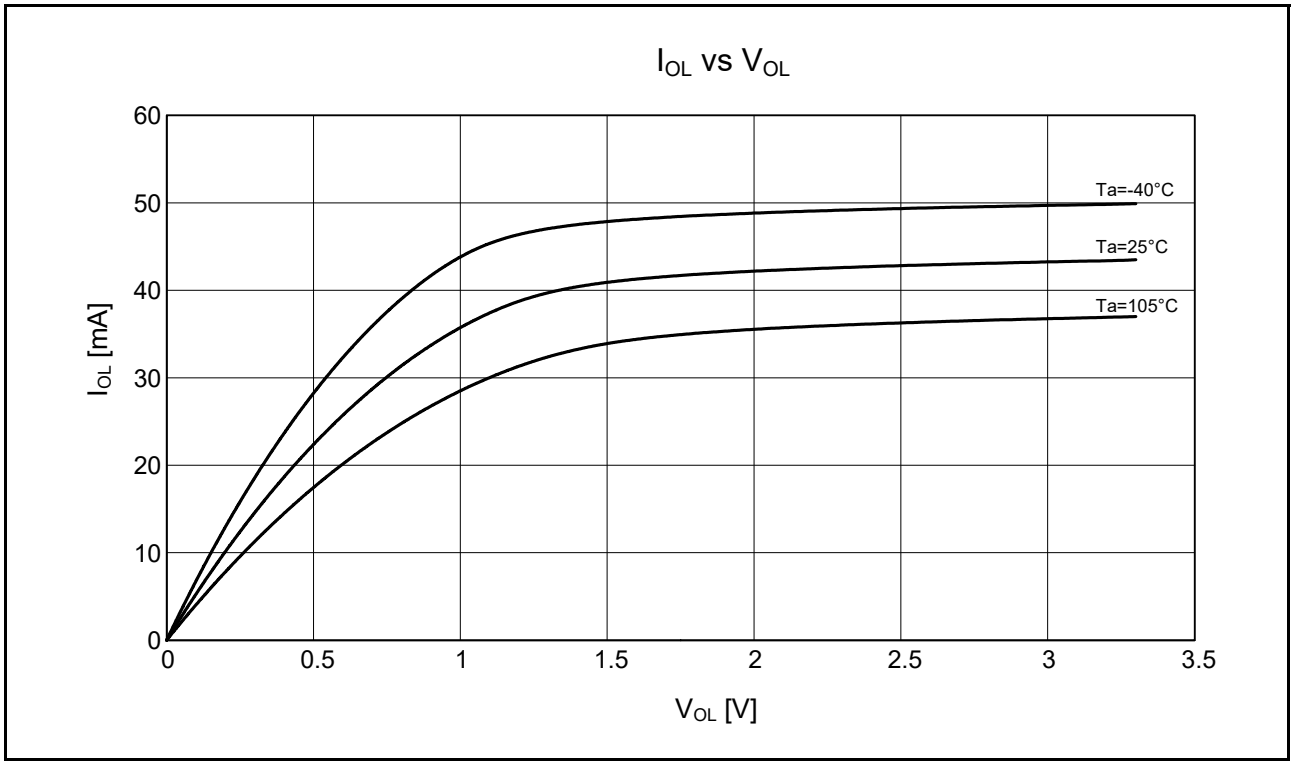


Figure 5.24 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

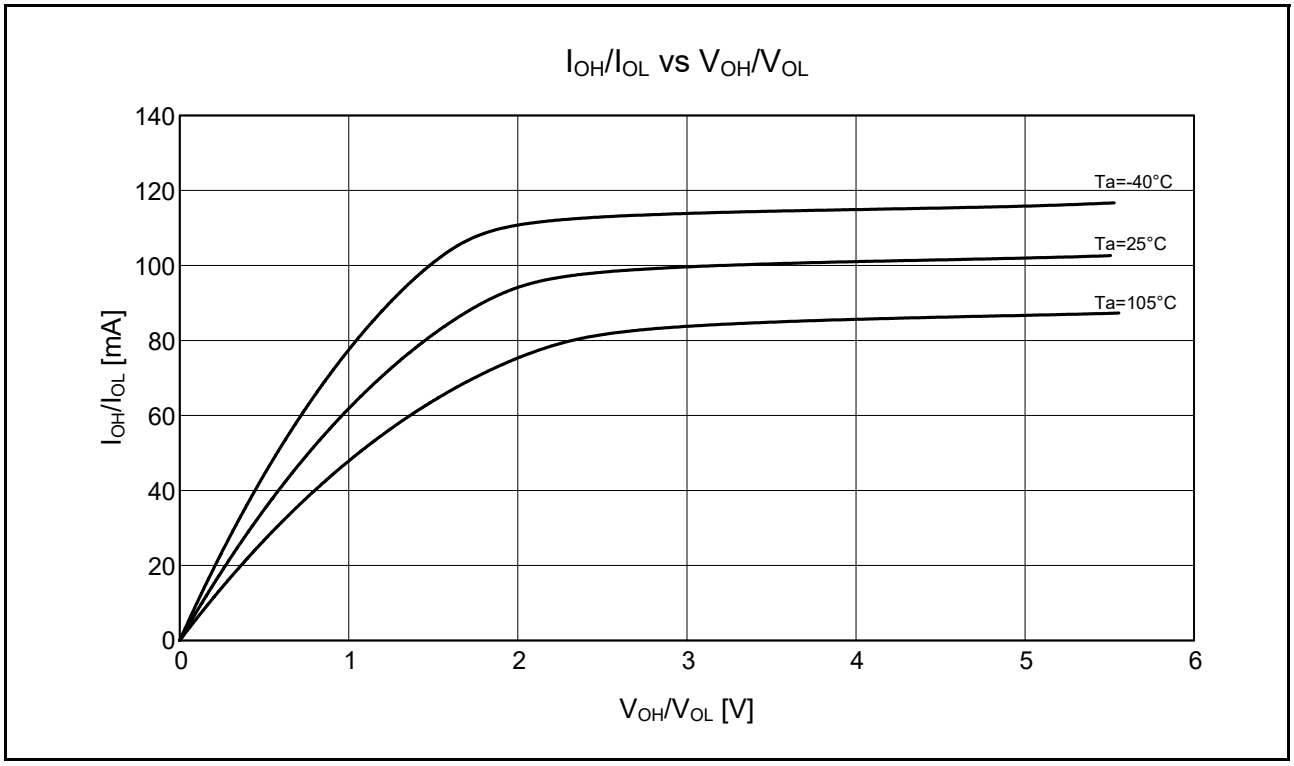


Figure 5.25 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.22 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*3		8	16	32	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 5.25, Clock Timing.

Table 5.23 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	
	Peripheral module clock (PCLKB)		8	12	12	
	Peripheral module clock (PCLKD)*3		8	12	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 5.25, Clock Timing

Table 5.24 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

Table 5.25 Clock Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.26
EXTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.27
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.28
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.29
HOCO clock oscillation frequency		f_{HOCO} (32 MHz)	31.52	32	32.48	MHz	T_a = –40 to + 85°C
			31.68	32	32.32		T_a = 0 to + 55°C
			31.36	32	32.64		T_a = –40 to +105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	30	μs	Figure 5.31
PLL input frequency*3		f_{PLLIN}	4	—	8	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	24	—	32	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.32
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
Sub-clock oscillator oscillation frequency*5		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 5.33

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Reference value when a 32.768-kHz resonator is used.
After changing the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 5. Only 32.768-kHz can be used.

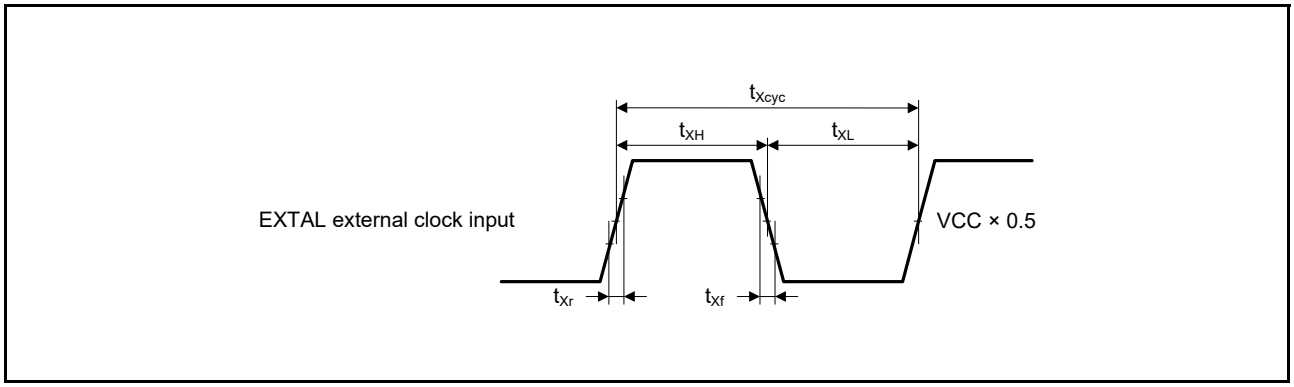


Figure 5.26 EXTAL External Clock Input Timing

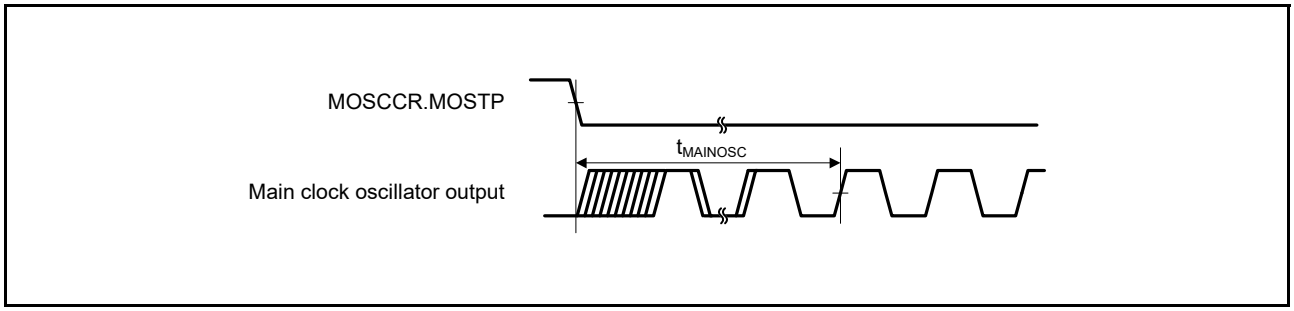


Figure 5.27 Main Clock Oscillation Start Timing

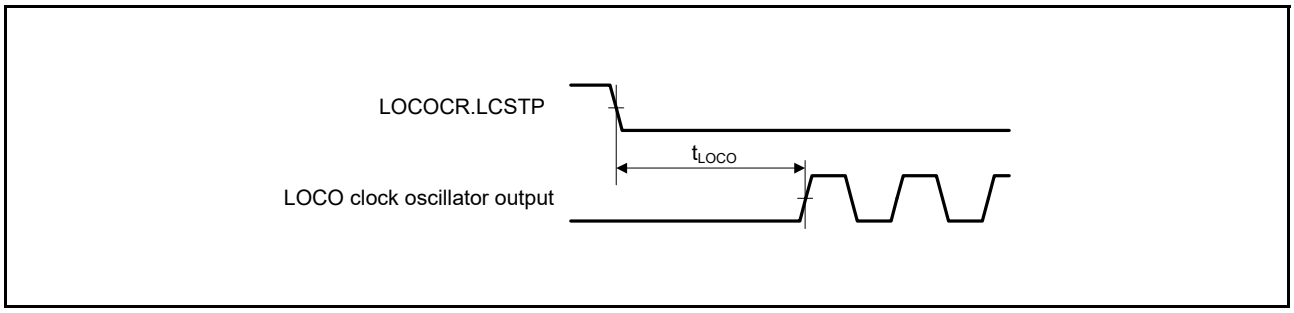


Figure 5.28 LOCO Clock Oscillation Start Timing

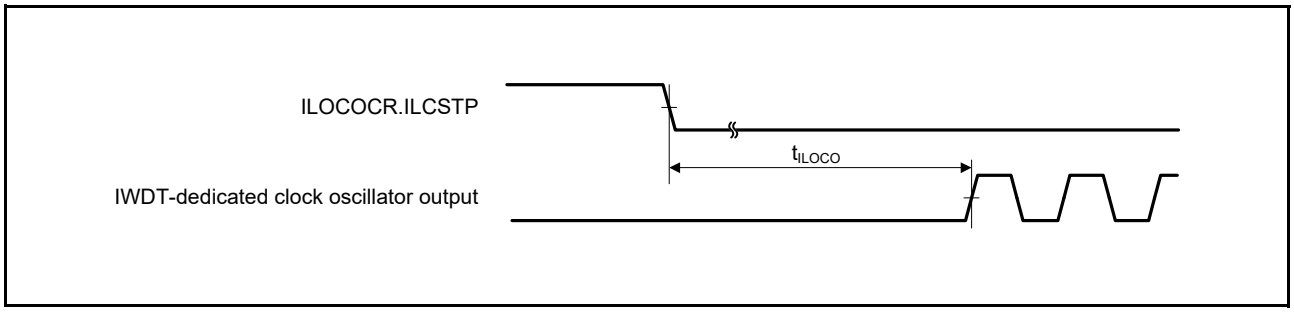


Figure 5.29 IWDT-Dedicated Clock Oscillation Start Timing

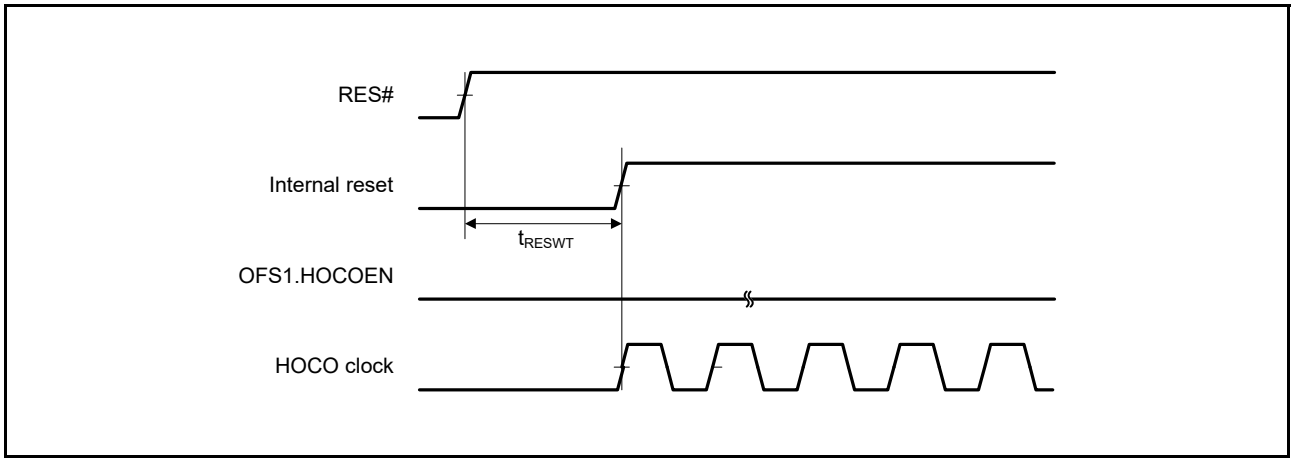


Figure 5.30 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

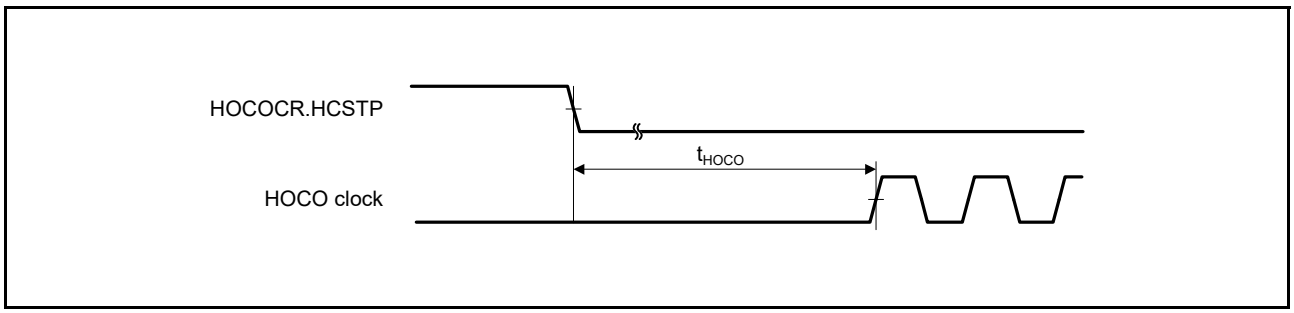


Figure 5.31 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

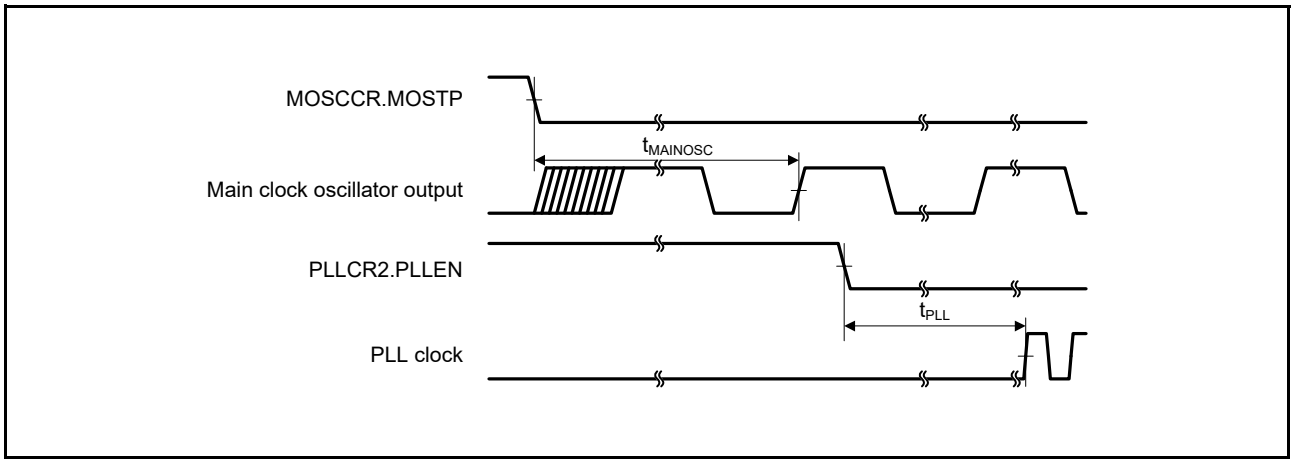


Figure 5.32 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

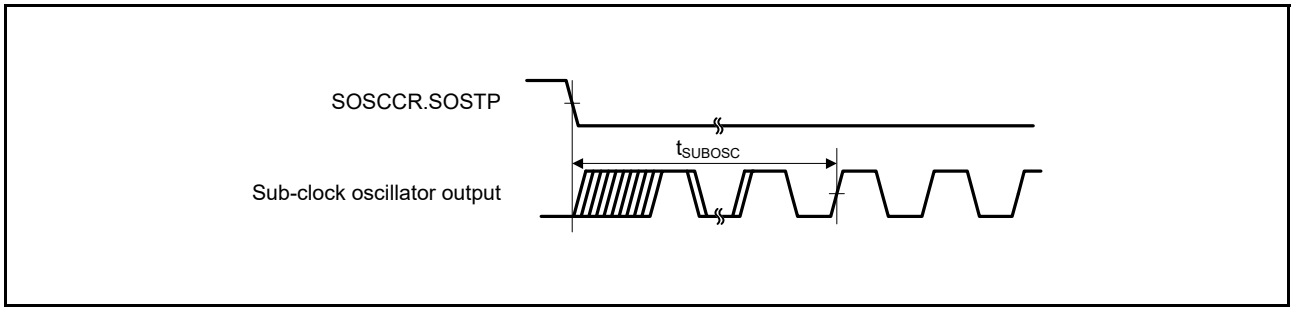


Figure 5.33 Sub-Clock Oscillation Start Timing

5.3.2 Reset Timing

Table 5.26 Reset Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.34
	Other than above	t_{RESW}	30	—	—	µs	Figure 5.35
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 5.34
	During fast startup time*2	t_{RESWT}	—	560	—	µs	
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	120	—	µs	Figure 5.35
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.36
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*3		t_{RESWT2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESWT2}	—	170	—	µs	

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.
Note 2. When OFS1.(LVDAS, FASTSTUP) = a value other than 11b.
Note 3. When IWDTCR.CKS[3:0] = 0000b.

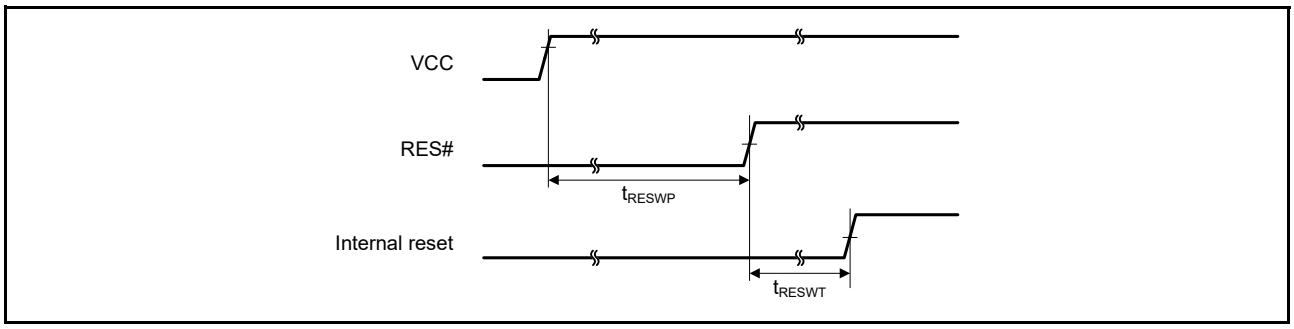


Figure 5.34 Reset Input Timing at Power-On

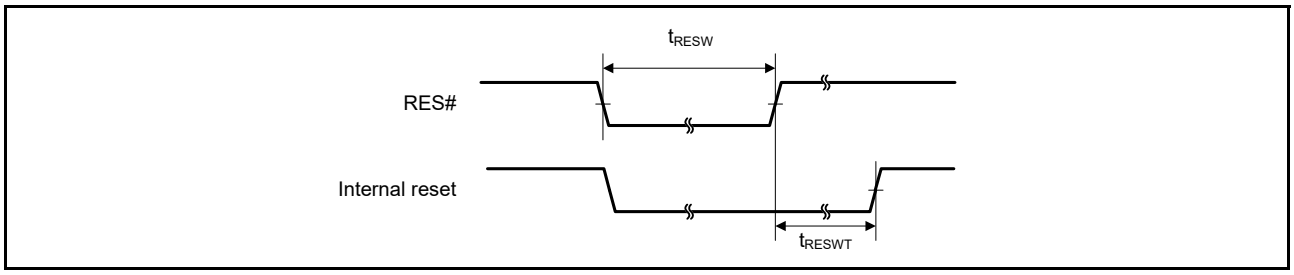


Figure 5.35 Reset Input Timing (1)

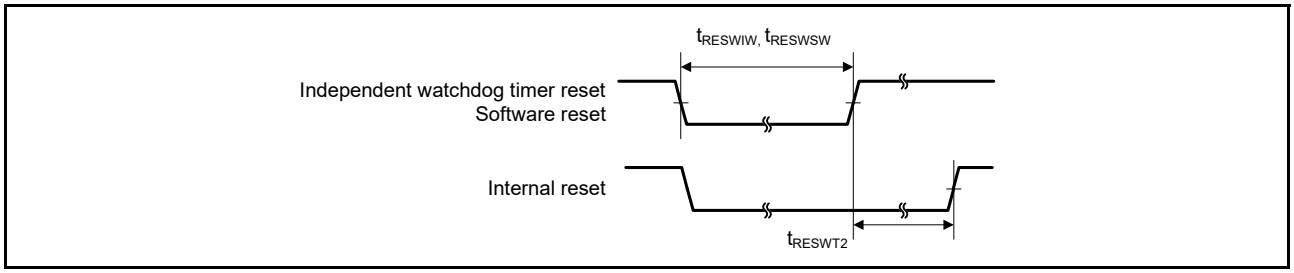


Figure 5.36 Reset Input Timing (2)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.27 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.37
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	35	50	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	70	95	µs	
		Sub-clock oscillator operating		t_{SBYSC}	—	650	800	µs	
		HOCO clock oscillator operating		t_{SBYHO}	—	40	55	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	40	55	µs	

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of PLL is 32 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 4. When the frequency of the external clock is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 5. When the frequency of PLL is 32 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 5.28 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.37
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		Sub-clock oscillator operating		t_{SBYSC}	—	600	750	µs	
		HOCO clock oscillator operating		t_{SBYHO}	—	40	50	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	5	7	µs	

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of PLL is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 4. When the frequency of the external clock is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 5. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 5.29 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 5.37

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

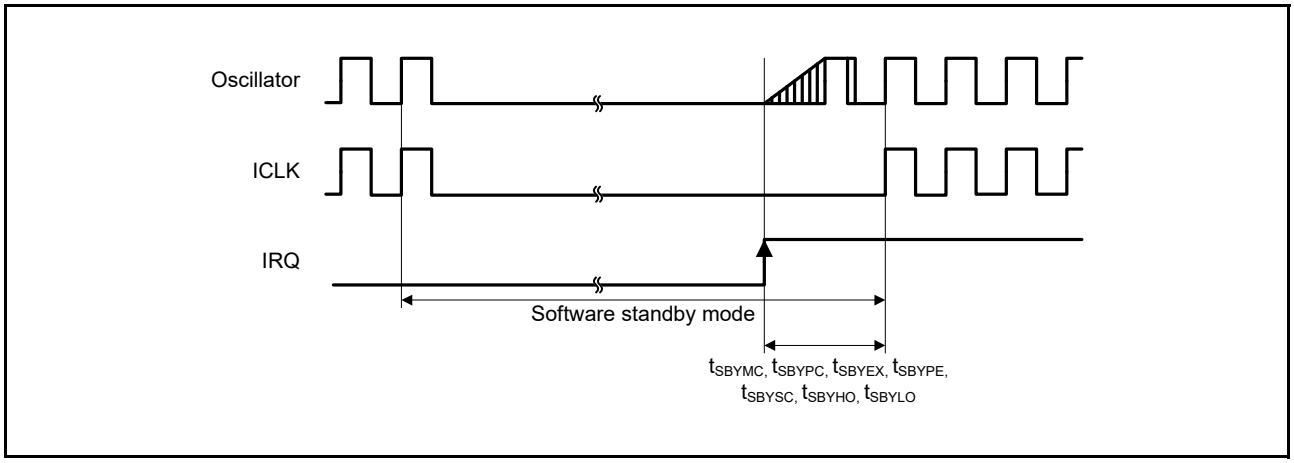


Figure 5.37 Software Standby Mode Recovery Timing

Table 5.30 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.38
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32.768 kHz.

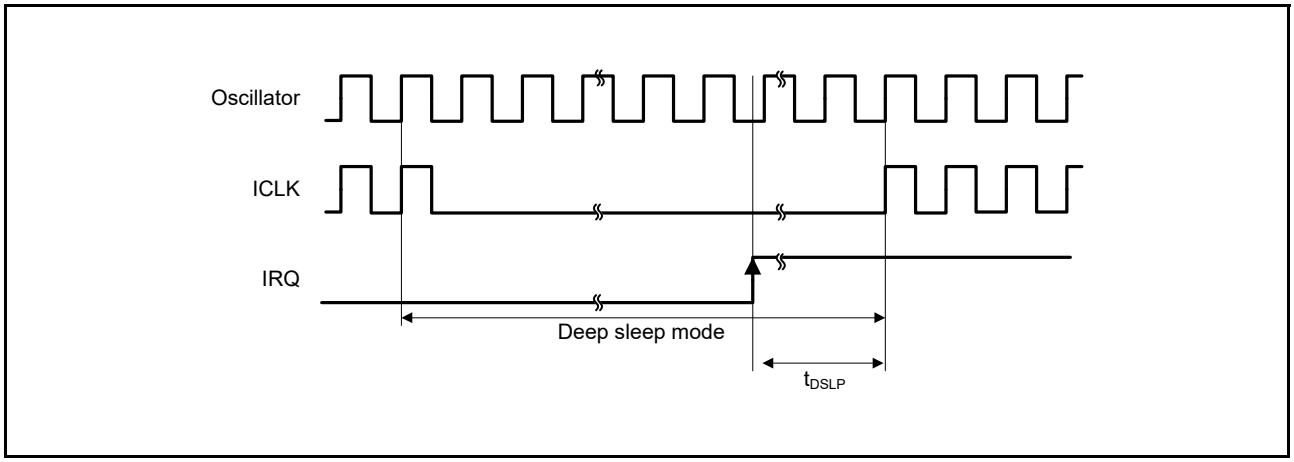


Figure 5.38 Deep Sleep Mode Recovery Timing

Table 5.31 Operating Mode Transition Time

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	215	—	µs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	185	—	µs

Note: Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.

5.3.4 Control Signal Timing

Table 5.32 Control Signal Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

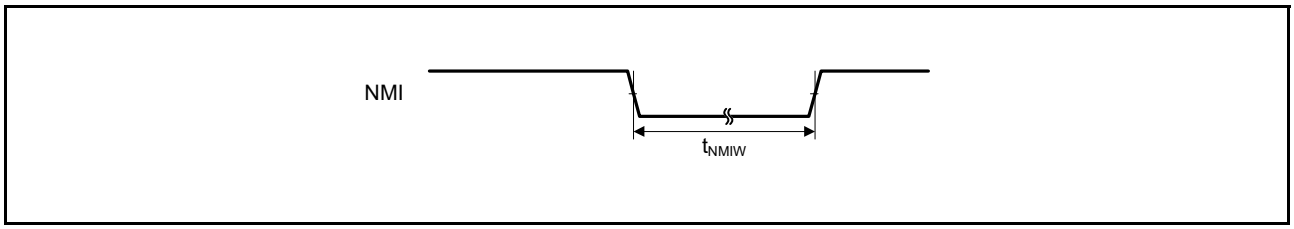


Figure 5.39 NMI Interrupt Input Timing

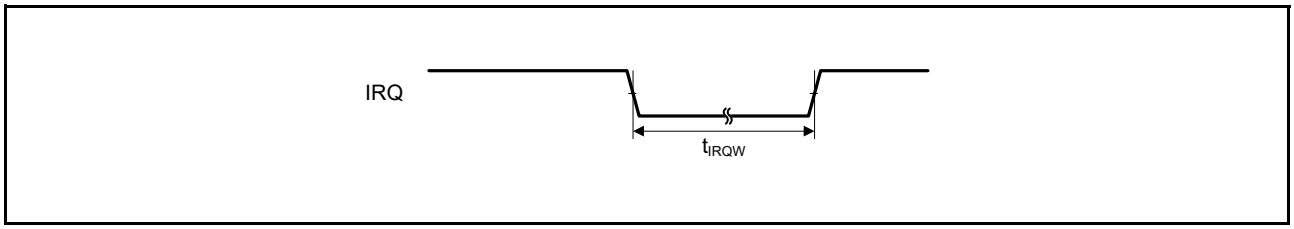


Figure 5.40 IRQ Interrupt Input Timing

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.33 Timing of On-Chip Peripheral Modules (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.41
MTU2	Input capture input pulse width		Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.42
			Both-edge setting		2.5	—		
	Input capture input rise/fall time			t_{TICr}, t_{TICf}	—	0.1	μs/V	
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.43
			Both-edge setting		2.5	—		
			Phase counting mode		2.5	—		
	Timer clock rise/fall time			t_{TCKr}, t_{TCKf}	—	0.1	μs/V	
POE2	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.44
	POE# input rise/fall time			t_{POEr}, t_{POEf}	—	0.1	μs/V	
TMR	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.45
			Both-edge setting		2.5	—		
	Timer clock rise/fall time			t_{TMCr}, t_{TMCf}	—	0.1	μs/V	
SCI	Input clock cycle time		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.46
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle time		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.47
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	2.7 V or above		—	65	ns	
			1.8 V or above		—	100	ns	
	Receive data setup time (master)	Clock synchronous	2.7 V or above	t_{RXS}	65	—	ns	
			1.8 V or above		90	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.48
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			
	CACREF input rise/fall time			$t_{CACREFr}$, $t_{CACREFf}$	—	0.1	μs/V	

Table 5.33 Timing of On-Chip Peripheral Modules (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
CLKOUT	CLKOUT pin output cycle*4	VCC = 2.7 V or above	t_{Ccyc}	62.5	—	ns	Figure 5.49
		VCC = 1.8 V or above		125			
	CLKOUT pin high pulse width*3	VCC = 2.7 V or above	t_{CH}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin low pulse width*3	VCC = 2.7 V or above	t_{CL}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	—	12	ns	
		VCC = 1.8 V or above			25		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	—	12	ns	
		VCC = 1.8 V or above			25		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle
Note 3. When the LOCO is selected as the clock output source (CKOCR.CKOSEL[3:0] bits = 0000b), set the clock output division ratio selection to divided by 2 (CKOCR.CKODIV[2:0] bits = 001b).
Note 4. When the XTAL external clock input or an oscillator is used with divided by 1 (CKOCR.CKOSEL[3:0] bits = 010b and CKOCR.CKODIV[2:0] bits = 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Table 5.34 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C, C = 30 pF, when high-drive output is selected by the drive capacity register

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 5.50
		Slave			8	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/ fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	0.1	µs/V	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.51 to Figure 5.54
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/ fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V or above		—	15	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.53, Figure 5.54
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.35 Timing of On-Chip Peripheral Modules (3)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.50
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.51, Figure 5.52
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	–10	—	ns	
		1.8 V or above		–20	—		
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.53, Figure 5.54
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.36 Timing of On-Chip Peripheral Modules (4)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.55
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.55
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

Table 5.37 Timing of On-Chip Peripheral Modules (5)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple I²C (Standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 5.55
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple I²C (Fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 5.55
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{Pcyc}: PCLK cycle

Note 1. C_b is the total capacitance of the bus lines.

Table 5.38 Timing of On-Chip Peripheral Modules (6)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Min.	Max.	Unit	Test Conditions
REMC	Increase of the operating clock frequency at a transition to software standby mode	—	1.5	%	REMCON1.CSRC[3:0] = x101b (with the HOCO clock/512 selected) HOFCR.HOFXIN = 1 (when the HOCO oscillation is set to be continued)
	The period for the change in the operating clock frequency at a transition to software standby mode	—	400	µs	

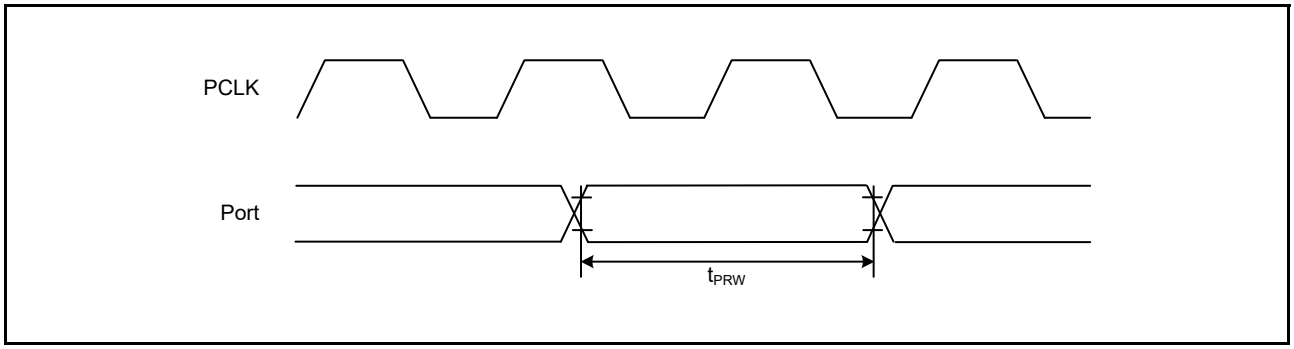


Figure 5.41 I/O Port Input Timing

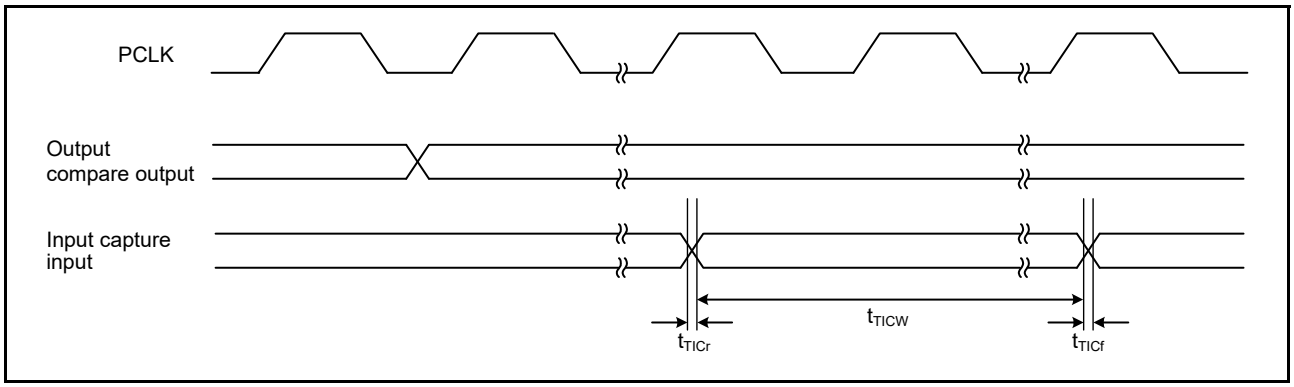


Figure 5.42 MTU2 Input/Output Timing

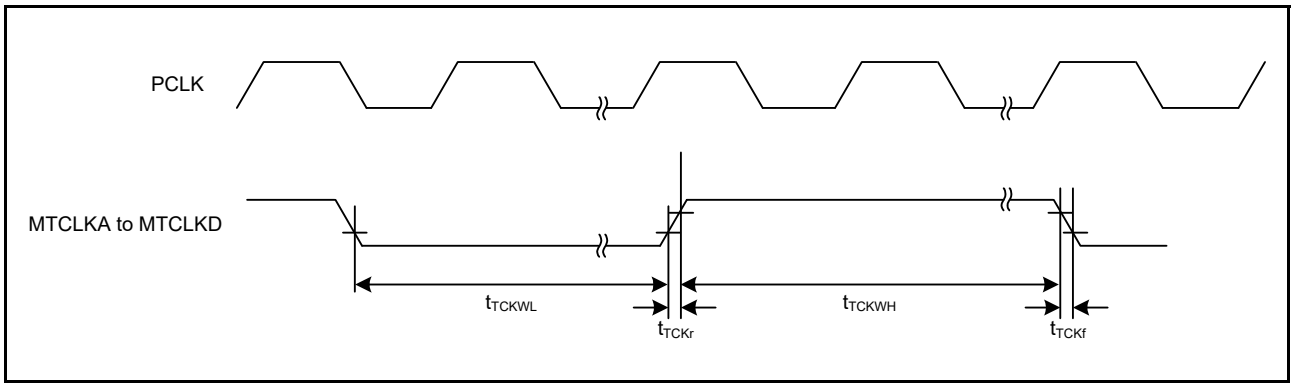


Figure 5.43 MTU2 Clock Input Timing

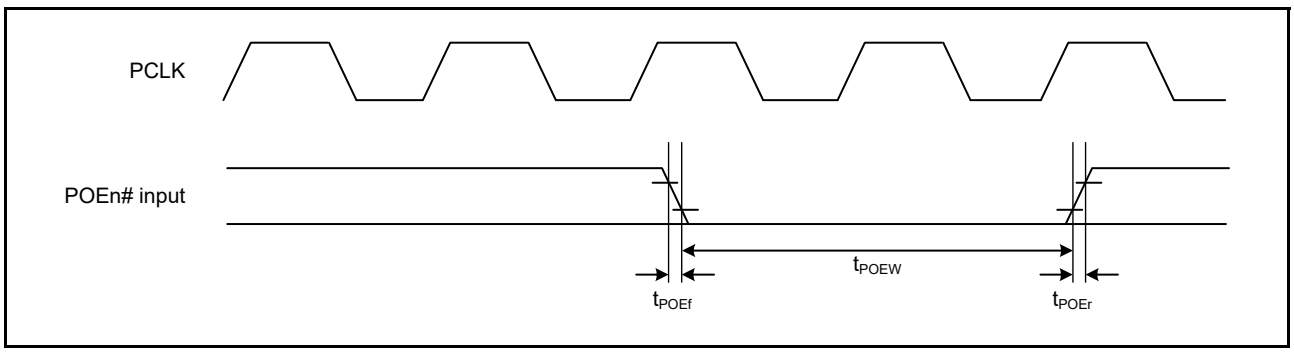


Figure 5.44 POE# Input Timing

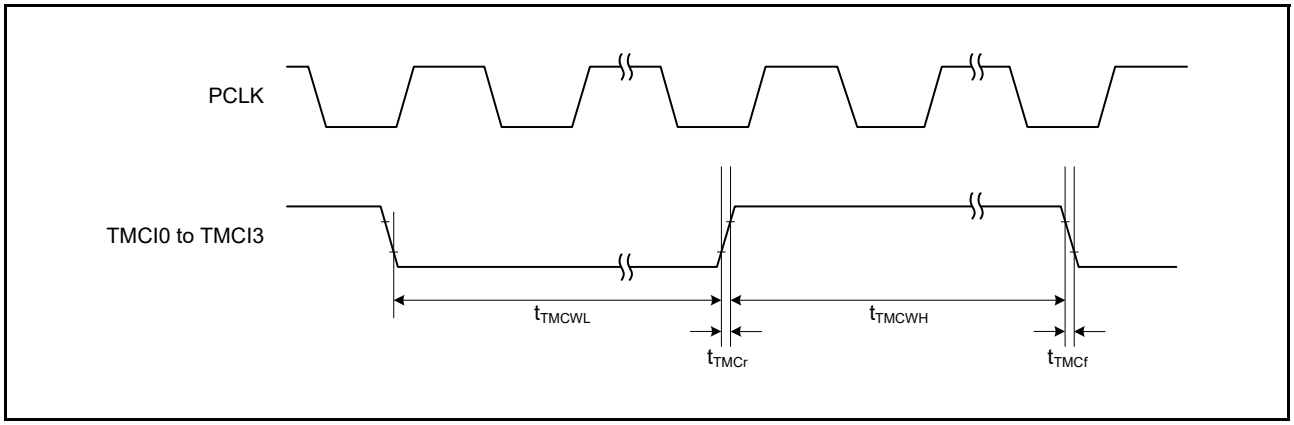


Figure 5.45 TMR Clock Input Timing

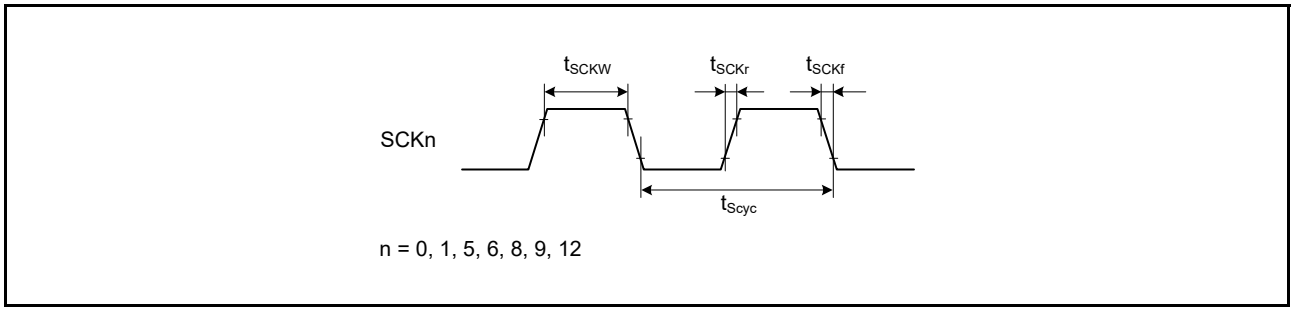


Figure 5.46 SCK Clock Input Timing

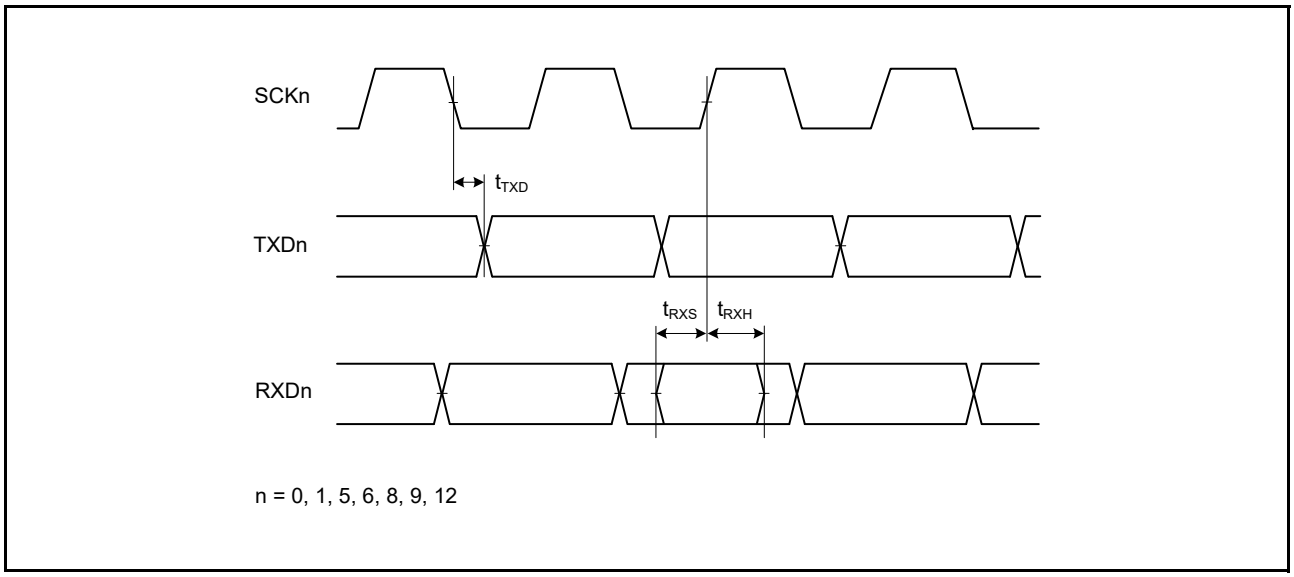


Figure 5.47 SCI Input/Output Timing: Clock Synchronous Mode

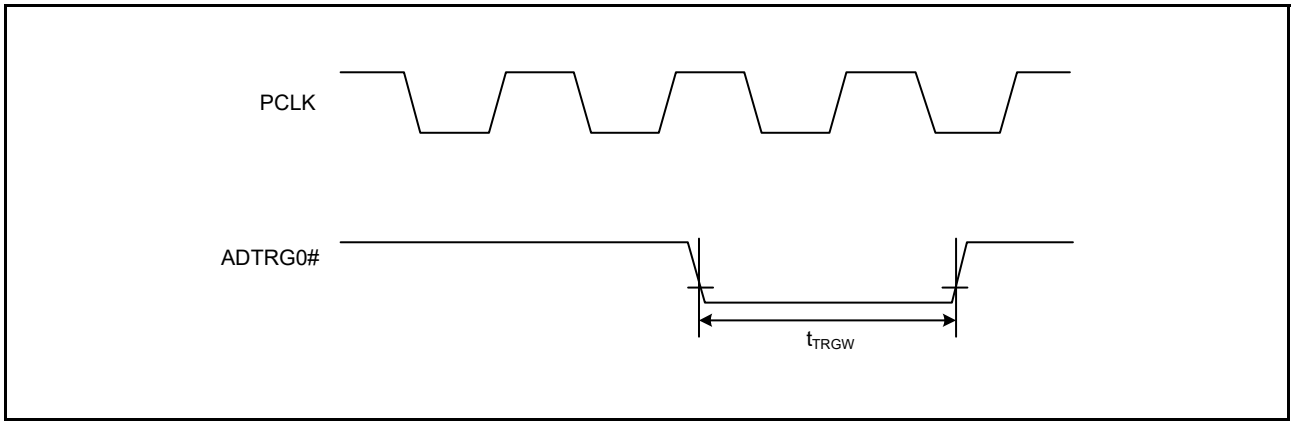


Figure 5.48 A/D Converter External Trigger Input Timing

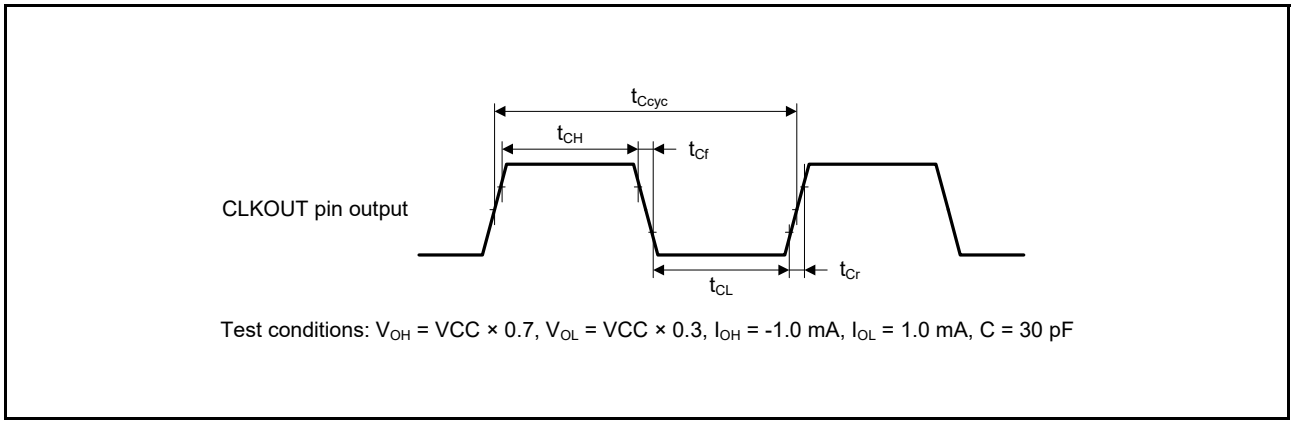


Figure 5.49 CLKOUT Output Timing

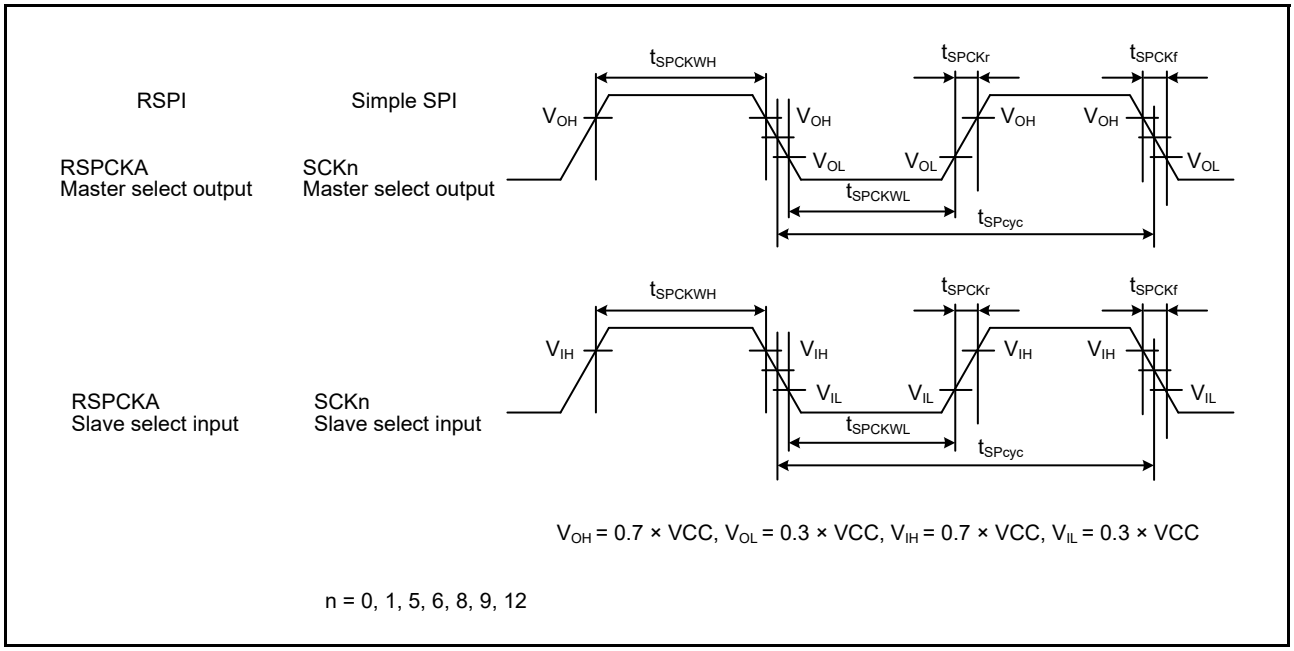


Figure 5.50 RSPI Clock Timing and Simple SPI Clock Timing

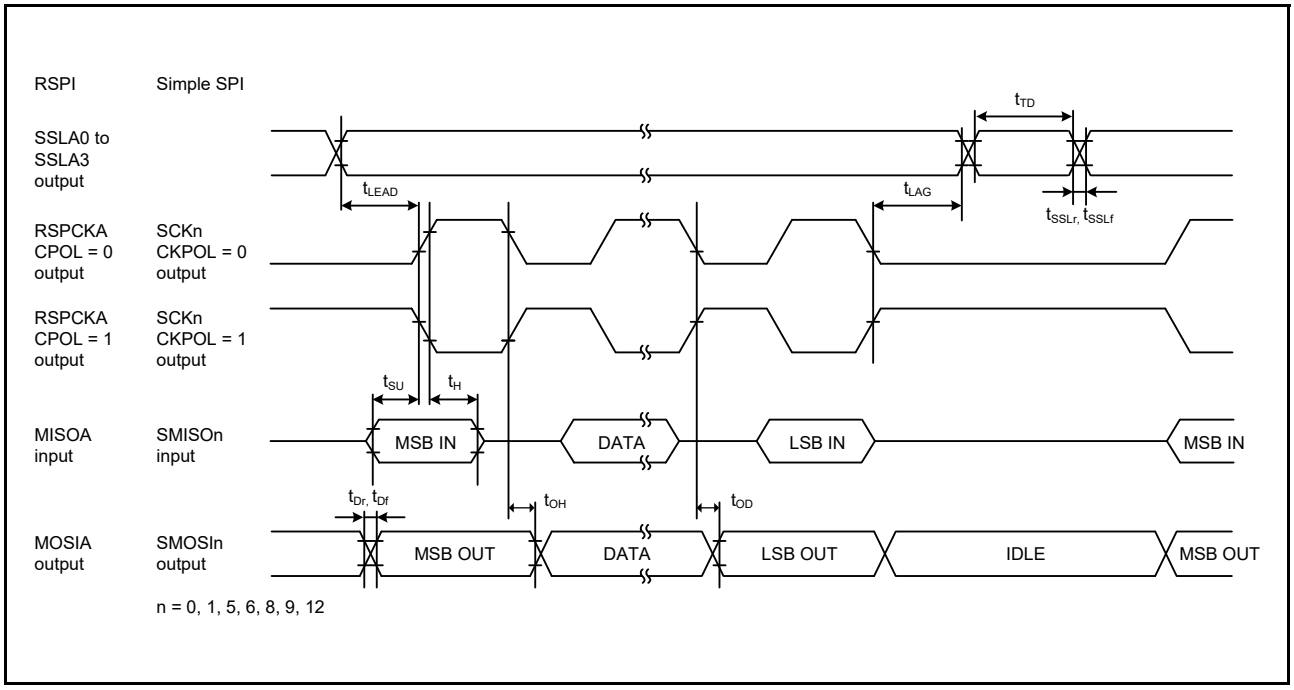


Figure 5.51 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

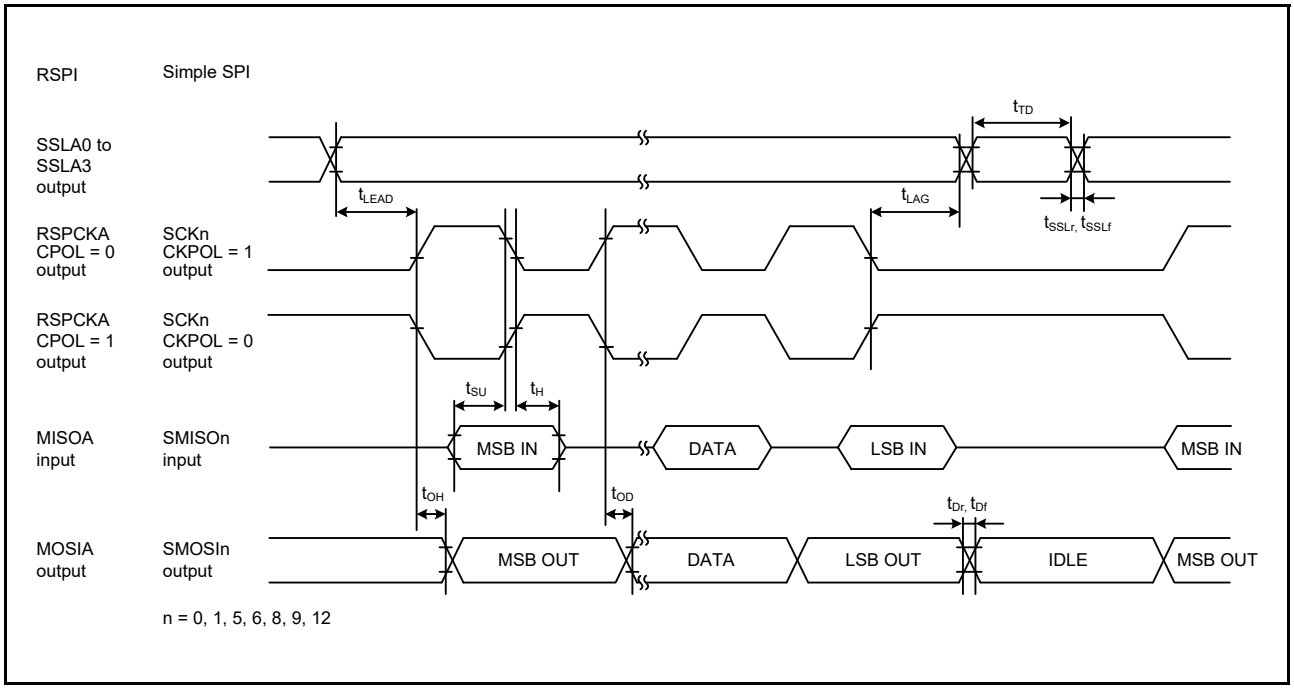


Figure 5.52 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

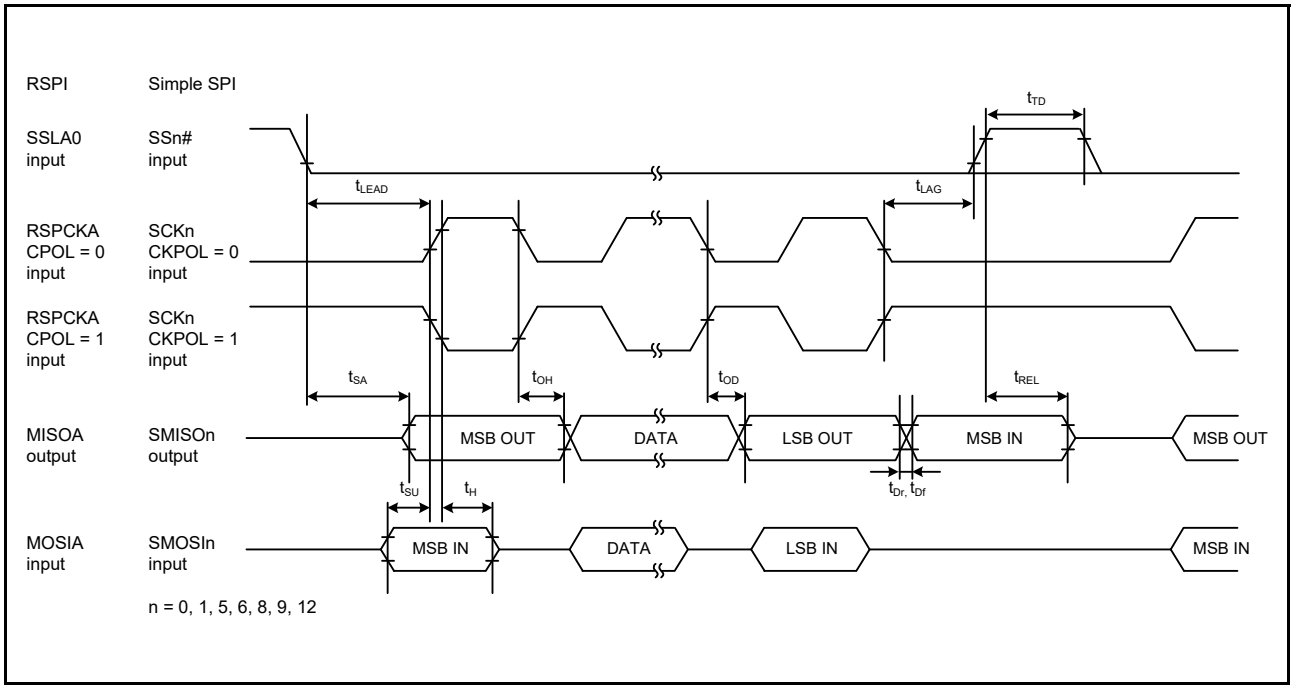


Figure 5.53 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

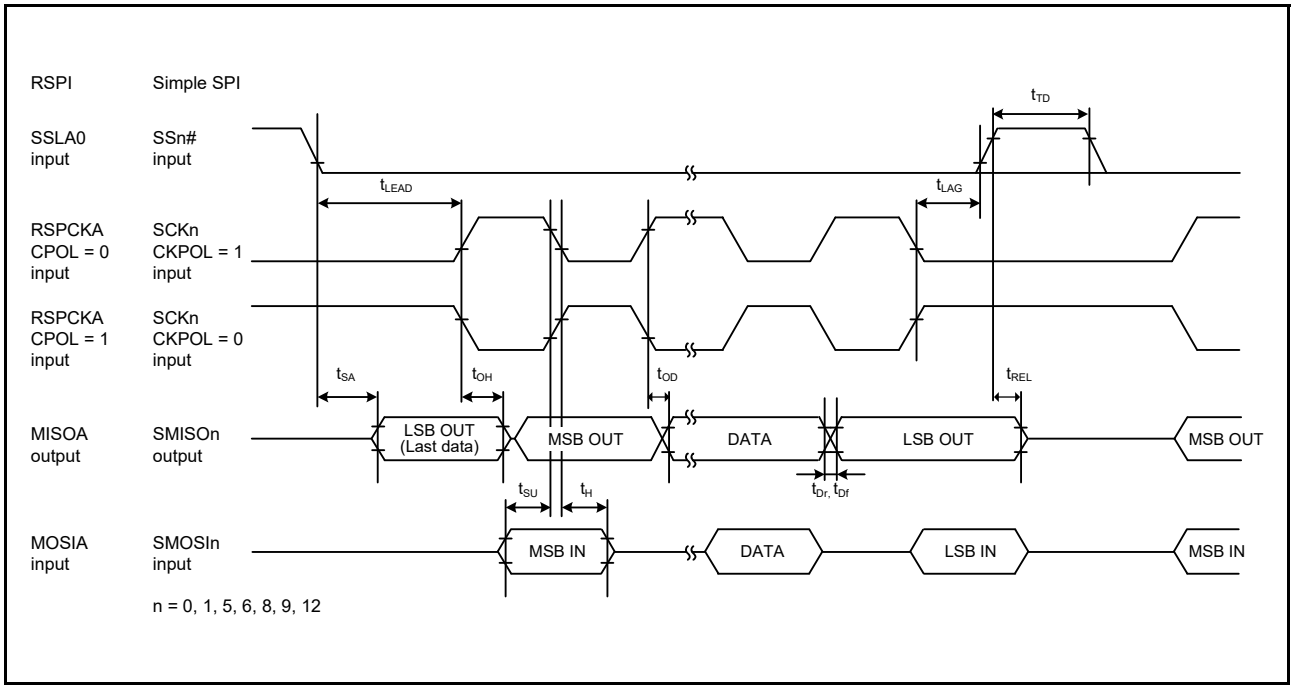
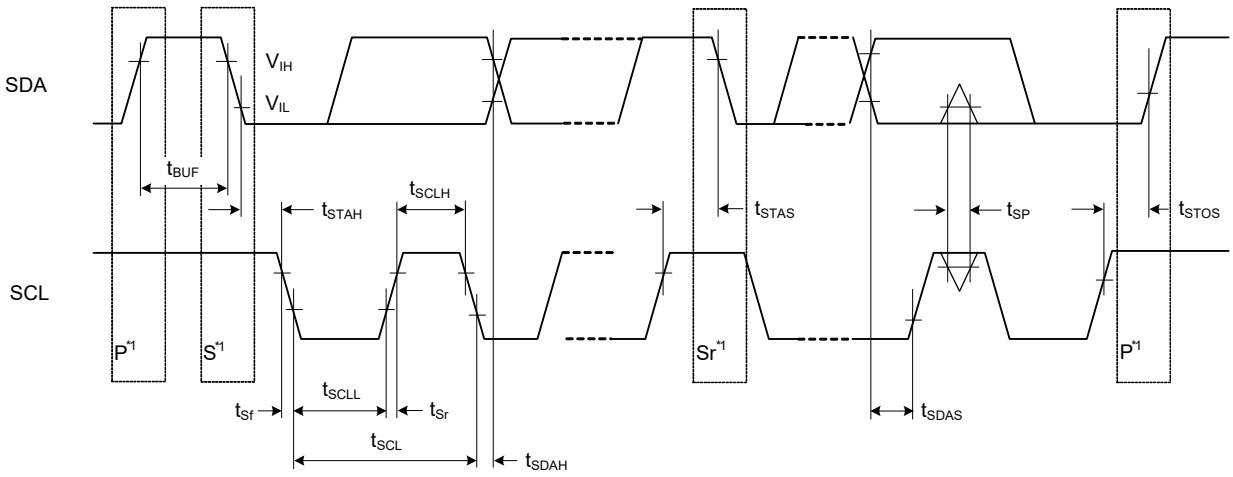


Figure 5.54 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.55 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

5.4 A/D Conversion Characteristics

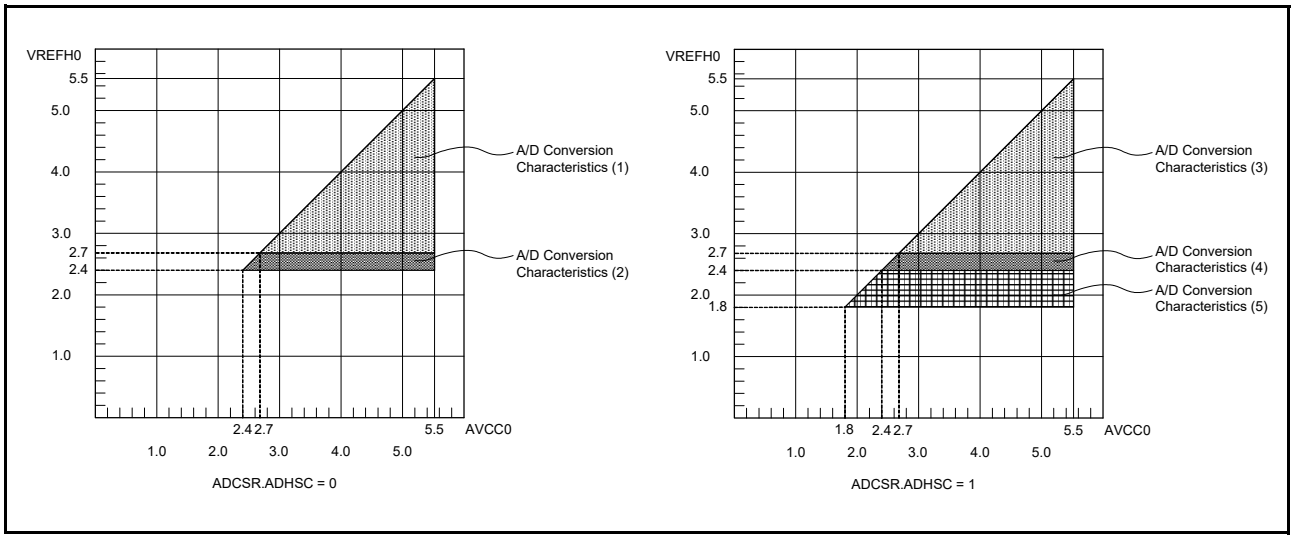


Figure 5.56 AVCC0 to VREFH0 Voltage Range

Table 5.39 A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 0.3 kΩ	1.41	—	—	µs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 0Dh
		2.25	—	—	µs	Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.40 A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ AVCC0 ≤ 5.5 V, 2.4 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 1.3 kΩ	2.82	—	—	µs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 0Dh
		4.5	—	—	µs	Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±4.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.41 A/D Conversion Characteristics (3)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	27	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 27 MHz)	Permissible signal source impedance (Max.) = 1.1 kΩ	2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Dh
		3	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.42 A/D Conversion Characteristics (4)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ AVCC0 ≤ 5.5 V, 2.4 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 2.2 kΩ	3.38	—	—	µs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Dh
		5.06	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.43 A/D Conversion Characteristics (5)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, 1.8 V ≤ VREFH0 ≤ AVCC0,
Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 kΩ	6.75	—	—	µs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Dh
		10.13	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.0	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.44 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.8 to 5.5 V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	

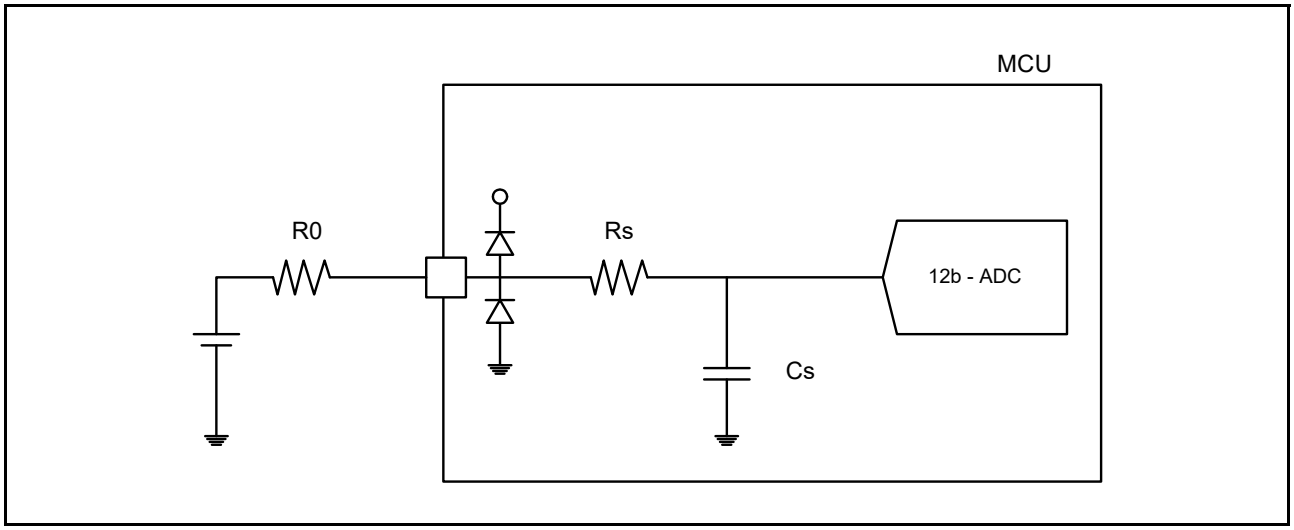


Figure 5.57 Equivalent Circuit

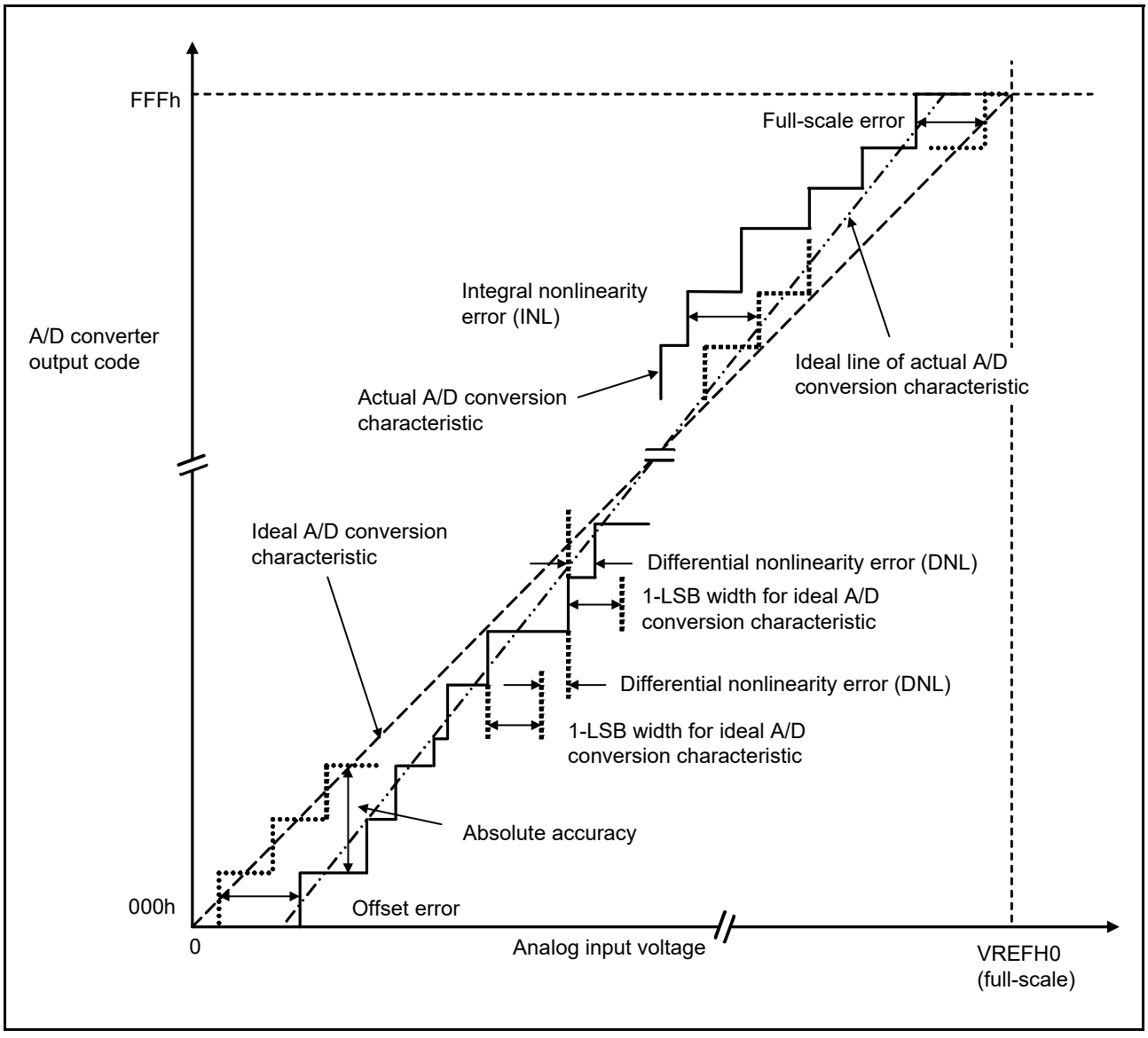


Figure 5.58 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.5 D/A Conversion Characteristics

Table 5.45 D/A Conversion Characteristics (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	—	8	Bit	
Conversion time	VCC=2.7 to 5.5 V	t_{DCONV}	—	—	3.0	µs	35-pF capacitive load
	VCC=1.8 to 2.7 V		—	—	6.0		
Absolute accuracy	VCC=2.4 to 5.5 V	—	—	—	±3.0	LSB	2-MΩ resistive load
	VCC=1.8 to 2.4 V	—	—	—	±3.5		
	VCC=2.4 to 5.5 V	—	—	—	±2.0	LSB	4-MΩ resistive load
	VCC=1.8 to 2.4 V	—	—	—	±2.5		
RO output resistance		—	—	6.4	—	kΩ	

5.6 Temperature Sensor Characteristics

Table 5.46 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

5.7 Comparator Characteristics

Table 5.47 Comparator Characteristics

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB1 input reference voltage		VREF	0	—	VCC – 1.4	V	
CMPB0 to CMPB1 input voltage		VI	–0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	µs	VCC = 3 V, input slew rate ≥ 50 mV/µs
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	µs	
	Comparator low-speed mode	Td	—	—	5.0	µs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	VCC × 0.76	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	VCC × 0.24	—	V	
Operation stabilization wait time		Tcmp	100	—	—	µs	

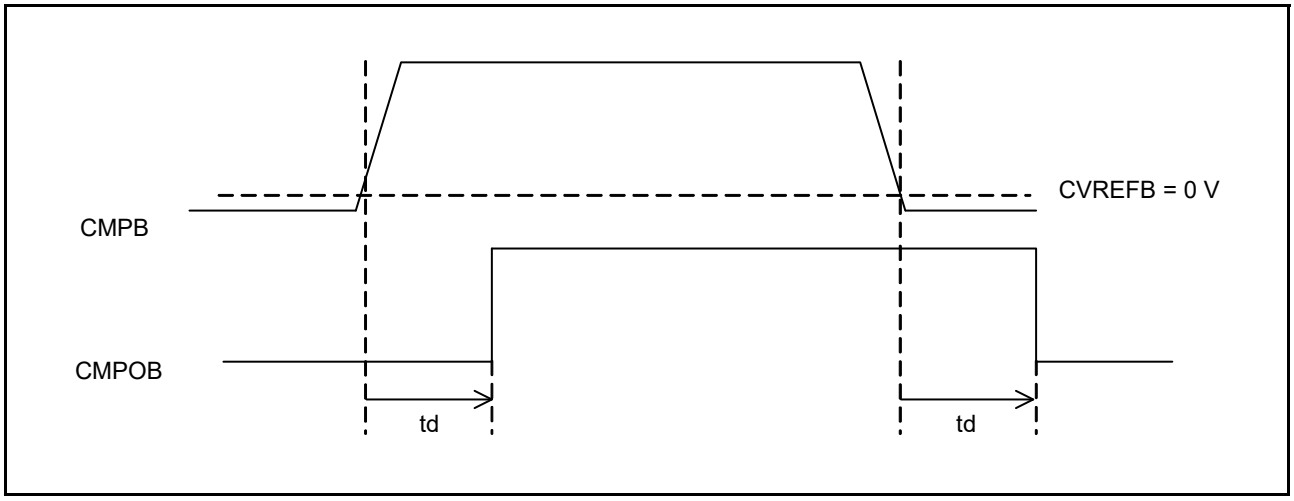


Figure 5.59 Comparator Output Delay Time in Comparator High-Speed Mode and Low-Speed Mode

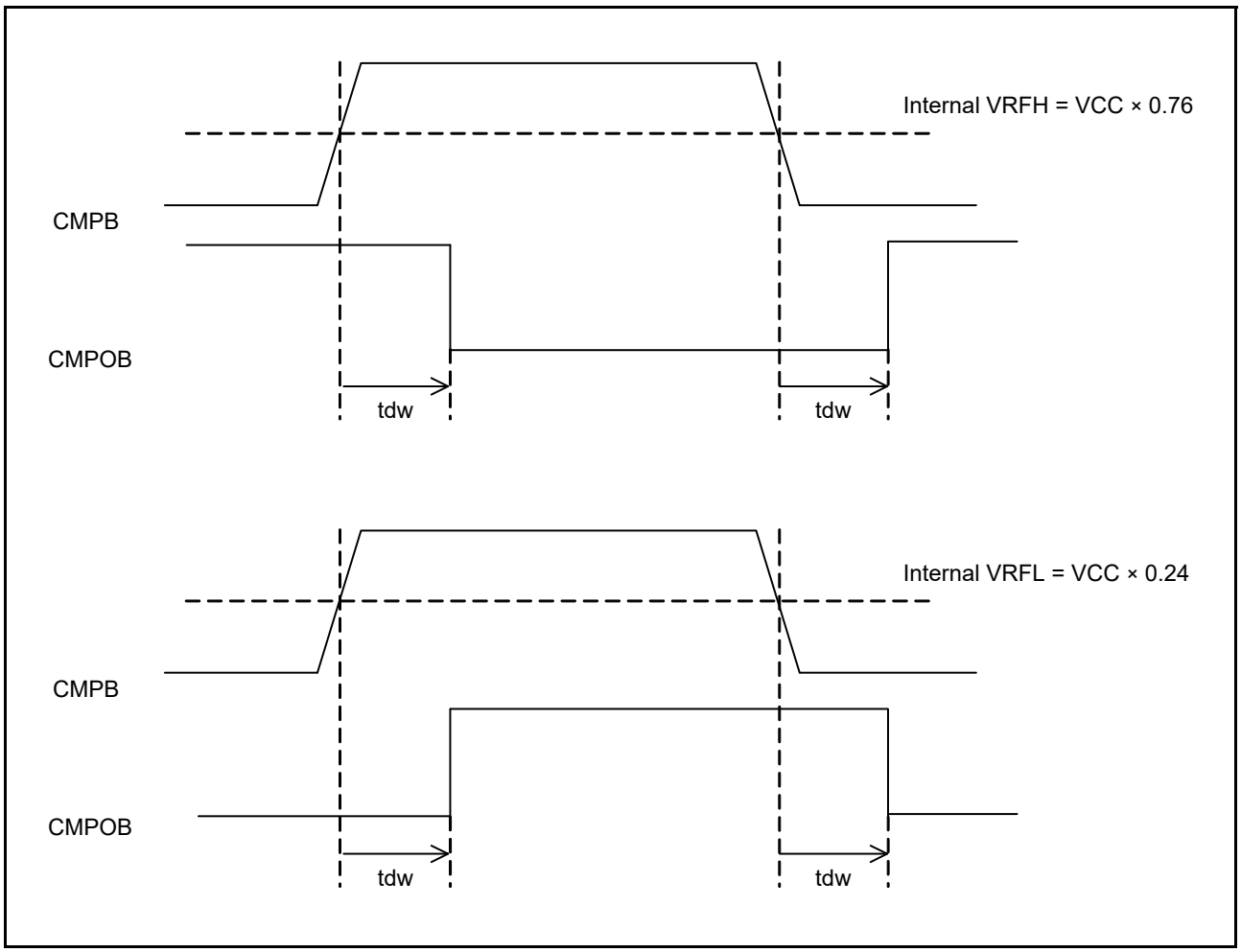


Figure 5.60 Comparator Output Delay Time in High-Speed Mode with Window Function Enabled

5.8 CTSU Characteristics

Table 5.48 CTSU Characteristics

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin		C_{tscap}	9	10	11	nF	
TS pin capacitive load		C_{base}	—	—	50	pF	
Permissible output high/low current	P12 to P17, P20 to P27, P30 to P35, P50 to P55, PB1 to PB7, PC0 to PC7, PH0 to PH3	$\lvert \Sigma I_{OH} \rvert$ $+\Sigma I_{OL}$	—	—	24	mA	When VXSEL = 0
	PA0 to PA6, PB0, PD0 to PD2, PE0 to PE5		—	—	16	mA	[Products with 128 Kbytes of flash memory or less (except for 100-pin packages] When VXSEL = 0
	PA0 to PA7, PB0, PD0 to PD7, PE0 to PE7		—	—	12	mA	[Products with at least 256 Kbytes of flash memory or 100-pin packages] When VXSEL = 0

5.9 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.49 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 5.61, Figure 5.62
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	Figure 5.63 At falling edge VCC
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
		V_{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 5.64 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.58	2.67		
		V_{det1_A}	2.37	2.48	2.57		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.86	1.96	2.06		
		V_{det1_D}	1.80	1.86	1.96		

Table 5.49 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*3	V_{det2_0}*4	4.08	4.29	4.48	V	Figure 5.65 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet0_n denotes the value of the LVDS1[1:0] bits.

Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.

Note 4. Vdet2_0 selection can be used only when the CMPA2 pin input voltage is selected, and cannot be used when the power supply voltage (VCC) is selected.

Table 5.50 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup*1	t_{POR}	—	9.1	—	ms	Figure 5.62
	During fast startup time*2	t_{POR}	—	1.6	—		
Wait time after voltage monitoring 0 reset cancellation	Power-on voltage monitoring 0 reset disabled*1	t_{LVD0}	—	568	—	µs	Figure 5.63
	Power-on voltage monitoring 0 reset enabled*2		—	100	—		
Wait time after voltage monitoring 1 reset cancellation		t_{LVD1}	—	100	—	µs	Figure 5.64
Wait time after voltage monitoring 2 reset cancellation		t_{LVD2}	—	100	—	µs	Figure 5.65
Response delay time		t_{det}	—	—	350	µs	Figure 5.61
Minimum VCC down time*3		t_{VOFF}	350	—	—	µs	Figure 5.61, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.62, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	300	µs	Figure 5.64, Figure 5.65
Hysteresis width (power-on rest (POR))		V_{PORH}	—	110	—	mV	
Hysteresis width (LVD0, LVD1, and LVD2)		V_{LVH}	—	70	—	mV	Vdet0_0 to Vdet0_3 selected
			—	70	—		Vdet1_0 to Vdet1_4 selected
			—	60	—		Vdet1_5 to 9 selected
			—	50	—		Vdet1_A to B selected
			—	40	—		Vdet1_C to D selected
			—	60	—		LVD2 selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) ≠ 11b.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

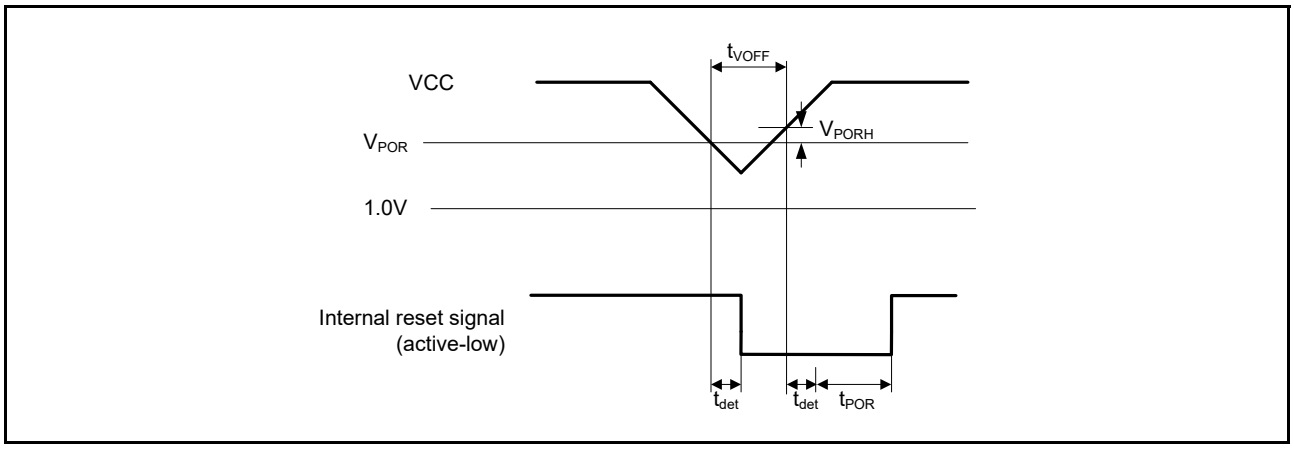
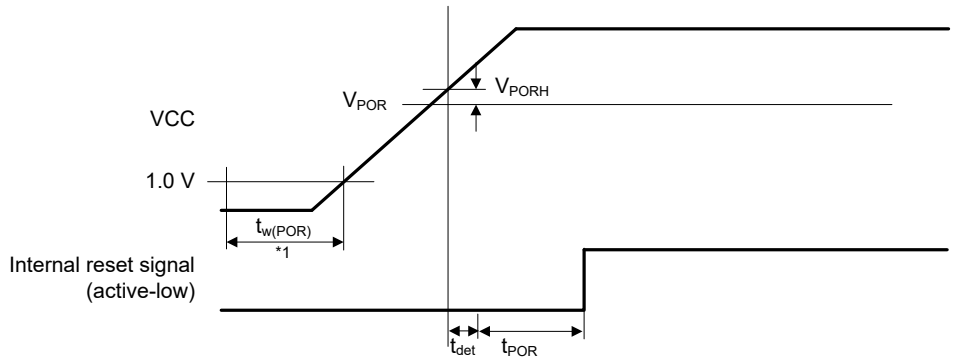


Figure 5.61 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 5.62 Power-On Reset Timing

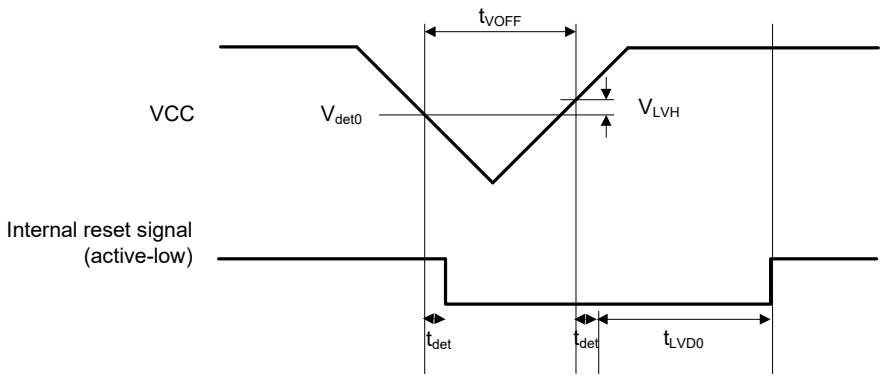


Figure 5.63 Voltage Detection Circuit Timing (V_{det0})

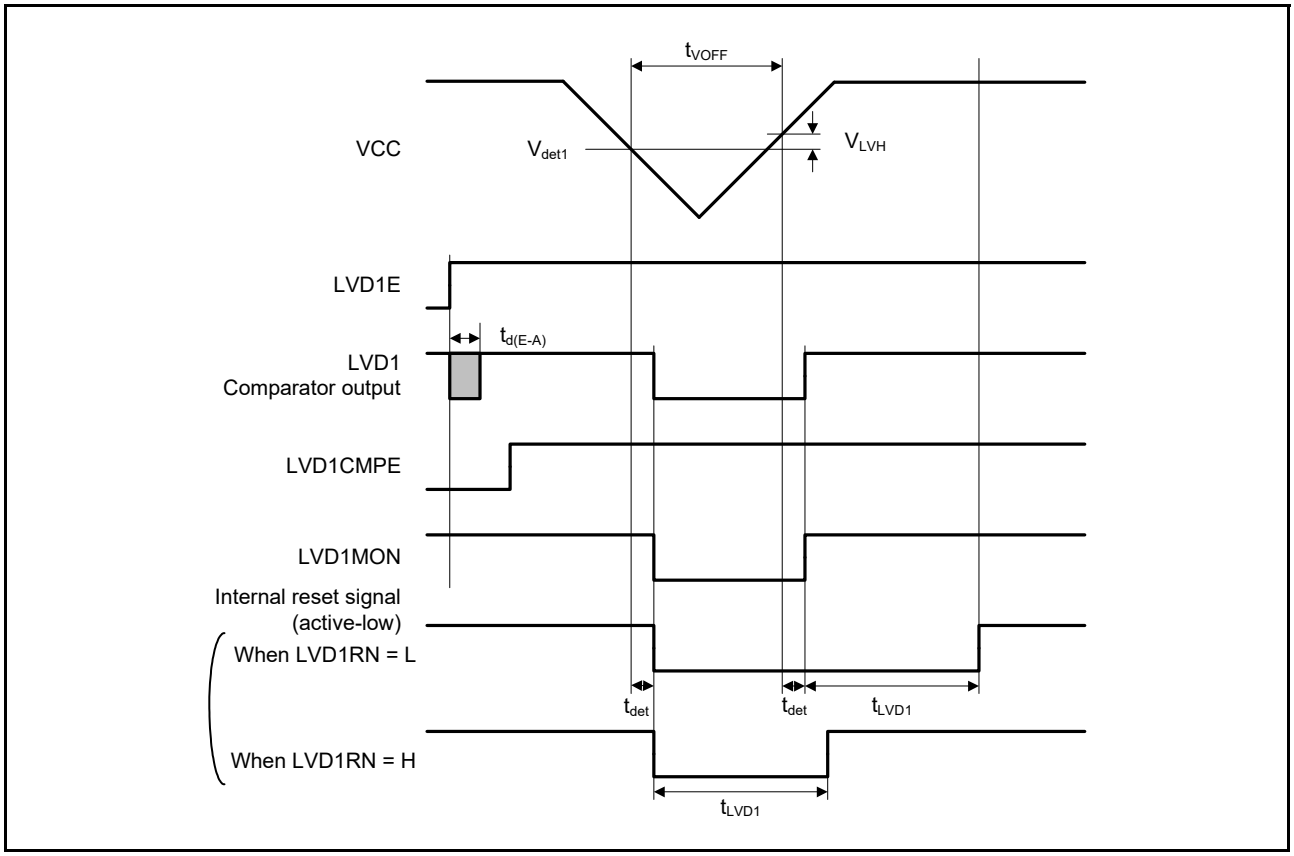


Figure 5.64 Voltage Detection Circuit Timing (V_{det1})

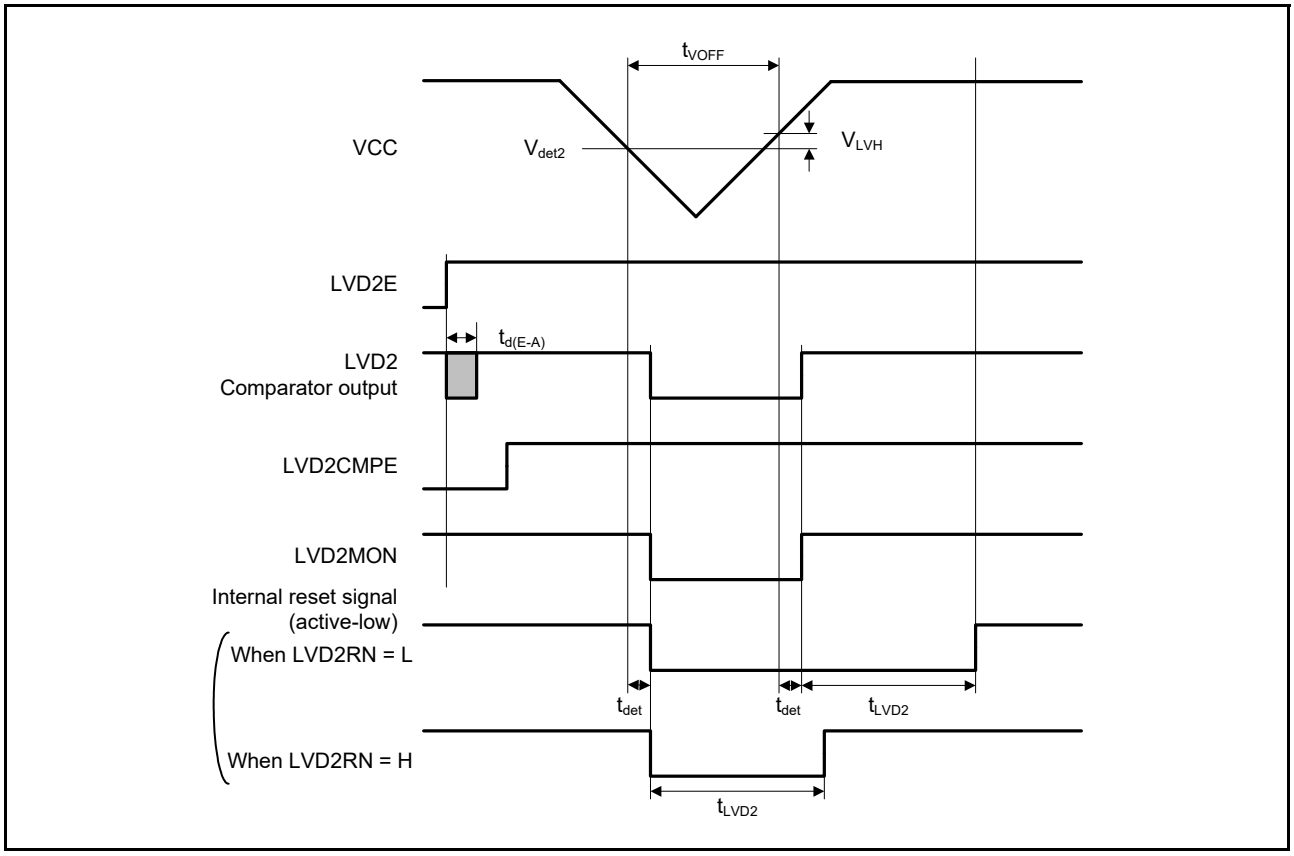


Figure 5.65 Voltage Detection Circuit Timing (V_{det2})

5.10 Oscillation Stop Detection Timing

Table 5.51 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.66

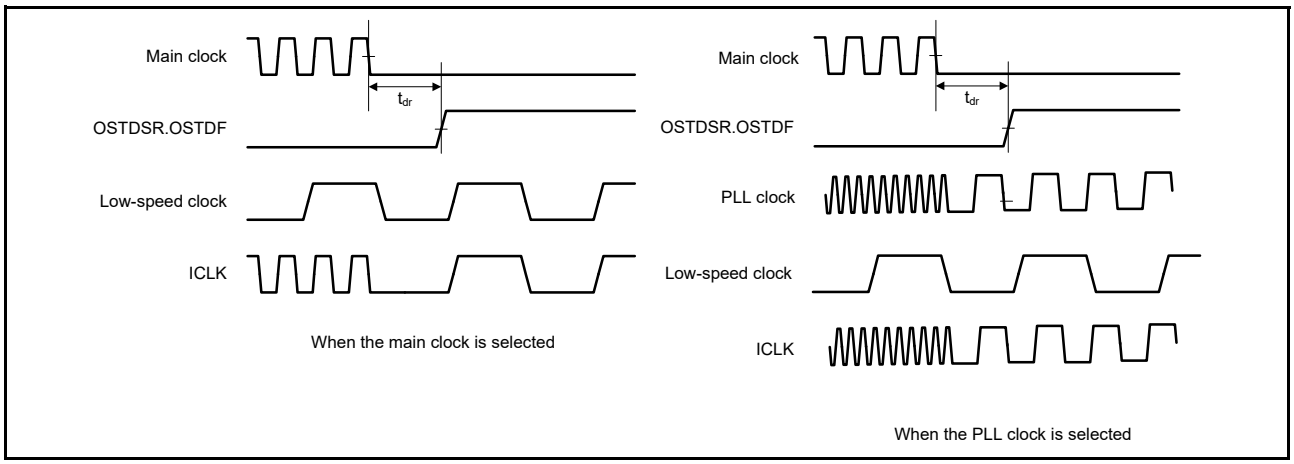


Figure 5.66 Oscillation Stop Detection Timing

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.52 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data retention	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 5.53 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t_{P4}	—	103	931	—	52	489	µs
Erasure time	1-Kbyte	t_{E1K}	—	8.23	267	—	5.48	214	ms
	256-Kbyte	t_{E256K}	—	407	928	—	39	457	ms
Blank check time	4-byte	t_{BC4}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{BC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t_{SED}	—	—	21.6	—	—	12.8	µs
Start-up area switching setting time		t_{SAS}	—	12.6	543	—	6.16	432	ms
Access window setting time		t_{AWS}	—	12.6	543	—	6.16	432	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
ROM mode transition wait time 2		t_{MS}	5	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 5.54 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t_{P4}	—	143	1330	—	96.8	932	µs
Erasure time	1-Kbyte	t_{E1K}	—	8.3	269	—	5.85	219	ms
	256-Kbyte	t_{E256K}	—	407	928	—	93	520	ms
Blank check time	4-byte	t_{BC4}	—	—	78	—	—	50	µs
	1-Kbyte	t_{BC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t_{SED}	—	—	33.6	—	—	25.6	µs
Start-up area switching setting time		t_{SAS}	—	13.2	549	—	7.6	445	ms
Access window setting time		t_{AWS}	—	13.2	549	—	7.6	445	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
ROM mode transition wait time 2		t_{MS}	3	—	—	3	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%.

5.12 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 5.55 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	
Data retention	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	T_a = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2, *3	—	Year	T_a = +25°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 5.56 E2 DataFlash Characteristics (2): high-speed operating mode

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	86	761	—	40.5	374	µs
Erasure time	1-Kbyte	t_{DE1K}	—	17.4	456	—	6.15	228	ms
	8-Kbyte	t_{DE8K}	—	60.4	499	—	9.3	231	ms
Blank check time	1-byte	t_{DBC1}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{DBC1K}	—	—	1.58	—	—	0.127	µs
Erase operation forcible stop time		t_{DSED}	—	—	21.5	—	—	12.8	µs
DataFlash STOP recovery time		t_{DSTOP}	5.0	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 5.57 E2 DataFlash Characteristics (3): middle-speed operating mode

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

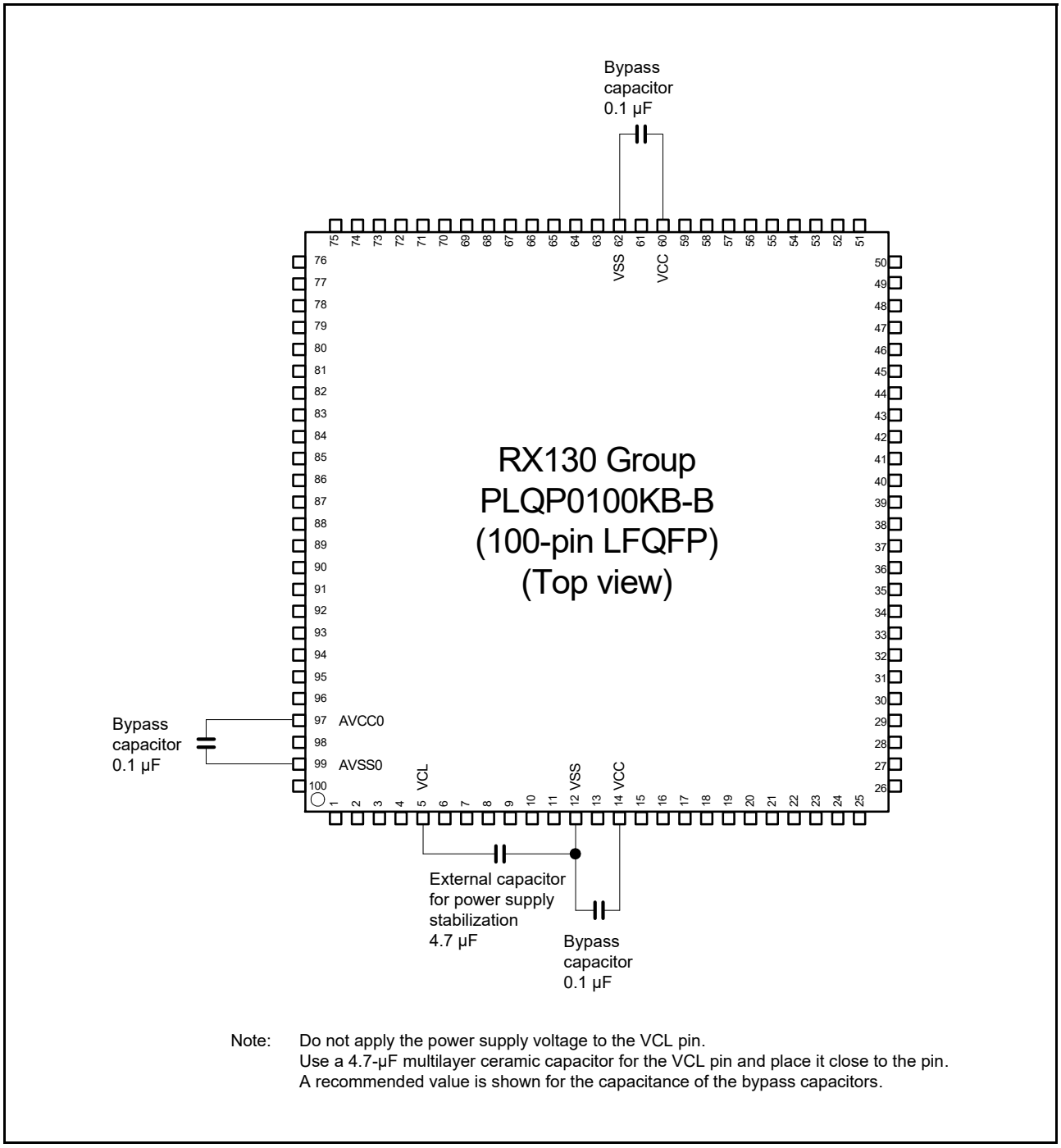
Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	126	1160	—	85.4	818	µs
Erasure time	1-Kbyte	t_{DE1K}	—	17.5	457	—	7.76	259	ms
	8-Kbyte	t_{DE8K}	—	60.5	500	—	4.2	66.9	ms
Blank check time	1-byte	t_{DBC1}	—	—	78	—	—	50	µs
	1-Kbyte	t_{DBC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t_{DSED}	—	—	33.5	—	—	25.5	µs
DataFlash STOP recovery time		t_{DSTOP}	720	—	—	720	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

5.13 Usage Notes

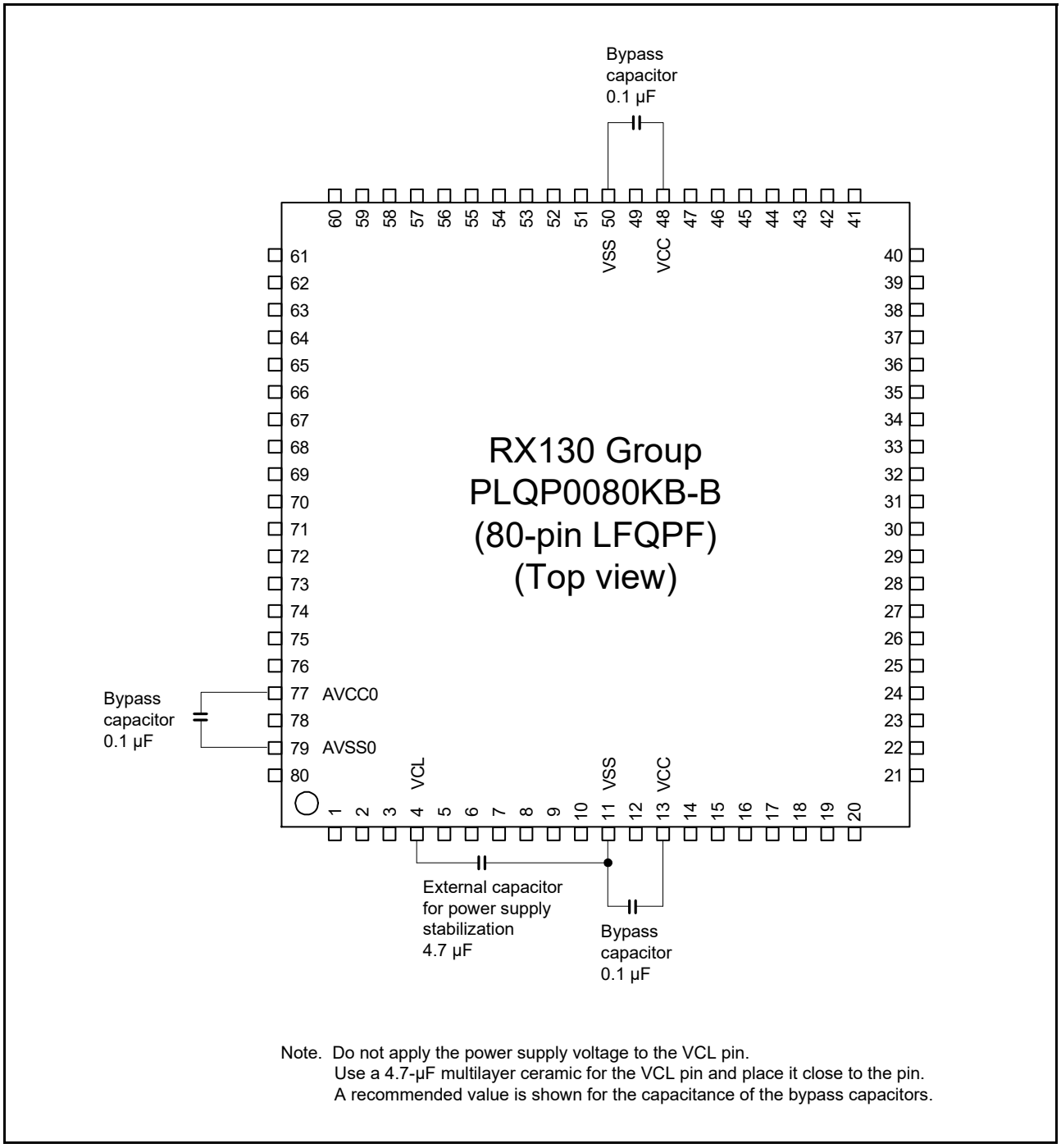
5.13.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 5.67 to Figure 5.70 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 33, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.
For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.67 Connecting Capacitors (100 Pins)



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.68 Connecting Capacitors (80 Pins)

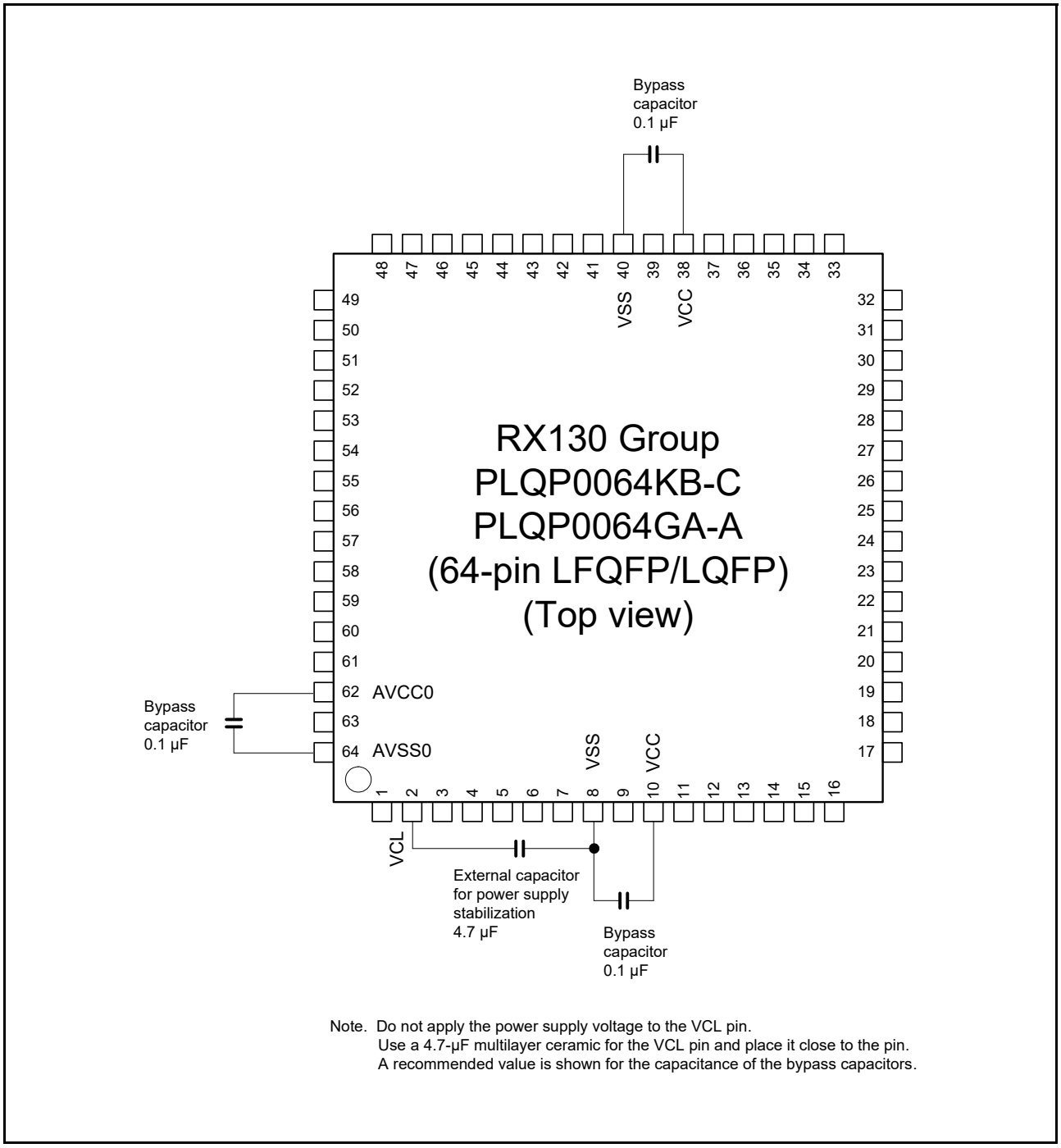
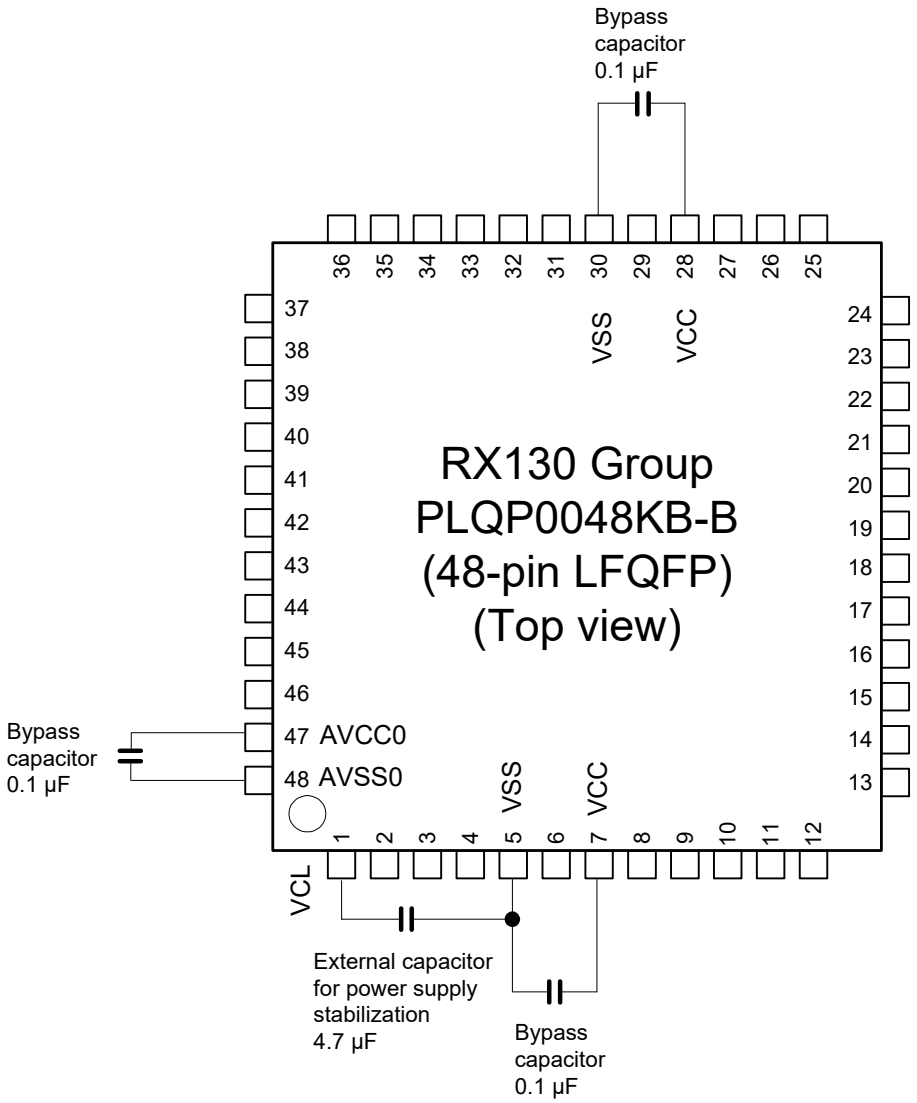


Figure 5.69 Connecting Capacitors (64 Pins)



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

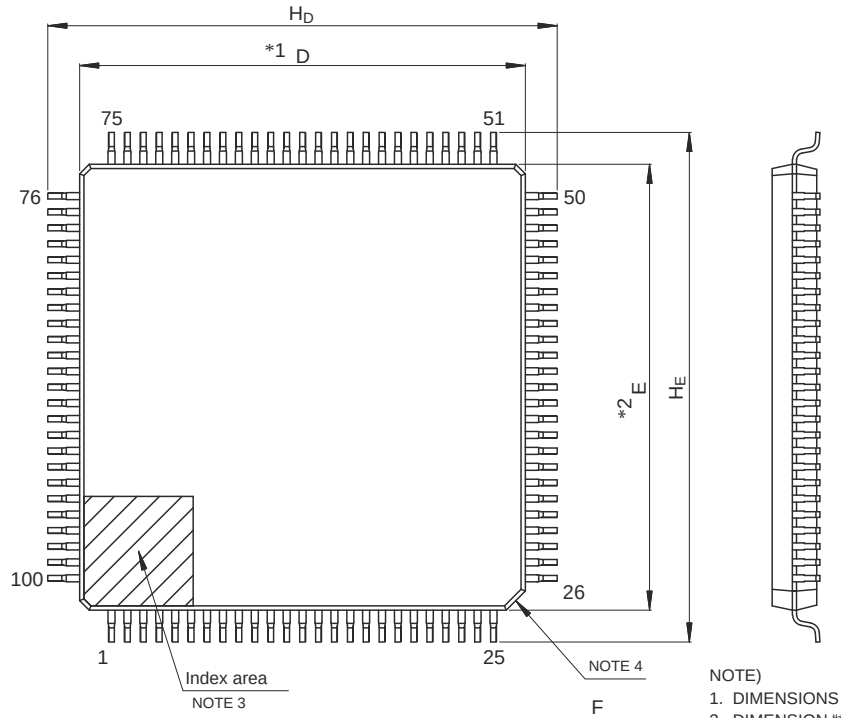
Figure 5.70 Connecting Capacitors (48 Pins)

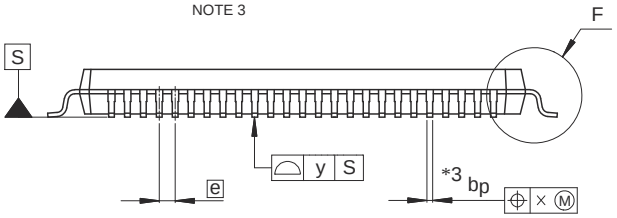
Appendix 1. Package Dimensions

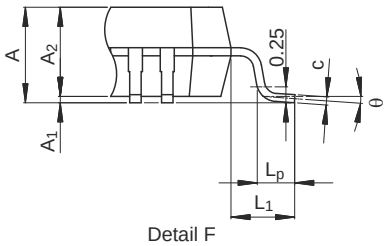
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm





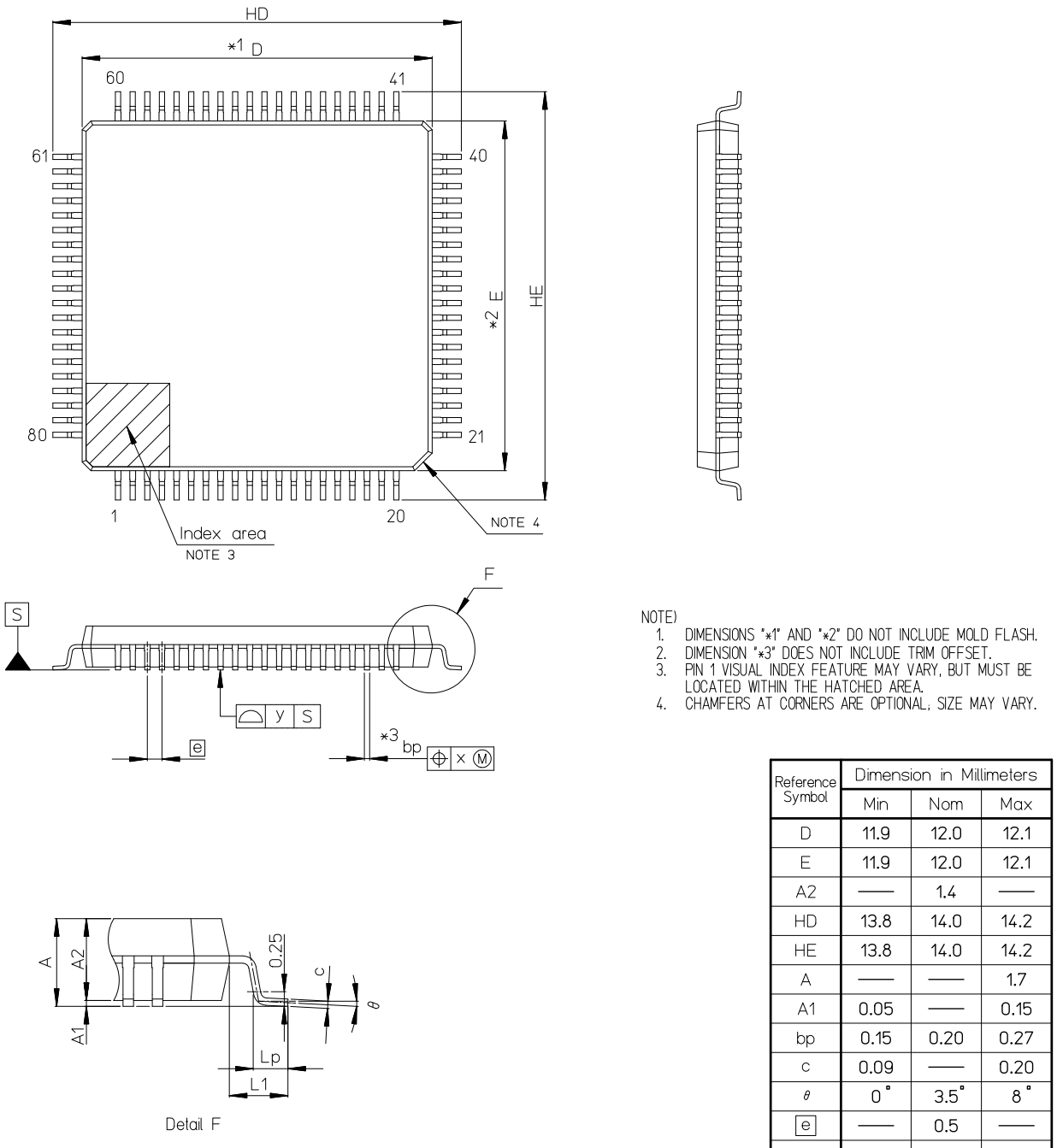


NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	——	0.5g

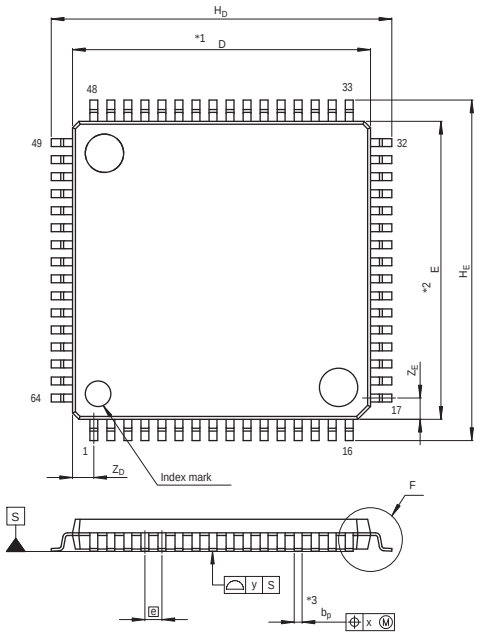


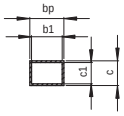
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A2	——	1.4	——
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

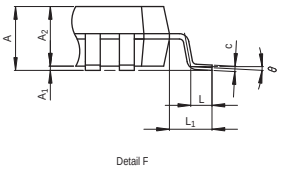
Figure B 80-Pin LFQFP (PLQP0080KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



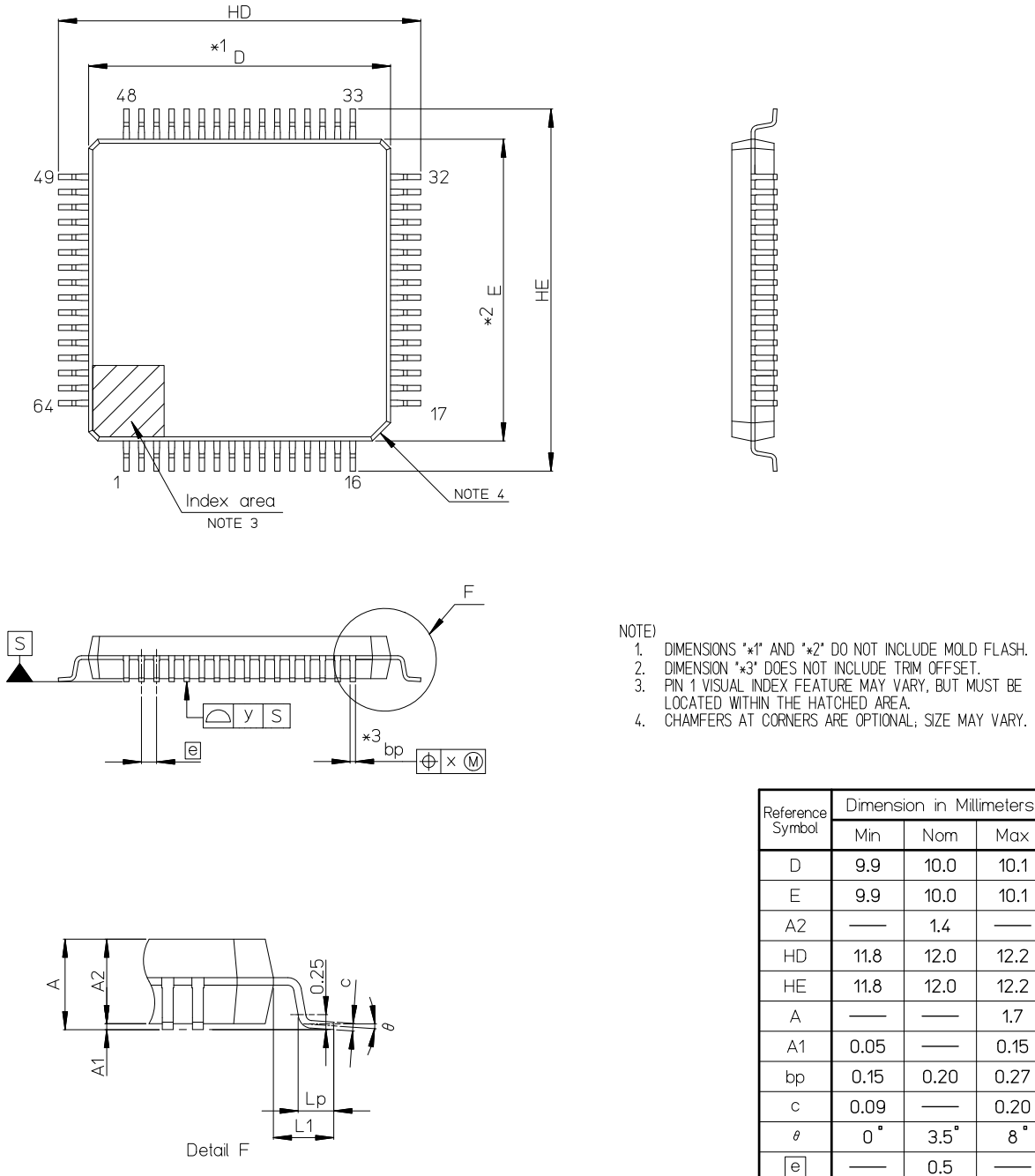
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure C 64-Pin LQFP (PLQP0064GA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g

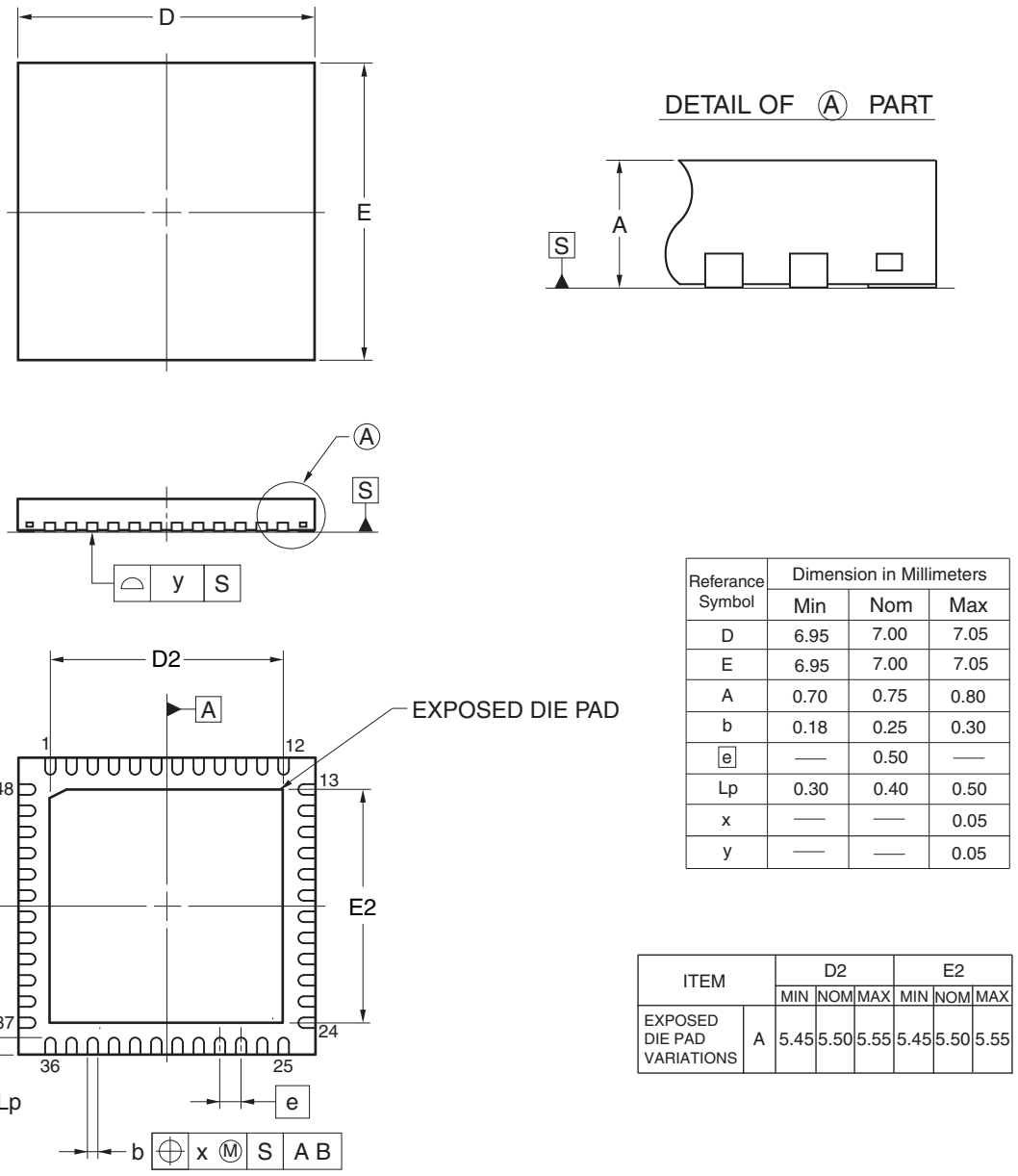


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure D 64-Pin LFQFP (PLQP0064KB-C)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-5	0.13



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

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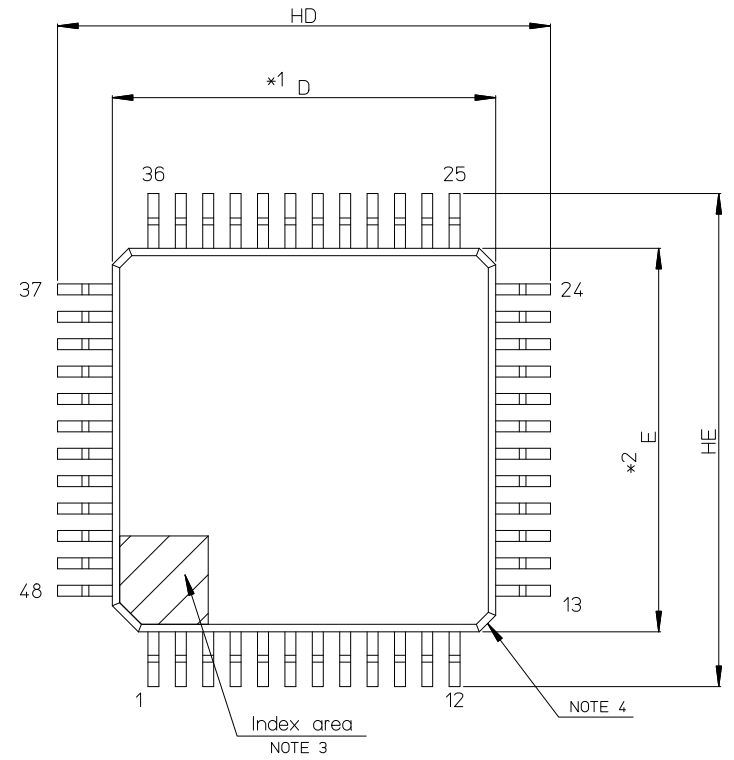
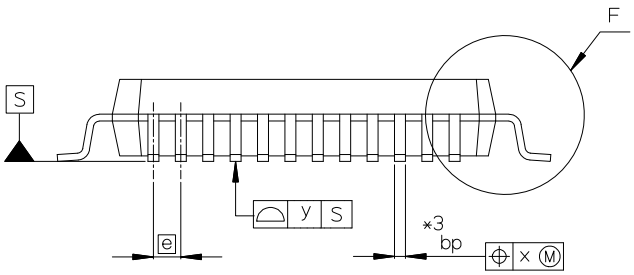
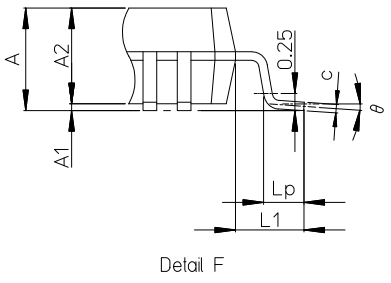
Figure E 48-Pin HWQFN (PWQN0048KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure F 48-Pin LFQFP (PLQP0048KB-B)

REVISION HISTORY	RX130 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Oct 30, 2015	—	First edition, issued	
2.00	Sep 01, 2017	All	Products with at least 256 Kbytes of code flash memory and 100-pin packages added	
		4. I/O Registers		
		42	Table 4.1 List of I/O Registers (Address Order), changed	TN-RX*-A179A/E
		5. Electrical Characteristics		
		49	Table 5.2 Recommended Operating Voltage Conditions Note 3, added	
		57 to 61	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		64, 65	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		90	Table 5.34 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A179A/E
		91	Table 5.35 Timing of On-Chip Peripheral Modules (3), changed	
		93	Table 5.38 Timing of On-Chip Peripheral Modules (6), added	
		111	Table 5.48 CTSU Characteristics, item for products with at least 256 Kbytes of flash memory or 100-pin packages added	
		113	Table 5.50 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2), item with Vdet0_0 to Vdet0_3 selected added	
		117	Table 5.53 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	
		118	Table 5.54 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	
3.00	Aug 09, 2018	1. Overview		
		45, 46	Table 1.3 List of Products, changed	TN-RX*-A199A/E

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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