31/2 Digit LCD, A/D Converter

1.

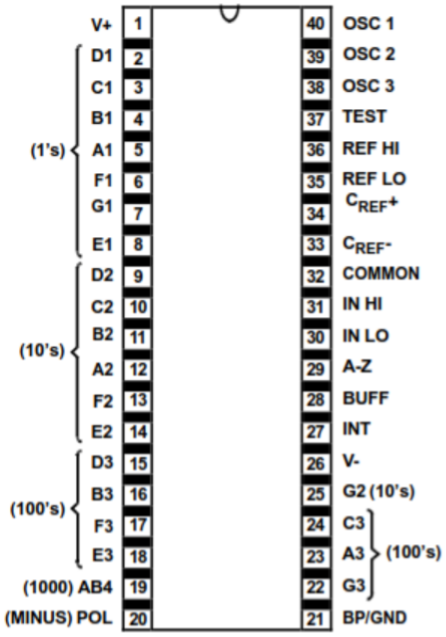
The HT7106A are high performance, low power 3½ Digit A/D Converter. All the necessary active devices are contained in a single CMOS IC, including seven-segment decoder, display driver, voltage reference and clock. HT7106A is designed to interface with a liquid crystal display (LCD). The HT7106A bring the combin ation of high accuracy, versatility and economy. High accuracy, like auto-zero to less than 100μV for 2.00V full-scale measurement, or 10μV for 200.0mV full-scale measurement, input bias current of 10pA max, and rollover of less than one count. The versatility of true differential high impedance inputs and voltage reference is useful in systems, such as strain gauges or bridge-type transducers. The built in auto-zero feature automatically correct the system offset without any external adjustments.

1.1 FEATURES

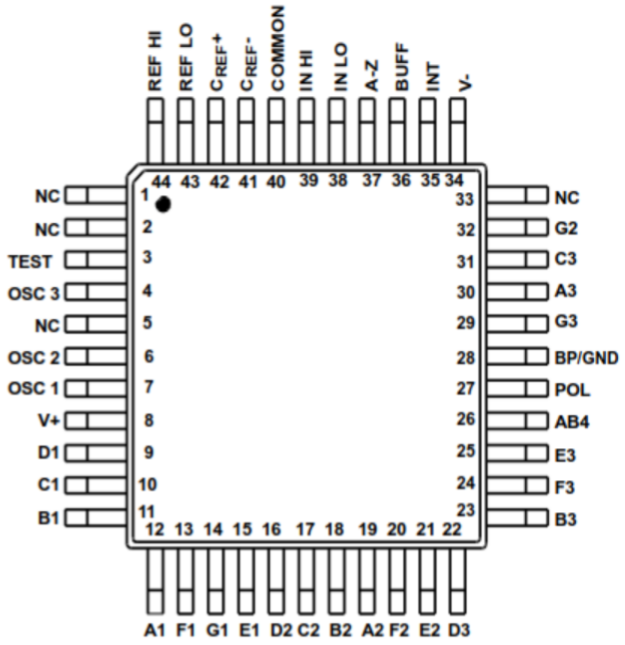
- Guaranteed zero reading with zero input
- True polarity indication for precision null detection
- Low noise – Less than 15μ Vp-p
- Low power operation – 10mW
- High Impedance CMOS differential inputs 1012 ∧
- True differential input and reference
- Display – Hold
- Low - Battery indication
- Integration Status indication
- De-Integration Status indication
- Direct display drive for LCD
- No additional active components required
- Low linearity error: guaranteed less than 1 count
- Internal reference with low temperature drift
- Applications: digital panel meters, digital multi-meters, thermometers, capacitance meters, PH meters, photometers etc.

1.3 PINOUTS

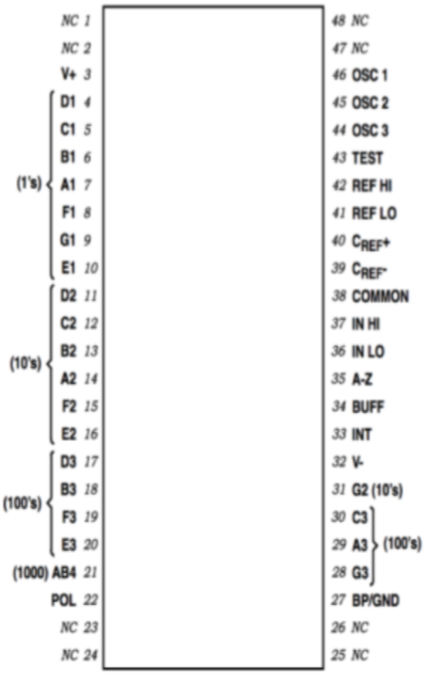
(DIP40)
TOP VIEW



(QFP44)
TOP VIEW



(SSOP48)
TOP VIEW



2. ABSOLUTE MAXIMUM RATINGS ($T_A = 25^oC$)

Characteristic	Symbol	Value	Unit
Supply Voltage (V^+ to V^-)		15	V
Analog Input Voltage (either input)		V+ to V-	V
Reference Input Voltage (either input)		V+ to V-	V
Clock Input		Test to V+	V
Power Dissipation		800	mW
Operating Temperature	T_{opr}	0 ~ +70	^oC
Storage and Junction Temperature	T_{stg}	-55 ~ +150	^oC

3. D/C ELECTRICAL CHARACTERISTICS

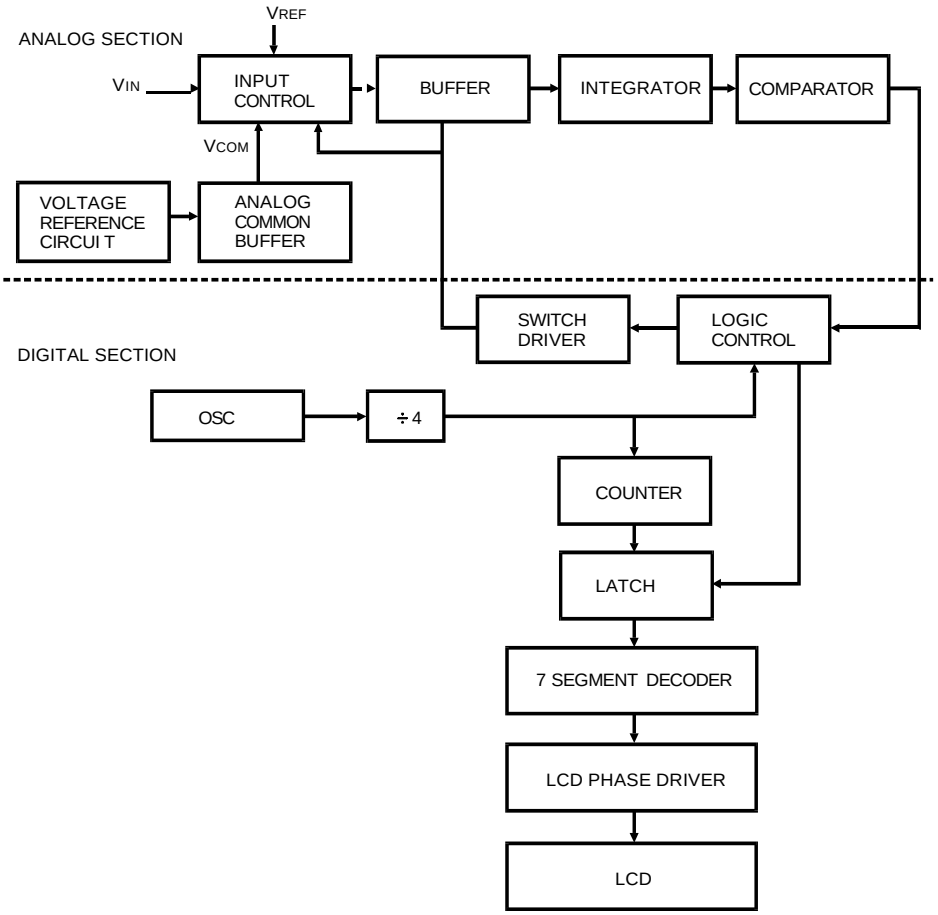
V_{supply} (V^+ to V^-) = 9.0V, $T_A = 25^oC$, f_{clock} = 48KHz, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{DD}	$V_{IN} = 0$		0.8	1.8	mA
Leakage Current Input	I_{LEAK}	$V_{IN} = 0$		1	10	pA
Segment and Back Plane Drive Voltage	V_{LCDS}		4	5	6	V
Analog Common Voltage (With Respect to Positive Supply)	V_{ANACOM}	25K∧ Between Common and Positive Supply	2.7	3.0	3.3	V
Noise (Pk-Pk Value Not exceeded 95% of Time)	V_N	$V_{IN} = 0$ Full Scale 200.0mV		15		μV
Zero Input Reading		$V_{IN} = 0$ Full Scale 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ =100.0mV	999	999/1000	1000	Digital Reading
Linearity (Max. Deviation From Best Strait Line Fit)		Full Scale 200.0mV or 2.000V	-1	±0.2	+1	Counts
Zero Reading Drift		$V_{IN} = 0$ 0 $^oC < T_A < 70\ ^oC$		0.2	1	μV/ ^oC
Scale Factor Temp Coeff.		V_{IN} = 199.0mV 0 $^oC < T_A < 70^oC$		1	5	ppm/ ^oC
Temp Coeff. of Analog Common		25K∧ Between Common and Positive Supply		20	80	ppm/ ^oC
Rollover Error		$V^-_{IN} = V^+_{IN}$ =200.0mV	-1	±0.2	+1	Counts
Common-mode Rejection Ratio		V_{cm}= ±1V V_{IN} =0V Full Scale 200.0mV		50	200	μV/V

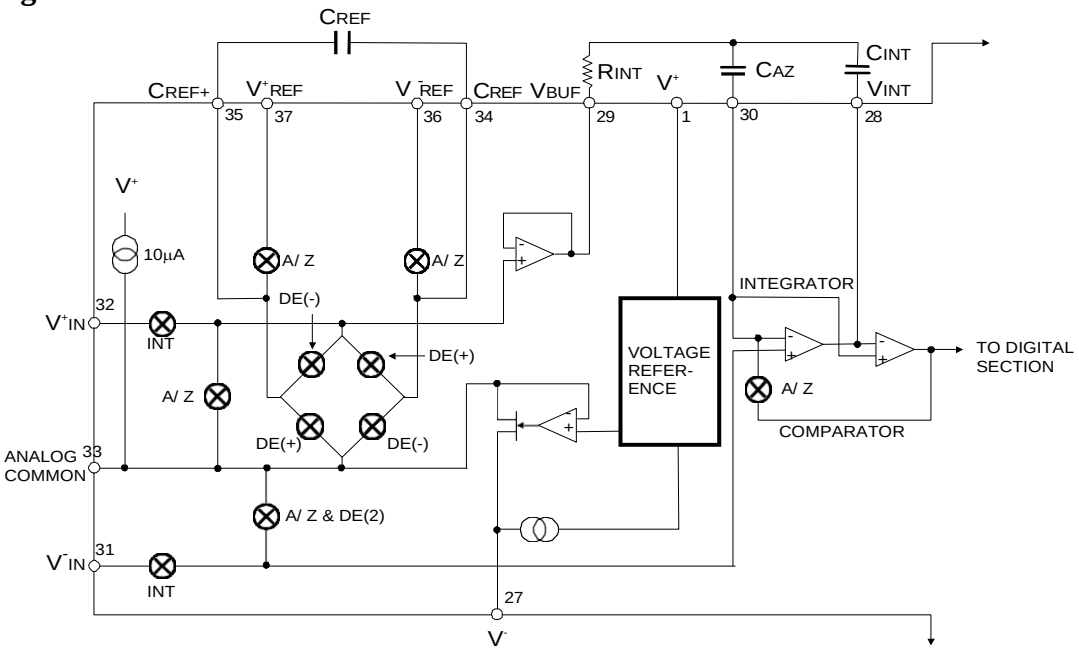
4. FUNCTIONAL DESCRIPTION

An input signal to be measured is applied to the integrating capacitance for a fixed time as determined by a clock counter. The accumulated charge will be proportional to the input signal, for a fixed clock rate and constant current. The resulting integral is returned to zero by integrating a reference signal of polarity opposite that of the input signal. The length of time required for the integrator to return to zero, as measured with the clock counter to display at output, is proportional to the average magnitude of the input signal over the integration period.

4.1 Block Diagram



4.2 Analog Selection



Above is the block diagram of the Analog Section for HT7106A.

Each measurement cycle is divided into three parts. They are:

(1) Auto-zero [A-Z]

During Auto-Zero, three things happen:

(i) Input high and low are disconnected from PIN and shorted to analog COMMON.

(ii) The reference capacitor is charged to the reference voltage.

(iii) A feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the buffer amplifier, integrator and comparator.

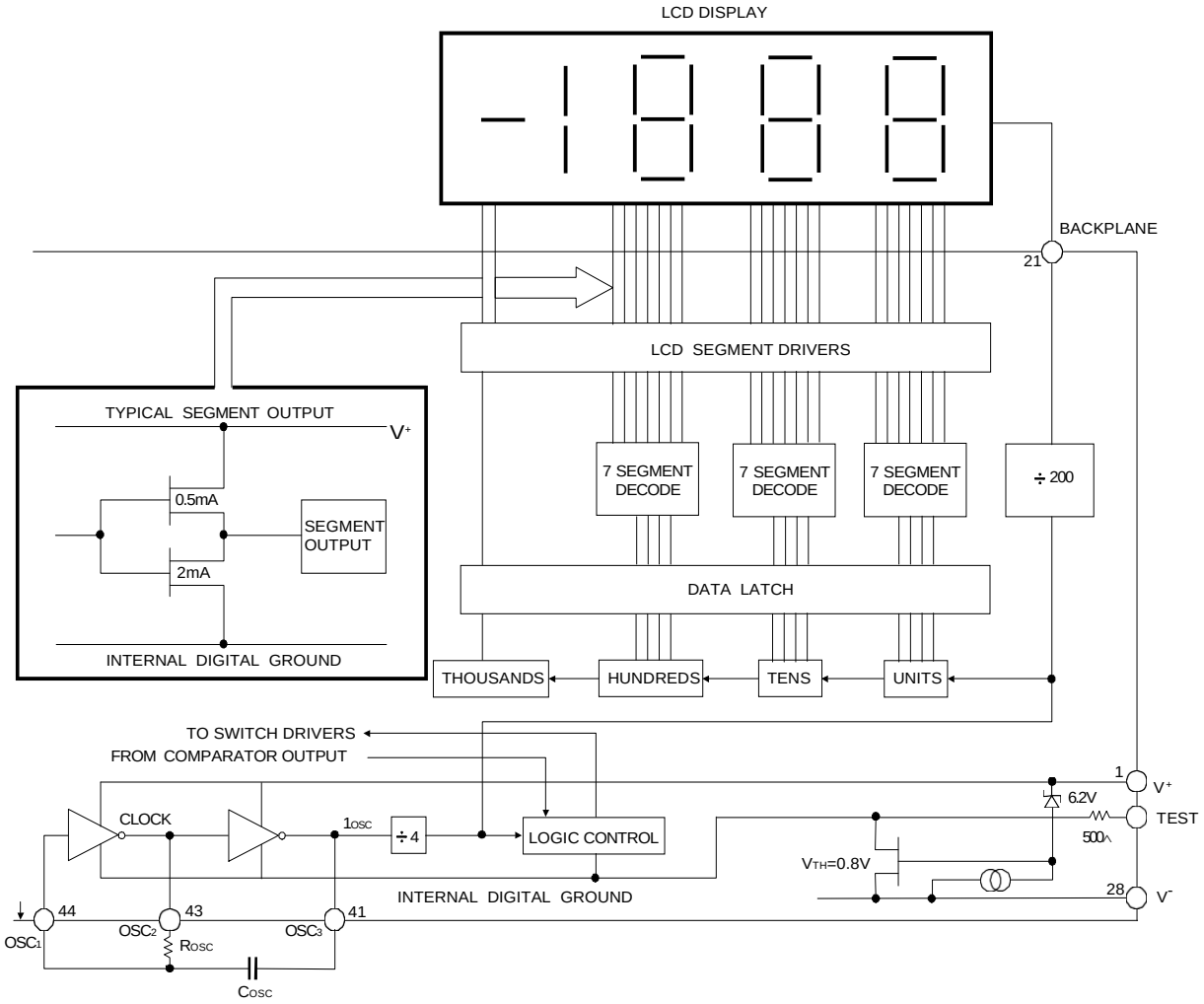
(2) Signal integrated [INT]

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal inputs high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time (1000 counts). At the end of this phase, the polarity of the integrated signal is determined.

(3) Deintegrated [DE].

The final phase is de-integrate, or reference integrate. Input low is internally connected to Analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000.

4.3 Digital Selection

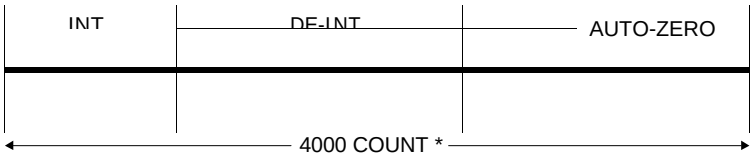


The internal digital ground is generated from a 6.2 volt Zener diode and a large p-channel follower. This supply is made stiff to adsorb the relatively large capacitive current when the back plane (BP) is switched. The BP frequency is the clock frequency divided by 800. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible DC voltage exists across the segments.

4.3.1 System Timing

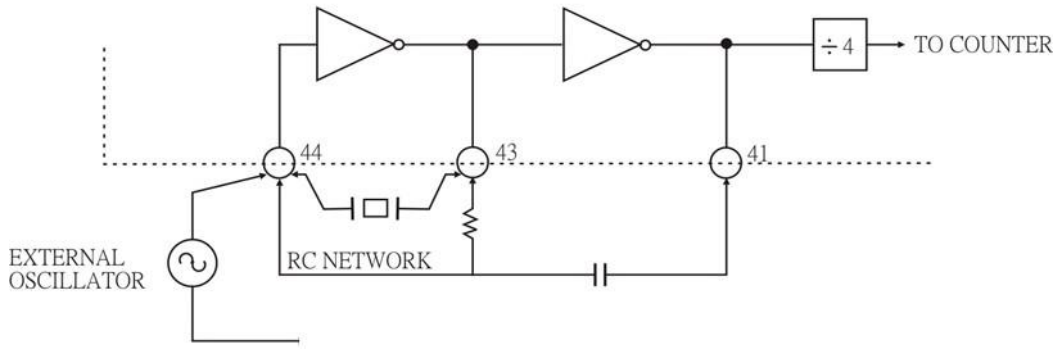
The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phase. These are: signal integrated (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes complete measure cycles of 4000 (16000 clock pulses) independent of input voltage.

* as a matter of fact, the total measurement cycle is 4001 counts for measured values less than 2000 counts The measurement cycle becomes 4000 counts for overflow measurement.



4.3.2 Clock Circuit

HT7106A may use the following three clocking methods:
(i) An external oscillator connected to pin 44.
(ii) A crystal between pin 44 and pin 43.
(iii) An RC oscillator using all three pins (pin 41, 43 & 44).



To achieve maximum rejection of 50/60 Hz pick up, the signal integrate cycle should be a multiple of 50/60 Hz. The following table describes the selection of oscillator frequencies for 50 or 60 Hz respectively.

	Oscillator Frequencies
50 Hz	40 KHz, 50 KHz, 66 2/3 KHz, 100 KHz…
60 Hz	33 1/3 KHz, 40 KHz, 60 KHz, 80 KHz, 100 KHz…

Note that 40 KHz (2.5 readings/second) will reject both 50 and 60 Hz.

4.4 Component Value Selection

4.4.1 Integrating Resistor (R_{INT}) :

The buffer amplifier and integrator are designed with class A output stages with 100μA of quiescent current each. They can supply 20μA drive current with negligible linearity errors. R_{INT} should be large enough to remain in linear region but small enough to reduce the leakage current on the PC board. For 200mv full scale, R_{INT} is 47K∧; 2 volt full scale needs a 470K∧ R_{INT}.

4.4.2 Integrating Capacitor (CINT)

C_{INT} should be chosen to give the maximum voltage swing without causing the saturation of integrator output swing. According to the superior temperature coefficient – 20ppm/°C of analog common will be normally used as the differential voltage reference. It is fine for a nominal ±2V full scale integrator output swing. For three readings/second (48KHz clock), a 0.22μF capacitor is suggested.

If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V full scale integrator output swing.

An additional requirement of C_{INT} is that C_{INT} must have low dielectric absorption to minimize rollover error. Polypropylene capacitors give undetectable errors at reasonable cost.

4.4.3 Reference Voltage Capacitor (CREF)

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1μF capacitor gives good performance when V^-_{IN} is tied to analog common. If a large analog common voltage exists (V^-_{IN} unequal analog common) and a 200.0mV scale is used, a larger value is required to prevent rollover error. Generally 0.1μF will hold the rollover error to 0.5 count. In this case a mylar type dielectric capacitor is adequate.

4.4.4 Auto-Zero Capacitor (CAZ)

The C_{AZ} value has some influence on system noise.
The following combination is recommended:

Application	Adequate C_{AZ}
200.0 mV Full Scale	0.47μF
2.000 V Full Scale	0.047μF

It is better to use a mylar type capacitor to implement C_{AZ}.

4.4.5 Oscillator Components (ROSC, COSC)

While using RC oscillator, the R_{OSC} (between pin 39 and pin 40) should be 100KΛ and C_{OSC} is selected from the following equation:

$$F_{OSC} = \frac{0.45}{R_{OSC} \bullet C_{OSC}} \qquad (R_{OSC} \text{ in } M\Lambda,\ C_{OSC} \text{ in } \mu F)$$

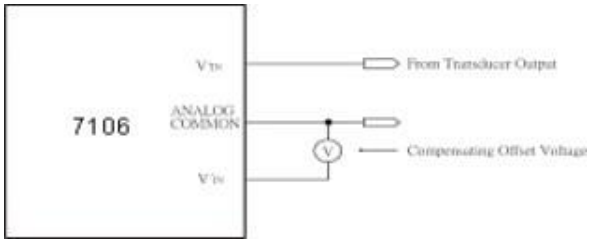
4.5 Reference Voltage Selection

The analog input required to generate full scale output (2000 counts) is $V_{IN} = V_{REF}$, thus:

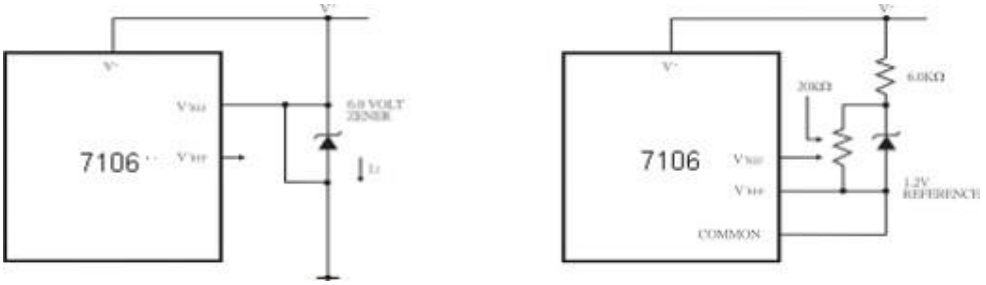
Required Full Scale Voltage	V_{REF}
200.0mV	100.0mV
2.000V	1.000V

However, in many applications where A/D converter is connected to a transducer, there may exist a non-unity scale factor between the input voltage and the digital reading. For instance, a pressure transducer output is 400mV for 2000lb/in^2, rather than dividing the input voltage by two, the V_{REF} should be set to 200.0mV, then permit the transducer input to be used directly.

The differential voltage reference can also be used to read a digital zero when V_{IN} is not zero. This case is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V^-_{IN} and the transducer output is connected between $V^+_{IN}$and analog common. The circuit is shown below:

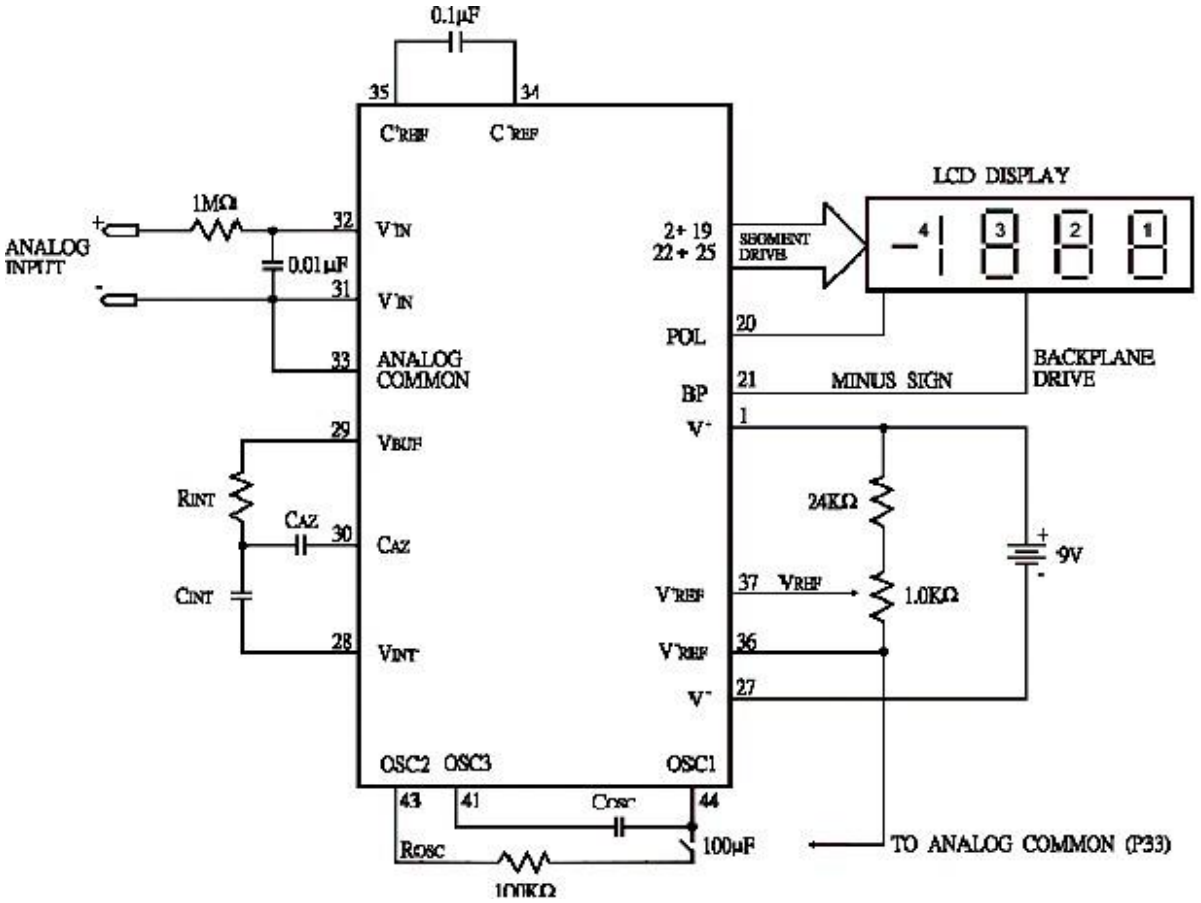


An external reference may be added to improve temperature stability; thus, the HT7106A device with lower analog common te mperature drift may be used. See the circuits below:



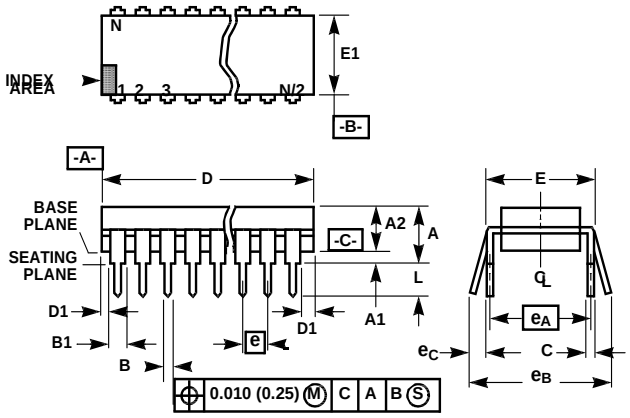
(a) (b)

5. APPLICATION CIRCUITS (for reference only)



Component Value	Nominal Full-Scale Voltage	
	2.000V	**200.0mV**
C_{AZ}	0.047μF	0.47μF
R_{INT}	470K∧	47K∧
C_{INT}	0.22μF	0.22μF
V_{REF}	1.000V	100.0mV

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

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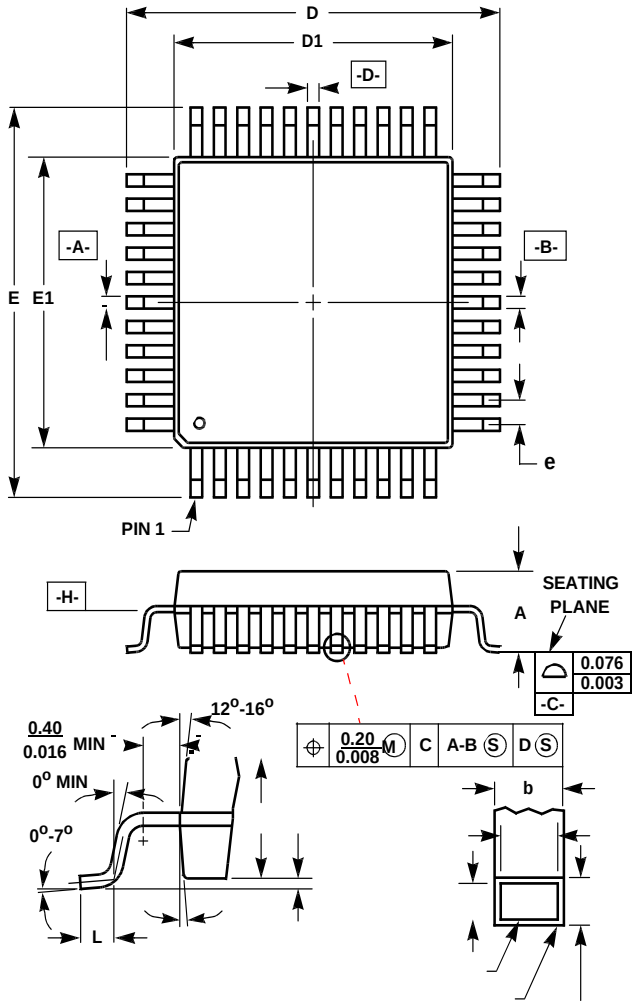
*Metric Plastic Quad Flatpack Packages (LQFP44-10*10)*



Q44.10x10 (JEDEC MS-022AB ISSUE B)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.096	-	2.45	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.515	0.524	13.08	13.32	3
D1	0.389	0.399	9.88	10.12	4, 5
E	0.516	0.523	13.10	13.30	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.029	0.65	0.75	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

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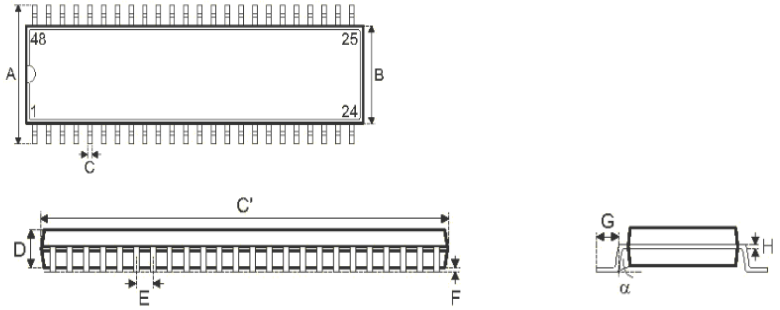
Package Information

48-pin SSOP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	395	—	420
B	291	—	299
C	8	—	12
C'	613	—	637
D	85	—	99
E	—	25	—
F	4	—	10
G	25	—	35
H	4	—	12
α	0°	—	8°