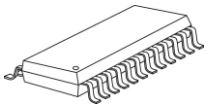
16 Channel Constant Current LED Driver with Ghosting Elimination

Features

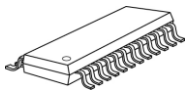
- 16 constant-current output channels
- Constant output current invariant to load voltage change:
  Constant output current range:
  1-25mA@V_{DD}=5V;
  1-10mA@V_{DD}=3.3V
- Excellent output current accuracy:
  between channels: ±1.5% (typ.) and ±2.5% (max.)
  between ICs: ±1.5% (typ.) and ±3% (max.)
- Output current adjusted through an external resistor
- Fast response of output current, $\overline{OE}$ (min.): 50ns with good uniformity between output channels
- Integrating ghosting elimination
- Staggered delay of output
- 25MHz clock frequency
- Schmitt trigger input
- 3.3V/ 5V supply voltage
- “Pb-free & Green” Package

Small Outline Package



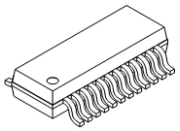
GF: SOP24L-300-1.00

Shrink SOP



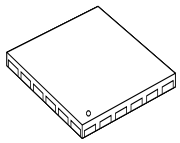
GP: SSOP24L-150-0.64

Mini SSOP



GM: mSSOP24L-100-0.5

Quad Flat No-Lead



GFN: QFN24L-4*4-0.5

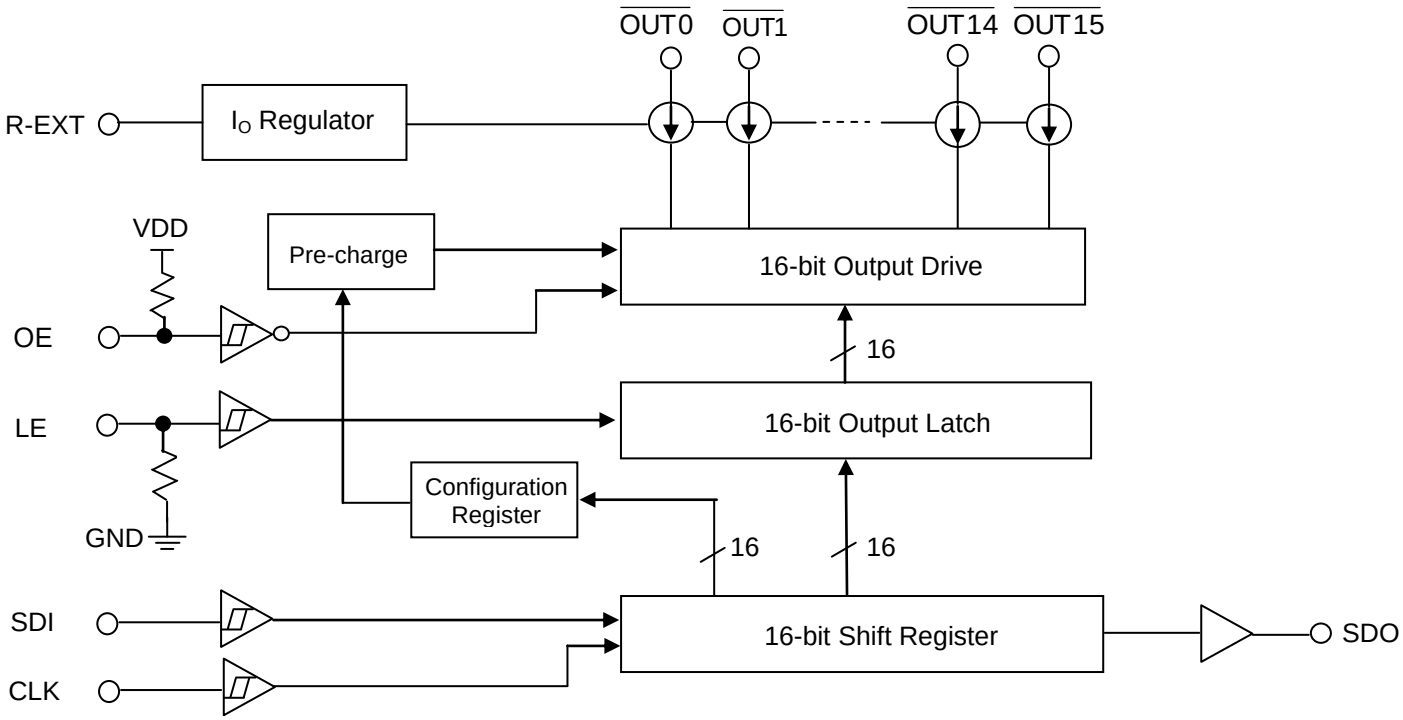
Product Description

With PrecisionDrive™ technology, MBI5124 is designed for LED displays which require to operate at low current and to match the luminous intensity of each channel. It provides supply voltage and accepts CMOS logic input at 3.3V and 5.0V to meet the trend of low power consumption. MBI5124 contains a serial buffer and data latches which convert serial input data into parallel output format. At MBI5124 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of V_F variations. Besides, MBI5124 integrates the pre-charge circuit which can relieve the ghosting.

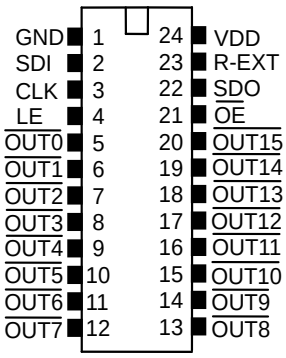
MBI5124 provides users with great flexibility and device performance while using MBI5124 in their system design for LED display applications, e.g. LED panels. It accepts an input voltage range from 3.3V to 5V and maintains a constant current up from 1mA to 25mA determined by an external resistor, R_{ext}, which gives users flexibility in controlling the light intensity of LEDs. MBI5124 guarantees to endure maximum 17V at the output port. The high clock frequency, 25 MHz, also satisfies the system requirements of high volume data transmission.

6F-4, No.18, Pu-Ting Rd., Hsinchu, Taiwan 30072, R.O.C.
TEL: +886-3-579-0068, FAX: +886-3-579-7534 E-mail: info@mblock.com.tw

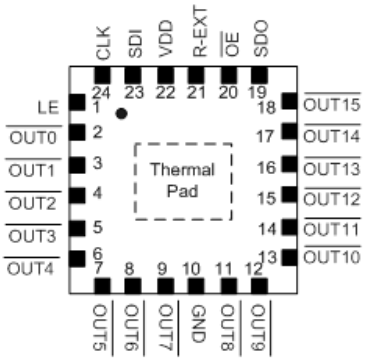
Block Diagram



Pin Configuration



MBI5124GF/GP/GM



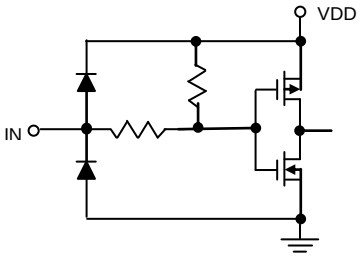
MBI5124GFN

Terminal Description

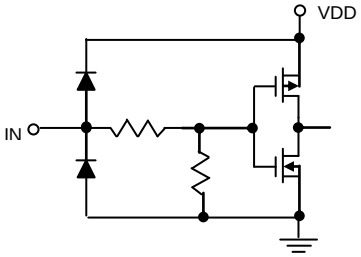
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
CLK	Clock input terminal for data shift on rising edge
LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
$\overline{OE}$	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
SDO	Serial-data output to the following SDI of next driver IC. SDO signal change on rising edge of CLK.
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

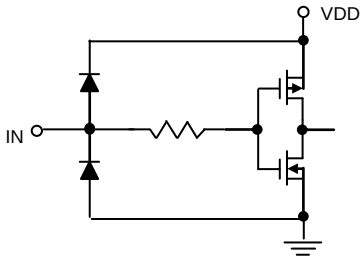
$\overline{OE}$ terminal



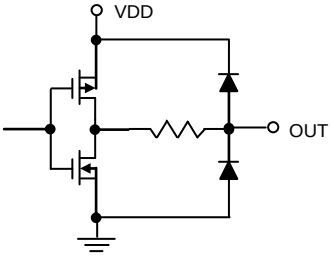
LE terminal



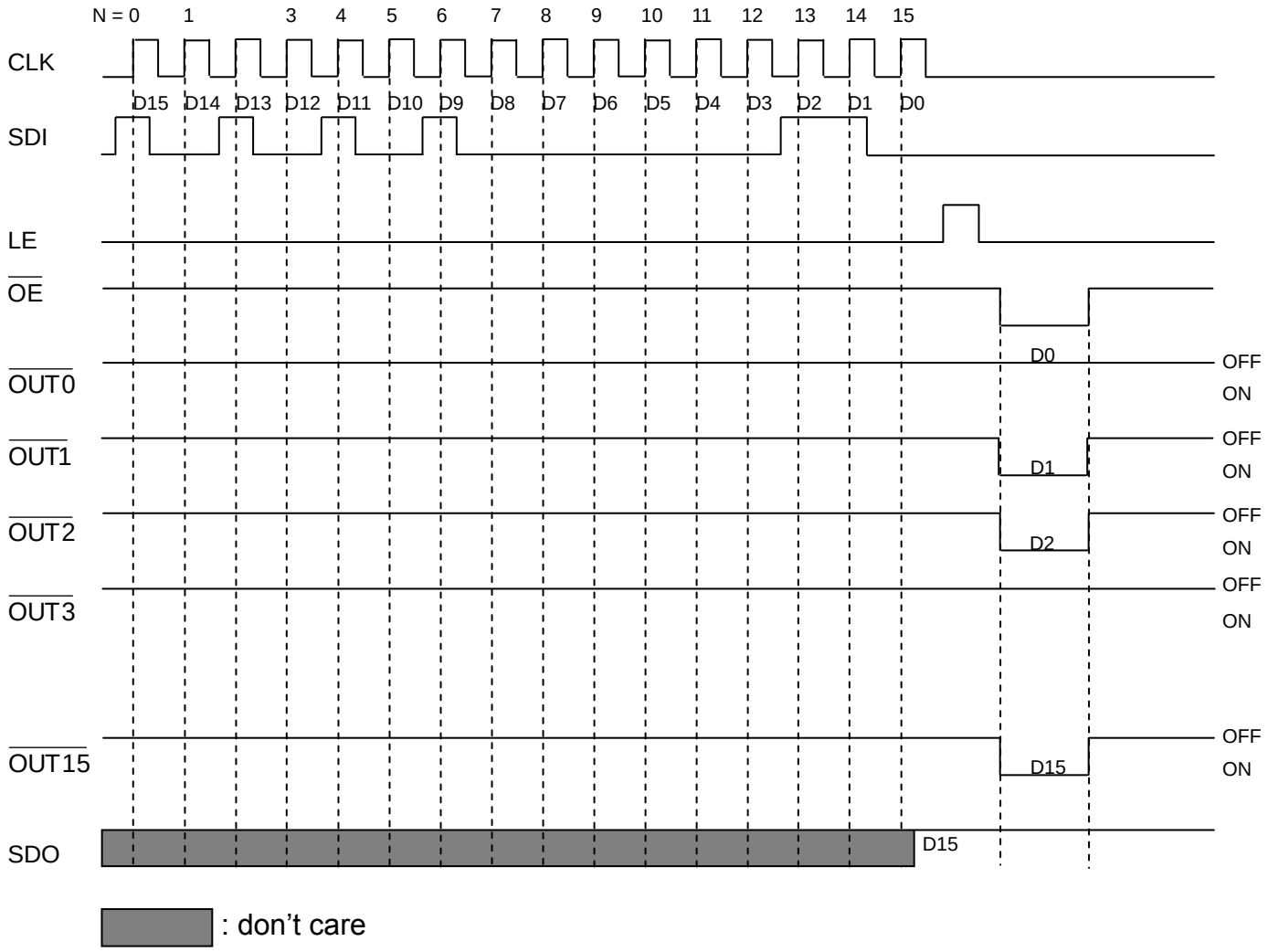
CLK, SDI terminal



SDO terminal



Timing Diagram



Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ ... $\overline{OUT7}$ ... $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ..... $\overline{D_{n-7}}$ .... $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ .... $\overline{D_{n-5}}$ .... $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ .... $\overline{D_{n-5}}$ .... $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+4}	Off	D_{n-13}

Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7.0	V
Input Voltage(SDI, CLK, LE, GCLK)		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+30	mA
Sustaining Voltage at OUT Port		V_{DS}	V_{DD}+0.3	V
GND Terminal Current		I_{GND}	480	mA
Power Dissipation (On PCB, Ta=25°C)*	GF-type	P_D	2.34	W
	GP-type		1.76	
	GM-type		1.33	
	GFN-type		3.12	
Thermal Resistance (On PCB, Ta=25°C)*	GF-type	$R_{th(j-a)}$	53.28	°C/W
	GP-type		70.90	
	GM-type		93.5	
	GFN-type		40.01	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM(MIL-STD-883G Method 3015.7)	HBM	Class 3A (5000V)	
	MM(JEDEC EIA/JESD22-A115)	MM	Class M4 (≧400V)	

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

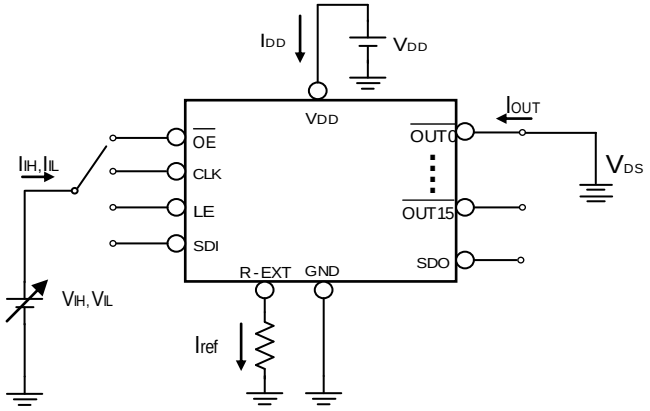
Electrical Characteristics (V_{DD}= 5.0V, Ta=25℃)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$~$\overline{OUT15}$		V_{DD}+0.3	-	-	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		1.0	-	25	mA
		I_{OH}	SDO		-	-1.0	-	mA
		I_{OL}	SDO		-	1.0	-	mA
Input Voltage	"H" level	V_{IH}	T_a=-40~85ºC		0.7 x V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	T_a=-40~85ºC		GND	-	0.3 x V_{DD}	V
Output Leakage Current		I_{OH}	V_{DD}+0.3V		100	-	-	nA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=10.05mA V_{DS}=1.0V	R_{ext}=1820Ω	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=10.05mA V_{DS}=1.0V	R_{ext}=1820Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.3	%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±0.5	±1.0	%/V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		125	350	600	KΩ
Pull-down Resistor		R_{IN}(down)	LE		125	350	600	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$~$\overline{OUT15}$ =Off		-	3.0	-	mA
		I_{DD}(off) 2	R_{ext}=1820Ω, (10.7mA) $\overline{OUT0}$~$\overline{OUT15}$ =Off		-	6.80	-	
		I_{DD}(off) 3	R_{ext}=1050Ω, (18.8mA) $\overline{OUT0}$~$\overline{OUT15}$ =Off		-	10.09	-	
	"ON"	I_{DD}(on) 1	R_{ext}=1820Ω, (10.7mA) $\overline{OUT0}$~$\overline{OUT15}$ =On		-	6.92	-	
		I_{DD}(on) 2	R_{ext}=1050Ω, (18.8mA) $\overline{OUT0}$~$\overline{OUT15}$ =On		-	10.31	-	

Electrical Characteristics (V_{DD}= 3.3V, Ta=25℃)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$~$\overline{OUT15}$		V_{DD}+0.3	-	-	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		1	-	10	mA
		I_{OH}	SDO , V_{OH}=2.9V		-	-1.0	-	mA
		I_{OL}	SDO, V_{OL} =0.4V		-	1.0	-	mA
Input Voltage	"H" level	V_{IH}	T_a=-40~85ºC		0.7 x V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	T_a=-40~85ºC		GND	-	0.3 x V_{DD}	V
Output Leakage Current		I_{OH}	V_{DD}+0.3V		100	-	-	nA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		2.9	-	-	V
Current Skew		dI_{OUT1}	I_{OUT}=25.8mA V_{DS}=1.0V	Rext=720Ω	-	±1.5	±2.5	%
Current Skew		dI_{OUT2}	I_{OUT}=25.8mA V_{DS}=1.0V	Rext=720Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.3	%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 3.0V and 4.5V		-	±0.5	±1.0	%/V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		125	350	600	KΩ
Pull-down Resistor		R_{IN}(down)	LE		125	350	600	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{ext}= Open, $\overline{OUT0}$~$\overline{OUT15}$=Off		-	2.45	-	mA
		I_{DD}(off) 2	R_{ext}=1820Ω, (10.05mA) $\overline{OUT0}$~$\overline{OUT15}$ =Off		-	6.42	-	
		I_{DD}(off) 3	R_{ext}=16KΩ, (1.14mA) $\overline{OUT0}$~$\overline{OUT15}$ =Off		-	2.53	-	
	"ON"	I_{DD}(on) 1	R_{ext}=1820Ω, (10.05mA) $\overline{OUT0}$~$\overline{OUT15}$ =On		-	6.52	-	
		I_{DD}(on) 2	R_{ext}=16KΩ, (1.14mA) $\overline{OUT0}$~$\overline{OUT15}$ =Off		-	2.55	-	

Test Circuit for Electrical Characteristics



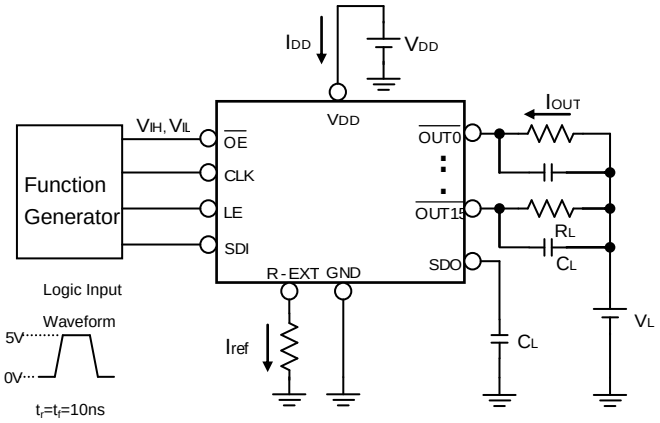
Switching Characteristics (V_{DD}= 5.0V , Ta=25 ºC)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	LE-$\overline{OUT0}$	t_{pLH2}	V_{DD}=5.0V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1820Ω V_L=4.0V R_L=300Ω C_L=10pF	23	29	35	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}		19	24	29	ns
	CLK-SDO	t_{pLH}		23	29	35	ns
Propagation Delay Time ("H" to "L")	LE-$\overline{OUT0}$	t_{pHL2}		15	19	23	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}		19	25	31	ns
	CLK-SDO	t_{pHL}		22	28	34	ns
Staggered Delay of Output	$\overline{OUTn}$ - $\overline{OUTn+1}$	t_{stag}		-	2	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$ *	$t_{w(OE)}$		45	55	65	ns
Hold Time for LE		$t_{h(L)}$		5	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
SDO Rise Time		$t_{r,SDO}$		3	10	15	ns
SDO Fall Time		$t_{f,SDO}$		3	10	15	ns
Output Rise Time of Output Ports		t_{or}		25	30	39	ns
Output Fall Time of Output Ports		t_{of}		25	30	39	ns

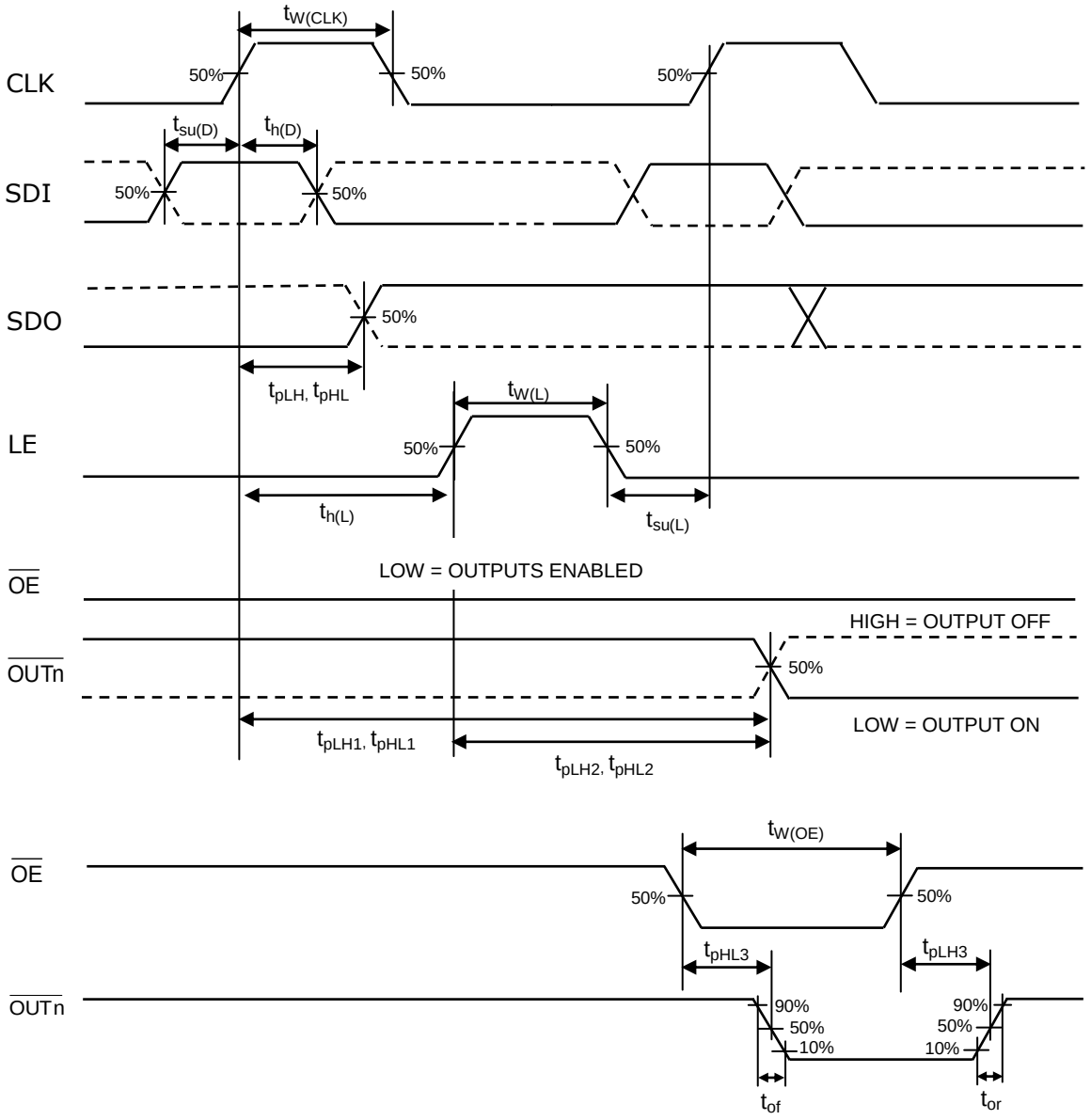
Switching Characteristics (V_{DD}= 3.3V , Ta=25ºC)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	LE-$\overline{OUT0}$	t_{pLH2}	V_{DD}=3.3V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1820Ω V_L=4.0V R_L=300Ω C_L=10pF	23	29	35	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}		29	37	45	ns
	CLK-SDO	t_{pLH}		34	42	50	ns
Propagation Delay Time ("H" to "L")	LE-$\overline{OUT0}$	t_{pHL2}		14	18	22	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}		22	28	34	ns
	CLK-SDO	t_{pHL}		32	40	48	ns
Staggered Delay of Output	$\overline{OUTn}$ - $\overline{OUTn+1}$	t_{stag}		-	2	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$*	$t_{w(OE)}$		50	60	70	ns
Hold Time for LE		$t_{h(L)}$		5	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
SDO Rise Time		$t_{r,SDO}$		3	10	15	ns
SDO Fall Time		$t_{f,SDO}$		3	10	15	ns
Output Rise Time of Output Ports		t_{or}		25	30	40	ns
Output Fall Time of Output Ports		t_{of}		25	30	40	ns

Test Circuit for Switching Characteristics



Timing Waveform



Control Command

Command Name	Signals Combination		Description
	LE	Number of CLK Rising Edge when LE is asserted	The Action After a Falling Edge of LE
Latch data	High	0	Latch the serial data to the output latch. Latch the serial data to the driver's internal latch.
	High	1	Latch the serial data/Buffer data to the output latch.
Write configuration	High	4	Serial data are transferred to the "configuration register"
Read configuration	High	5	"Configuration register" is shifted out to SDO.
No Action	High	2,3, >5	No action. Please do not use it.

Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

According the driven LED, please set the configuration register by the following settings:

Red LED (R)

0	1	1	1	1	1	0	1	0	1	1	0	1	0	1	1

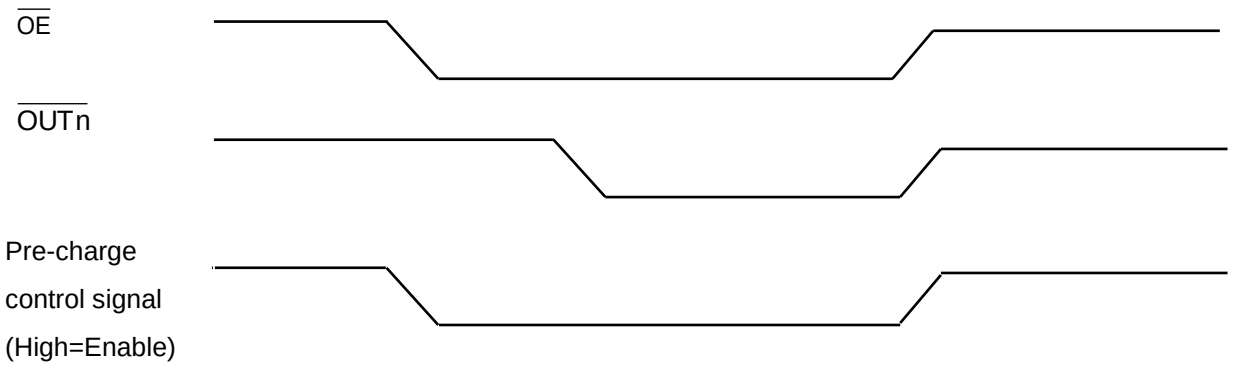
Green LED (G)

1	1	1	1	0	0	0	1	0	1	1	0	1	0	1	1

Blue LED (B)

1	1	1	0	1	1	0	1	0	1	1	0	1	0	1	1

Pre-charge waveform



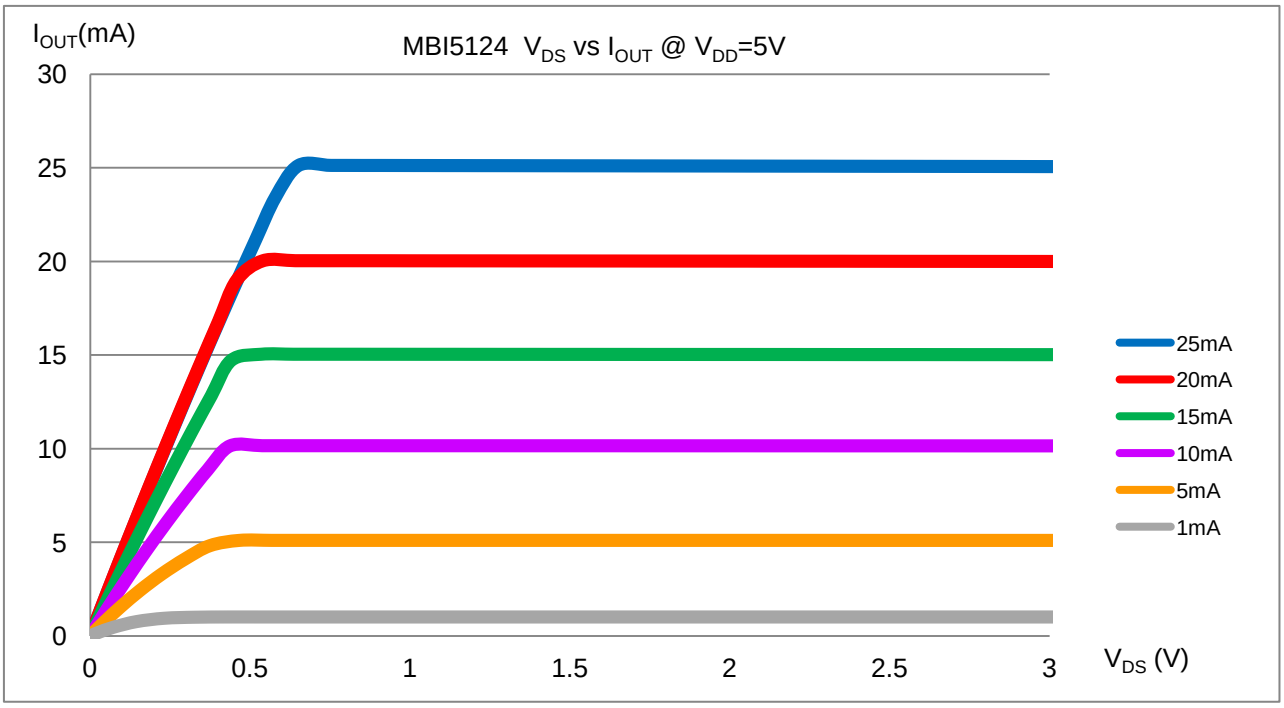
Application Information

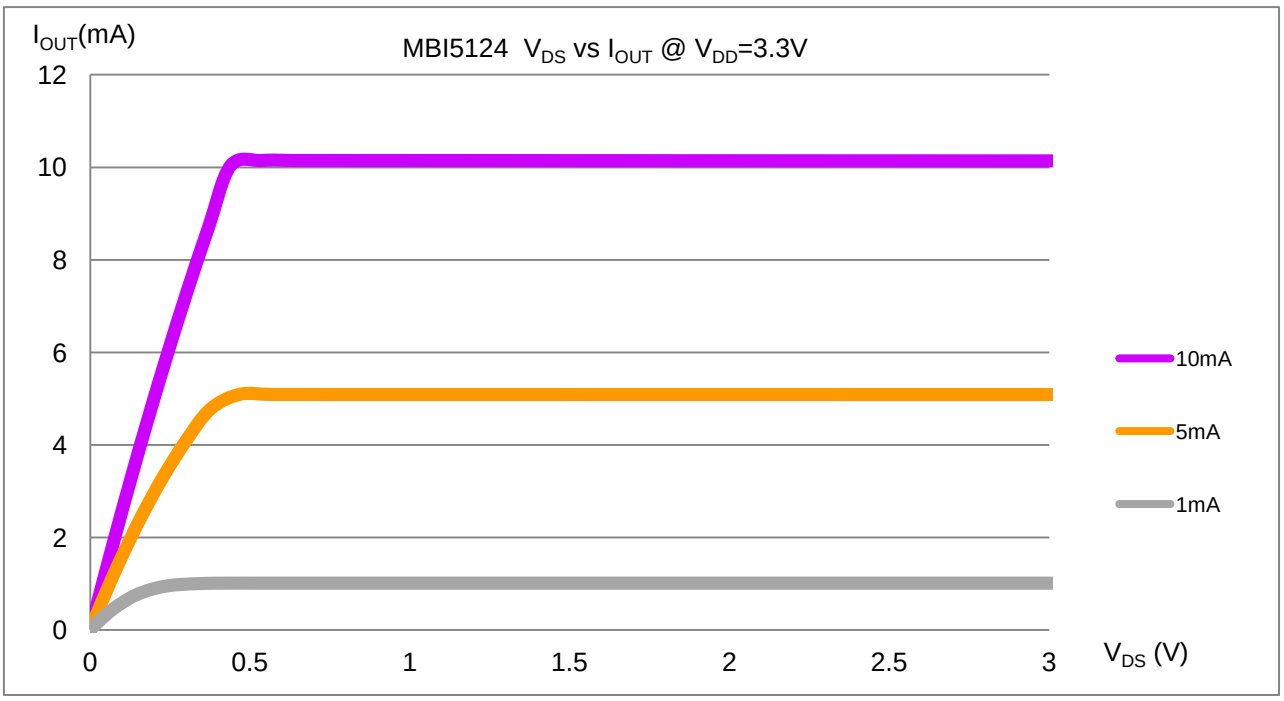
Constant Current

To design LED displays, MBI5124 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than ±2.5%, and that between ICs is less than ±3%.

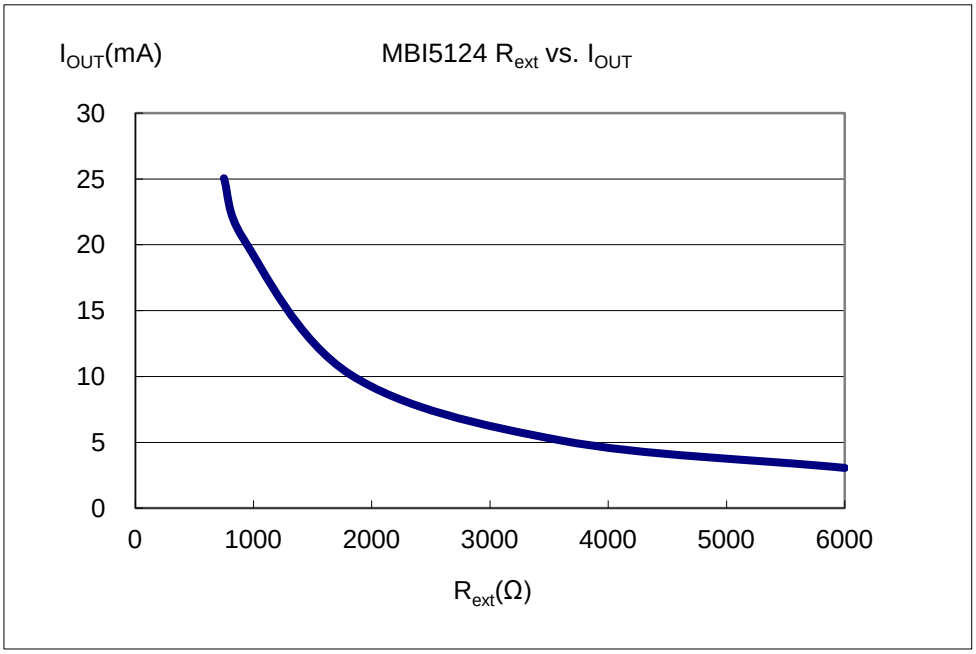
2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This performs as a perfection of load regulation.





Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.



Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=1.23V； $I_{OUT}=V_{R\text{-}EXT}$*(1/Rext)x15; $R_{ext}=(V_{R\text{-}EXT}/I_{OUT})$x15

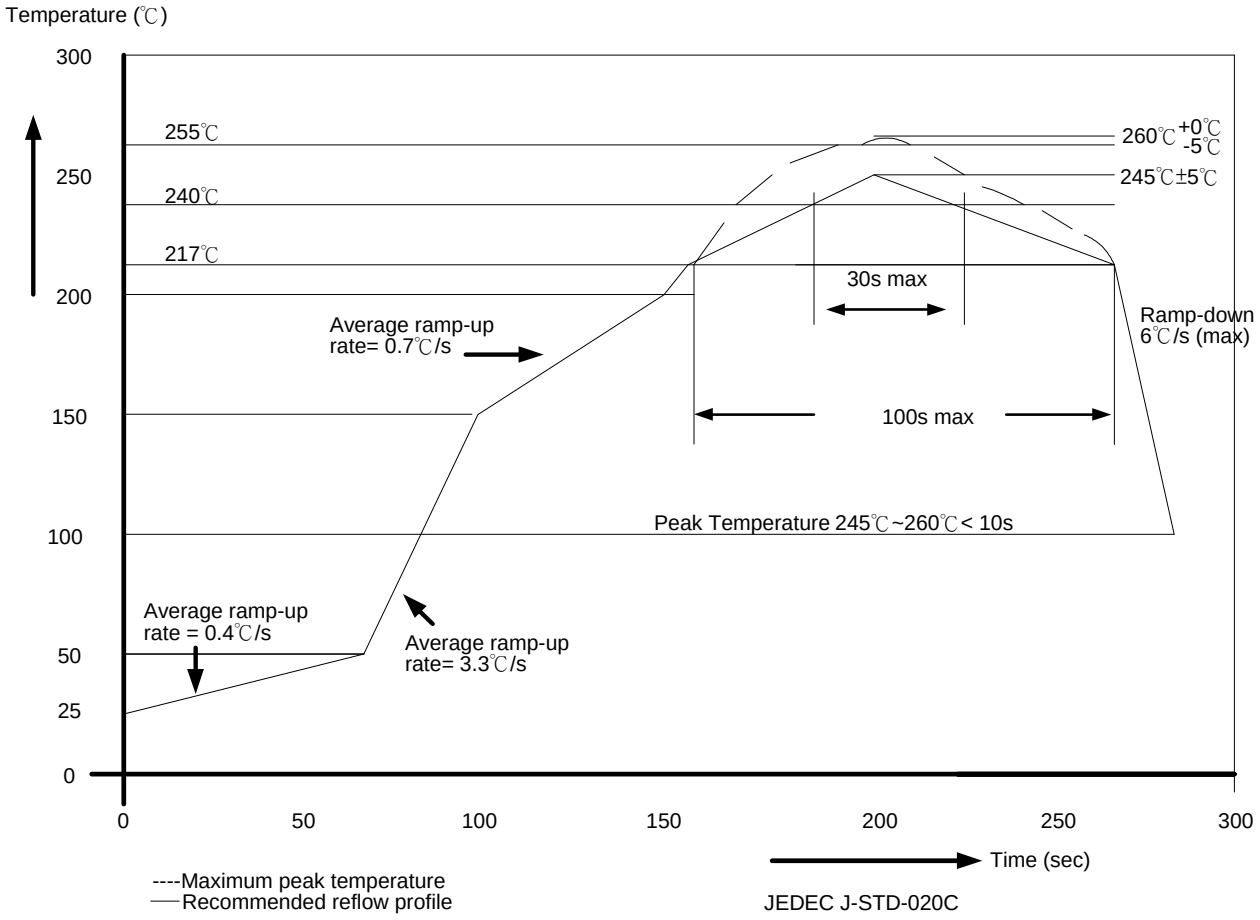
Where R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is the voltage of R-EXT terminal. The magnitude of current (as a function of R_{ext}) is around 20mA at 930Ω and 10mA at 1860Ω.

Output Staggered Delay

MBI5124 has a built-in staggered circuit to perform delay mechanism. The 16 output channels are categorized into 2 groups $\overline{OUT2r}$ and $\overline{OUT2n+1}$, and each group outputs current by the staggered sequence, 2ns.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with the higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

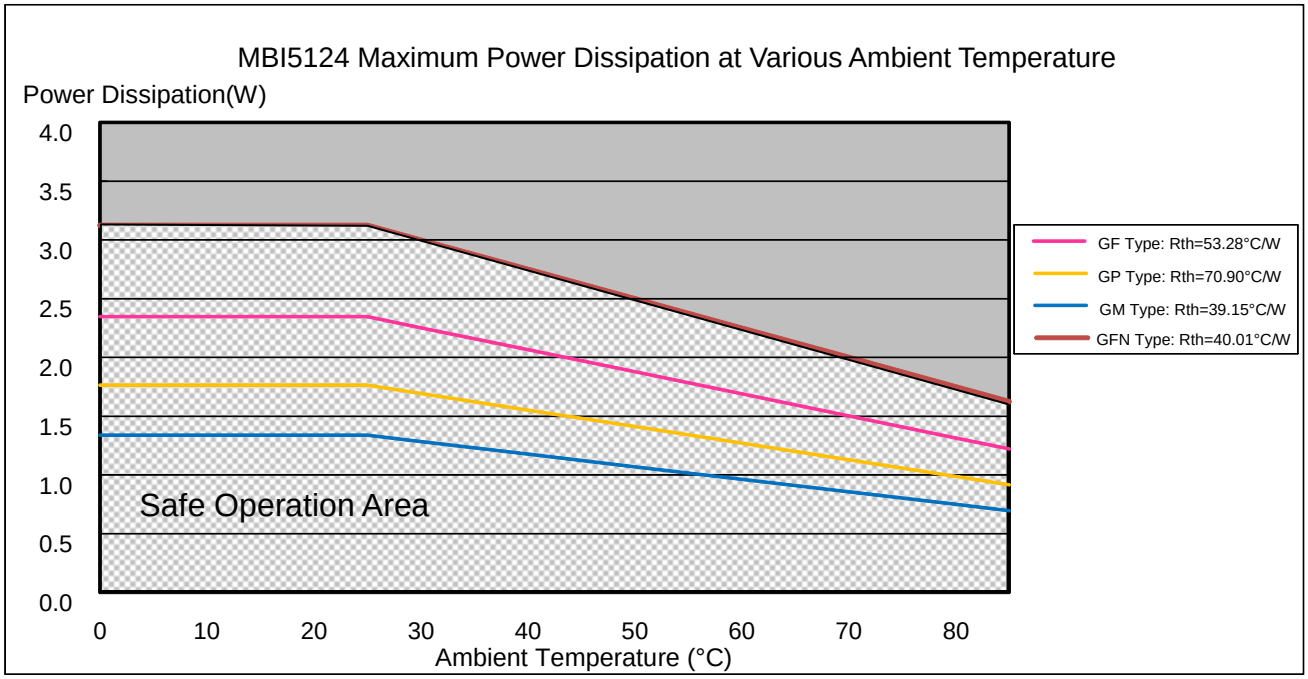
*For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Power Dissipation (P_D)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

Package	$R_{th(j-a)}$ (°C/W)	P_D(W)
GF	53.28	2.34
GP	70.90	1.76
GM	93.50	1.33

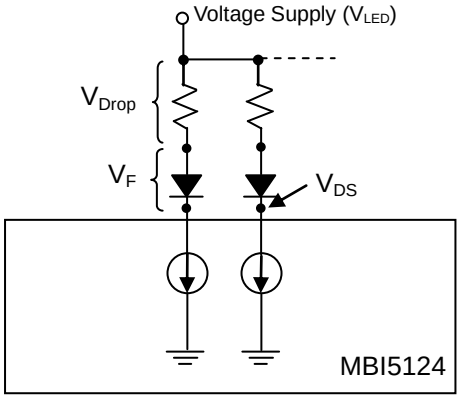


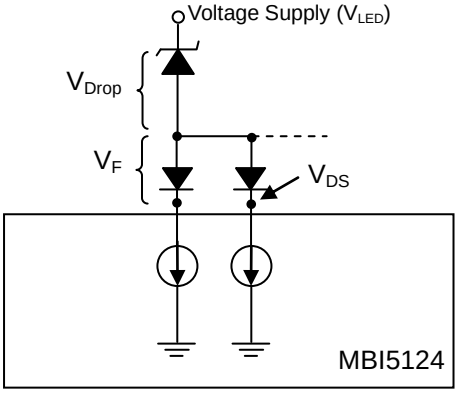
Load Supply Voltage (V_{LED})

MBI5124 are designed to operate with V_{DS} ranging from 0.4V to 0.8V (depending on I_{OUT}=1~25mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)} > P_{D(max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

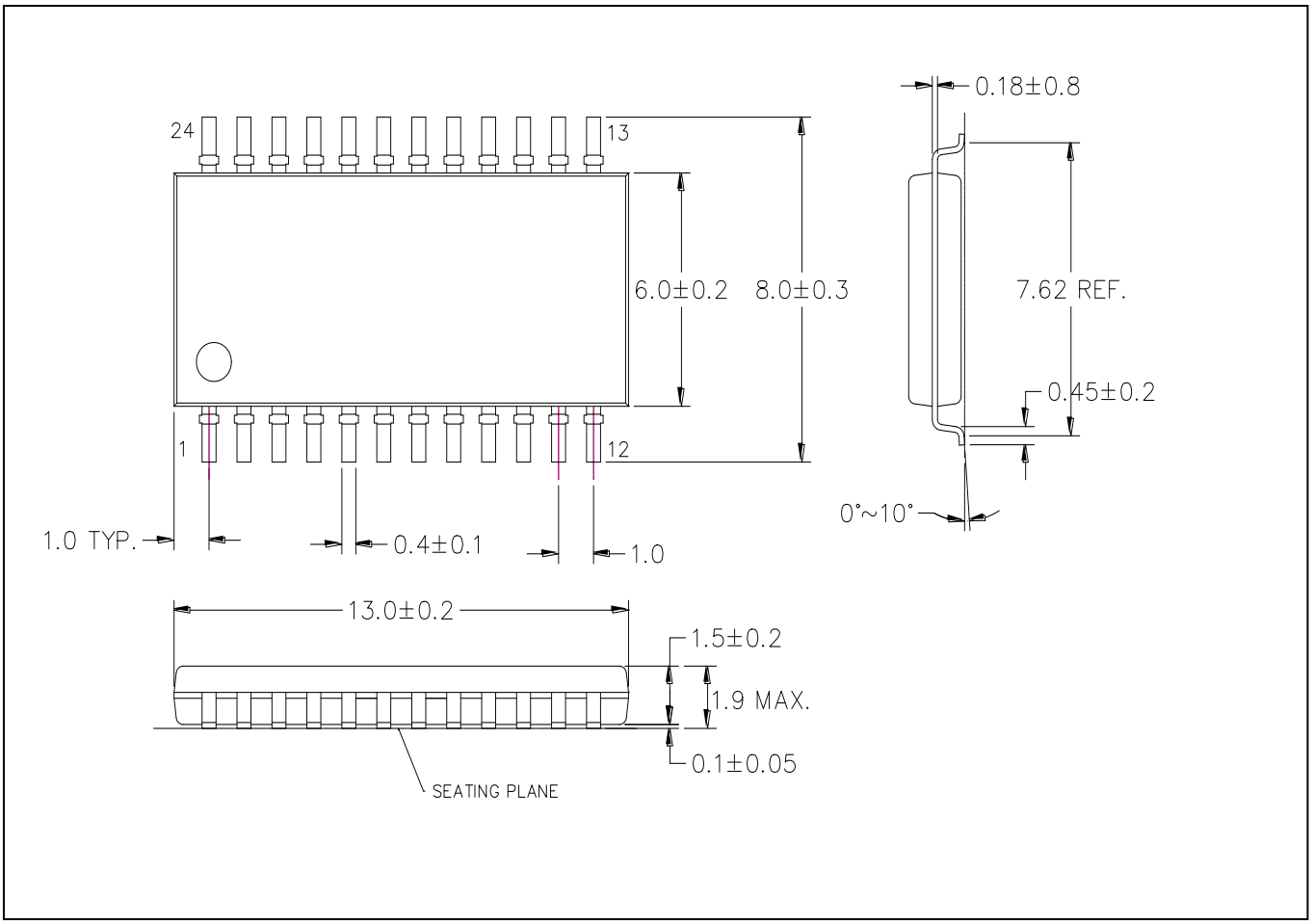
A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.



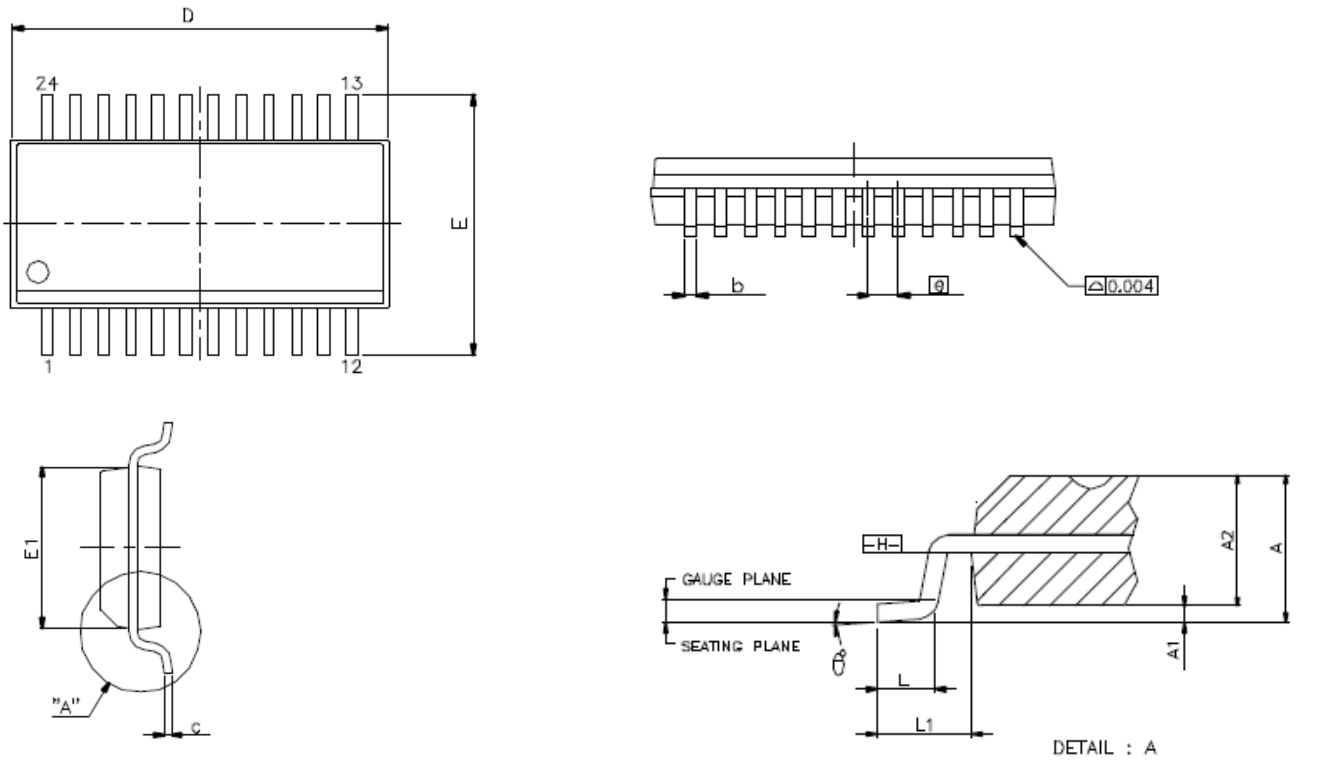


Package Outline



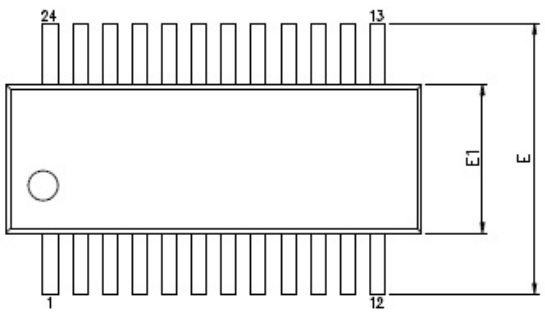
MBI5124GF Outline Drawing

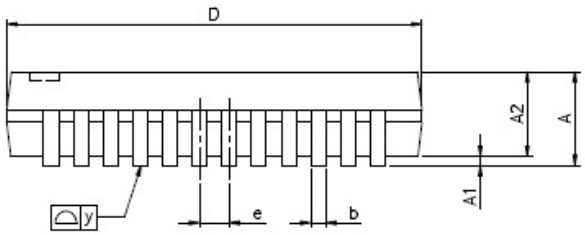
Note: The unit for the outline drawing is mm

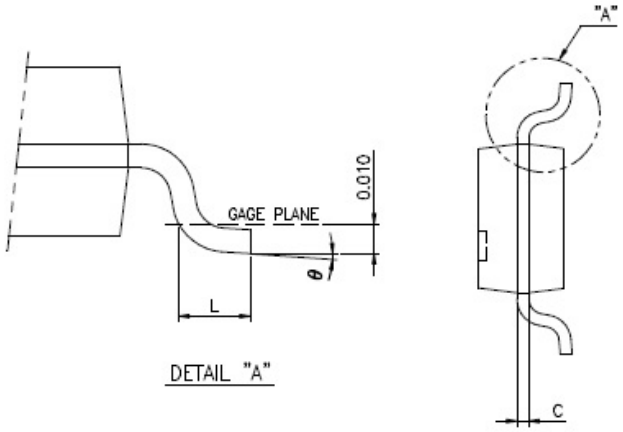


SYMBOLS	Dimensions shown in inches			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ °	0	—	8	0	—	8

MBI5124GP Outline Drawing

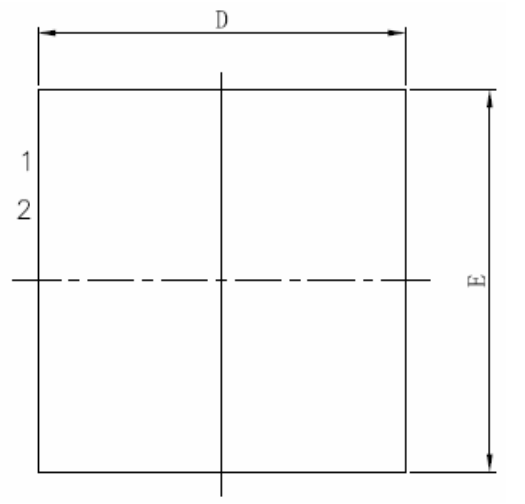


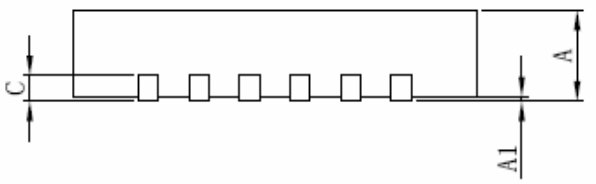


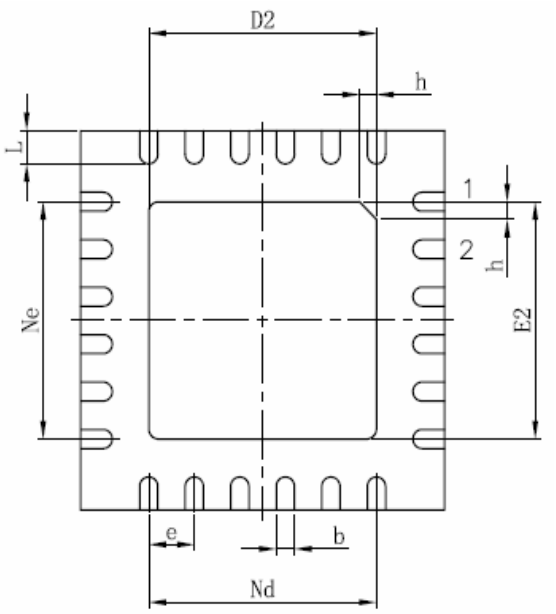


SYMBOLS	DIMENSIONS SHOWN IN INCH			DIMENSIONS SHOWN IN MM		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.058	0.063	0.068	1.473	1.600	1.727
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	0.054	0.057	0.060	1.372	1.448	1.524
b	0.008	0.010	0.012	0.203	0.254	0.305
C	0.007	0.008	0.010	0.178	0.203	0.254
D	0.276	0.280	0.284	7.010	7.112	7.214
E	0.178	0.182	0.185	4.521	4.623	4.699
E1	0.096	0.100	0.103	2.438	2.540	2.616
e	–	0.020	0.0203	–	0.50	0.508
L	0.016	0.025	0.050	0.406	0.635	1.270
y	–	–	0.003	–	–	0.076
θ	0°	–	8°	0°	–	8°

MBI5120GM Outline Drawing





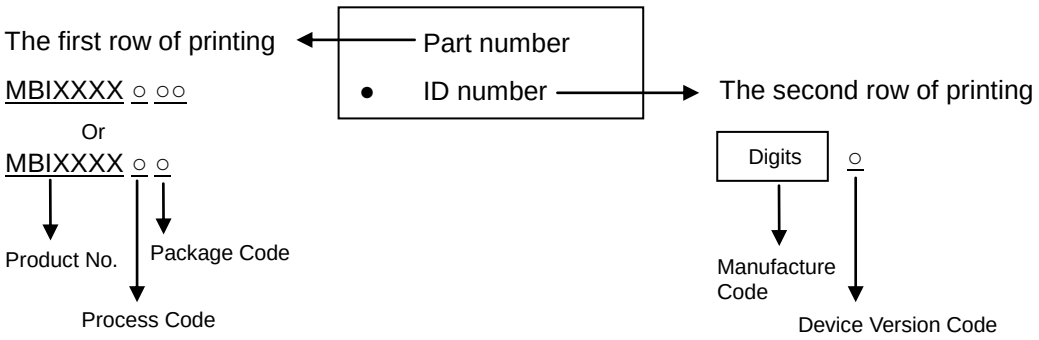


SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	—	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.50REF(MAX.)		
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.50REF(MAX.)		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

MBI5124GFN Outline Drawing

Note: The thermal pad size may exist a tolerance due to the manufacturing process, please use the maximum dimensions-D2(max. 2.50mm) x E2(max. 2.50mm) for the thermal pad layout. In addition, to avoid the short circuit risk, the vias or circuit traces shall not pass through the maximum area of thermal pad.

Product Top-mark Information



Product Revision History

Datasheet Version	Device Version Code
V1.00	A
V1.01	A
V1.02	A
V0.01	B

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5124GF-B	SOP24L-300-1.00	0.28
MBI5124GP-B	SSOP24L-150-0.64	0.11
MBI5124GM-B	mSSOP24L-100-0.5	0.079
MBI5124GFN-B	QFN24L-4*4-0.5	0.0379

*Please place your order with the “product ordering number” information on your purchase order (PO).

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