

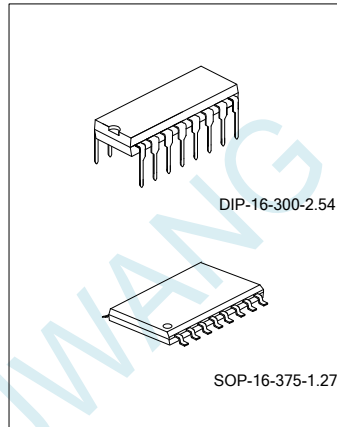
**CURRENT MODE PWM CONTROLLER**

**DESCRIPTION**

The UTC3846 control IC provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a  $\pm 1\%$  trimmed bandgap reference.



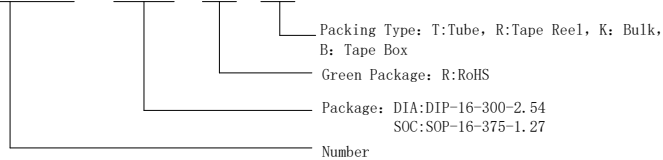
**FEATURES**

- \* Automatic Feed Forward Compensation
- \* Programmable Pulse-by-Pulse Current Limiting
- \* Automatic Symmetry Correction in Push-pull Configuration
- \* Enhanced Load Response Characteristics
- \* Parallel Operation Capability for Modular Power Systems
- \* Differential Current Sense Amplifier with Wide Common Mode Range
- \* Double Pulse Suppression
- \* 500mA (Peak) Totem-pole Outputs
- \* 1% Bandgap Reference
- \* Under-voltage Lockout
- \* Soft Start Capability
- \* Shutdown Terminal
- \* 500kHz Operation

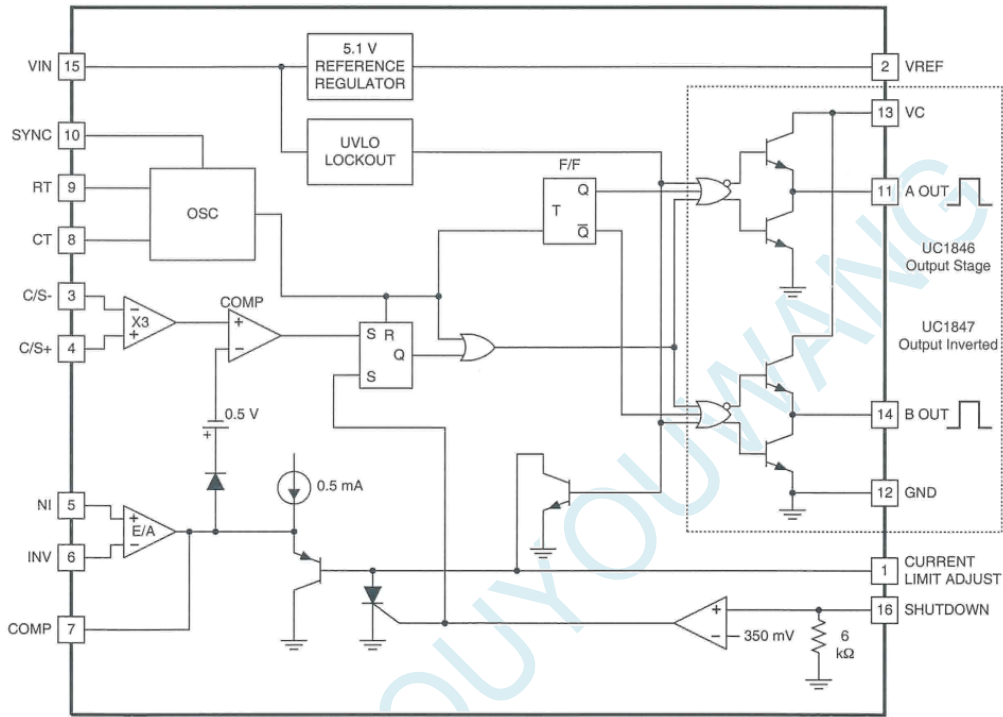
**ORDERING INFORMATION**

Ordering Number	Package	Print Number	Free	Packing
UTC3846-DIA-R-T	DIP-16-300-2.54	UTC3846	RoHS	Tube
UTC3846-SOC-R-T	SOP-16-375-1.27	UTC3846	RoHS	Tube
UTC3846-SOC-R-R	SOP-16-375-1.27	UTC3846	RoHS	Tape Reel

**UTC3846 - DIA - R - T**



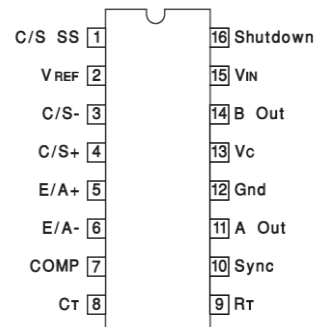
**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**(Note 1)

Supply Voltage (Pin 15).....	+40V
Collector Supply Voltage (Pin 13).....	+40V
Output Current, Source or Sink (Pins 11, 14).....	500mA
Analog Inputs (Pins 3, 4, 5, 6, 16).....	-0.3V to +VIN
Reference Output Current (Pin 2).....	-30mA
Sync Output Current (Pin 10).....	-5mA
Error Amplifier Output Current (Pin 7) .....	-5mA
Soft Start Sink Current (Pin 1) .....	50mA
Oscillator Charging Current (Pin 9) .....	5mA
Power Dissipation at TA=25°C.....	1000mW
Power Dissipation at TC=25°C.....	2000mW
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (soldering, 10 seconds) .....	+300°C

**CONNECTION DIAGRAMS**



Note 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

**ELECTRICAL CHARACTERISTICS**( $T_A=0^{\circ}\text{C}$  to  $+7^{\circ}\text{C}$ ,  $V_{IN}=15\text{V}$ ,  $R_T=10\text{k}$ ,  $C_T=4.7\text{nF}$ ,  $T_A=T_J$ .)

PARAMETER	Test Condition	Min	Typ.	Max	Unit
<b>Reference Section</b>					
Output Voltage	$T_J=25^{\circ}\text{C}$ , $I_O=1\text{mA}$	5.00	5.10	5.20	V
Line Regulation	$V_{IN}=8\text{V}$ to $40\text{V}$		5	20	mV
Load Regulation	$I_L=1\text{mA}$ to $10\text{mA}$		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4		mV/ $^{\circ}\text{C}$
Total Output Variation	Line, Load, and Temperature (Note 2)	4.95		5.25	V
Output Noise Voltage	$10\text{Hz}\leq f\leq 10\text{kHz}$ , $T_J=25^{\circ}\text{C}$ (Note 2)		100		$\mu\text{V}$
Long Term Stability	$T_J=125^{\circ}\text{C}$ , 1000 Hrs. (Note 2)		5		mV
Short Circuit Output Current	$V_{REF}=0\text{V}$	-10	-45		mA
<b>Oscillator Section</b>					
Initial Accuracy	$T_J=25^{\circ}\text{C}$	39	43	47	kHz
Voltage Stability	$V_{IN}=8\text{V}$ to $40\text{V}$		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1		%
Sync Output High Level		3.9	4.35		V
Sync Output Low Level			2.3	2.5	V
Sync Input High Level	Pin 8=0V	3.9			V
Sync Input Low Level	Pin 8=0V			2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.1	1.5	mA
<b>Oscillator Section</b>					
Input Offset Voltage			0.5	10	mV
Input Bias Current			-0.6	-2	$\mu\text{A}$
Input Offset Current			40	250	nA
Common Mode Range	$V_{IN}=8\text{V}$ to $40\text{V}$	0		$V_{IN}-2\text{V}$	V
Open Loop Voltage Gain	$\Delta V_O=1.2$ to $3\text{V}$ , $V_{CM}=2\text{V}$	80	105		dB
Unity Gain Bandwidth	$T_J=25^{\circ}\text{C}$ (Note 2)	0.7	1.0		MHz
CMRR	$V_{CM}=0\text{V}$ to $38\text{V}$ , $V_{IN}=40\text{V}$	75	100		dB
PSRR	$V_{IN}=8\text{V}$ to $40\text{V}$	80	105		dB
Output Sink Current	$V_{ID}=-15\text{mV}$ to $-5\text{V}$ , $V_{PIN 7}=1.2\text{V}$	2	6		mA
Output Source Current	$V_{ID}=15\text{mV}$ to $5\text{V}$ , $V_{PIN 7}=2.5\text{V}$	-0.4	-0.5		mA
High Level Output Voltage	$R_L=(\text{Pin } 7) 15\text{k}\Omega$	4.1	4.6		V
Low Level Output Voltage			0.7	1	V
<b>Current Sense Amplifier Section</b>					
Amplifier Gain	$V_{PIN 3}=0\text{V}$ , Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	V
Maximum Differential Input Signal ( $V_{PIN 4}-V_{PIN 3}$ )	Pin 1 Open (Note 3) $R_L(\text{Pin } 7)=15\text{k}\Omega$	1.1	1.2		V
Input Offset Voltage	$V_{PIN 1}=0.5\text{V}$ , Pin 7 Open (Note 3)		5	25	mV
CMRR	$V_{CM}=1\text{V}$ to $12\text{V}$	60	83		dB
PSRR	$V_{IN}=8\text{V}$ to $40\text{V}$	60	84		dB
Input Bias Current	$V_{PIN 1}=0.5\text{V}$ , Pin 7 Open (Note 3)		-2.5	-10	$\mu\text{A}$

Input Offset Current	V <sub>PIN 1</sub> =0.5V, Pin 7 Open (Note 3)		0.08	1	μA
Input Common Mode Range		0		V <sub>IN</sub> -3	V
Delay to Outputs	T <sub>J</sub> =25°C, (Note 2)		200	500	ns
<b>Current Limit Adjust Section</b>					
Current Limit Offset	V <sub>PIN 3</sub> =0V, V <sub>PIN 4</sub> =0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	V
Input Bias Current	V <sub>PIN 5</sub> =V <sub>REF</sub> , V <sub>PIN 6</sub> =0V		-10	-30	μA
<b>Shutdown Terminal Section</b>					
Threshold Voltage		250	350	400	mV
Input Voltage Range		0		V <sub>IN</sub>	V
Minimum Latching Current (I <sub>PIN 1</sub> )	(Note 6)	3.0	1.5		mA
Maximum Non-Latching Current (I <sub>PIN 1</sub> )	(Note 7)		1.5	0.8	mA
Delay to Outputs	T <sub>J</sub> =25°C (Note 2)		300	600	ns
<b>Output Section</b>					
Collector-Emitter Voltage		40			V
Collector Leakage Current	V <sub>C</sub> =40V (Note 5)			200	μA
Output Low Level	I <sub>SINK</sub> =20mA		0.1	0.4	V
Output Low Level	I <sub>SINK</sub> =100mA		0.4	2.1	V
Output High Level	I <sub>SOURCE</sub> =20mA	13	13.5		V
Output High Level	I <sub>SOURCE</sub> =100mA	12	13.5		V
Rise Time	C <sub>L</sub> =1nF, T <sub>J</sub> =25°C (Note 2)		50	300	ns
<b>Under-Voltage Lockout Section</b>					
Start-Up Threshold			7.7	8.0	V
Threshold Hysteresis			0.75		V
<b>Total Standby Current</b>					
Supply Current			14	21	mA

Note 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 3. Parameter measured at trip point of latch with V<sub>PIN 5</sub> = V<sub>REF</sub>, V<sub>PIN 6</sub> = 0V.

Note 4. Amplifier gain defined as: V<sub>PIN 4</sub>= 0 to 1.0V.

$$G = \frac{\Delta V_{PIN7}}{\Delta V_{PIN4}}$$

Note 5. Applies to UTC3846 only due to polarity of outputs.

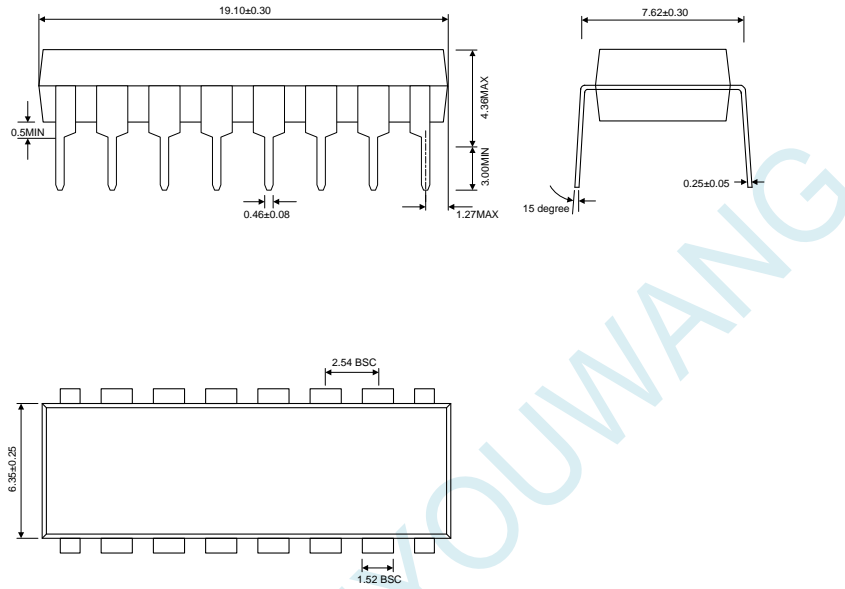
Note 6. Current into Pin 1 guaranteed to latch circuit in shutdown state.

Note 7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

PACKAGE

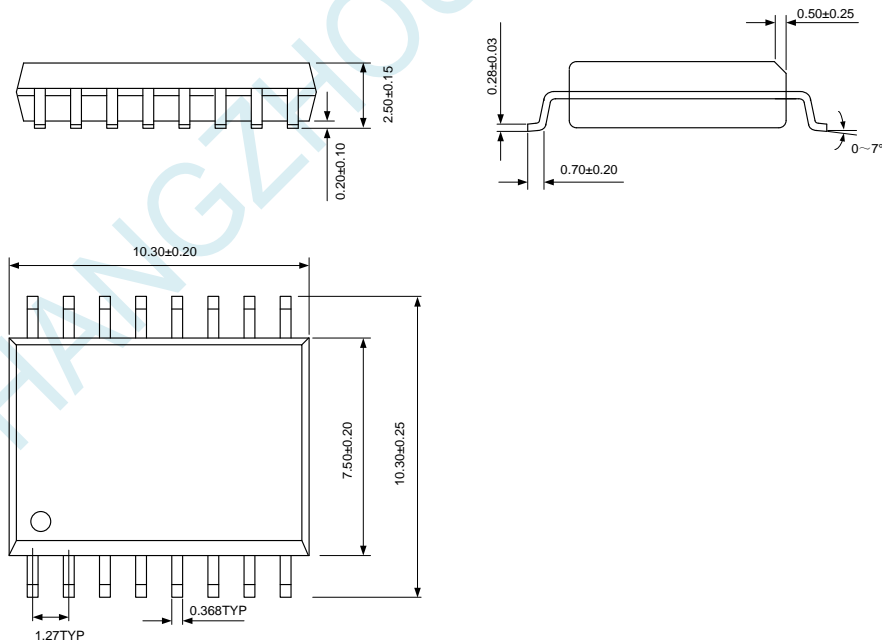
DIP-16-300-2.54

UNIT: mm



SOP-16-375-1.27

UNIT: mm



**ELECTROSTATIC DISCHARGE CAUTION**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage handling to prevent electrostatic damage to the device.

**NOTICE**

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