



深圳市富满电子集团股份有限公司
SHEN ZHEN FINE MADE ELECTRONICS GROUP CO., LTD.

4060K(文件编号: S&CIC1774)

N-Channel Trench Power MOSFET

Description

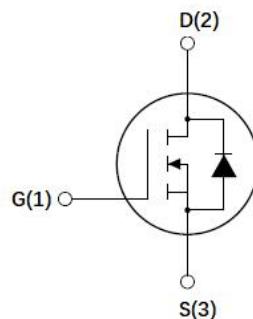
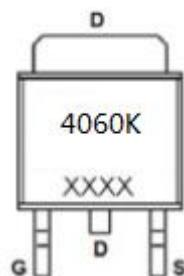
Features

- 40V,60A
- $R_{DS(ON)}=6.8m\Omega$ (Typ.) @ $V_{GS} = 10V$
- $R_{DS(ON)}=9.5m\Omega$ (Typ.) @ $V_{GS} = 4.5V$
- High Density Cell Design for Ultra Low $R_{DS(ON)}$
- Fully Characterized Avalanche Voltage and Current
- Good Stability and Uniformity with High E_{AS}
- Excellent Package for Good Heat Dissipation

Application

- Load Switch
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

Package



Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_c = 25^\circ C$	60	A
		$T_c = 100^\circ C$	42	A
I_{DM}	Pulsed Drain Current ^{note1}		210	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		106	mJ
P_D	Power Dissipation	$T_c = 25^\circ C$	42	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.8	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^\circ C$



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Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}, V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.1	1.65	2.4	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}, I_D=30\text{A}$	-	6.8	8	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$	-	9.5	12	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=15\text{A}$	10	25	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=20\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$	-	2246	-	pF
C_{oss}	Output Capacitance		-	195	-	pF
C_{rss}	Reverse Transfer Capacitance		-	176	-	pF
Q_g	Total Gate Charge	$V_{DS}=20\text{V}, I_D=30\text{A}, V_{GS}=10\text{V}$	-	52	-	nC
Q_{gs}	Gate-Source Charge		-	8	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	14	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=20\text{V}, I_D=30\text{A}, R_L=1\Omega, R_{GEN}=3\Omega, V_{GS}=10\text{V}$	-	13	-	ns
t_r	Turn-on Rise Time		-	37	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	46	-	ns
t_f	Turn-off Fall Time		-	15	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	60	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	210	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}, I_s=30\text{A}$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$T_J=25^\circ\text{C}, I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}$	-	15	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	8	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}, V_{DD}=30\text{V}, V_G=10\text{V}, R_G=25\Omega, L=0.5\text{mH}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

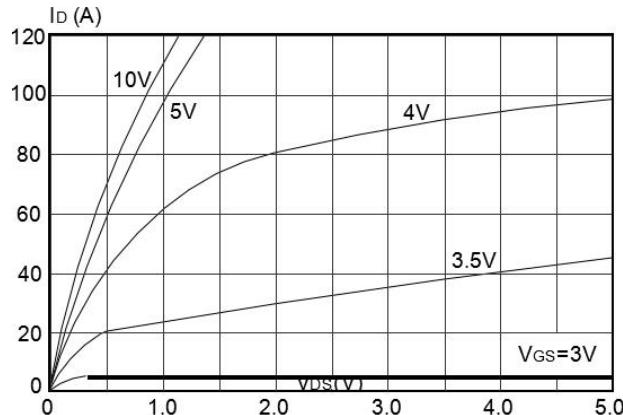


Figure 2: Typical Transfer Characteristics

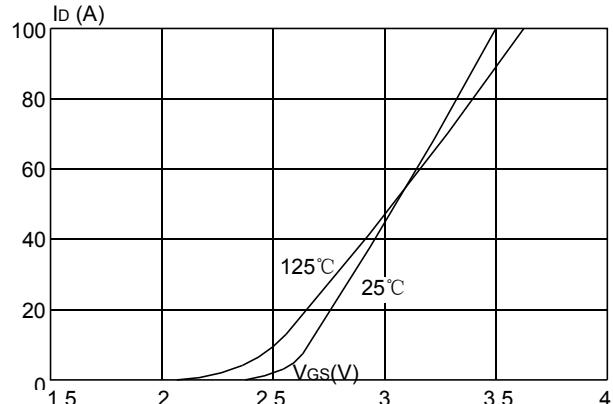


Figure 3: On-resistance vs. Drain Current

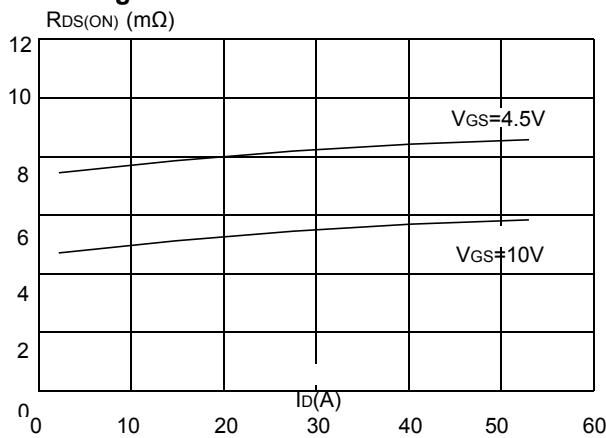


Figure 4: Body Diode Characteristics

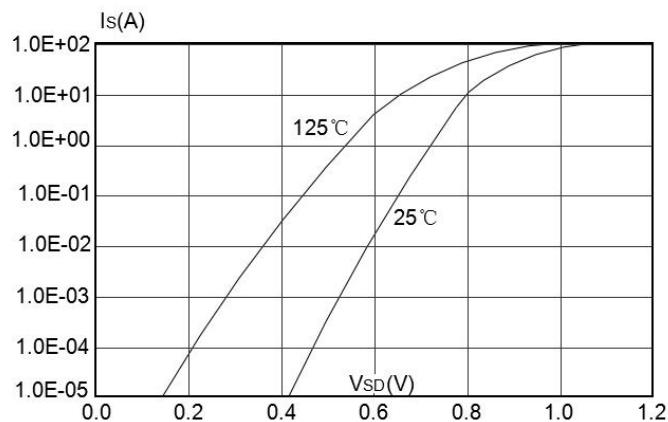


Figure 5: Gate Charge Characteristics

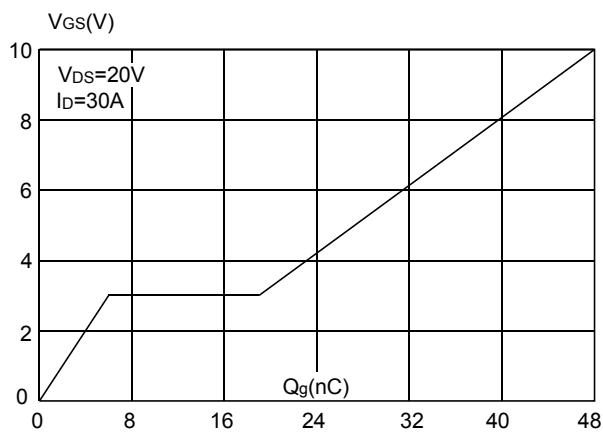


Figure 6: Capacitance Characteristics

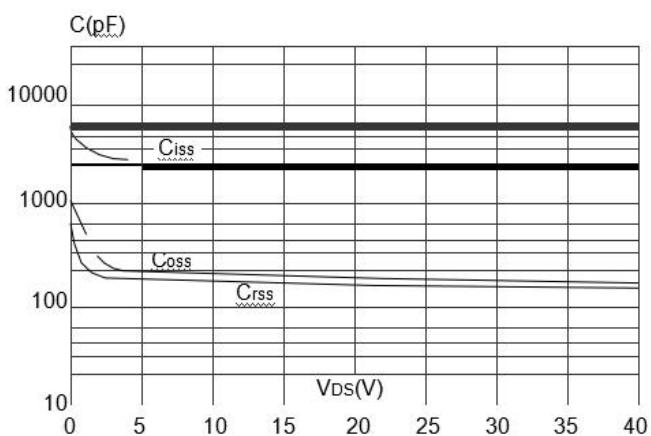


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

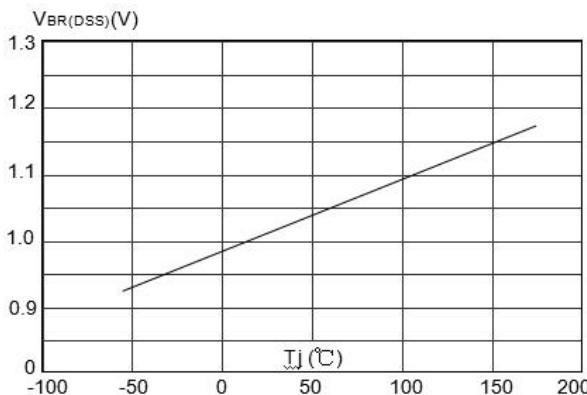


Figure 8: Normalized on Resistance vs. Junction Temperature

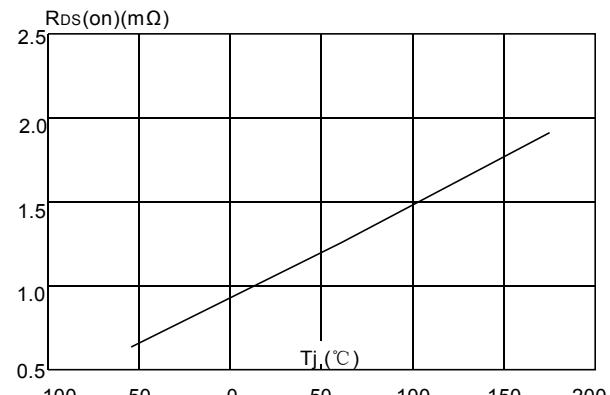


Figure 9: Maximum Safe Operating Area

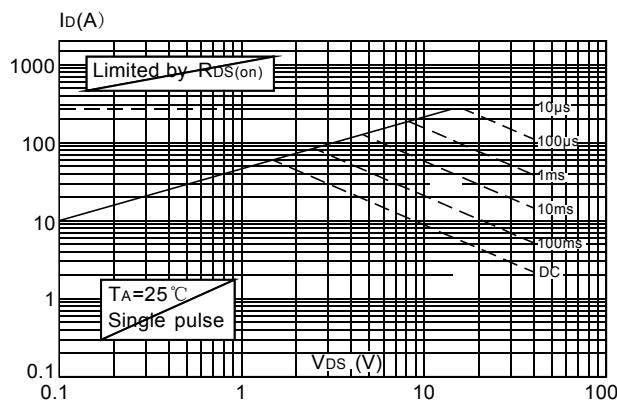


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-252, TO-251S)

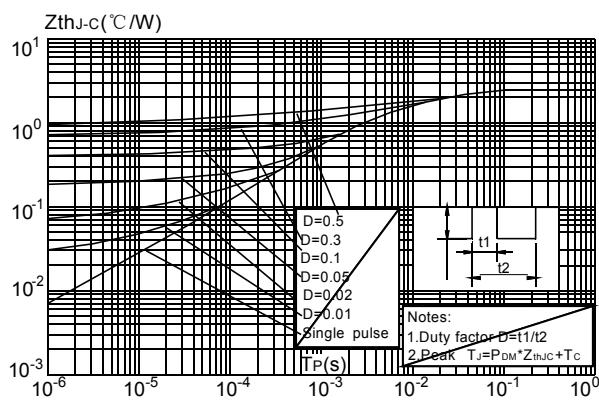
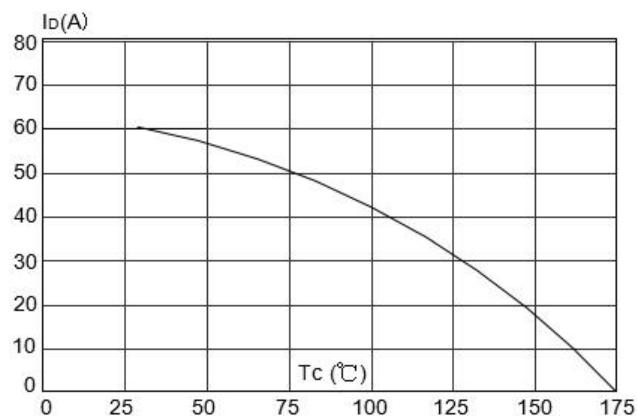


Figure 10: Maximum Continuous Drain Current vs. Case Temperature



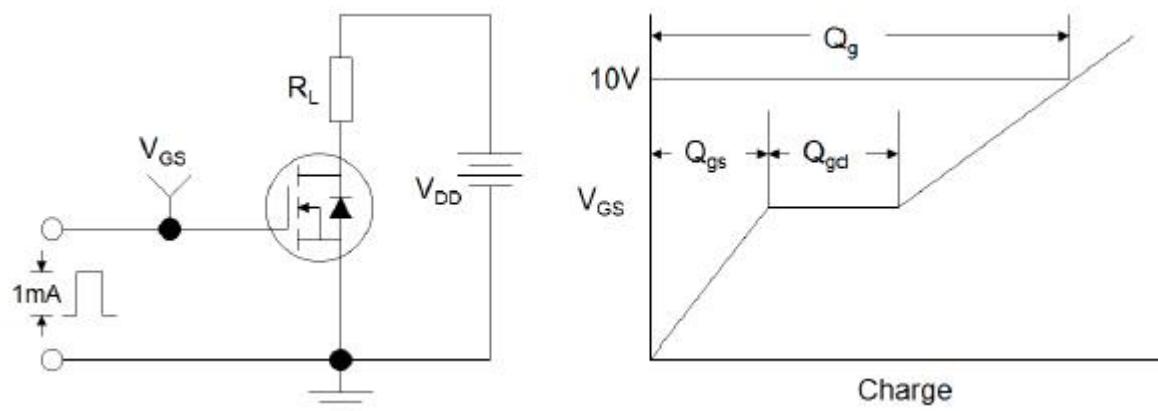


Figure1:Gate Charge Test Circuit & Waveform

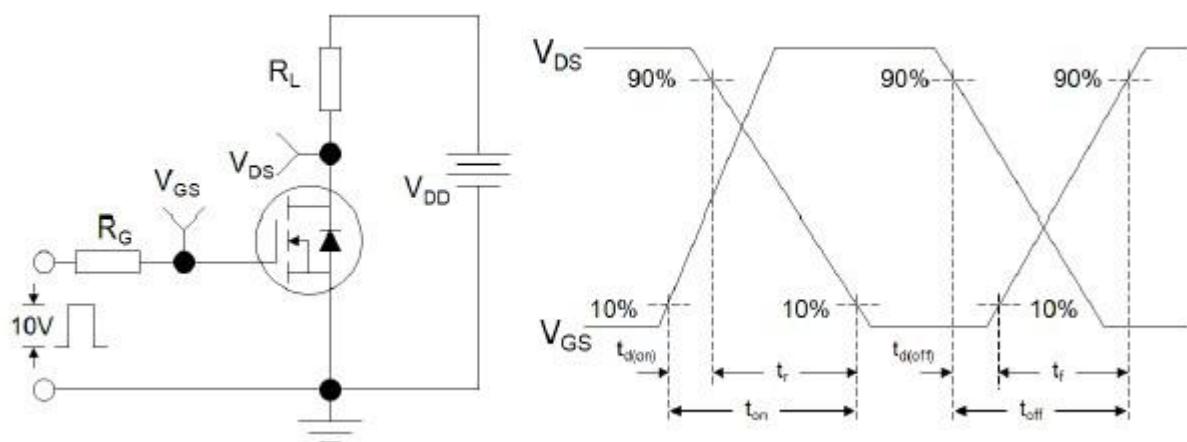


Figure 2: Resistive Switching Test Circuit & Waveforms

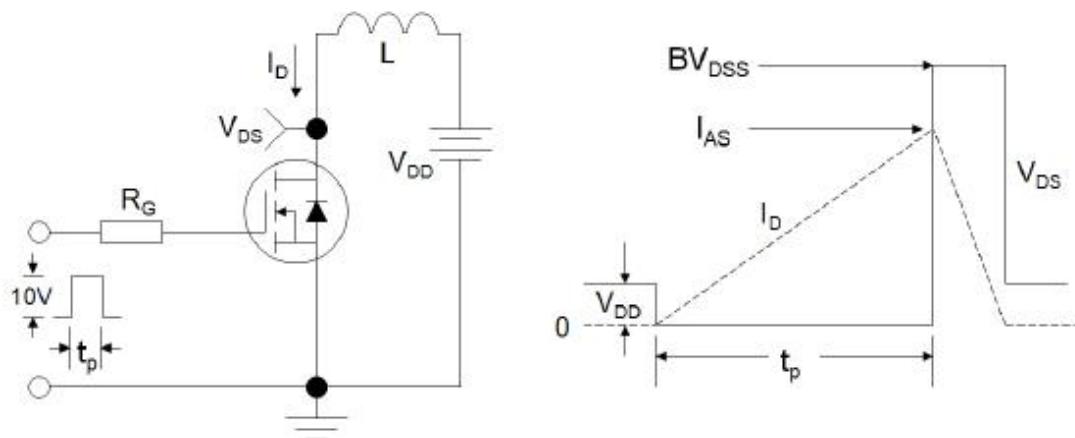
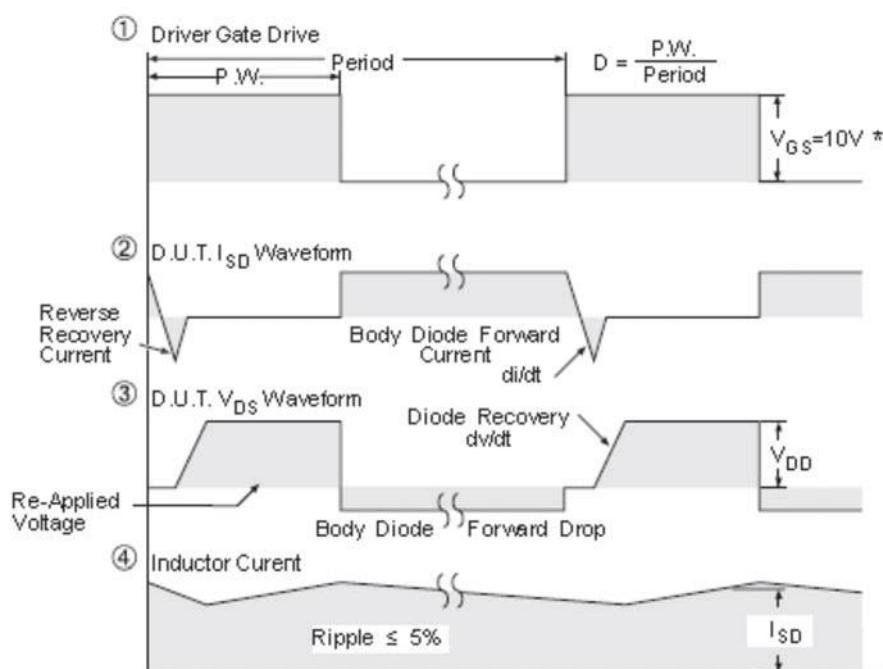
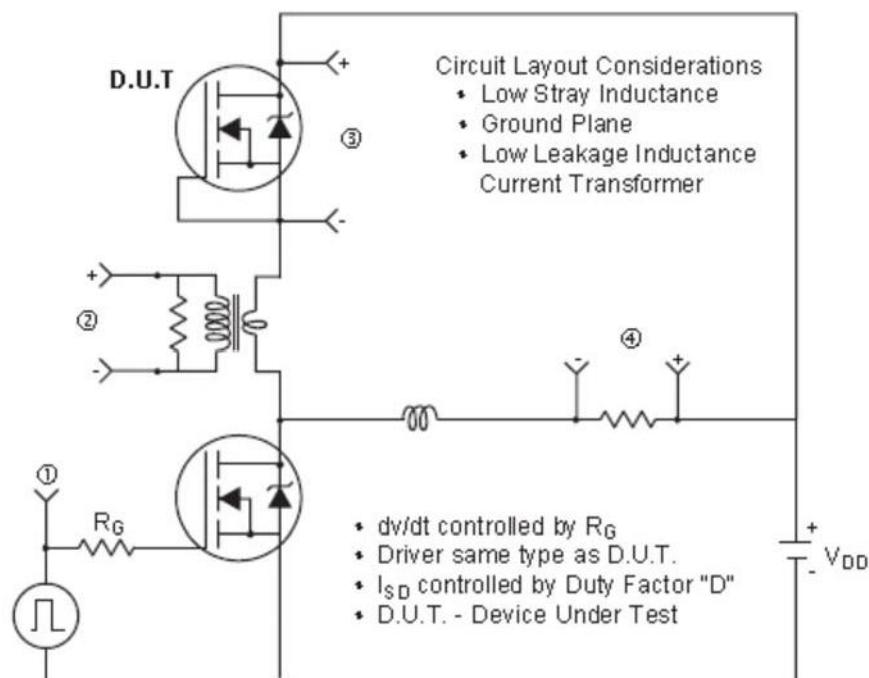


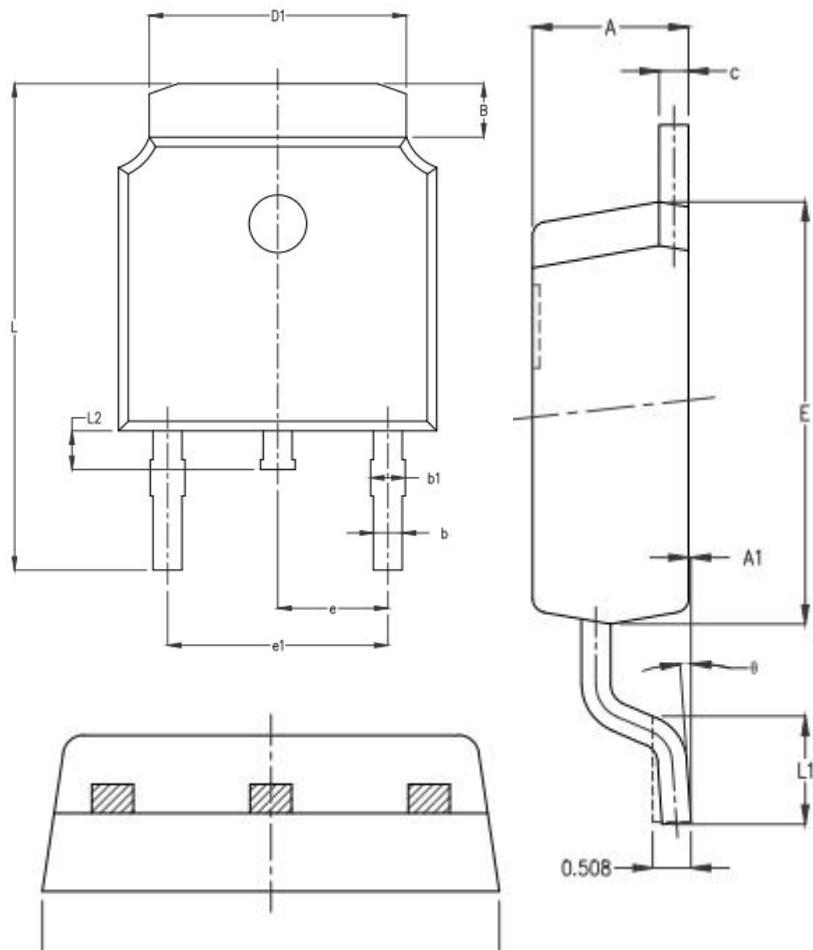
Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



* $V_{GS} = 5V$ for Logic Level Devices

Figure 4:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

TO-252 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.15	2.25	2.35
A1	0.00	0.06	0.12
B	0.96	1.11	1.26
b	0.59	0.69	0.79
b1	0.69	0.81	0.93
c	0.34	0.42	0.50
D	6.45	6.60	6.75
D1	5.23	5.33	5.43
E	5.95	6.10	6.25
e	2.286TYP.		
e1	4.47	4.57	4.67
L	9.90	10.10	10.30
L1	1.40	1.55	1.70
L2	0.60	0.80	1.00
θ	0°	4°	8°