WS7808QM-14/TR

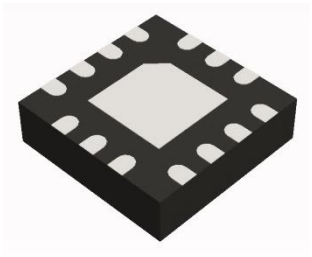
0.1GHz–3GHz SP8T Diversity Antenna Switch with MIPI RFFE Interface

http://omnivision-group.com

Descriptions

The WS7808QM-14/TR is a single-pole, eight-throw (SP8T) antenna switch with a Mobile Industry Processor Interface (MIPI). Using advanced switching technologies, the WS7808QM-14/TR maintains low insertion loss and high isolation for receive switching path. The high linearity performance and low insertion loss achieved by the WS7808QM-14/TR makes it an ideal choice for WCDMA and LTE applications.

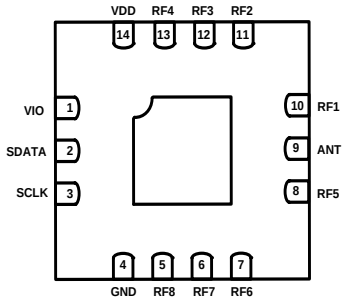
The WS7808QM-14/TR is manufactured in a compact 2.0x2.0x0.55mm, 14-pin surface mount Quad Flat No-Lead (QFN) package.



QFN 2.0x2.0-14L (Bottom view)

Features

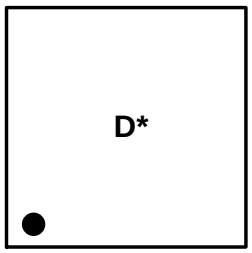
- Small, low profile package 2.0mm x 2.0mm x 0.55mm
- Working frequency up to 3GHz
- Very low insertion loss
- Excellent isolation performance
- Low power consumption
- Exceptional linearity performance for 3G/4G application
- Very good ESD performance



Pin configuration (Top view)

Applications

- Cell phones
- Tablets
- Other RF front-end modules



D= Device code

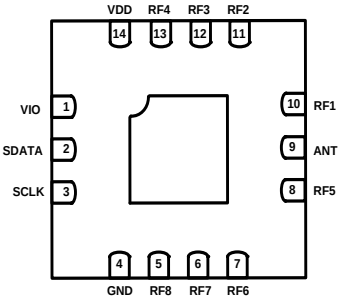
* = Month code（A~Z）

Marking (Top view)

Order information

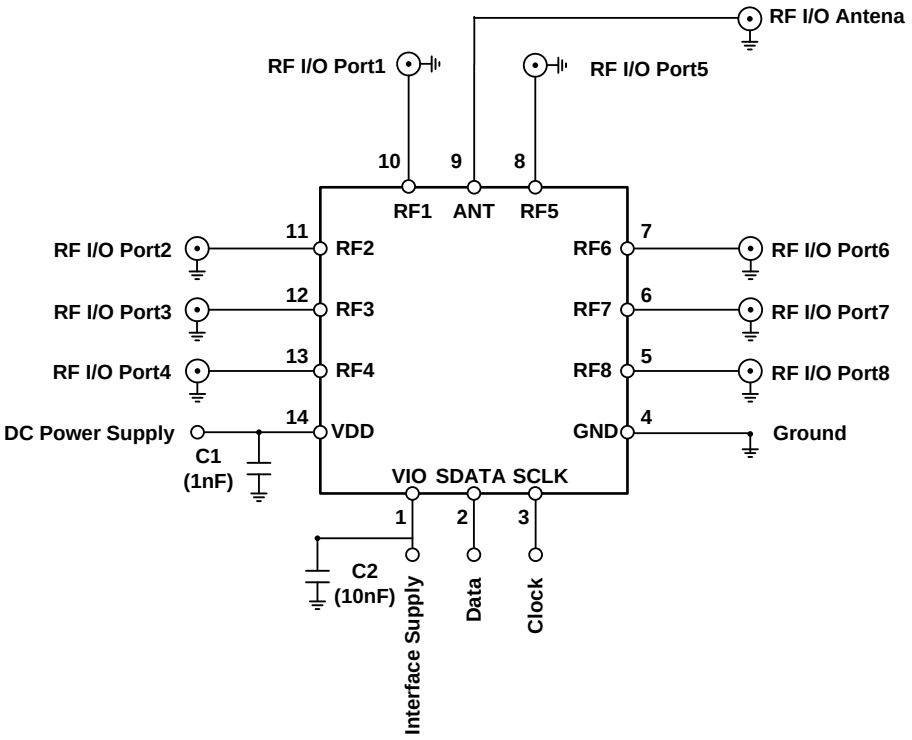
Device	Package	Shipping
WS7808QM-14/TR	QFN 2.0x2.0-14L	3000/Reel &Tape

Pin information

Pin	Function	Description	Transparent top view
1	VIO	MIPI Interface voltage	
2	SDATA	Data input/output	
3	SCLK	Clock signal	
4	GND	Ground	
5	RF8	RF I/O path 8	
6	RF7	RF I/O path 7	
7	RF6	RF I/O path 6	
8	RF5	RF I/O path 5	
9	ANT	Antenna input/output	
10	RF1	RF I/O path 1	
11	RF2	RF I/O path 2	
12	RF3	RF I/O path 3	
13	RF4	RF I/O path 4	
14	VDD	VDD	

Note 1: Bottom ground paddles must be connected to ground.

Application information



WS7808QM-14/TR Evaluation Board Schematic

Note 2: filter capacitor is needed on VDD and VIO respectively

Recommended operating conditions

Parameters	Conditions	Specifications			Unit
		Min.	Typ	Max.	
ESD Rating					
ESD All Pins	HBM, JESD22-A114	-1000		+1000	V
	CDM	-500		+500	V
Power Supply					
Power Supply Voltage	Operating Voltage	2.5	2.8	3.6	V
Power Supply Current	VDD≤3.0V		29	44	μA
Interface supply voltage level		1.65	1.8	1.95	V
Control Voltage					
SCLK port voltage		0.8 x VIO		VIO	V
SDATA port voltage		0		0.2 x VIO	V
RF Impedance					
RF Port Input and Output Impedance			50		Ω
Turn-On Switching Time	50% of final control voltage to 90% of final RF power, switching between RF ports		5		μs

Absolute maximum ratings

Maximum ratings are absolute ratings, exceeding only one of these values may cause irreversible damage to the integrated circuit.

Items	Value	Unit
VDD Voltage	-0.3 to +4.0	V
SDATA, SCLK	-0.3 to +2.0	V
Maximum Input Power	**Value**	**Unit**
Momentary, infrequent occurrence, 50 ohms	+29	dBm
Momentary, infrequent occurrence, 6:1	+27	dBm
Continuous Operation, 50 ohms	+28	dBm
Continuous Operation, 6:1	+26	dBm
Operation Temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C
MSL	3	
Reflow Times	3	

Characteristics (RF spec)

Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated.
VDD=2.8V, Temp=+25°C, P_{IN}=0dBm.

Parameters	Conditions	Specifications			Unit
		Min.	Typ.	Max.	
Insertion Loss (ANT to RFX)	0.1GHz to 1.0GHz		0.40	0.55	dB
	1.0GHz to 2.0GHz		0.45	0.65	
	2.0GHz to 2.7GHz		0.70	1.00	
Isolation (ANT to RFX, RFXm to RFXn)	0.1GHz to 1.0GHz	28	33		dB
	1.0GHz to 2.0GHz	19	24		
	2.0GHz to 2.7GHz	14	19		
Input Return Loss (ANT to RFX)	0.1GHz to 1.0GHz	19	22		dB
	1.0GHz to 2.0GHz	17	20		
	2.0GHz to 2.7GHz	12	15		
Second Harmonics (ANT to RFX)	0.7GHz to 1.0GHz, P_{IN}=+26dBm	80	90		dBc
	1.0GHz to 2.0GHz, P_{IN}=+26dBm	78	88		
	2.0GHz to 2.7GHz, P_{IN}=+26dBm	76	86		
Third Harmonics (ANT to RFX)	0.7GHz to 1.0GHz, P_{IN}=+26dBm	71	81		dBc
	1.0GHz to 2.0GHz, P_{IN}=+26dBm	69	79		
	2.0GHz to 2.7GHz, P_{IN}=+26dBm	67	77		
0.1dB Compression Point (ANT to RFX)	0.7GHz to 2.7GHz		+28		dBm
3rd Order Input Intercept Point (ANT to RFX)	0.7GHz to 2.7GHz P_{IN}=+26dBm Δf =1MHz		62		dBm

IMD2 Test Conditions

Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated.

VDD=2.8V, Temp=+25°C, P_{IN}=0dBm.

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	-15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

IMD3 Test Conditions

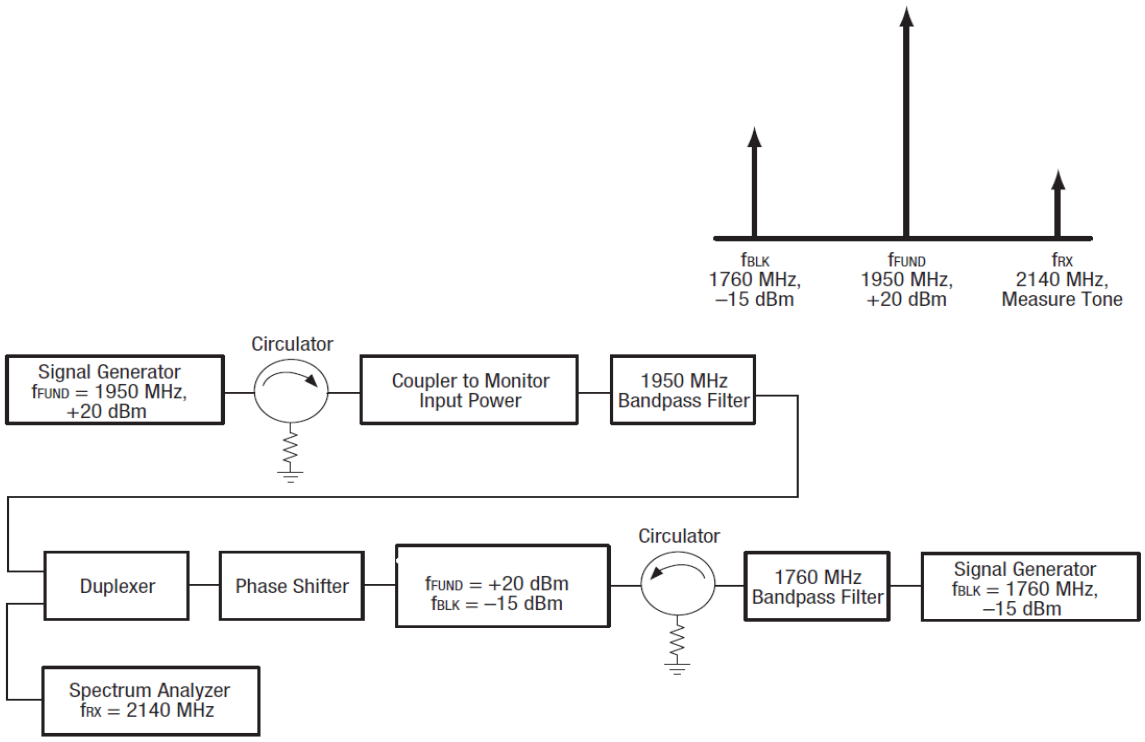
Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated.

VDD=2.8V, Temp =+25°C, P_{IN}=0dBm.

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	-15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Triple Beat Ratio Test Conditions

Band	Transmit Frequency 1 (MHz)	Transmit Power 1 (dBm)	Transmit Frequency 2 (MHz)	Transmit Power 2 (dBm)	Frequency Blocker @ ANT (MHz)	Power Blocker (dBm)	TBR Product Frequency (MHz)
2	1880.0	+21.5	1881.0	+21.5	1960.0	-30	1960.0±1
5	836.5		881.5		881.5		881.5±1



Typical Third Order Intermodulation Test Setup

Power ON and OFF sequence

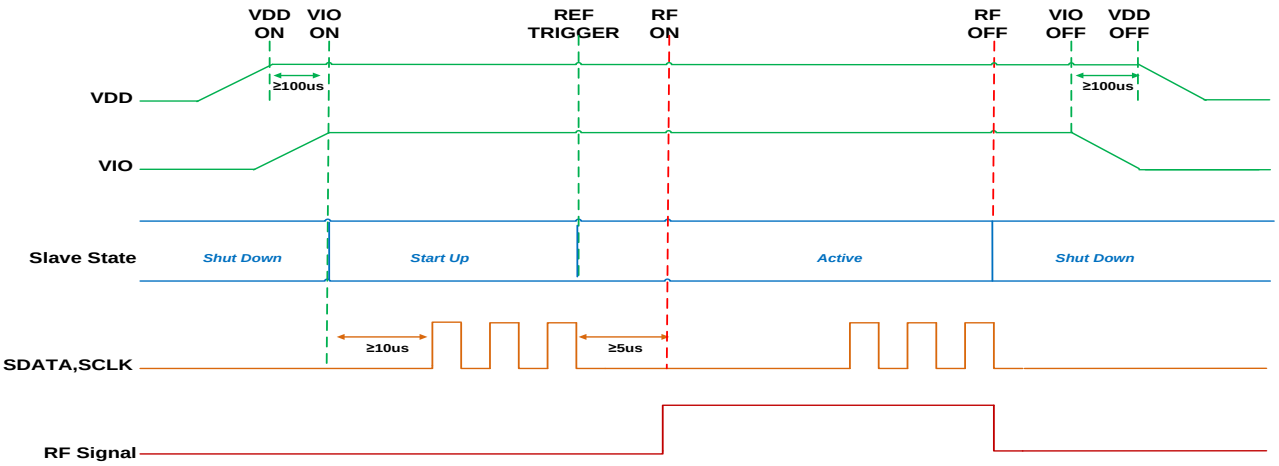
It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device (Note 3).

Power ON

1) Apply voltage supply - VDD
2) Wait 100μs or greater and then apply logic supply - VIO
3) Wait 10μs or greater and then apply RFFE
4) Wait 5μs or greater after RFFE Trigger falling edge and then apply the RF Signal

Power OFF

1) Remove the RF Signal
2) Remove RFFE
3) Remove logic supply - VIO
4) Remove voltage supply – VDD



Note 3: VIO can be applied to the device after VDD or removed before VDD .It is important to wait 10μs after VIO & VDD are applied before sending SDATA to ensure correction data transmission. The minimum time between a power up and power down sequence (and vice versa) is ≥ 100us.

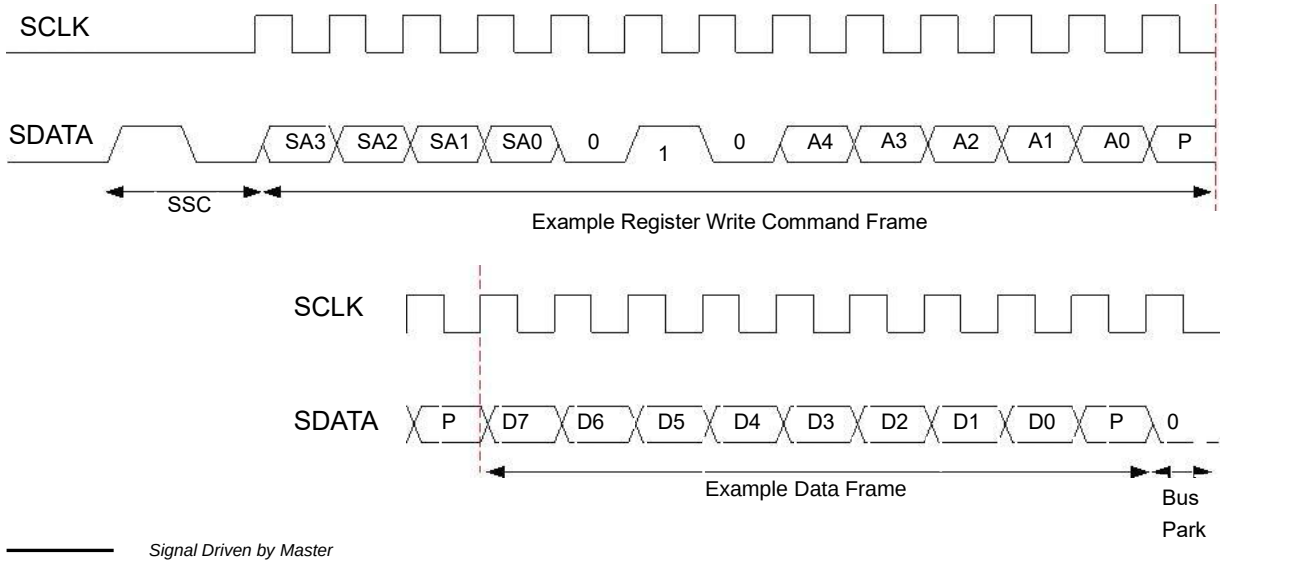
Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg_0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	-	-	-	-	-	-
Reg_1 Write	Y	SA[3:0]	0	10	Addr[4]	Data{3:0]	Y	-	Data[7:0]	-	-	-	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Data{3:0]	Y	Y	Data[7:0]	-	-	-	Y	Y

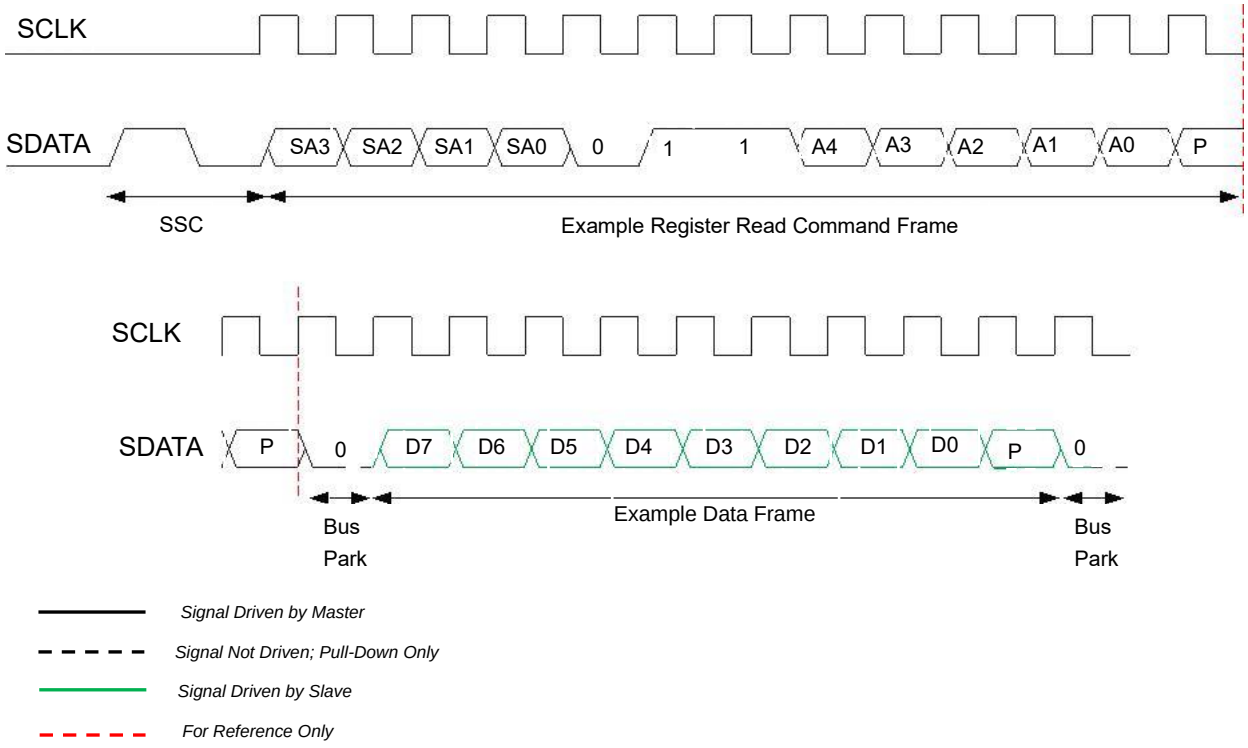
Legend:

SSC = Sequence start command DA = Data/address frame bits BC = Byte count (# of consecutive addresses)

C = Command frame bits BPC = Bus park cycle



Register Write Command Timing Diagram



Register Read Command Timing Diagram

Register Truth Table (ANT)

Mode	Register Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
Isolation		0	0	0	0	0	0	0
RF1		0	0	0	0	0	1	0
RF2		0	0	0	1	0	1	0
RF3		0	0	0	1	1	1	0
RF4		0	0	0	1	0	1	1
RF5		0	0	0	0	0	0	1
RF6		0	0	0	1	0	0	1
RF7		0	0	0	0	1	1	0
RF8		0	0	0	0	1	0	0

Register Description and Programming

Register		Parameter	Description	Default Name (Binary)
Name	Address (Hex)			
Register	0000	MODE_CTRL	Bits[6:0]: See Register Truth Table for logic	0000000
RFFE_STATUS	001A	SOFTWARE RESET	Bits[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation (active) 1 = Software reset	0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error =1.	0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the MIPI Alliance Specification) or GSID.	0
PM_TRIG (Note 4)	001C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	00

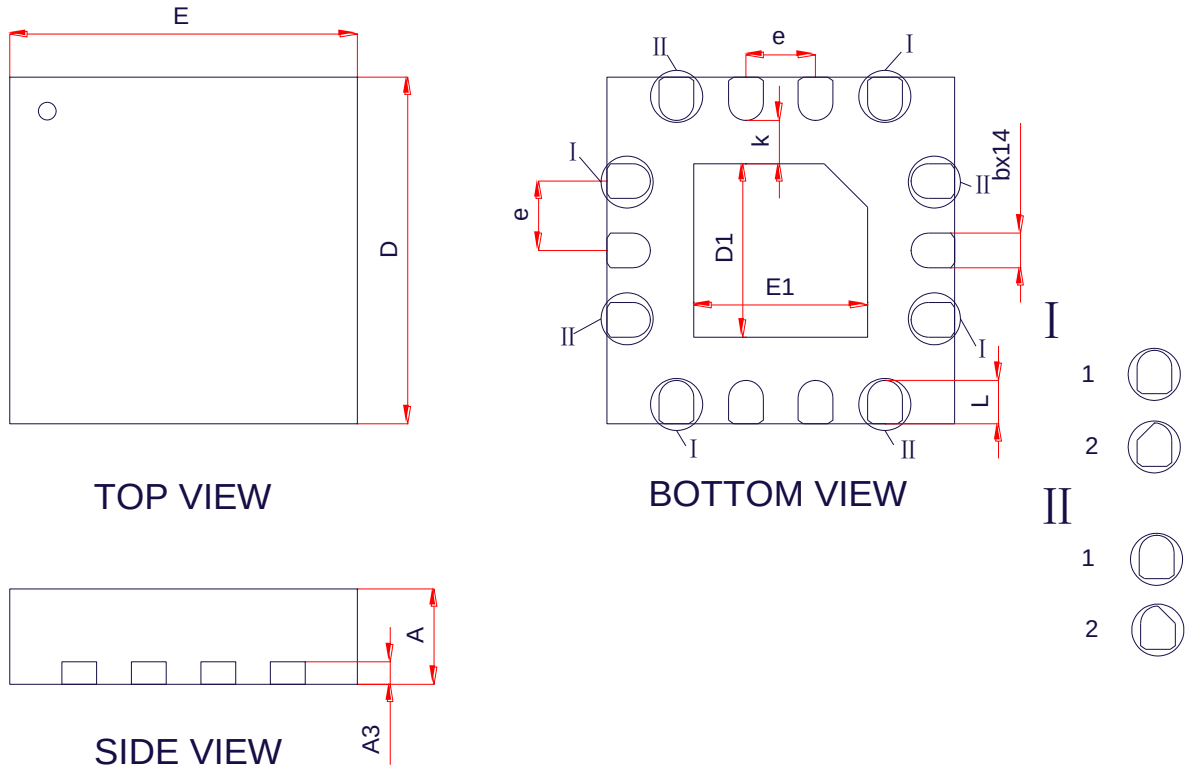
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers.	0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers.	0
PRODUCT_ID	001D	PRODUCT_ID	Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	00001000
MANUFAC-TURER_ID	001E	MANUFACTURER_ID[7:0]	Bits[7:0]: Read-only register	10111100
MAN_USID	001F	Reserved	Bits[7:6]: Reserved	00
		MANUFACTURER_ID[9:8]	Bits[5:4]: Read-only register	11
		USID	Bits[3:0]: Programmable USID. A write to these bits programs the USID.	1010

Note 4: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification this device uses additional interactions between the provided trigger functions. The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular triggerable used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Package Dimensions

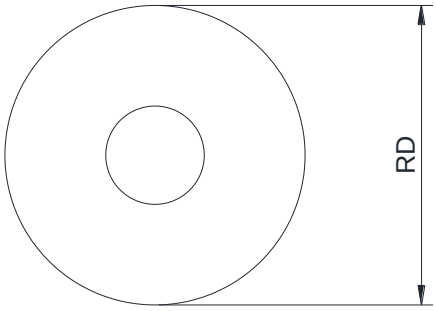
QFN2x2-14L



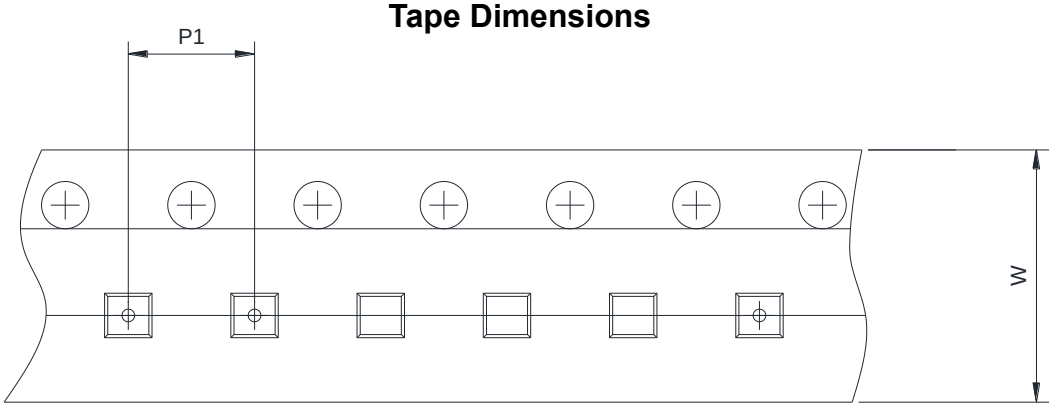
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A3		0.152Ref.	
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D1	0.90	1.00	1.10
E1	0.90	1.00	1.10
b	0.15	0.20	0.25
e		0.40 BSC..	
L	0.19	0.25	0.30
K	0.20	0.25	0.31

Tape and Reel Information

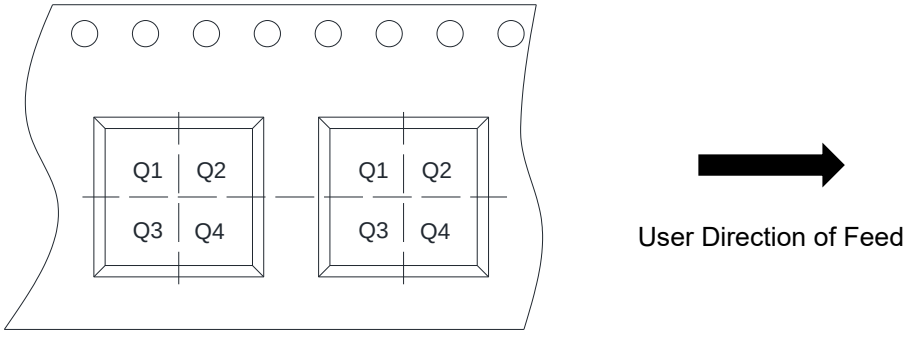
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4