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TPM2021NEC3

N-Channel Enhancement Mode MOSFET

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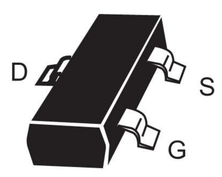
Features

- Surface Mount Package
- N-Channel Switch with Low $R_{DS(on)}$
- Operated at Low Logic Level Gate Drive
- ESD Protected
-

Application

- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

Package and Pin Configuration



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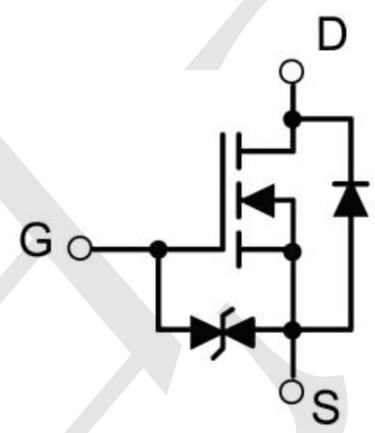
Circuit diagram



Marking: 21P

Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	0.7	A
Pulsed Drain Current (t=300μs) (1)	I_{DM}	1.8	A
Power Dissipation (2)	P_D	100	mW
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	833	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =20V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±10V, V_{DS} = 0V			±10	μA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.35	0.75	1.1	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =4.5V, I_D =650mA		130	250	mΩ
		V_{GS} =2 5V I_D =550mA		190	370	
Forward tranconductance	g_{FS}	V_{DS} =10V, I_D =500mA			1.2	S
Dynamic characteristics(4)						
Input Capacitance	C_{iss}	V_{DS} =16V,V_{GS} =0V,f =1MHz			120	pF
Output Capacitance	C_{oss}				20	
Reverse Transfer Capacitance	C_{rss}				15	
Switching Characteristics(4)						
Turn-on delay time	$t_{d(on)}$	V_{DD}=10V,I_D=500mA, V_{GS}=4.5V,R_G=10Ω		6.7		ns
Turn-on rise time	t_r			4.8		
Turn-off delay time	$t_{d(off)}$			17.3		
Turn-off fall time	t_f			7.4		
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{DS}	I_S=0.15A, V_{GS} = 0V			1.2	V

Characteristic Curves

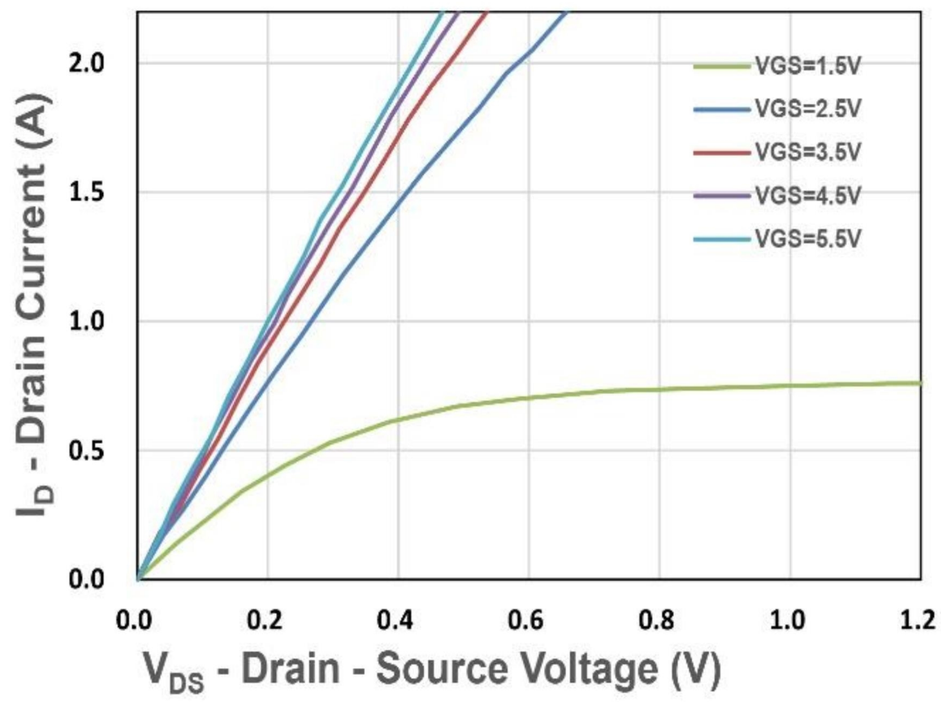


Figure 1. Output Characteristics

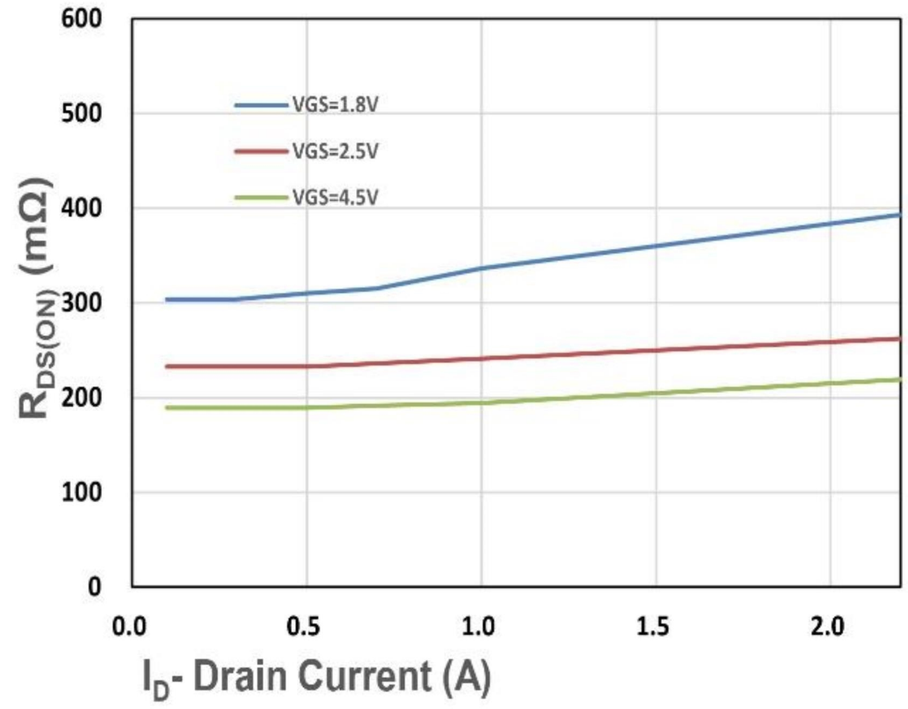


Figure 2. On-Resistance vs. ID

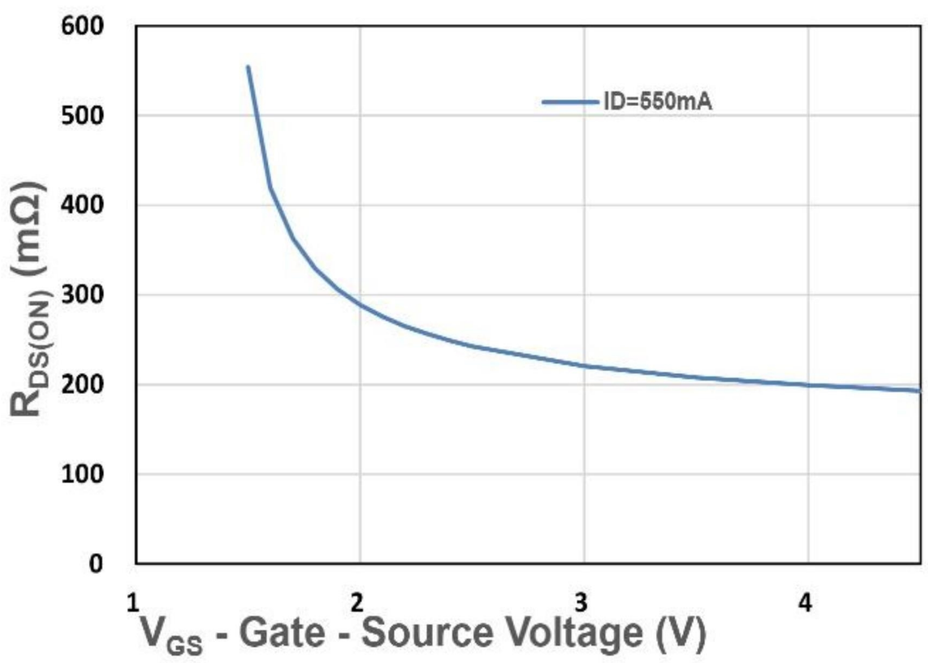


Figure 3. On-Resistance vs. VGS

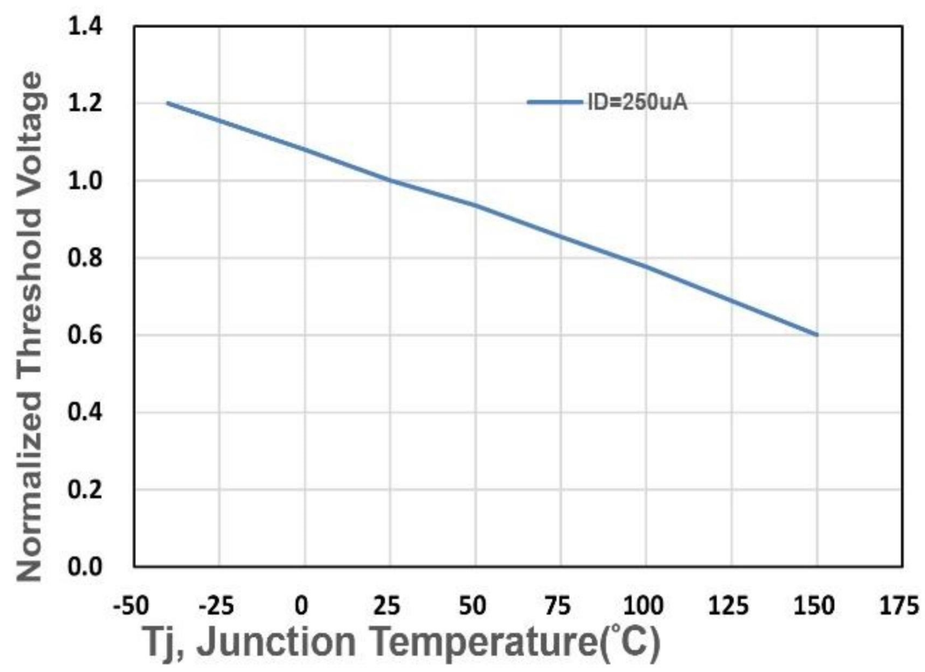


Figure 4. Gate Threshold Voltage

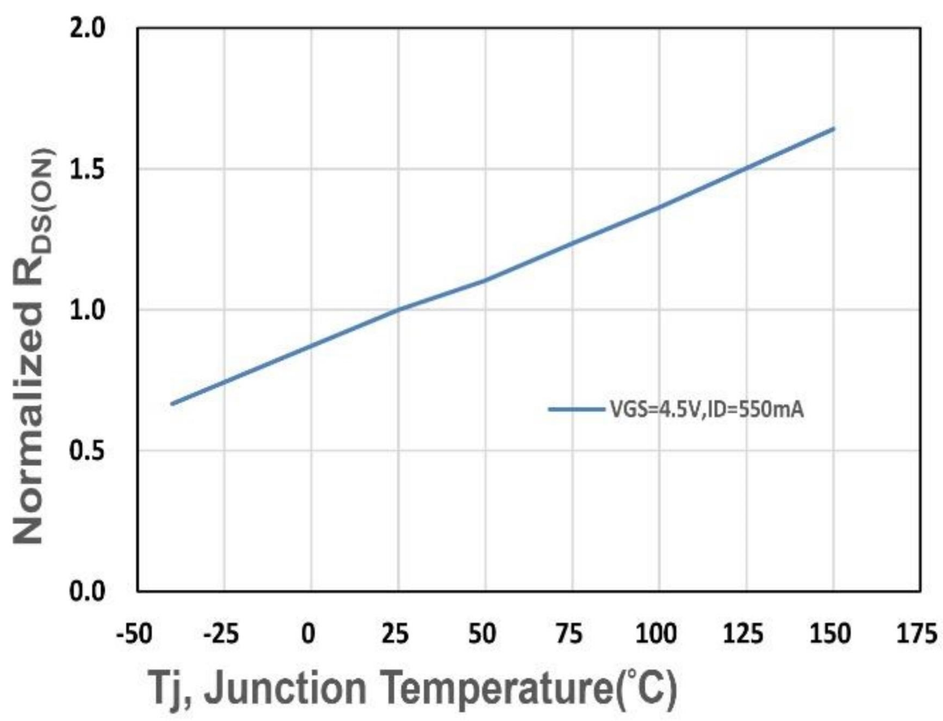


Figure 5. Drain-Source On Resistance

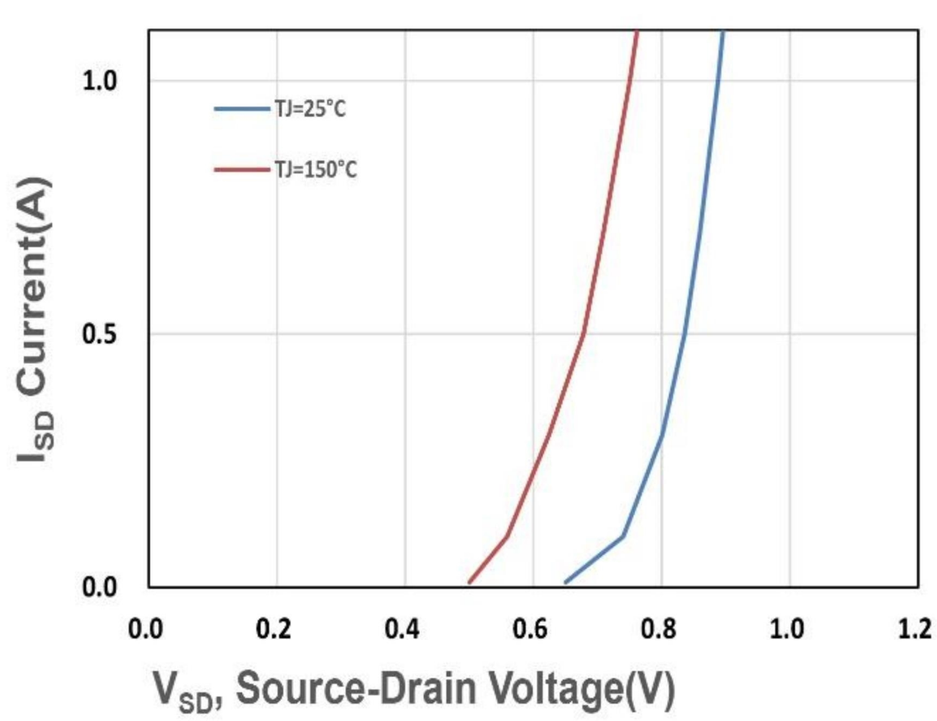


Figure 6. Source-Drain Diode Forward

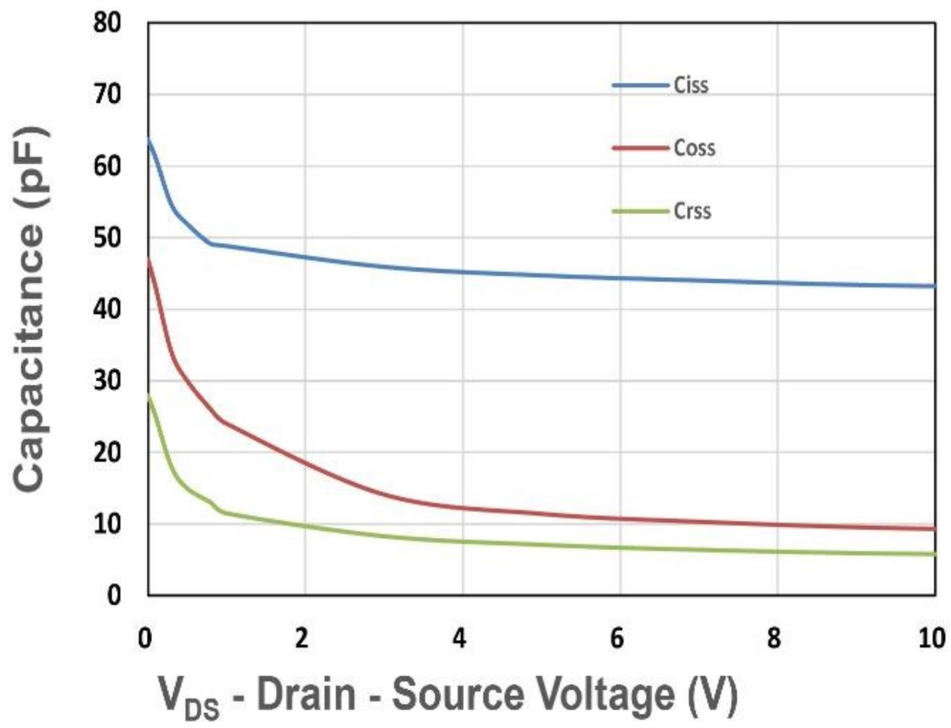


Figure 7. Capacitance

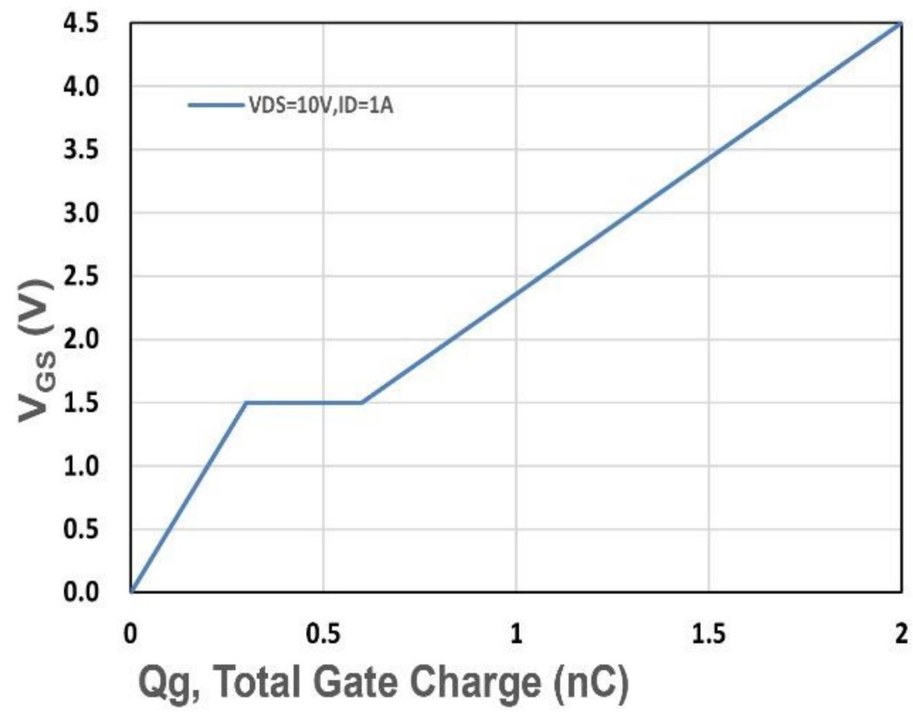


Figure 8. Gate Charge Characteristics

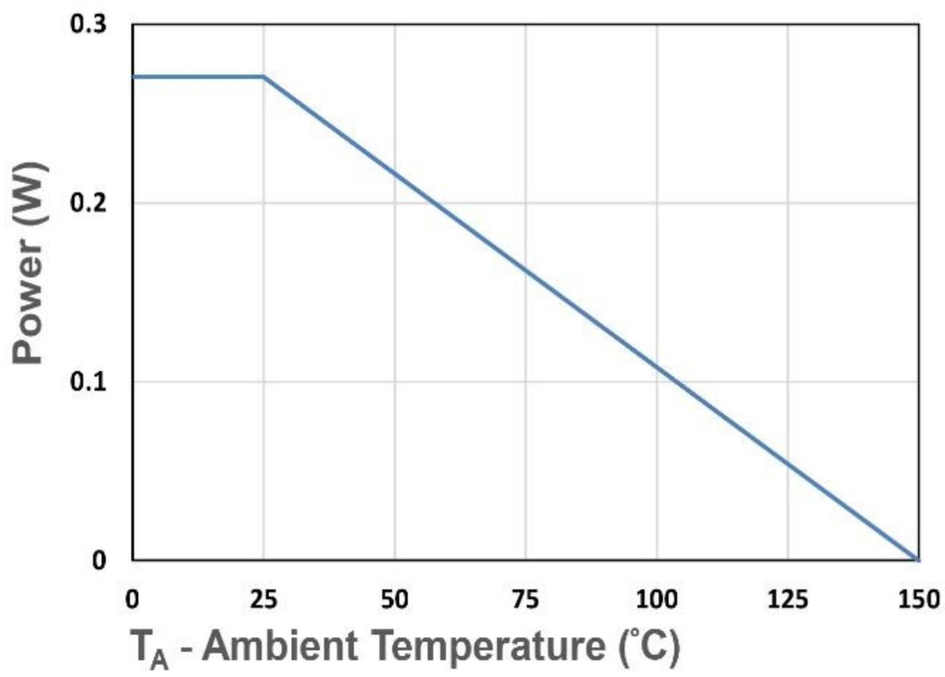


Figure 9. Power Dissipation

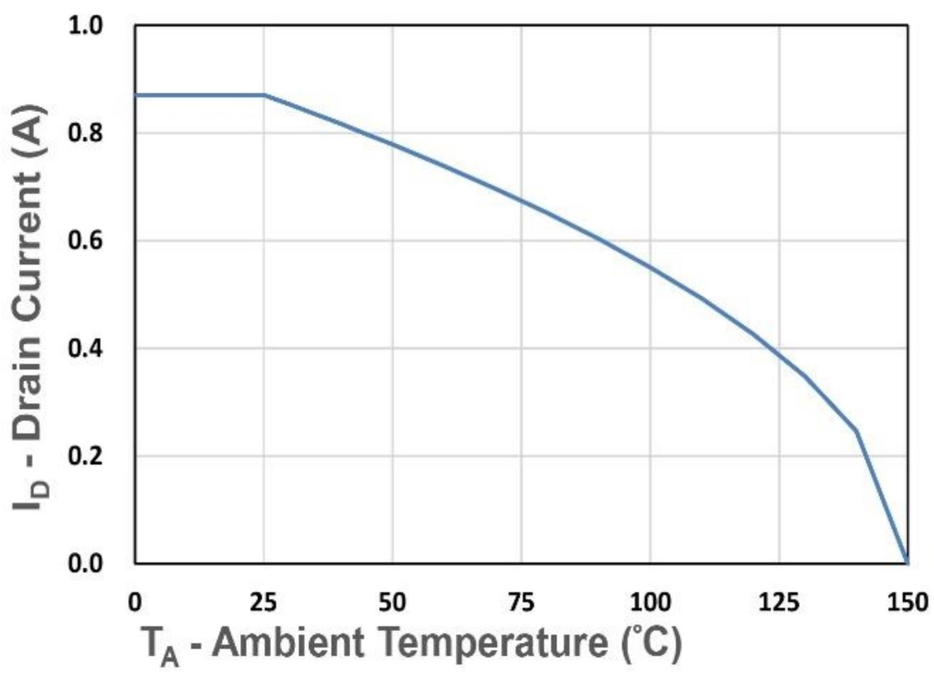


Figure 10. Drain Current

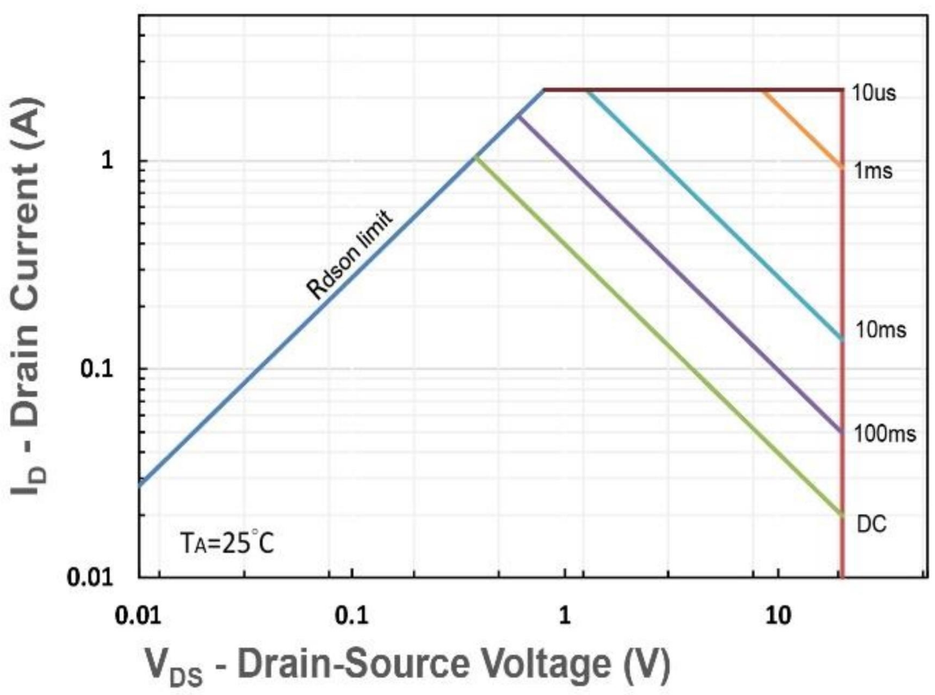


Figure 11. Safe Operating Area

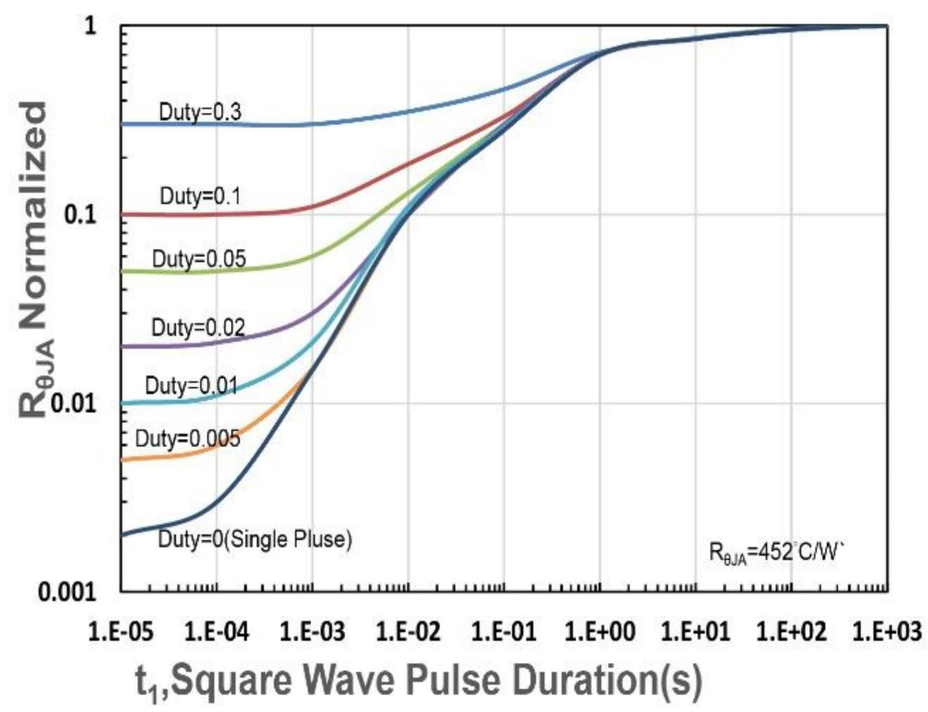
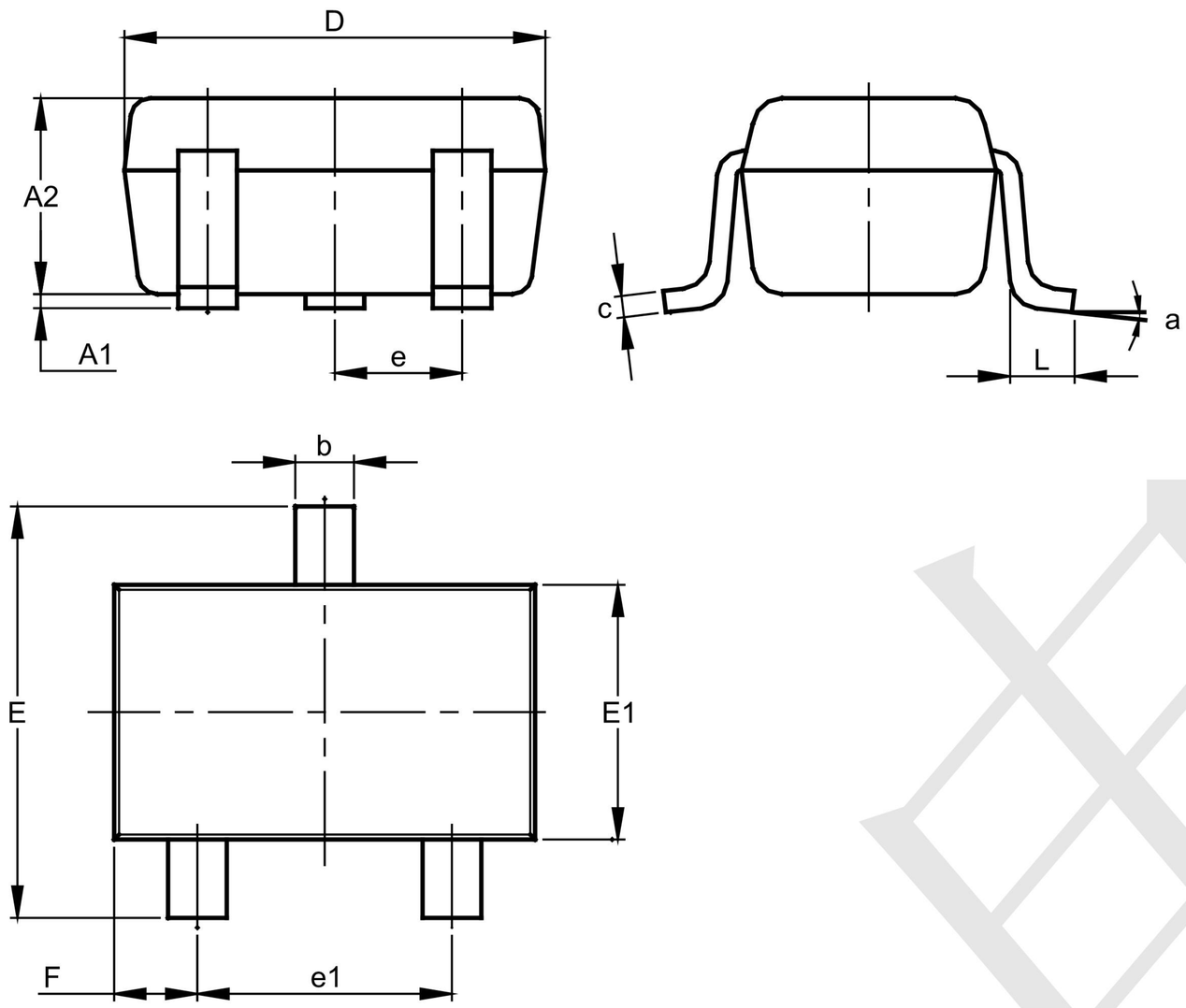


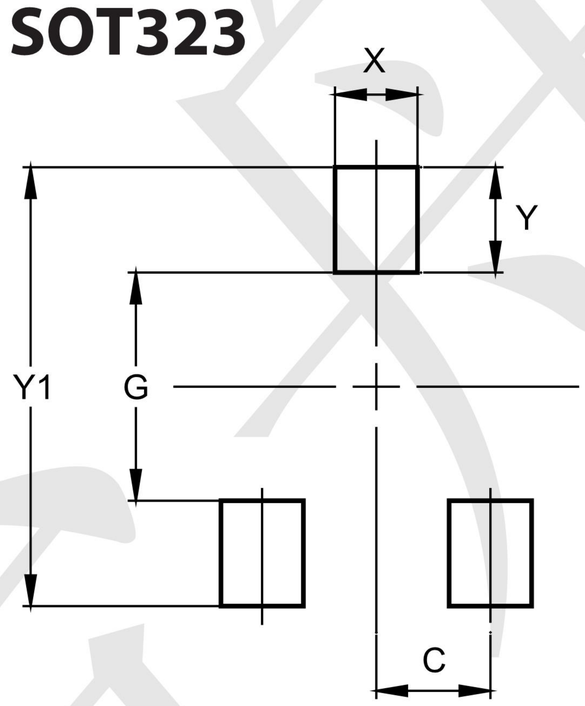
Figure 12. RθJA Transient Thermal Impedance

Outline Drawing - SOT323(SC70-3)



SOT323			
Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.90	1.00	0.95
b	0.25	0.40	0.30
c	0.10	0.18	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
e1	1.20	1.40	1.30
F	0.375	0.475	0.425
L	0.25	0.40	0.30
a	0°	8°	--
All Dimensions in mm			

Land Pattern - SOT323



Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.470
Y	0.600
Y1	2.500