# RL78/G13

RENESAS MCU

R01DS0131EJ0350
Rev.3.50
Jun 30, 2020

True low-power platform (66 µA/MHz, and 0.57 µA for operation with only RTC and LVD) for the general-purpose applications, with 1.6-V to 5.5-V operation, 16- to 512-Kbyte code flash memory, and 41 DMIPS at 32 MHz

## 1. OUTLINE

### 1.1 Features

**Ultra-low power consumption technology**
- $V_{DD}$ = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

**RL78 CPU core**
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 µs: @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 µs: @ 32.768 kHz operation with subsystem clock)
- Address space: 1 MB
- <R> General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 2 to 32 KB

**Code flash memory**
- Code flash memory: 16 to 512 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

**Data Flash Memory**
- Data flash memory: 4 KB to 8 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: $V_{DD}$ = 1.8 to 5.5 V

**High-speed on-chip oscillator**
- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: +/- 1.0 % ($V_{DD}$ = 1.8 to 5.5 V, $T_A$ = -20 to +85°C)

**Operating ambient temperature**
- $T_A$ = -40 to +85°C (A: Consumer applications, D: Industrial applications )
- $T_A$ = -40 to +105°C (G: Industrial applications)

**Power management and reset function**
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

**DMA (Direct Memory Access) controller**
- 2/4 channels
- Number of clocks during transfer between 8/16-bit SFR and internal RAM: 2 clocks

**Multiplier and divider/multiply-accumulator**
- 16 bits × 16 bits = 32 bits (Unsigned or signed)
- 32 bits ÷ 32 bits = 32 bits (Unsigned)
- 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)

**Serial interface**
- CSI: 2 to 8 channels
- UART/UART (LIN-bus supported): 2 to 4 channels
- $I^2C$/Simplified $I^2C$ communication: 3 to 10 channels

**Timer**
- 16-bit timer: 8 to 16 channels
- 12-bit interval timer: 1 channel
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

**A/D converter**
- 8/10-bit resolution A/D converter ($V_{DD}$ = 1.6 to 5.5 V)
- Analog input: 6 to 26 channels
- Internal reference voltage (1.45 V) and temperature sensor Note 1

**I/O port**
- I/O port: 16 to 120 (N-ch open drain I/O [withstand voltage of 6 V]: 0 to 4, N-ch open drain I/O [$V_{DD}$ withstand voltage Note 2/$EV_{DD}$ withstand voltage Note 3]: 5 to 25)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

**Others**
- On-chip BCD (binary-coded decimal) correction circuit

**Notes 1.** Can be selected only in HS (high-speed main) mode
**2.** Products with 20 to 52 pins
**3.** Products with 64 to 128 pins

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

O ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/G13 | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 20 pins | 24 pins | 25 pins | 30 pins | 32 pins | 36 pins |
| 128 KB | 8 KB | 12 KB | – | – | – | R5F100AG | R5F100BG | R5F100CG |
| | – | | – | – | – | R5F101AG | R5F101BG | R5F101CG |
| 96 KB | 8 KB | 8 KB | – | – | – | R5F100AF | R5F100BF | R5F100CF |
| | – | | – | – | – | R5F101AF | R5F101BF | R5F101CF |
| 64 KB | 4 KB | 4 KB Note | R5F1006E | R5F1007E | R5F1008E | R5F100AE | R5F100BE | R5F100CE |
| | – | | R5F1016E | R5F1017E | R5F1018E | R5F101AE | R5F101BE | R5F101CE |
| 48 KB | 4 KB | 3 KB Note | R5F1006D | R5F1007D | R5F1008D | R5F100AD | R5F100BD | R5F100CD |
| | – | | R5F1016D | R5F1017D | R5F1018D | R5F101AD | R5F101BD | R5F101CD |
| 32 KB | 4 KB | 2 KB | R5F1006C | R5F1007C | R5F1008C | R5F100AC | R5F100BC | R5F100CC |
| | – | | R5F1016C | R5F1017C | R5F1018C | R5F101AC | R5F101BC | R5F101CC |
| 16 KB | 4 KB | 2 KB | R5F1006A | R5F1007A | R5F1008A | R5F100AA | R5F100BA | R5F100CA |
| | – | | R5F1016A | R5F1017A | R5F1018A | R5F101AA | R5F101BA | R5F101CA |

| Flash ROM | Data flash | RAM | RL78/G13 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 40 pins | 44 pins | 48 pins | 52 pins | 64 pins | 80 pins | 100 pins | 128 pins |
| 512 KB | 8 KB | 32 KB Note | – | R5F100FL | R5F100GL | R5F100JL | R5F100LL | R5F100ML | R5F100PL | R5F100SL |
| | – | | – | R5F101FL | R5F101GL | R5F101JL | R5F101LL | R5F101ML | R5F101PL | R5F101SL |
| 384 KB | 8 KB | 24 KB | – | R5F100FK | R5F100GK | R5F100JK | R5F100LK | R5F100MK | R5F100PK | R5F100SK |
| | – | | – | R5F101FK | R5F101GK | R5F101JK | R5F101LK | R5F101MK | R5F101PK | R5F101SK |
| 256 KB | 8 KB | 20 KB Note | – | R5F100FJ | R5F100GJ | R5F100JJ | R5F100LJ | R5F100MJ | R5F100PJ | R5F100SJ |
| | – | | – | R5F101FJ | R5F101GJ | R5F101JJ | R5F101LJ | R5F101MJ | R5F101PJ | R5F101SJ |
| 192 KB | 8 KB | 16 KB | R5F100EH | R5F100FH | R5F100GH | R5F100JH | R5F100LH | R5F100MH | R5F100PH | R5F100SH |
| | – | | R5F101EH | R5F101FH | R5F101GH | R5F101JH | R5F101LH | R5F101MH | R5F101PH | R5F101SH |
| 128 KB | 8 KB | 12 KB | R5F100EG | R5F100FG | R5F100GG | R5F100JG | R5F100LG | R5F100MG | R5F100PG | – |
| | – | | R5F101EG | R5F101FG | R5F101GG | R5F101JG | R5F101LG | R5F101MG | R5F101PG | – |
| 96 KB | 8 KB | 8 KB | R5F100EF | R5F100FF | R5F100GF | R5F100JF | R5F100LF | R5F100MF | R5F100PF | – |
| | – | | R5F101EF | R5F101FF | R5F101GF | R5F101JF | R5F101LF | R5F101MF | R5F101PF | – |
| 64 KB | 4 KB | 4 KB Note | R5F100EE | R5F100FE | R5F100GE | R5F100JE | R5F100LE | – | – | – |
| | – | | R5F101EE | R5F101FE | R5F101GE | R5F101JE | R5F101LE | – | – | – |
| 48 KB | 4 KB | 3 KB Note | R5F100ED | R5F100FD | R5F100GD | R5F100JD | R5F100LD | – | – | – |
| | – | | R5F101ED | R5F101FD | R5F101GD | R5F101JD | R5F101LD | – | – | – |
| 32 KB | 4 KB | 2 KB | R5F100EC | R5F100FC | R5F100GC | R5F100JC | R5F100LC | – | – | – |
| | – | | R5F101EC | R5F101FC | R5F101GC | R5F101JC | R5F101LC | – | – | – |
| 16 KB | 4 KB | 2 KB | R5F100EA | R5F100FA | R5F100GA | – | – | – | – | – |
| | – | | R5F101EA | R5F101FA | R5F101GA | – | – | – | – | – |

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xD, R5F101xD (x = 6 to 8, A to C, E to G, J, L): Start address FF300H

R5F100xE, R5F101xE (x = 6 to 8, A to C, E to G, J, L): Start address FEF00H

R5F100xJ, R5F101xJ (x = F, G, J, L, M, P): Start address FAF00H

R5F100xL, R5F101xL (x = F, G, J, L, M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

## 1.2 List of Part Numbers

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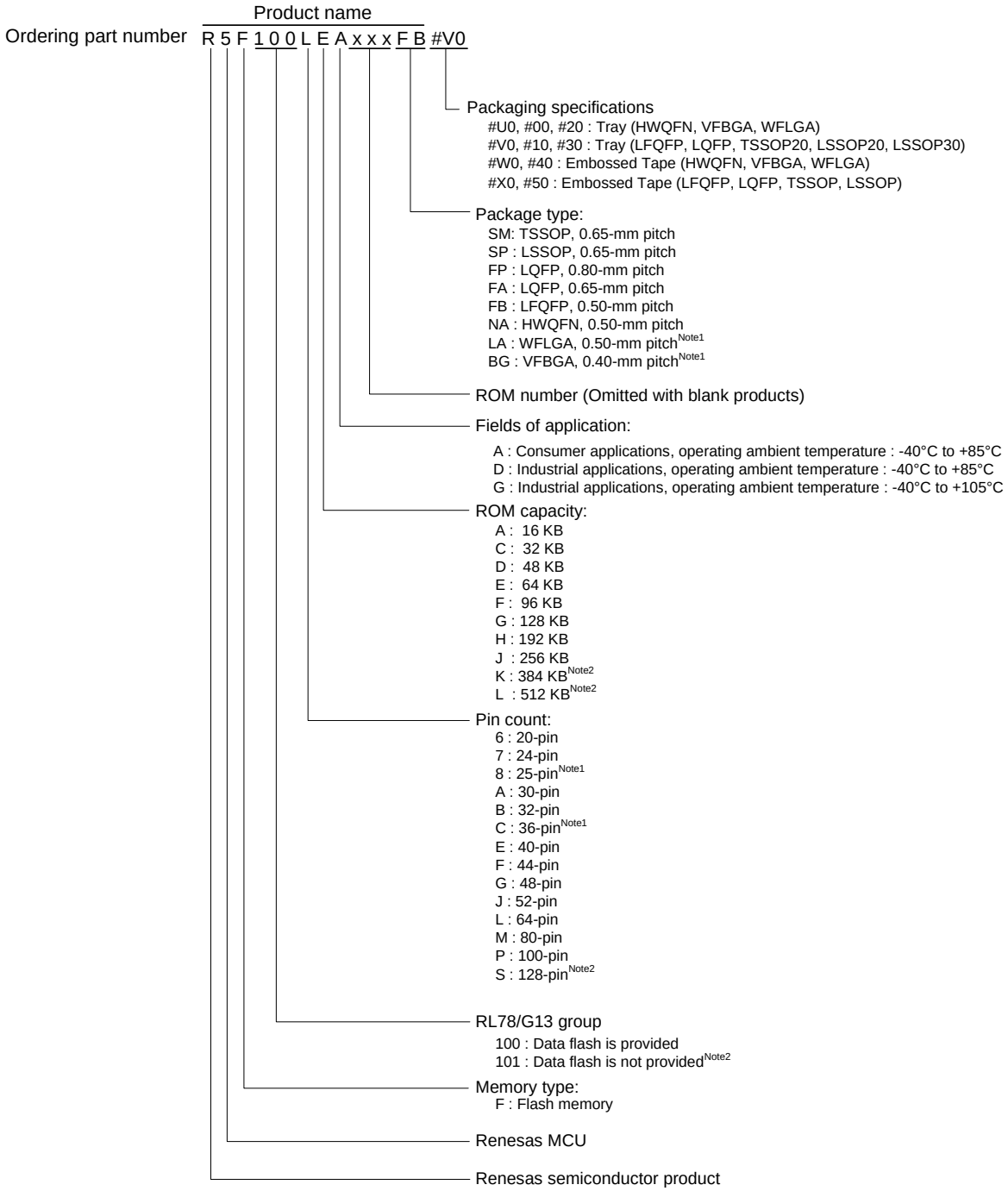
**Figure 1-1. Part Number, Memory Size, and Package of RL78/G13**




**Notes** **1.** Products only for “A: Consumer applications ($T_A$ = –40 to +85°C)”, and "G: Industrial applications ($T_A$ = –40 to +105°C)"

**2.** Products only for “A: Consumer applications ($T_A$ = –40 to +85°C)”, and "D: Industrial applications ($T_A$ = –40 to +85°C)"

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**Table 1-1. List of Ordering Part Numbers**

(1/8)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number | | RENESAS Code |
|---|---|---|---|---|---|---|
| | | | | Product Name | Packaging Specifications | |
| 20 pins | 20-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch) | Mounted | A | R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP | #V0, #10, #30, #X0, #50 | PLSP0020JC-A |
| | | | D | R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP | | |
| | | | G | R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP | | |
| | | Not mounted | A | R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP | #V0, #10, #30, #X0, #50 | PLSP0020JC-A |
| | | | D | R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP | | |
| | 20-pin plastic TSSOP (4.4 x 6.5 mm, 0.65-mm pitch) | Mounted | A | R5F1006AASM, R5F1006CASM, R5F1006DASM, R5F1006EASM | #10, #30, #50 | PTSP0020JI-A |
| | | | G | R5F1006AGSM, R5F1006CGSM, R5F1006DGSM, R5F1006EGSM | | |
| | | Not mounted | A | R5F1016AASM, R5F1016CASM, R5F1016DASM, R5F1016EASM | | |
| 24 pins | 24-pin plastic HWQFN (4 × 4 mm, 0.5-mm pitch) | Mounted | A | R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA | #U0, #W0 | PWQN0024KE-A |
| | | | | | #00, #20, #40 | PWQN0024KF-A |
| | | | D | R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA | #U0, #W0 | PWQN0024KE-A |
| | | | G | R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA | | |
| | | | | R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA | #00, #20, #40 | PWQN0024KF-A |
| | | Not mounted | A | R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA | #U0, #W0 | PWQN0024KE-A |
| | | | | | #00, #20, #40 | PWQN0024KF-A |
| | | | D | R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA | #U0, #W0 | PWQN0024KE-A |
| 25 pins | 25-pin plastic WFLGA (3 × 3 mm, 0.5-mm pitch) | Mounted | A | R5F1008AALA, R5F1008CALA, R5F1008DALA, R5F1008EALA | #U0, #W0 | PWLG0025KA-A |
| | | | G | R5F1008AGLA, R5F1008CGLA, R5F1008DGLA, R5F1008EGLA | | |
| | | Not mounted | A | R5F1018AALA, R5F1018CALA, R5F1018DALA, R5F1018EALA | #U0, #W0 | PWLG0025KA-A |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

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**Table 1-1. List of Ordering Part Numbers**

(2/8)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number | | RENESAS Code |
|---|---|---|---|---|---|---|
| | | | | Product Name | Packaging Specifications | |
| 30 pins | 30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch) | Mounted | A | R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP | #V0, #10, #30, #X0, #50 | PLSP0030JB-B |
| | | | D | R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP | | |
| | | | G | R5F100AAGSP, R5F100ACGSP, R5F100ADGSP, R5F100AEGSP, R5F100AFGSP, R5F100AGGSP | | |
| | | Not mounted | A | R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP | #V0, #10, #30, #X0, #50 | PLSP0030JB-B |
| | | | D | R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP | | |
| 32 pins | 32-pin plastic HWQFN (5 × 5 mm, 0.5-mm pitch) | Mounted | A | R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA | #U0, #W0 | PWQN0032KB-A |
| | | | | | #00, #20, #40 | PWQN0032KE-A |
| | | | D | R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA | #U0, #W0 | PWQN0032KB-A |
| | | | G | R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA | | |
| | | | | R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA | #00, #20, #40 | PWQN0032KE-A |
| | | Not mounted | A | R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA | #U0, #W0 | PWQN0032KB-A |
| | | | | | #00, #20, #40 | PWQN0032KE-A |
| | | | D | R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA | #U0, #W0 | PWQN0032KB-A |
| 36 pins | 36-pin plastic WFLGA (4 × 4 mm, 0.5-mm pitch) | Mounted | A | R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA | #U0, #W0 | PWLG0036KA-A |
| | | | G | R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA | | |
| | | Not mounted | A | R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA | #U0, #W0 | PWLG0036KA-A |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

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**Table 1-1. List of Ordering Part Numbers**

(3/8)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number | | RENESAS Code |
|---|---|---|---|---|---|---|
| | | | | Product Name | Packaging Specifications | |
| 40 pins | 40-pin plastic HWQFN (6 × 6 mm, 0.5-mm pitch) | Mounted | A | R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA | #U0, #W0 | PWQN0040KC-A |
| | | | | | #00, #20, #40 | PWQN0040KD-A |
| | | | D | R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA, R5F100EHDNA | #U0, #W0 | PWQN0040KC-A |
| | | | G | R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA, R5F100EHGNA | #U0, #W0 | PWQN0040KC-A |
| | | | | | #00, #20, #40 | PWQN0040KD-A |
| | | Not mounted | A | R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA | #U0, #W0 | PWQN0040KC-A |
| | | | | | #00, #20, #40 | PWQN0040KD-A |
| | | | D | R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA, R5F101EHDNA | #U0, #W0 | PWQN0040KC-A |
| 44 pins | 44-pin plastic LQFP (10 × 10 mm, 0.8-mm pitch) | Mounted | A | R5F100FAAFP, R5F100FCAFP, R5F100FDAFP, R5F100FEAFP, R5F100FFAFP, R5F100FGAFP, R5F100FHAFP, R5F100FJAFP, R5F100FKAFP, R5F100FLAFP | #V0, #X0 | PLQP0044GC-A |
| | | | | | #10, #30, #50 | PLQP0044GC-A/ PLQP0044GC-D |
| | | | D | R5F100FADFP, R5F100FCDFP, R5F100FDDFP, R5F100FEDFP, R5F100FFDFP, R5F100FGDFP, R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP | #V0, #X0 | PLQP0044GC-A |
| | | | | | #10, #30, #50 | PLQP0044GC-A/ PLQP0044GC-D |
| | | | G | R5F100FAGFP, R5F100FCGFP, R5F100FDGFP, R5F100FEGFP, R5F100FFGFP, R5F100FGGFP, R5F100FHGFP, R5F100FJGFP | #V0, #X0 | PLQP0044GC-A |
| | | | | | #10, #30, #50 | PLQP0044GC-A/ PLQP0044GC-D |
| | | Not mounted | A | R5F101FAAFP, R5F101FCAFP, R5F101FDAFP, R5F101FEAFP, R5F101FFAFP, R5F101FGAFP, R5F101FHAFP, R5F101FJAFP, R5F101FKAFP, R5F101FLAFP | #V0, #X0 | PLQP0044GC-A |
| | | | | | #10, #30, #50 | PLQP0044GC-A/ PLQP0044GC-D |
| | | | D | R5F101FADFP, R5F101FCDFP, R5F101FDDFP, R5F101FEDFP, R5F101FFDFP, R5F101FGDFP, R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP | #V0, #X0 | PLQP0044GC-A |
| | | | | | #10, #30, #50 | PLQP0044GC-A/ PLQP0044GC-D |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

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**Table 1-1. List of Ordering Part Numbers**

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| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number | | RENESAS Code |
|---|---|---|---|---|---|---|
| | | | | Product Name | Packaging Specifications | |
| 48 pins | 48-pin plastic LFQFP (7 × 7 mm, 0.5-mm pitch) | Mounted | A | R5F100GAAFB, R5F100GCAFB, R5F100GDAFB, R5F100GEAFB, R5F100GFAFB, R5F100GGAFB, R5F100GHAFB, R5F100GJAFB, R5F100GKAFB, R5F100GLAFB | #V0, #X0 | PLQP0048KF-A |
| | | | | | #10, #30, #50 | PLQP0048KB-B |
| | | | D | R5F100GADFB, R5F100GCDFB, R5F100GDDFB, R5F100GEDFB, R5F100GFDFB, R5F100GGDFB, R5F100GHDFB, R5F100GJDFB, R5F100GKDFB, R5F100GLDFB | #V0, #X0 | PLQP0048KF-A |
| | | | | | #10, #30, #50 | PLQP0048KB-B |
| | | | G | R5F100GAGFB, R5F100GCGFB, R5F100GDGFB, R5F100GEGFB, R5F100GFGFB, R5F100GGGFB, R5F100GHGFB, R5F100GJGFB | #V0, #X0 | PLQP0048KF-A |
| | | | | | #10, #30, #50 | PLQP0048KB-B |
| | | Not mounted | A | R5F101GAAFB, R5F101GCAFB, R5F101GDAFB, R5F101GEAFB, R5F101GFAFB, R5F101GGAFB, R5F101GHAFB, R5F101GJAFB, R5F101GKAFB, R5F101GLAFB | #V0, #X0 | PLQP0048KF-A |
| | | | | | #10, #30, #50 | PLQP0048KB-B |
| | | | D | R5F101GADFB, R5F101GCDFB, R5F101GDDFB, R5F101GEDFB, R5F101GFDFB, R5F101GGDFB, R5F101GHDFB, R5F101GJDFB, R5F101GKDFB, R5F101GLDFB | #V0, #X0 | PLQP0048KF-A |
| | | | | | #10, #30, #50 | PLQP0048KB-B |
| | 48-pin plastic HWQFN (7 × 7 mm, 0.5-mm pitch) | Mounted | A | R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA, R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA | #U0, #W0 | PWQN0048KB-A |
| | | | | | #00, #20, #40 | PWQN0048KE-A |
| | | | D | R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA, R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA | #U0, #W0 | PWQN0048KB-A |
| | | | | R5F100GKDNA, R5F100GLDNA | #00, #20, #40 | PWQN0048KE-A |
| | | | G | R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA, R5F100GHGNA, R5F100GJGNA | #U0, #W0 | PWQN0048KB-A |
| | | | | | #00, #20, #40 | PWQN0048KE-A |
| | | Not mounted | A | R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA, R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA | #U0, #W0 | PWQN0048KB-A |
| | | | | | #00, #20, #40 | PWQN0048KE-A |
| | | | D | R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA, R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA | #U0, #W0 | PWQN0048KB-A |
| | | | | R5F101GKDNA, R5F101GLDNA | #00, #20, #40 | PWQN0048KE-A |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

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**Table 1-1. List of Ordering Part Numbers**

(5/8)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number | | RENESAS Code |
|---|---|---|---|---|---|---|
| | | | | Product Name | Packaging Specifications | |
| 52 pins | 52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch) | Mounted | A | R5F100JCAFA, R5F100JDAFA, R5F100JEAFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJAFA, R5F100JKAFA, R5F100JLAFA | #V0, #10, #30, #X0, #50 | PLQP0052JA-A |
| | | | D | R5F100JCDFA, R5F100JDDFA, R5F100JEDFA, R5F100JFDFA, R5F100JGDFA, R5F100JHDFA, R5F100JJDFA, R5F100JKDFA, R5F100JLDFA | | |
| | | | G | R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA | | |
| | | Not mounted | A | R5F101JCAFA, R5F101JDAFA, R5F101JEAFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJAFA, R5F101JKAFA, R5F101JLAFA | #V0, #10, #30, #X0, #50 | PLQP0052JA-A |
| | | | D | R5F101JCDFA, R5F101JDDFA, R5F101JEDFA, R5F101JFDFA, R5F101JGDFA, R5F101JHDFA, R5F101JJDFA, R5F101JKDFA, R5F101JLDFA | | |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

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**Table 1-1. List of Ordering Part Numbers**

(6/8)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number | | RENESAS Code |
|---|---|---|---|---|---|---|
| | | | | Product Name | Packaging Specifications | |
| 64 pins | 64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch) | Mounted | A | R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA, R5F100LKAFA, R5F100LLAFA | #V0, #10, #30, #X0, #50 | PLQP0064JA-A |
| | | | D | R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LGDFA, R5F100LHDFA, R5F100LJDFA, R5F100LKDFA, R5F100LLDFA | | |
| | | | G | R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA, R5F100LJGFA | | |
| | 64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch) | Not mounted | A | R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA, R5F101LKAFA, R5F101LLAFA | #V0, #10, #30, #X0, #50 | PLQP0064JA-A |
| | | | D | R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LGDFA, R5F101LHDFA, R5F101LJDFA, R5F101LKDFA, R5F101LLDFA | | |
| | 64-pin plastic LFQFP (10 × 10 mm, 0.5-mm pitch) | Mounted | A | R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB | #V0, #X0 | PLQP0064KF-A |
| | | | | | #10, #30, #50 | PLQP0064KB-C |
| | | | D | R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LFDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB, R5F100LKDFB, R5F100LLDFB | #V0, #X0 | PLQP0064KF-A |
| | | | | | #10, #30, #50 | PLQP0064KB-C |
| | | | G | R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB, R5F100LJGFB | #V0, #X0 | PLQP0064KF-A |
| | | | | | #10, #30, #50 | PLQP0064KB-C |
| | | Not mounted | A | R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB | #V0, #X0 | PLQP0064KF-A |
| | | | | | #10, #30, #50 | PLQP0064KB-C |
| | | | D | R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LFDFB, R5F101LGDFB, R5F101LHDFB, R5F101LJDFB, R5F101LKDFB, R5F101LLDFB | #V0, #X0 | PLQP0064KF-A |
| | | | | | #10, #30, #50 | PLQP0064KB-C |
| | 64-pin plastic VFBGA (4 × 4 mm, 0.4-mm pitch) | Mounted | A | R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG | #U0, #W0 | PVBG0064LA-A |
| | | | G | R5F100LCGBG, R5F100LDGBG, R5F100LEGBG, R5F100LFGBG, R5F100LGGBG, R5F100LHGBG, R5F100LJGBG | | |
| | | Not mounted | A | R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG | #U0, #W0 | PVBG0064LA-A |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

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**Table 1-1. List of Ordering Part Numbers**

(7/8)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number | | RENESAS Code |
|---|---|---|---|---|---|---|
| | | | | Product Name | Packaging Specifications | |
| 80 pins | 80-pin plastic LQFP (14 × 14 mm, 0.65-mm pitch) | Mounted | A | R5F100MFAFA, R5F100MGAFA, R5F100MHAFA, R5F100MJAFA, R5F100MKAFA, R5F100MLAFA | #V0, #10, #30, #X0, #50 | PLQP0080JB-E |
| | | | D | R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA | | |
| | | | G | R5F100MFGFA, R5F100MGGFA, R5F100MHGFA, R5F100MJGFA | | |
| | | Not mounted | A | R5F101MFAFA, R5F101MGAFA, R5F101MHAFA, R5F101MJAFA, R5F101MKAFA, R5F101MLAFA | #V0, #10, #30, #X0, #50 | PLQP0080JB-E |
| | | | D | R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA | | |
| | 80-pin plastic LFQFP (12 × 12 mm, 0.5-mm pitch) | Mounted | A | R5F100MFAFB, R5F100MGAFB, R5F100MHAFB, R5F100MJAFB, R5F100MKAFB, R5F100MLAFB | #V0, #X0 | PLQP0080KE-A |
| | | | | | #10, #30, #50 | PLQP0080KB-B |
| | | | D | R5F100MFDFB, R5F100MGDFB, R5F100MHDFB, R5F100MJDFB, R5F100MKDFB, R5F100MLDFB | #V0, #X0 | PLQP0080KE-A |
| | | | | | #10, #30, #50 | PLQP0080KB-B |
| | | | G | R5F100MFGFB, R5F100MGGFB, R5F100MHGFB, R5F100MJGFB | #V0, #X0 | PLQP0080KE-A |
| | | | | | #10, #30, #50 | PLQP0080KB-B |
| | | Not mounted | A | R5F101MFAFB, R5F101MGAFB, R5F101MHAFB, R5F101MJAFB, R5F101MKAFB, R5F101MLAFB | #V0, #X0 | PLQP0080KE-A |
| | | | | | #10, #30, #50 | PLQP0080KB-B |
| | | | D | R5F101MFDFB, R5F101MGDFB, R5F101MHDFB, R5F101MJDFB, R5F101MKDFB, R5F101MLDFB | #V0, #X0 | PLQP0080KE-A |
| | | | | | #10, #30, #50 | PLQP0080KB-B |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

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**Table 1-1. List of Ordering Part Numbers**

(8/8)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number | | RENESAS Code |
|---|---|---|---|---|---|---|
| | | | | Product Name | Packaging Specifications | |
| 100 pins | 100-pin plastic LFQFP (14 × 14 mm, 0.5-mm pitch) | Mounted | A | R5F100PFAFB, R5F100PGAFB, R5F100PHAFB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB | #V0, #X0 | PLQP0100KE-A |
| | | | | | #10, #30, #50 | PLQP0100KB-B |
| | | | D | R5F100PFDFB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB | #V0, #X0 | PLQP0100KE-A |
| | | | | | #10, #30, #50 | PLQP0100KB-B |
| | | | G | R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB | #V0, #X0 | PLQP0100KE-A |
| | | | | | #10, #30, #50 | PLQP0100KB-B |
| | | Not mounted | A | R5F101PFAFB, R5F101PGAFB, R5F101PHAFB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB | #V0, #X0 | PLQP0100KE-A |
| | | | | | #10, #30, #50 | PLQP0100KB-B |
| | | | D | R5F101PFDFB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB | #V0, #X0 | PLQP0100KE-A |
| | | | | | #10, #30, #50 | PLQP0100KB-B |
| | 100-pin plastic LQFP (14 × 20 mm, 0.65-mm pitch) | Mounted | A | R5F100PFAFA, R5F100PGAFA, R5F100PHAFA, R5F100PJAFA, R5F100PKAFA, R5F100PLAFA | #V0, #10, #30, #X0, #50 | PLQP0100JC-A |
| | | | D | R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFA, R5F100PKDFA, R5F100PLDFA | | |
| | | | G | R5F100PFGFA, R5F100PGGFA, R5F100PHGFA, R5F100PJGFA | | |
| | | Not mounted | A | R5F101PFAFA, R5F101PGAFA, R5F101PHAFA, R5F101PJAFA, R5F101PKAFA, R5F101PLAFA | #V0, #10, #30, #X0, #50 | PLQP0100JC-A |
| | | | D | R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFA, R5F101PKDFA, R5F101PLDFA | | |
| 128 pins | 128-pin plastic LFQFP (14 × 20 mm, 0.5-mm pitch) | Mounted | A | R5F100SHAFB, R5F100SJAFB, R5F100SKAFB, R5F100SLAFB | #V0, #10, #30, #X0, #50 | PLQP0128KD-A |
| | | | D | R5F100SHDFB, R5F100SJDFB, R5F100SKDFB, R5F100SLDFB | | |
| | | Not mounted | A | R5F101SHAFB, R5F101SJAFB, R5F101SKAFB, R5F101SLAFB | #V0, #10, #30, #X0, #50 | PLQP0128KD-A |
| | | | D | R5F101SHDFB, R5F101SJDFB, R5F101SKDFB, R5F101SLDFB | | |

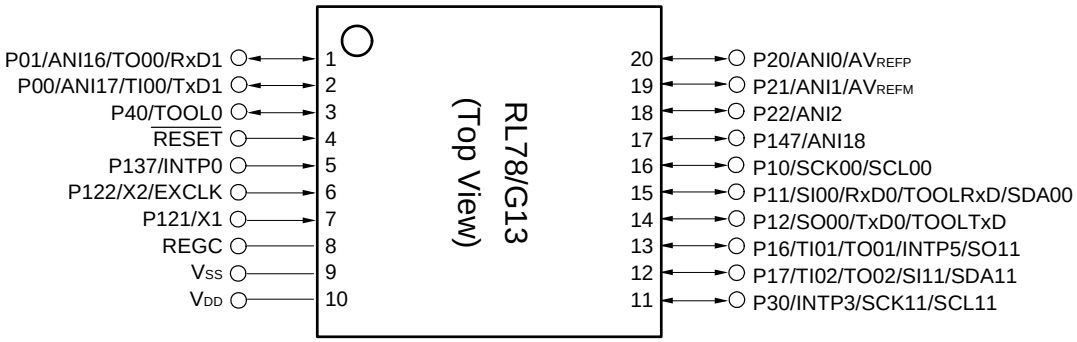
**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

## 1.3 Pin Configuration (Top View)

### 1.3.1 20-pin products

- 20-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)
<R> - 20-pin plastic TSSOP (4.4 × 6.5 mm, 0.65-mm pitch)

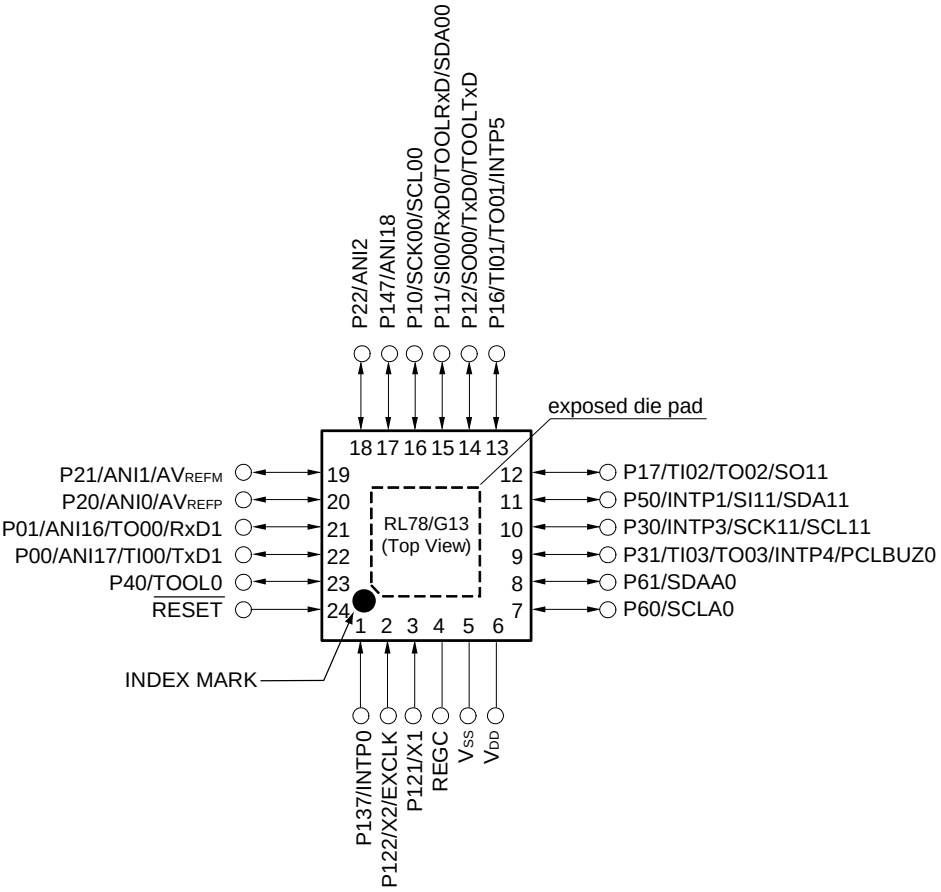



**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remark** For pin identification, see **1.4 Pin Identification**.

### 1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5-mm pitch)



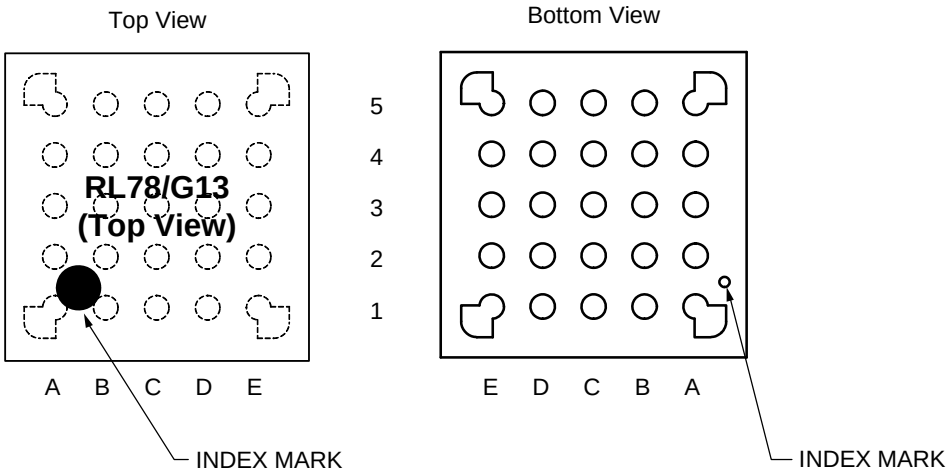

**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** It is recommended to connect an exposed die pad to $V_{SS}$.

### 1.3.3 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50-mm pitch)



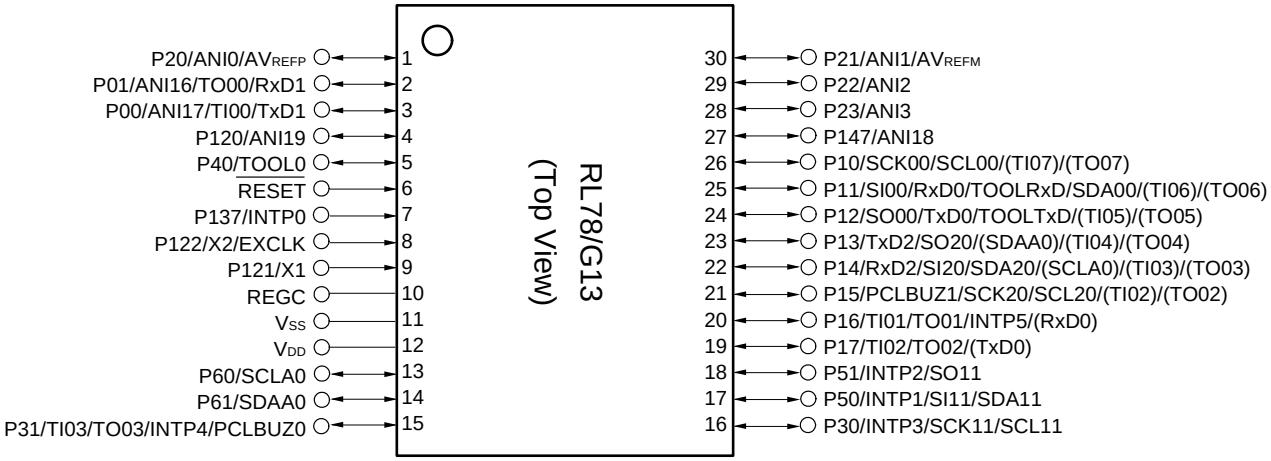

| | A | B | C | D | E | |
|---|---|---|---|---|---|---|
| 5 | P40/TOOL0 | $\overline{\text{RESET}}$ | P01/ANI16/ TO00/RxD1 | P22/ANI2 | P147/ANI18 | 5 |
| 4 | P122/X2/ EXCLK | P137/INTP0 | P00/ANI17/ TI00/TxD1 | P21/ANI1/ $AV_{REFM}$ | P10/SCK00/ SCL00 | 4 |
| 3 | P121/X1 | $V_{DD}$ | P20/ANI0/ $AV_{REFP}$ | P12/SO00/ TxD0/ TOOLTxD | P11/SI00/ RxD0/ TOOLRxD/ SDA00 | 3 |
| 2 | REGC | $V_{SS}$ | P30/INTP3/ SCK11/SCL11 | P17/TI02/ TO02/SO11 | P50/INTP1/ SI11/SDA11 | 2 |
| 1 | P60/SCLA0 | P61/SDAA0 | P31/TI03/ TO03/INTP4/ PCLBUZ0 | P16/TI01/ TO01/INTP5 | P130 | 1 |
| | A | B | C | D | E | |

**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remark** For pin identification, see **1.4 Pin Identification**.

### 1.3.4 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)



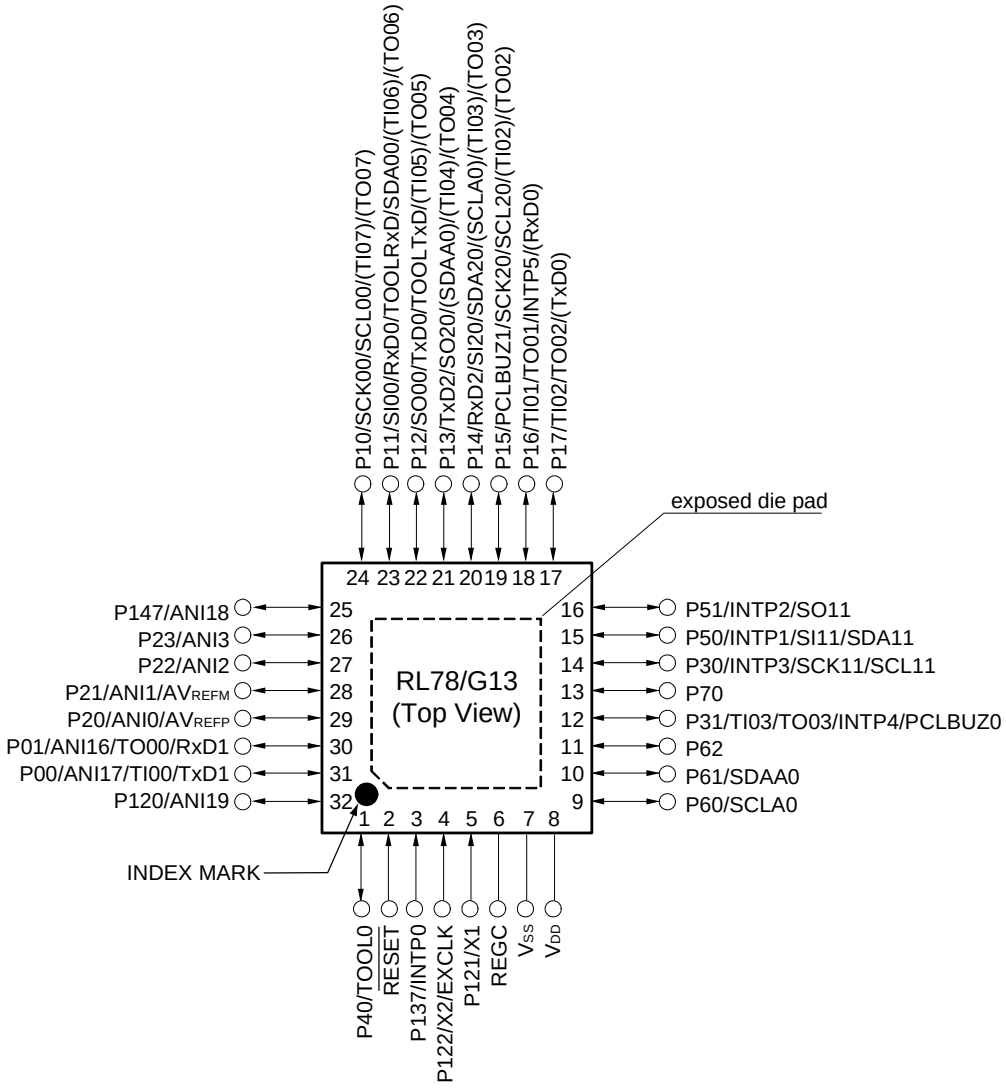

**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.3.5 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5-mm pitch)




**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

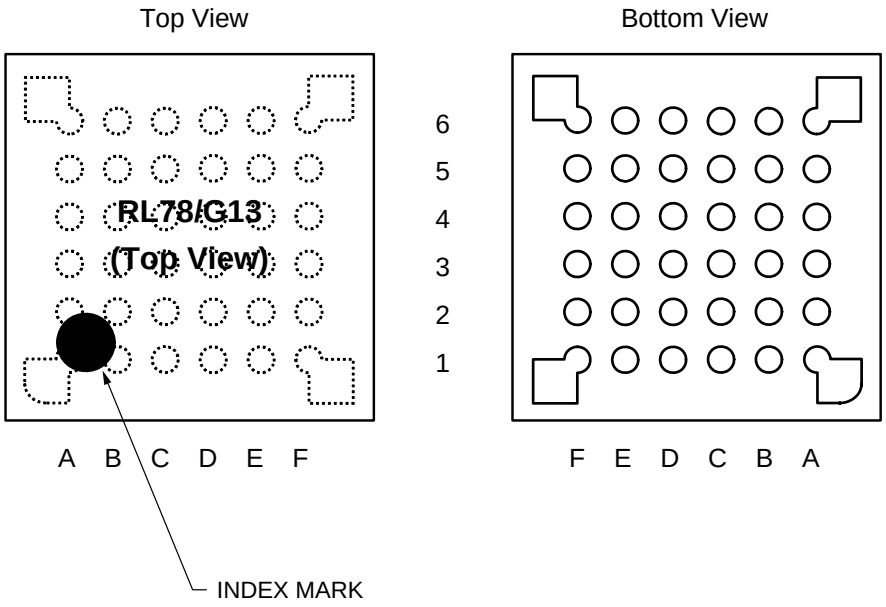
**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

**3.** It is recommended to connect an exposed die pad to $V_{SS}$.

### 1.3.6 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5-mm pitch)




| | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|
| 6 | P60/SCLA0 | $V_{DD}$ | P121/X1 | P122/X2/EXCLK | P137/INTP0 | P40/TOOL0 | 6 |
| 5 | P62 | P61/SDAA0 | $V_{SS}$ | REGC | $\overline{\text{RESET}}$ | P120/ANI19 | 5 |
| 4 | P72/SO21 | P71/SI21/ SDA21 | P14/RxD2/SI20/ SDA20/(SCLA0) /(TI03)/(TO03) | P31/TI03/TO03/ INTP4/ PCLBUZ0 | P00/TI00/TxD1 | P01/TO00/RxD1 | 4 |
| 3 | P50/INTP1/ SI11/SDA11 | P70/SCK21/ SCL21 | P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02) | P22/ANI2 | P20/ANI0/ $AV_{REFP}$ | P21/ANI1/ $AV_{REFM}$ | 3 |
| 2 | P30/INTP3/ SCK11/SCL11 | P16/TI01/TO01/ INTP5/(RxD0) | P12/SO00/ TxD0/TOOLTxD /(TI05)/(TO05) | P11/SI00/RxD0/ TOOLRxD/ SDA00/(TI06)/ (TO06) | P24/ANI4 | P23/ANI3 | 2 |
| 1 | P51/INTP2/ SO11 | P17/TI02/TO02/ (TxD0) | P13/TxD2/ SO20/(SDAA0)/ (TI04)/(TO04) | P10/SCK00/ SCL00/(TI07)/ (TO07) | P147/ANI18 | P25/ANI5 | 1 |
| | A | B | C | D | E | F | |

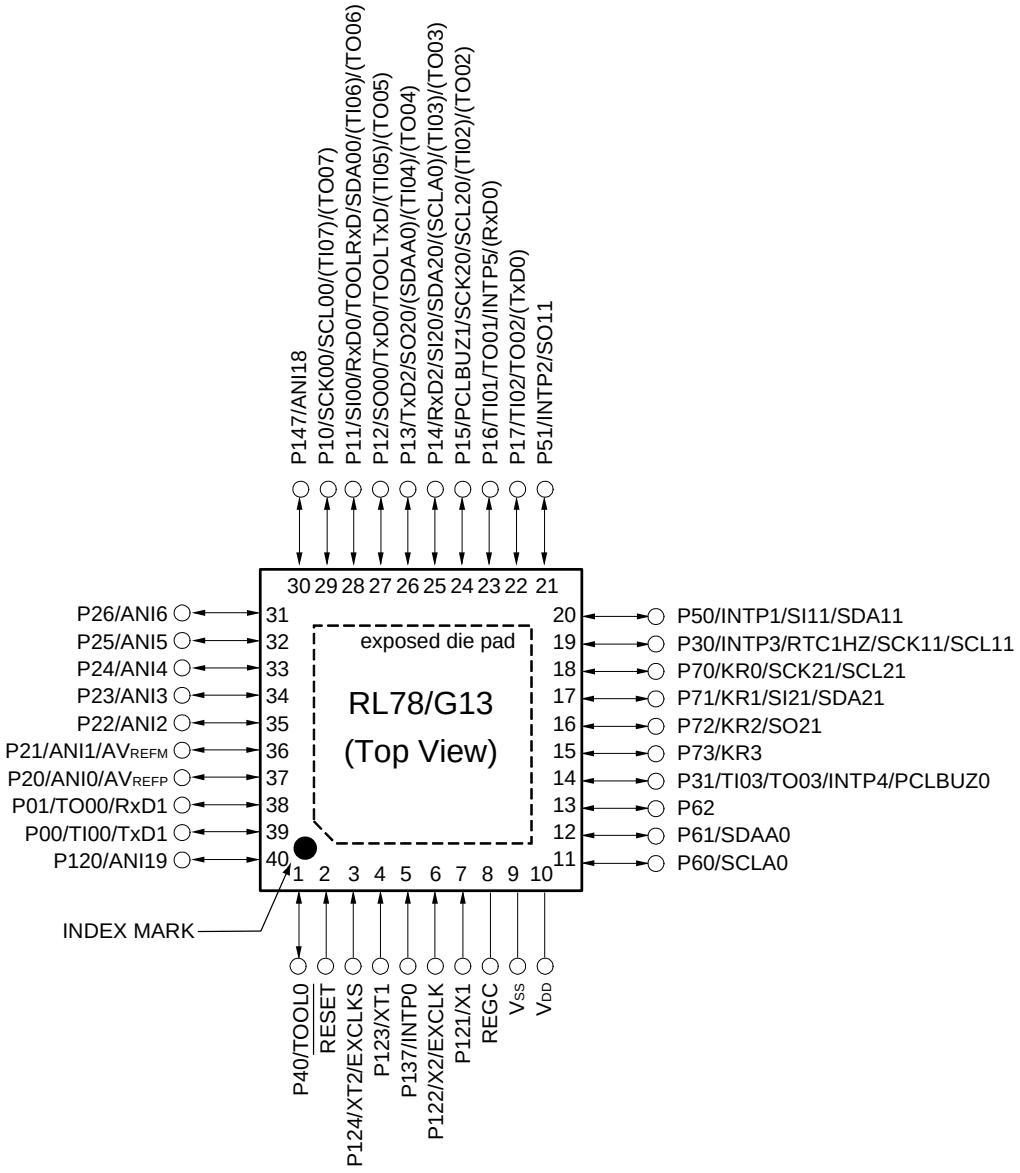
**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.3.7 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5-mm pitch)




**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

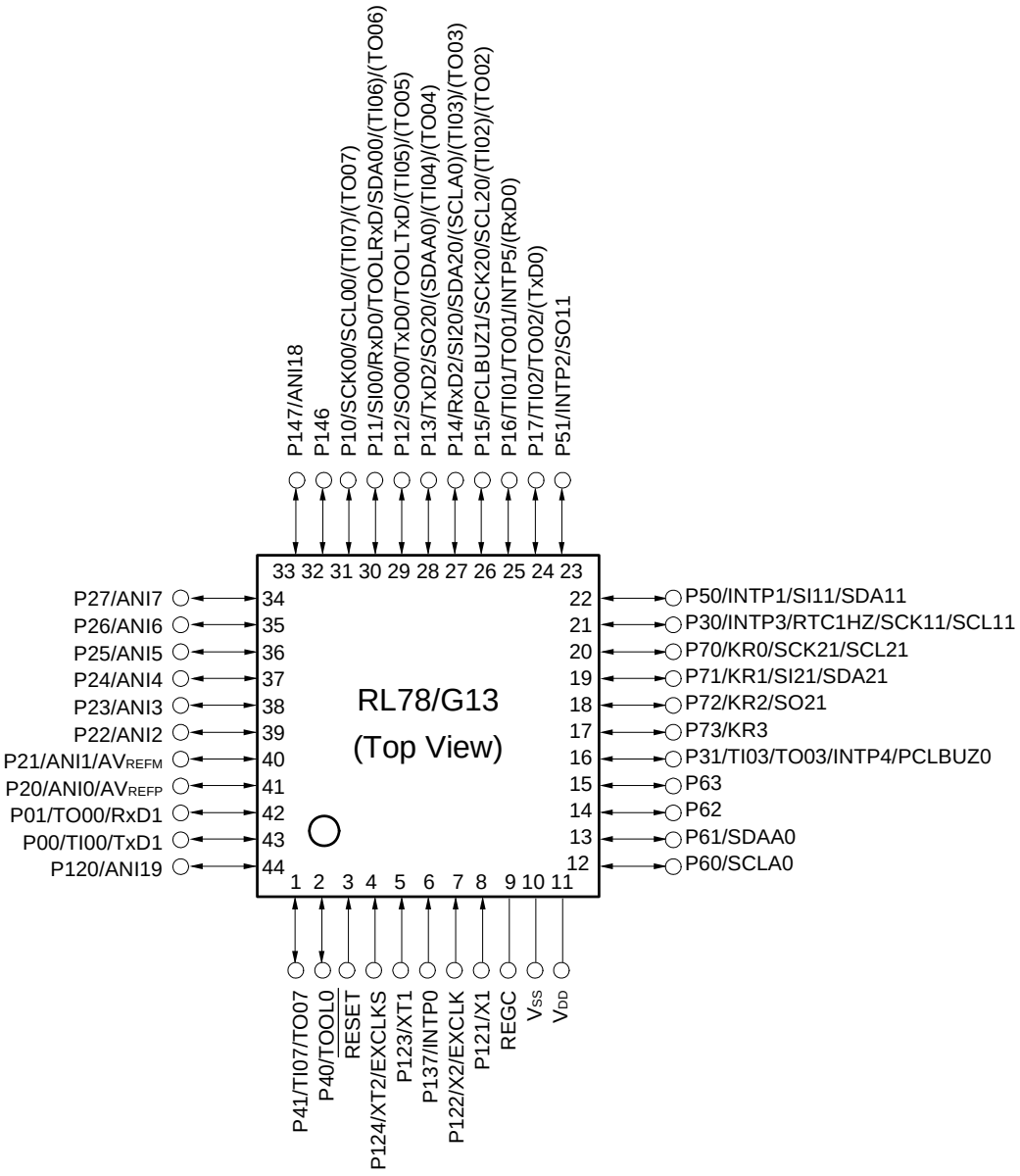
**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

**3.** It is recommended to connect an exposed die pad to $V_{SS}$.

### 1.3.8 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8-mm pitch)



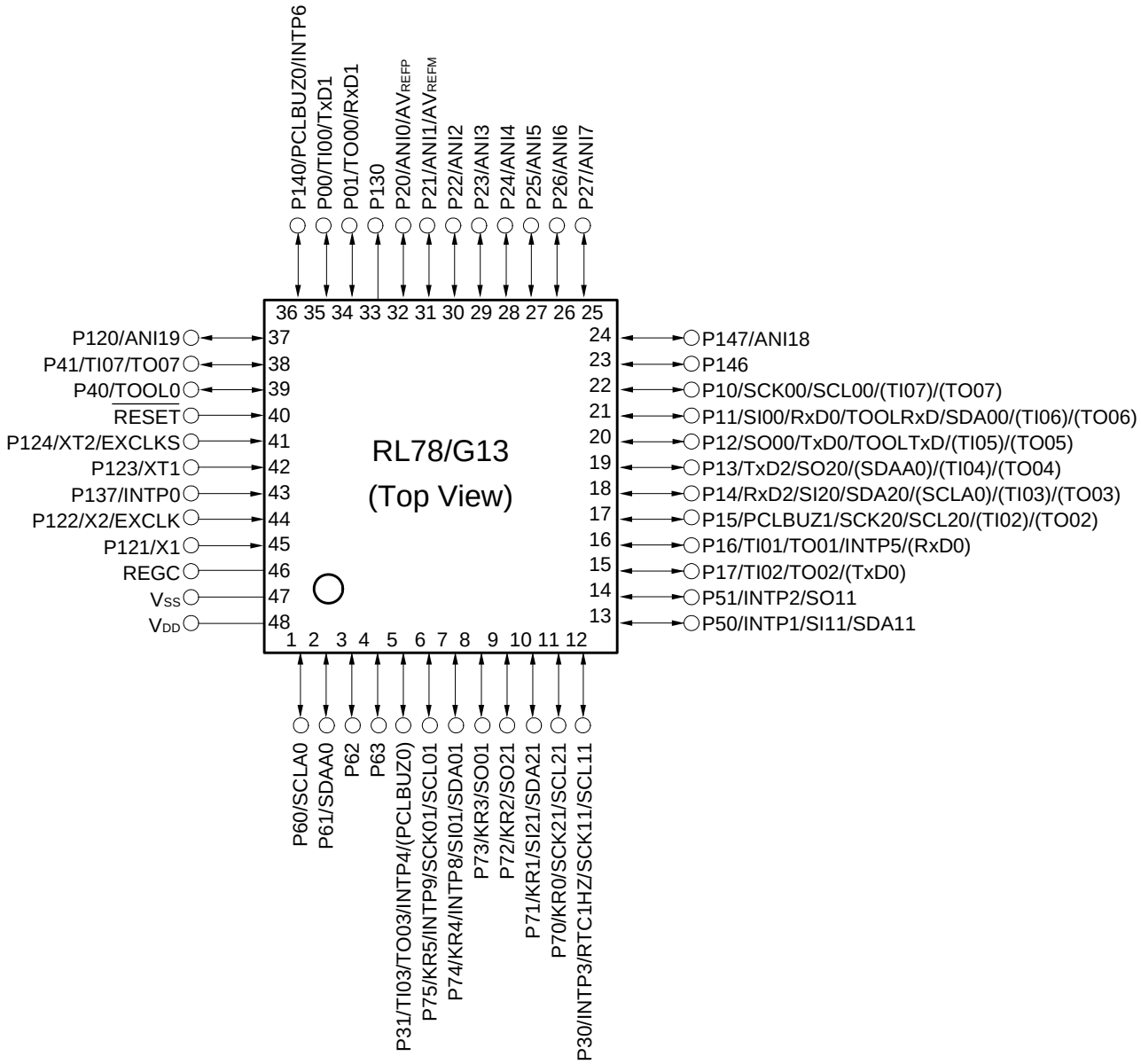

**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.3.9 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5-mm pitch)

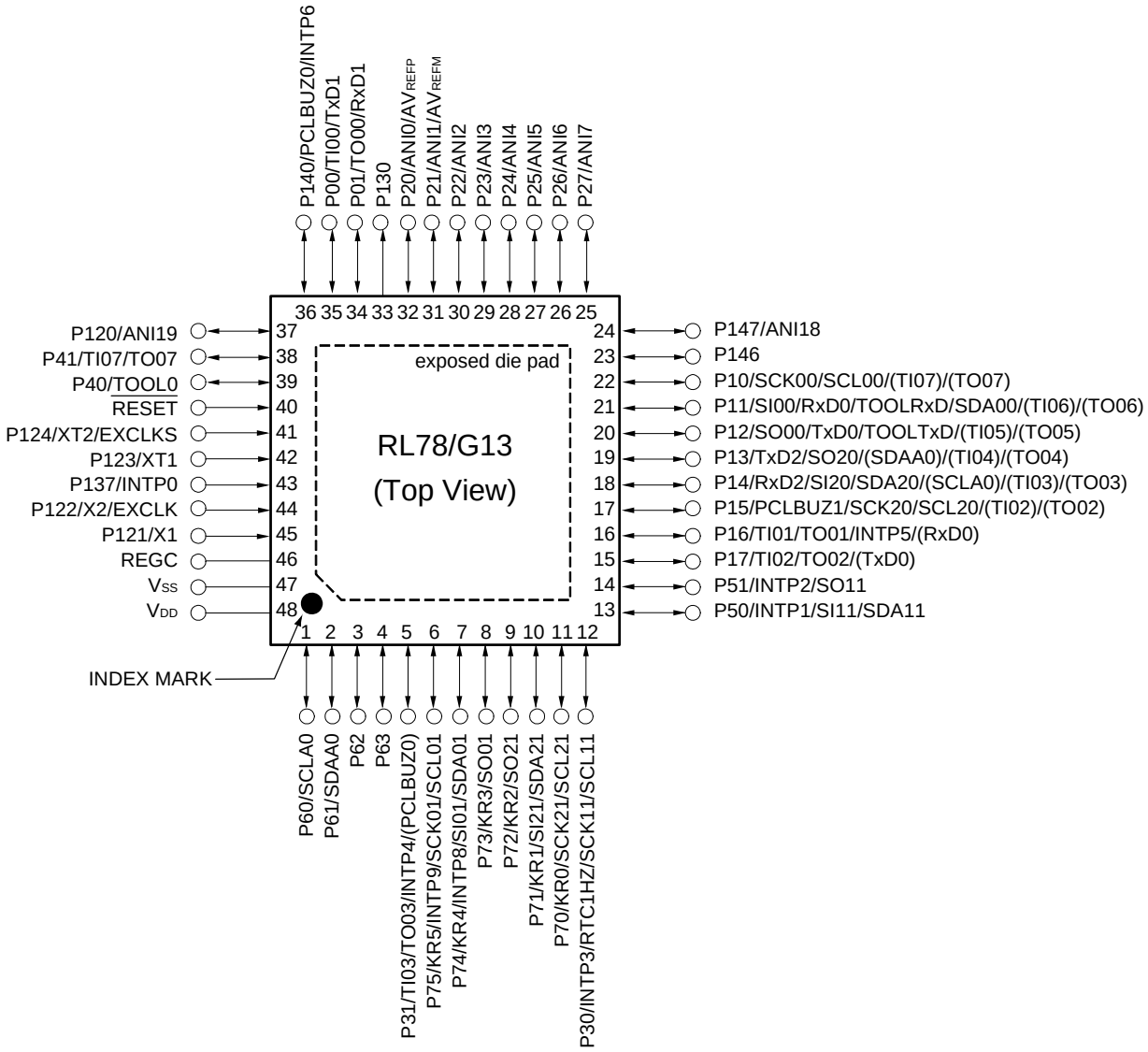



**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5-mm pitch)




**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

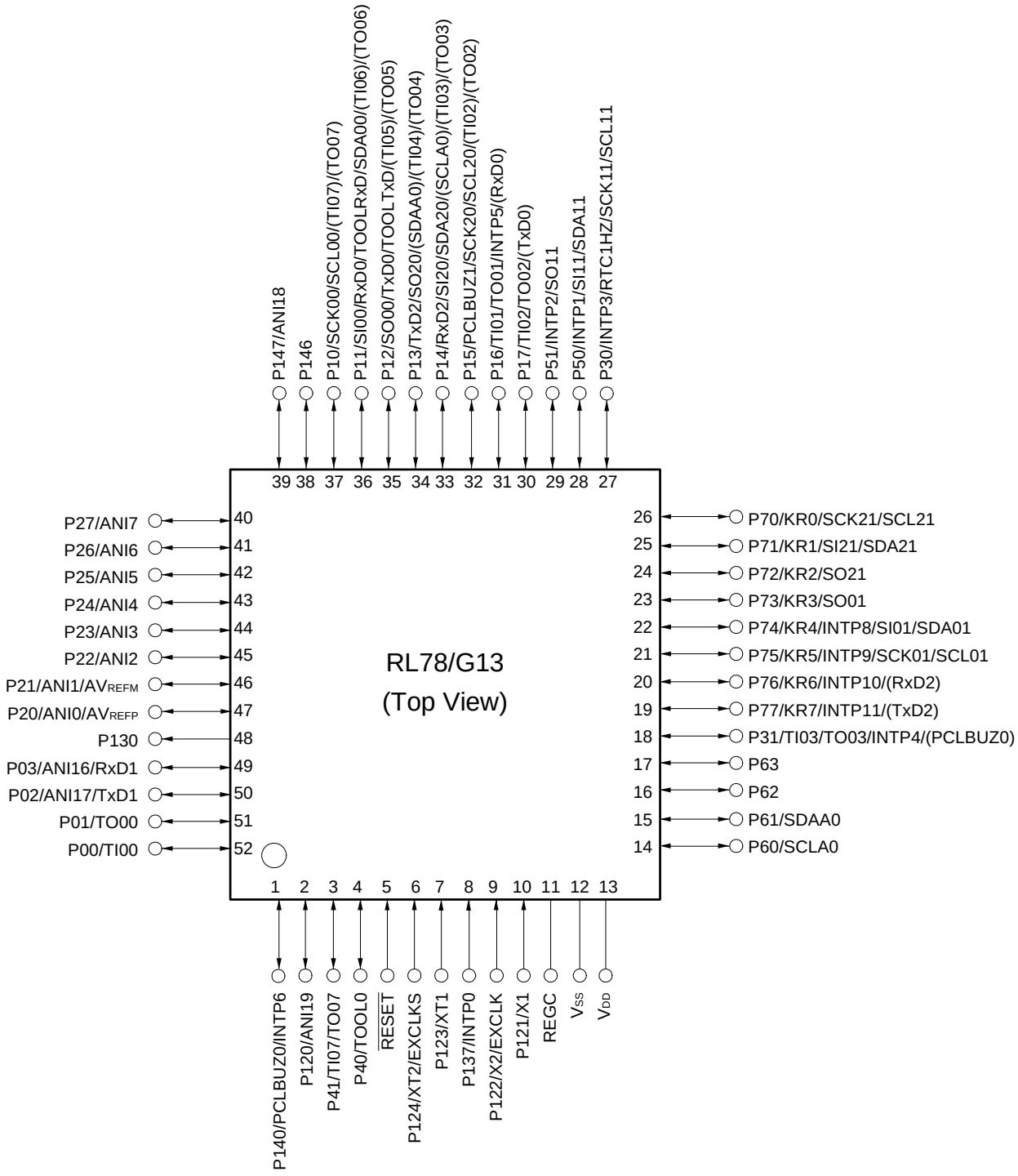
**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

**3.** It is recommended to connect an exposed die pad to $V_{SS}$.

### 1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)



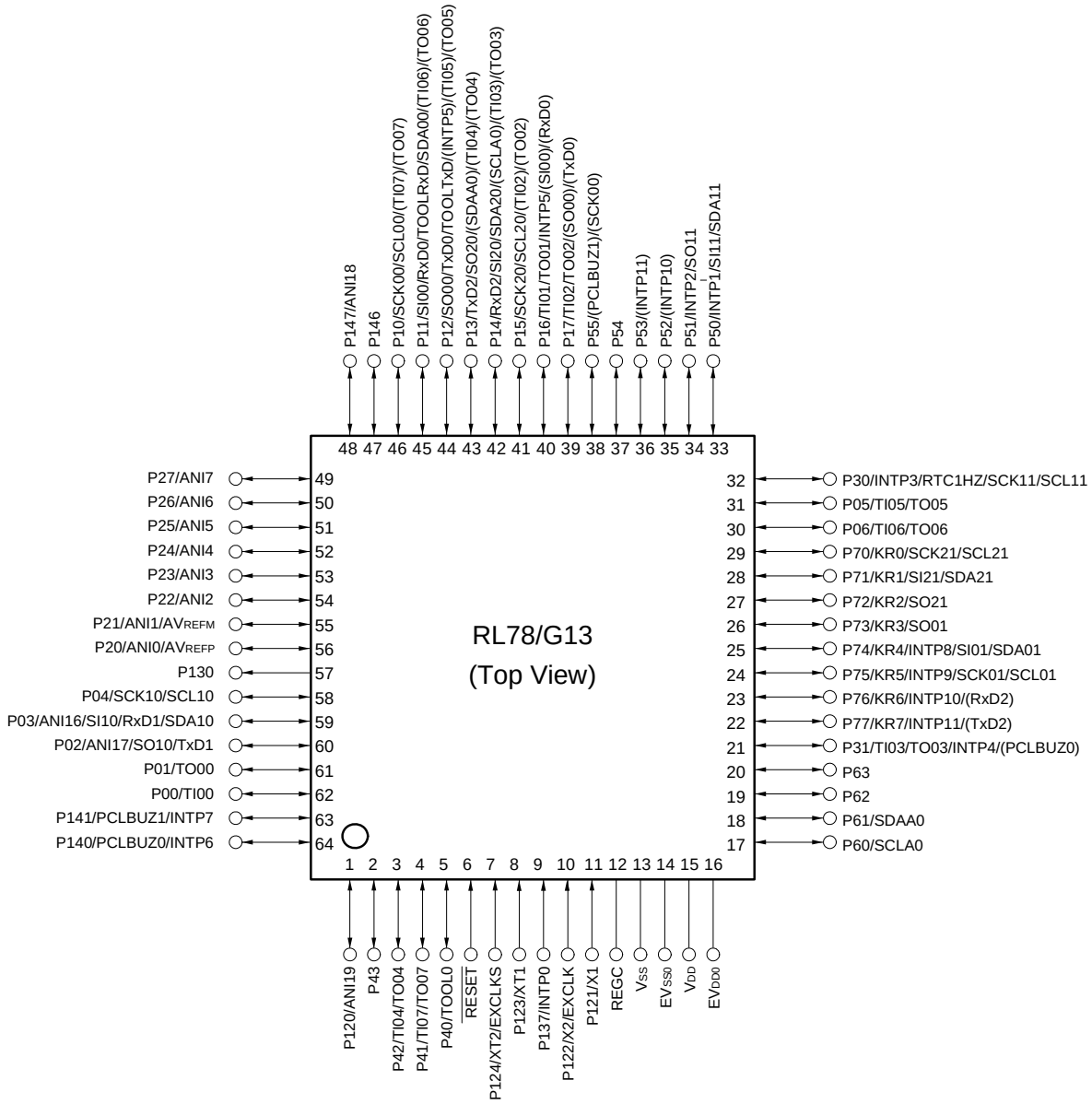

**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5-mm pitch)




**Cautions 1. Make $EV_{SS0}$ pin the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is no less than $EV_{DD0}$ pin.**

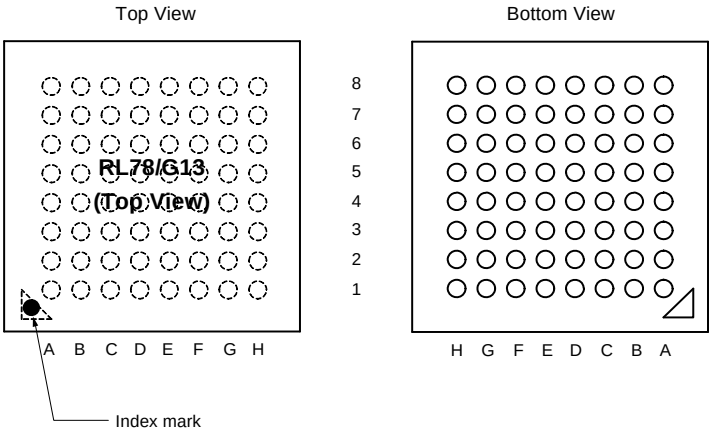
**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS0}$ pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 64-pin plastic VFBGA (4 × 4 mm, 0.4-mm pitch)




| Pin No. | Name | Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---|---|---|---|---|---|---|---|
| A1 | P05/TI05/TO05 | C1 | P51/INTP2/SO11 | E1 | P13/TxD2/SO20/ (SDAA0)/(TI04)/(TO04) | G1 | P146 |
| A2 | P30/INTP3/RTC1HZ /SCK11/SCL11 | C2 | P71/KR1/SI21/SDA21 | E2 | P14/RxD2/SI20/SDA20 /(SCLA0)/(TI03)/(TO03) | G2 | P25/ANI5 |
| A3 | P70/KR0/SCK21 /SCL21 | C3 | P74/KR4/INTP8/SI01 /SDA01 | E3 | P15/SCK20/SCL20/ (TI02)/(TO02) | G3 | P24/ANI4 |
| A4 | P75/KR5/INTP9 /SCK01/SCL01 | C4 | P52/(INTP10) | E4 | P16/TI01/TO01/INTP5 /(SI00)/(RxD0) | G4 | P22/ANI2 |
| A5 | P77/KR7/INTP11/ (TxD2) | C5 | P53/(INTP11) | E5 | P03/ANI16/SI10/RxD1 /SDA10 | G5 | P130 |
| A6 | P61/SDAA0 | C6 | P63 | E6 | P41/TI07/TO07 | G6 | P02/ANI17/SO10/TxD1 |
| A7 | P60/SCLA0 | C7 | $V_{SS}$ | E7 | $\overline{RESET}$ | G7 | P00/TI00 |
| A8 | $EV_{DD0}$ | C8 | P121/X1 | E8 | P137/INTP0 | G8 | P124/XT2/EXCLKS |
| B1 | P50/INTP1/SI11 /SDA11 | D1 | P55/(PCLBUZ1)/ (SCK00) | F1 | P10/SCK00/SCL00/ (TI07)/(TO07) | H1 | P147/ANI18 |
| B2 | P72/KR2/SO21 | D2 | P06/TI06/TO06 | F2 | P11/SI00/RxD0 /TOOLRxD/SDA00/ (TI06)/(TO06) | H2 | P27/ANI7 |
| B3 | P73/KR3/SO01 | D3 | P17/TI02/TO02/ (SO00)/(TxD0) | F3 | P12/SO00/TxD0 /TOOLTxD/(INTP5)/ (TI05)/(TO05) | H3 | P26/ANI6 |
| B4 | P76/KR6/INTP10/ (RxD2) | D4 | P54 | F4 | P21/ANI1/$AV_{REFM}$ | H4 | P23/ANI3 |
| B5 | P31/TI03/TO03 /INTP4/(PCLBUZ0) | D5 | P42/TI04/TO04 | F5 | P04/SCK10/SCL10 | H5 | P20/ANI0/$AV_{REFP}$ |
| B6 | P62 | D6 | P40/TOOL0 | F6 | P43 | H6 | P141/PCLBUZ1/INTP7 |
| B7 | $V_{DD}$ | D7 | REGC | F7 | P01/TO00 | H7 | P140/PCLBUZ0/INTP6 |
| B8 | $EV_{SS0}$ | D8 | P122/X2/EXCLK | F8 | P123/XT1 | H8 | P120/ANI19 |

**Cautions 1. Make $EV_{SS0}$ pin the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is no less than $EV_{DD0}$ pin.**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

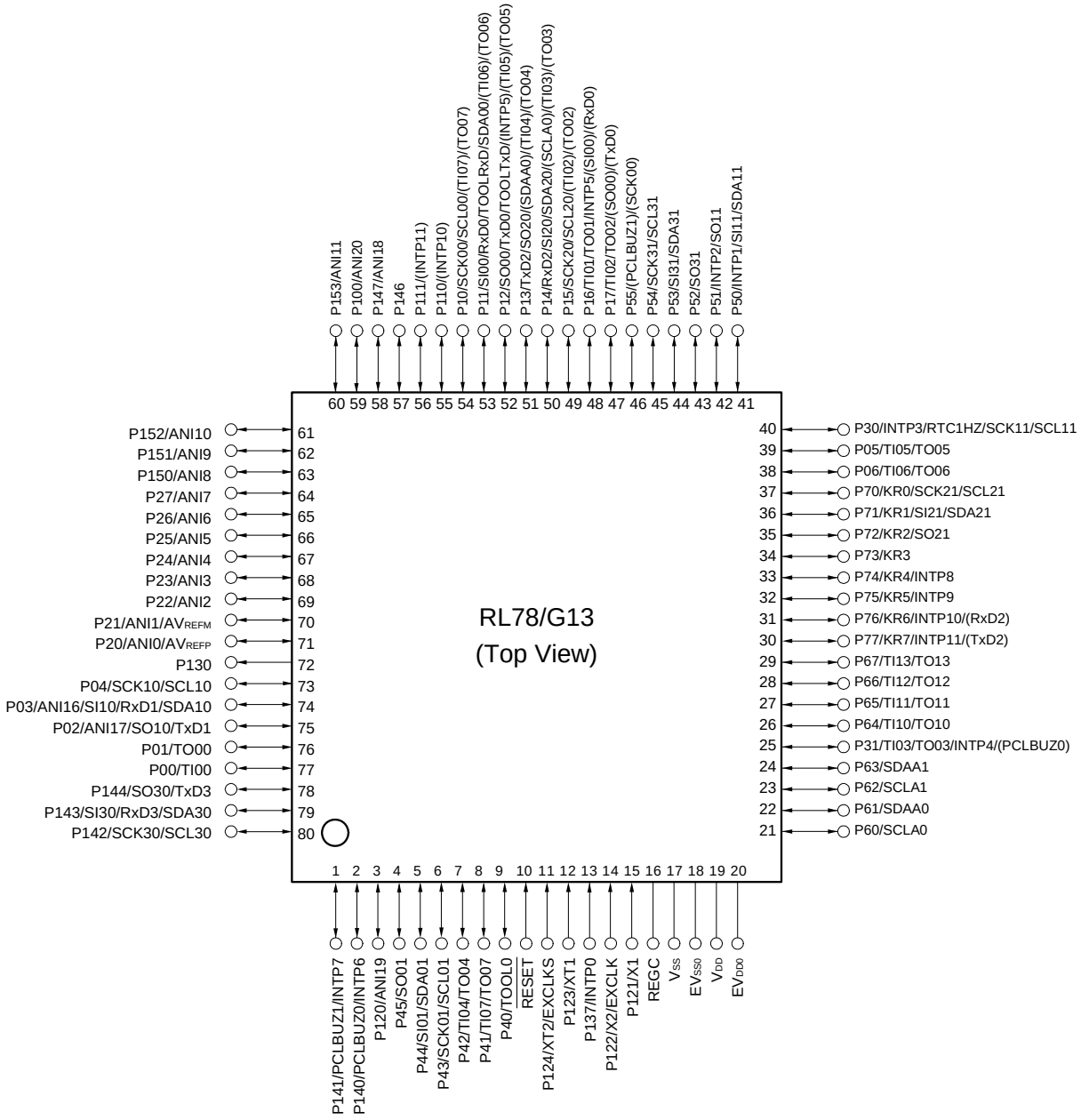
**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS0}$ pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.3.12 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65-mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5-mm pitch)




**Cautions 1. Make $EV_{SS0}$ pin the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is no less than $EV_{DD0}$ pin.**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

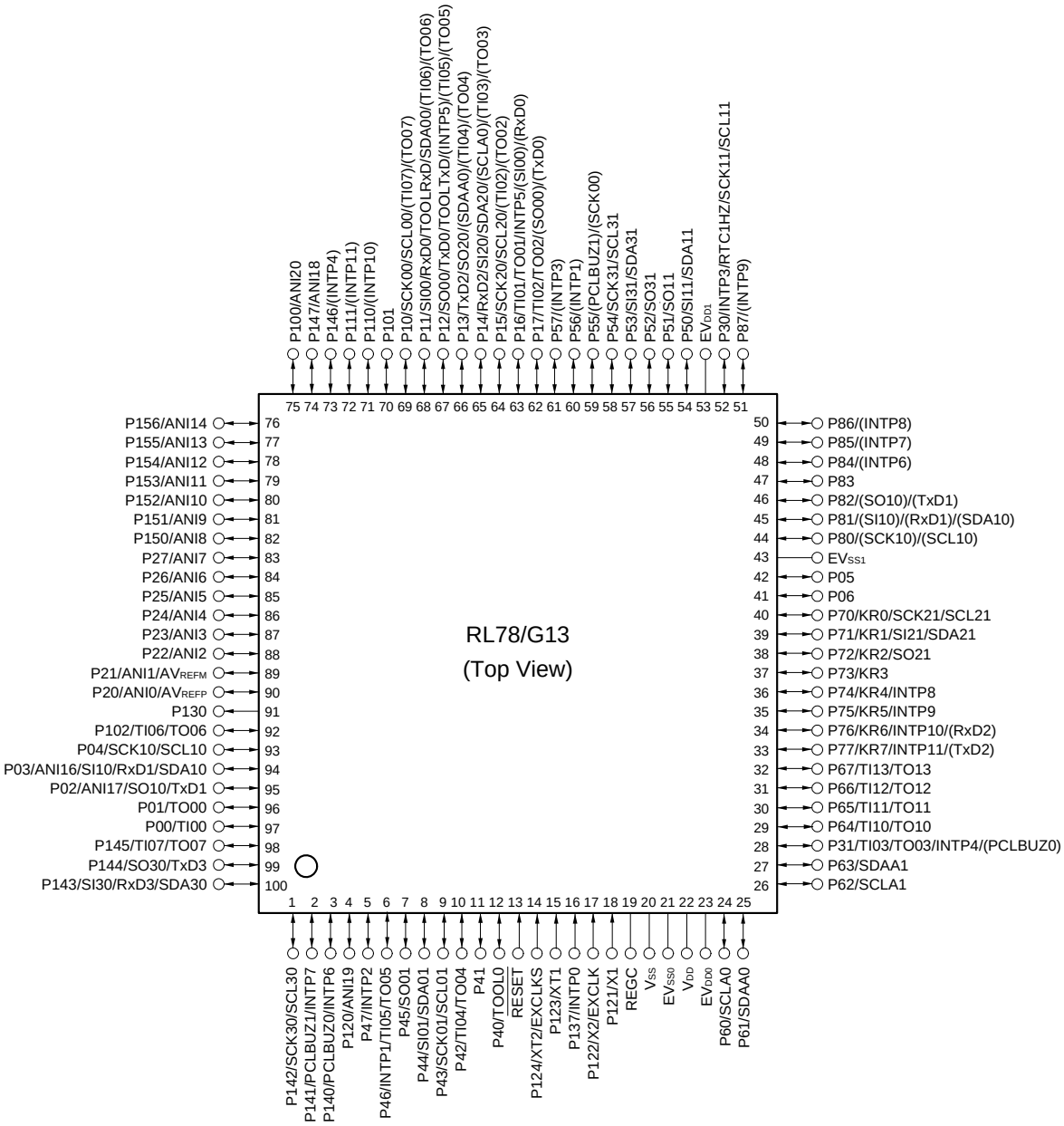
**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS0}$ pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.3.13 100-pin products

- 100-pin plastic LFQFP (14 × 14 mm, 0.5-mm pitch)




**Cautions 1. Make $EV_{SS0}$ and $EV_{SS1}$ pins the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is no less than $EV_{DD0}$ and $EV_{DD1}$ pins ($EV_{DD0}$ = $EV_{DD1}$).**

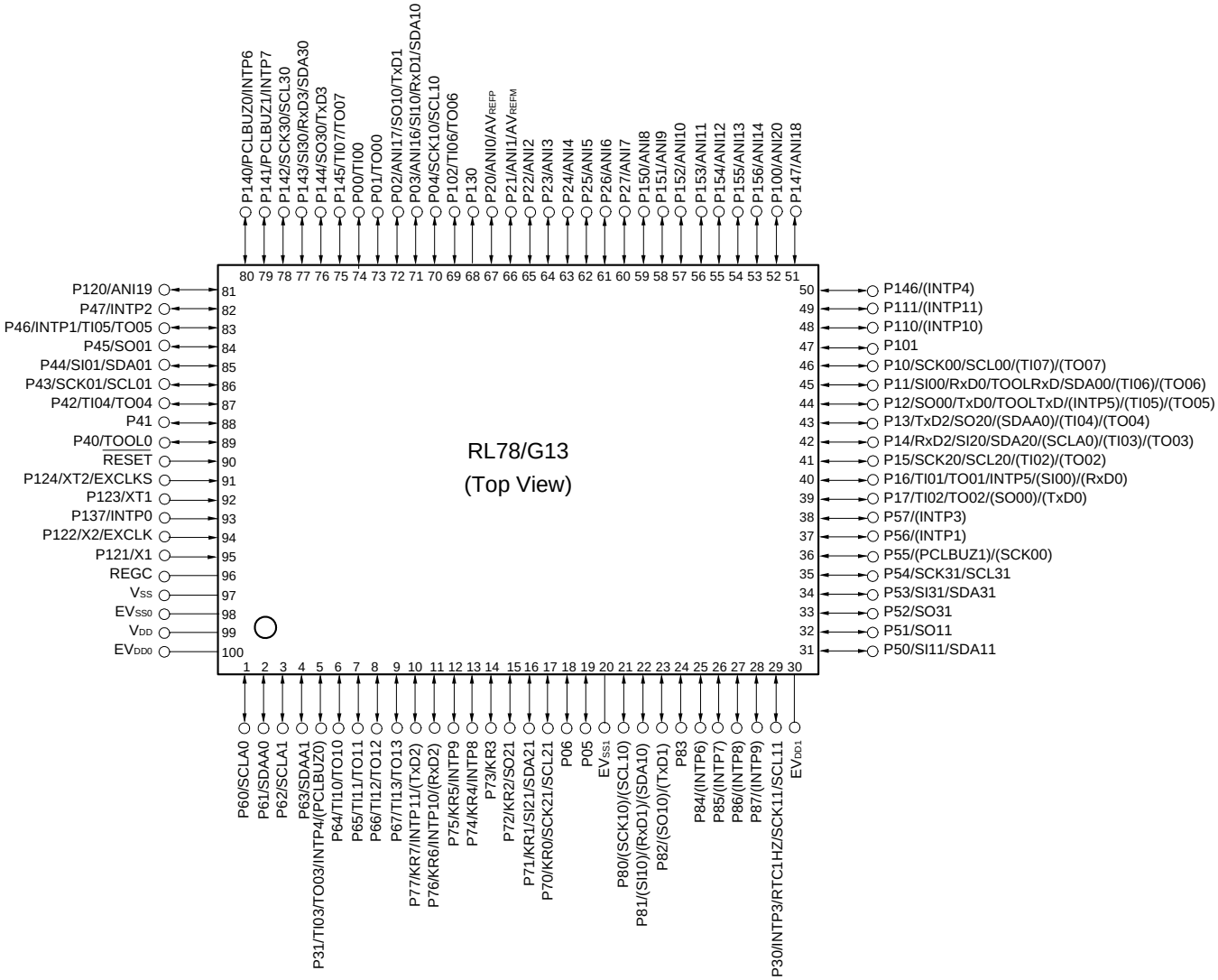
**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$, $EV_{DD0}$ and $EV_{DD1}$ pins and connect the $V_{SS}$, $EV_{SS0}$ and $EV_{SS1}$ pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 100-pin plastic LQFP (14 × 20 mm, 0.65-mm pitch)




**Cautions 1. Make $EV_{SS0}$ and $EV_{SS1}$ pins the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is no less than $EV_{DD0}$ and $EV_{DD1}$ pins ($EV_{DD0}$ = $EV_{DD1}$).**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

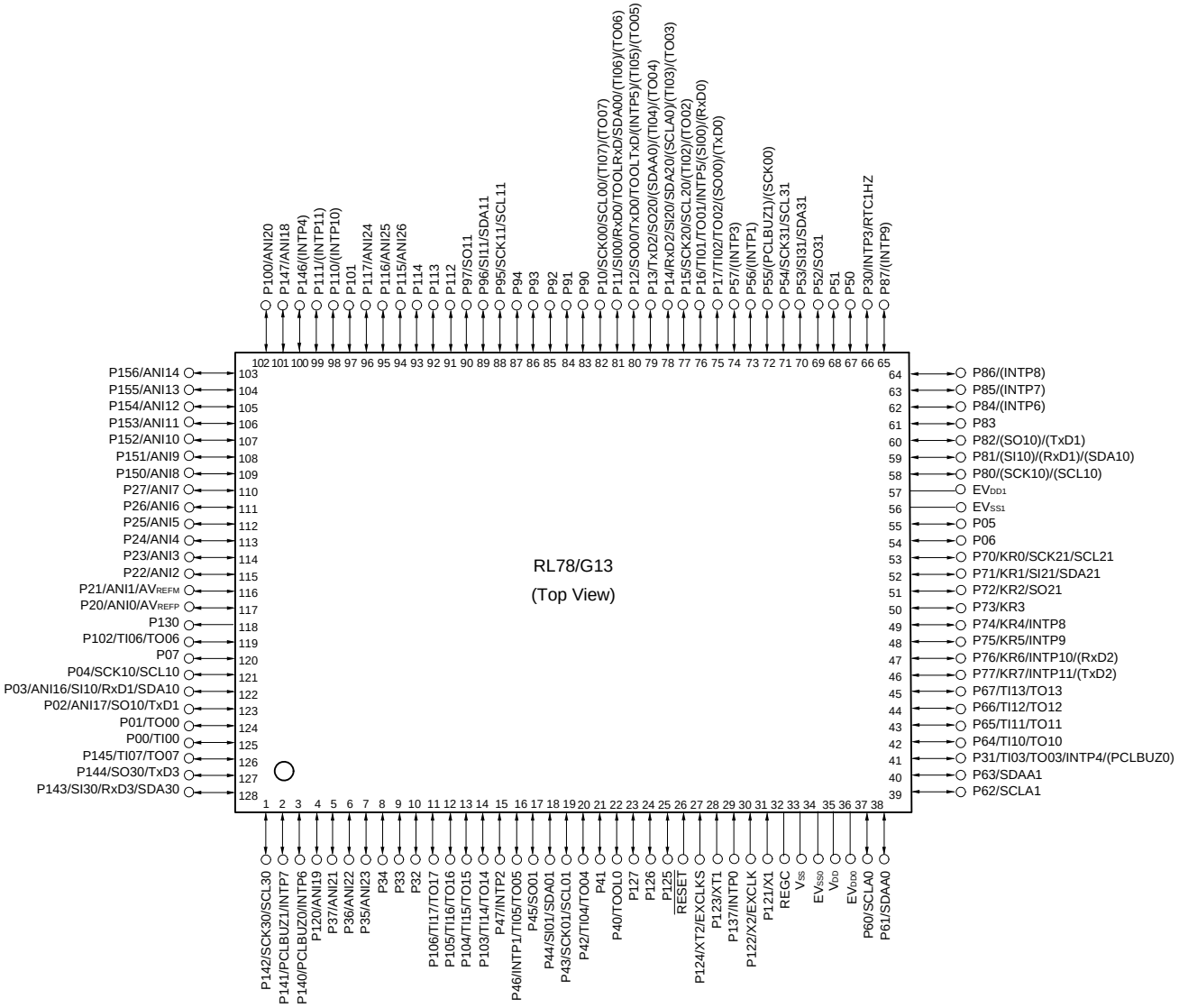
**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$, $EV_{DD0}$ and $EV_{DD1}$ pins and connect the $V_{SS}$, $EV_{SS0}$ and $EV_{SS1}$ pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.3.14 128-pin products

- 128-pin plastic LFQFP (14 × 20 mm, 0.5-mm pitch)




**Cautions 1. Make $EV_{SS0}$ and $EV_{SS1}$ pins the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is no less than $EV_{DD0}$ and $EV_{DD1}$ pins ($EV_{DD0}$ = $EV_{DD1}$).**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$, $EV_{DD0}$ and $EV_{DD1}$ pins and connect the $V_{SS}$, $EV_{SS0}$ and $EV_{SS1}$ pins to separate ground lines.

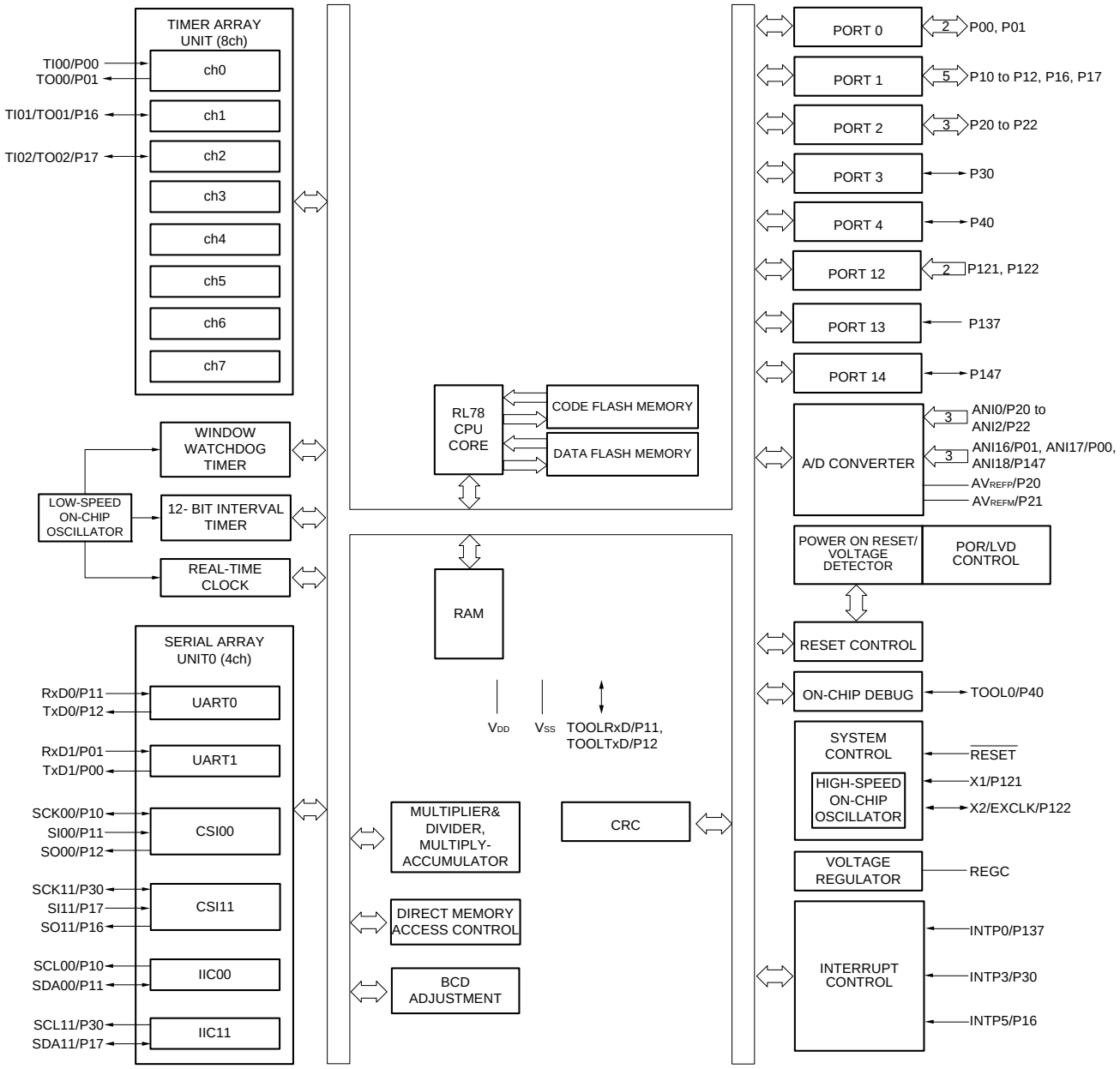
**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.4 Pin Identification

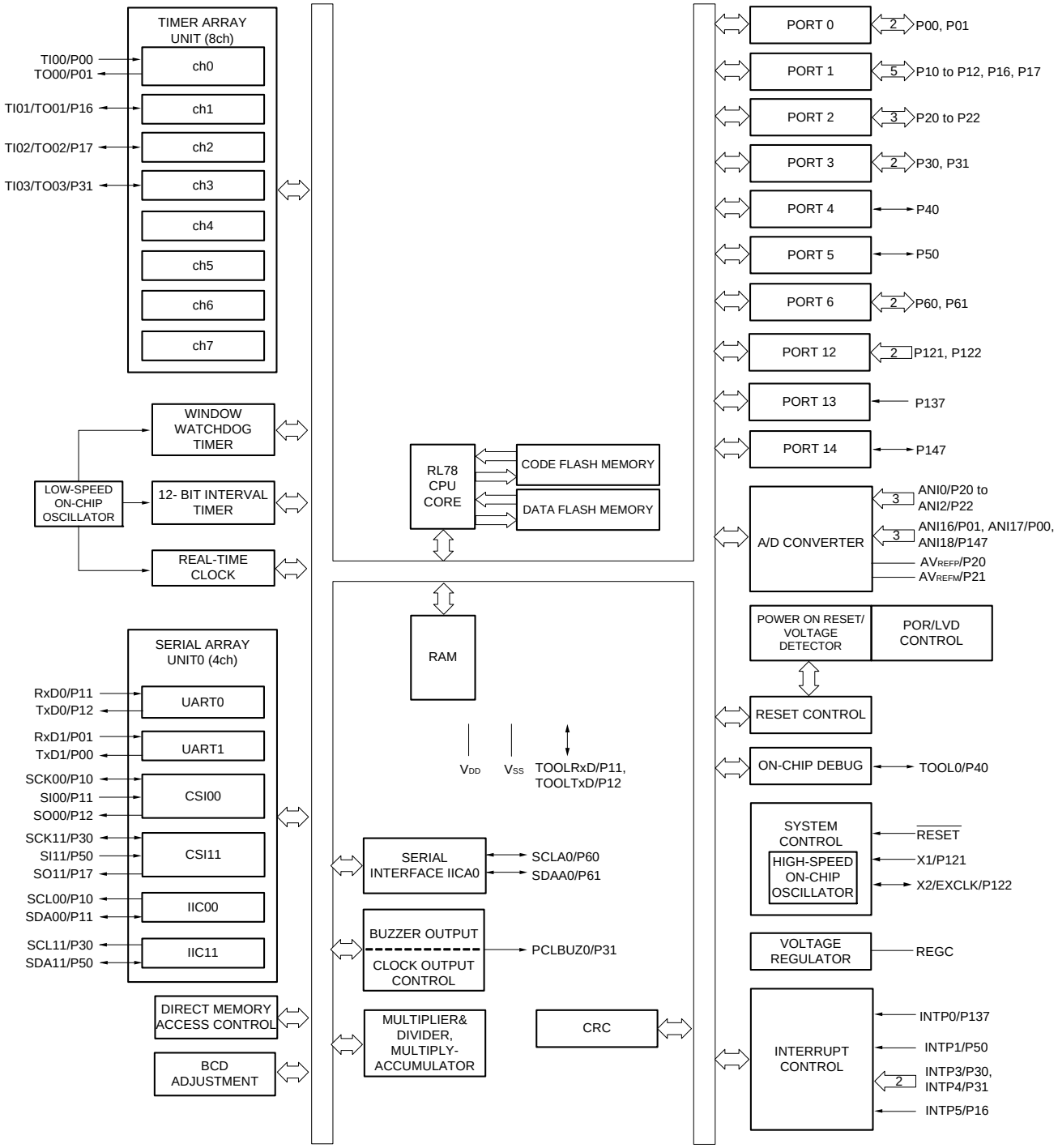
| | | | |
|---|---|---|---|
| ANI0 to ANI14, ANI16 to ANI26: | Analog input | REGC: | Regulator capacitance |
| $AV_{REFM}$: | A/D converter reference potential (– side) input | $\overline{RESET}$: | Reset |
| | | RTC1HZ: | Real-time clock correction clock (1 Hz) output |
| $AV_{REFP}$: | A/D converter reference potential (+ side) input | RxD0 to RxD3: | Receive data |
| $EV_{DD0}$, $EV_{DD1}$: | Power supply for port | SCLA0, SCLA1, SCK00, SCK01, SCK10, SCK11, SCK20, SCK21, SCK30, SCK31: | Serial clock input/output |
| $EV_{SS0}$, $EV_{SS1}$: | Ground for port | | |
| EXCLK: | External clock input (Main system clock) | | |
| EXCLKS: | External clock input (Subsystem clock) | SCL00, SCL01, SCL10, SCL11, SCL20, SCL21, SCL30, SCL31: | Serial clock output |
| INTP0 to INTP11: | Interrupt request from peripheral | SDAA0, SDAA1, SDA00, SDA01,SDA10, SDA11, SDA20,SDA21, SDA30, SDA31: | Serial data input/output |
| KR0 to KR7: | Key return | | |
| P00 to P07: | Port 0 | | |
| P10 to P17: | Port 1 | SI00, SI01, SI10, SI11, SI20, SI21, SI30, SI31: | Serial data input |
| P20 to P27: | Port 2 | | |
| P30 to P37: | Port 3 | SO00, SO01, SO10, SO11, SO20, SO21, SO30, SO31: | Serial data output |
| P40 to P47: | Port 4 | | |
| P50 to P57: | Port 5 | | |
| P60 to P67: | Port 6 | TI00 to TI07, TI10 to TI17: | Timer input |
| P70 to P77: | Port 7 | | |
| P80 to P87: | Port 8 | TO00 to TO07, TO10 to TO17: | Timer output |
| P90 to P97: | Port 9 | | |
| P100 to P106: | Port 10 | TOOL0: | Data input/output for tool |
| P110 to P117: | Port 11 | TOOLRxD, TOOLTxD: | Data input/output for external device |
| P120 to P127: | Port 12 | TxD0 to TxD3: | Transmit data |
| P130, P137: | Port 13 | $V_{DD}$: | Power supply |
| P140 to P147: | Port 14 | $V_{SS}$: | Ground |
| P150 to P156: | Port 15 | X1, X2: | Crystal oscillator (main system clock) |
| PCLBUZ0, PCLBUZ1: | Programmable clock output/buzzer output | XT1, XT2: | Crystal oscillator (subsystem clock) |

## 1.5 Block Diagram

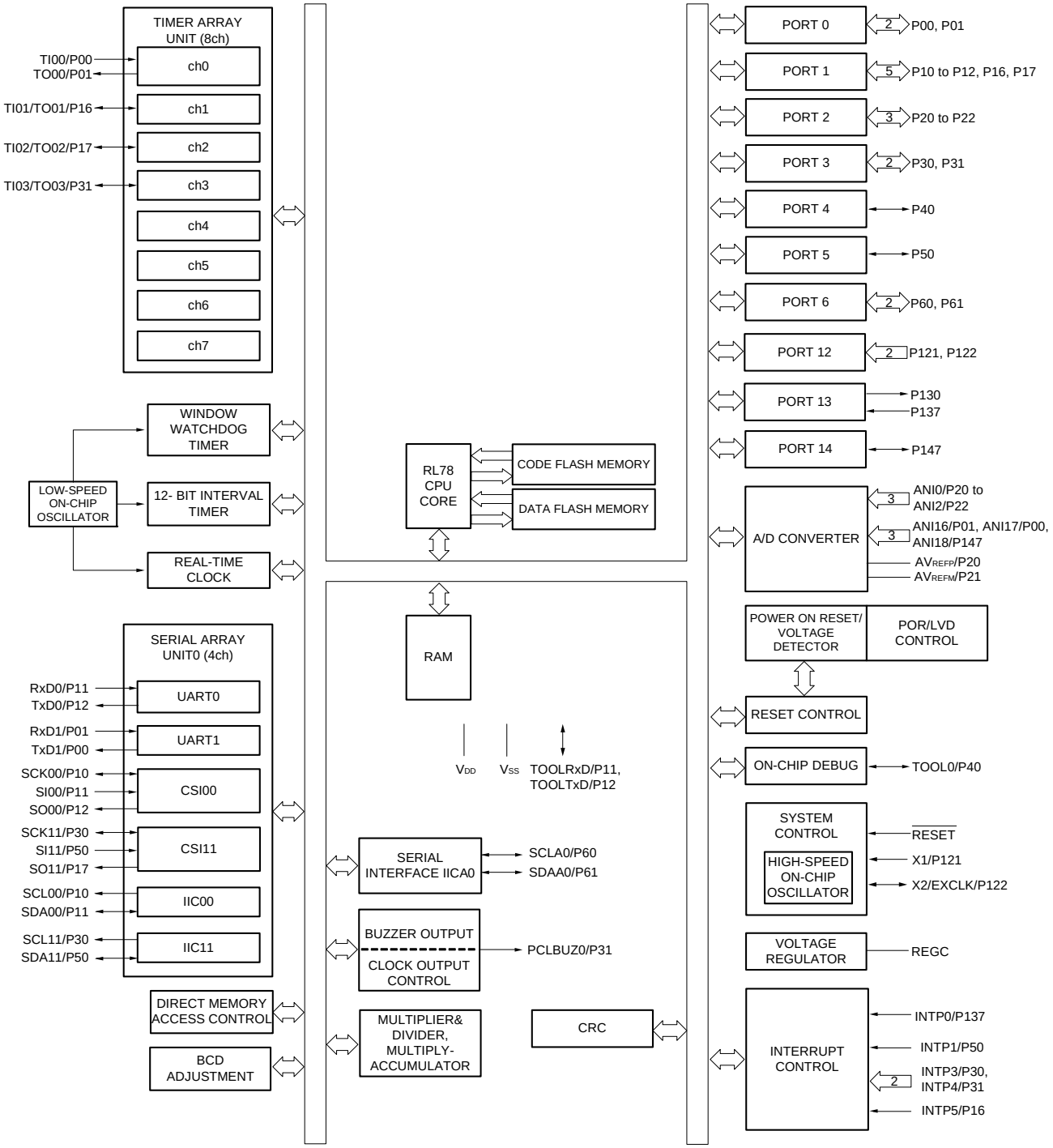
### 1.5.1 20-pin products



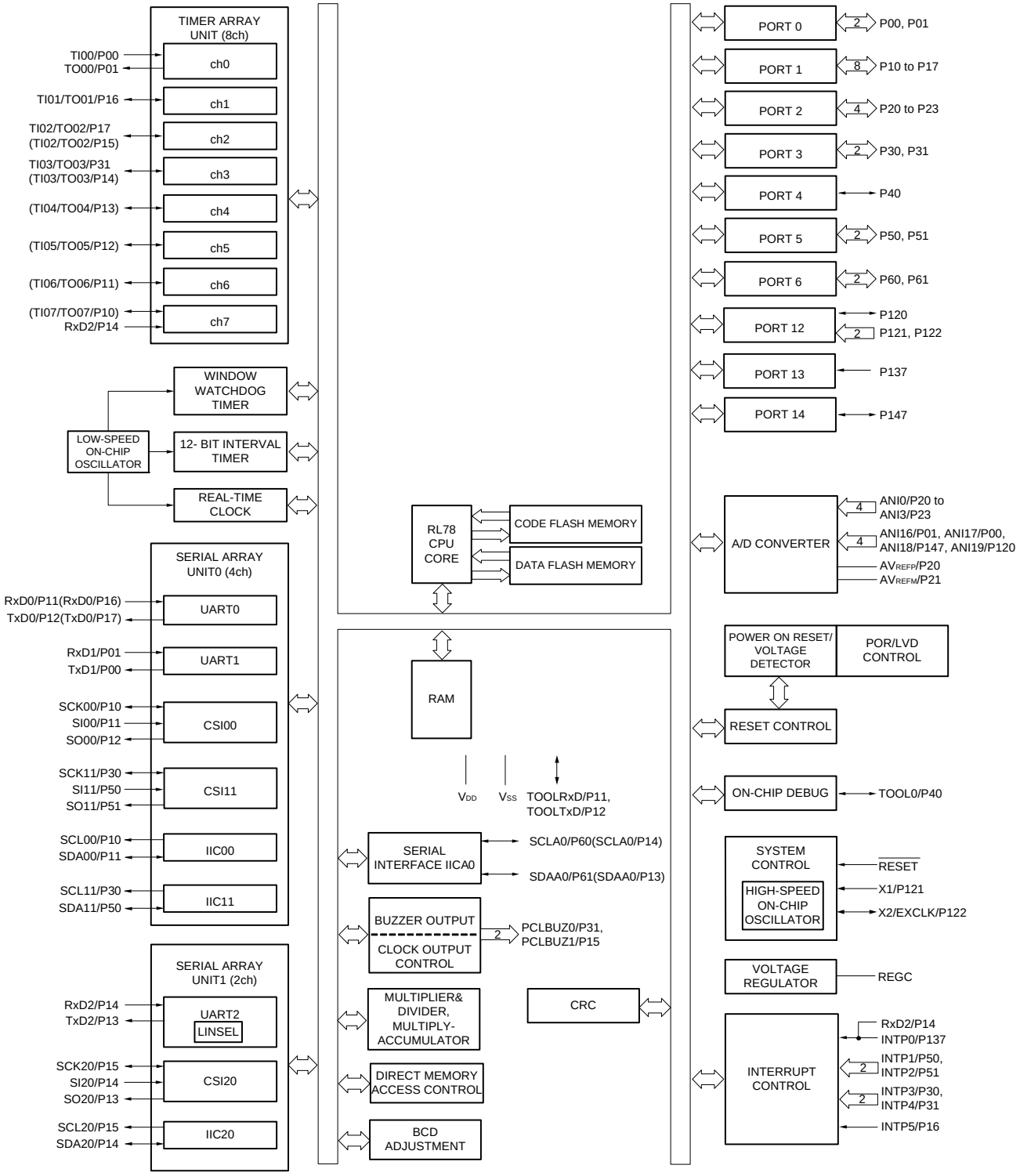
### 1.5.2 24-pin products



### 1.5.3 25-pin products

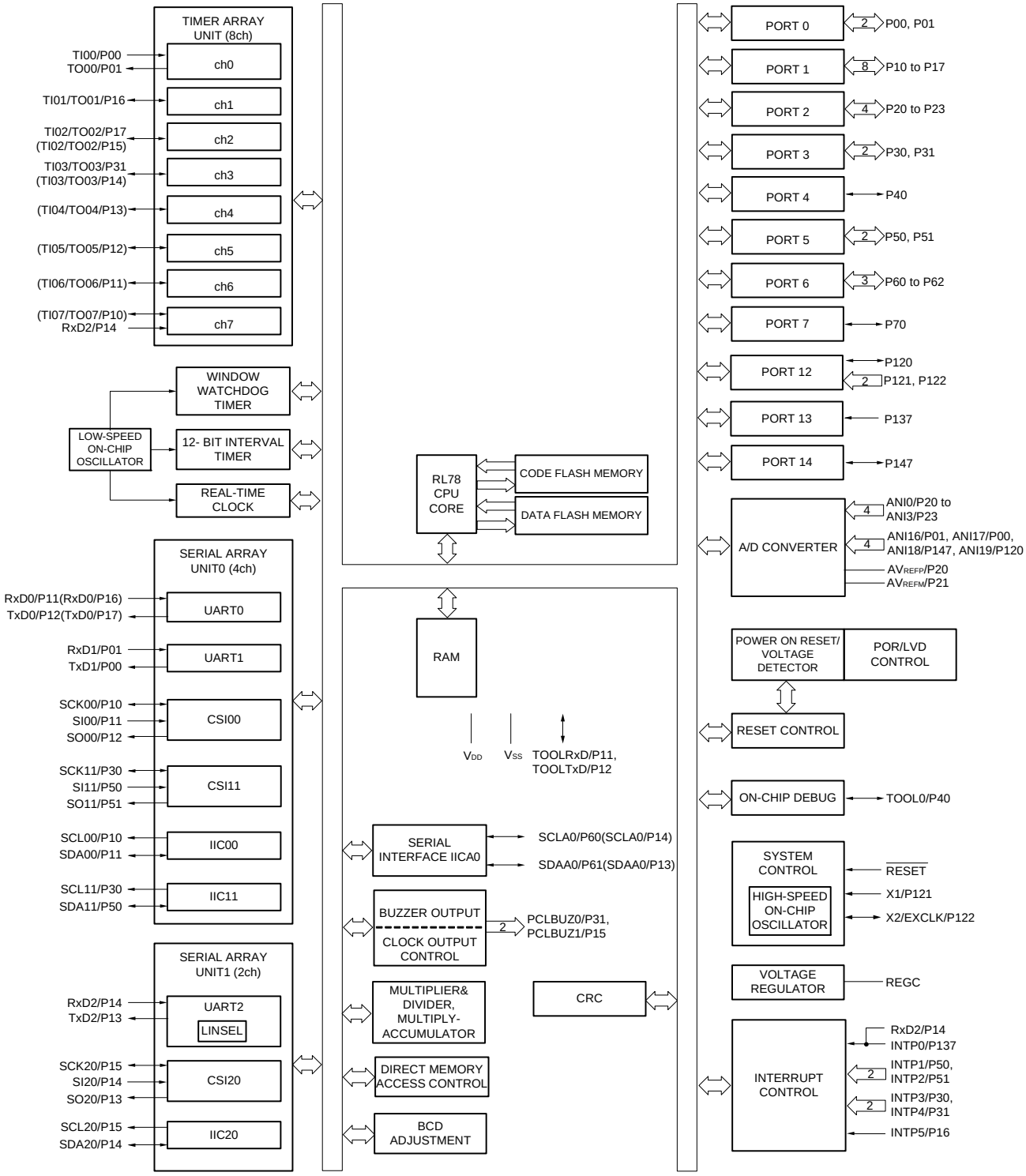


### 1.5.4 30-pin products



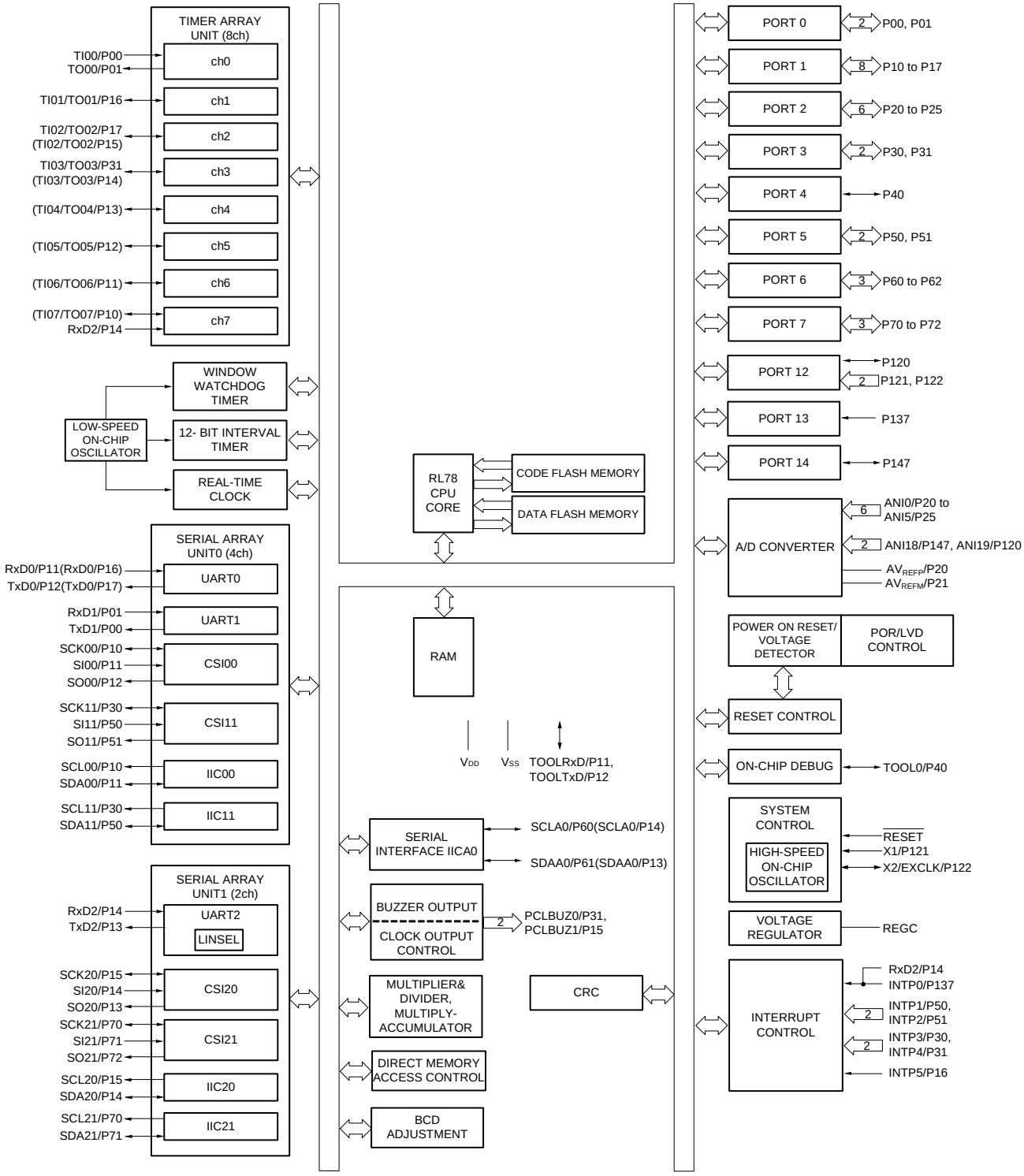

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.5 32-pin products



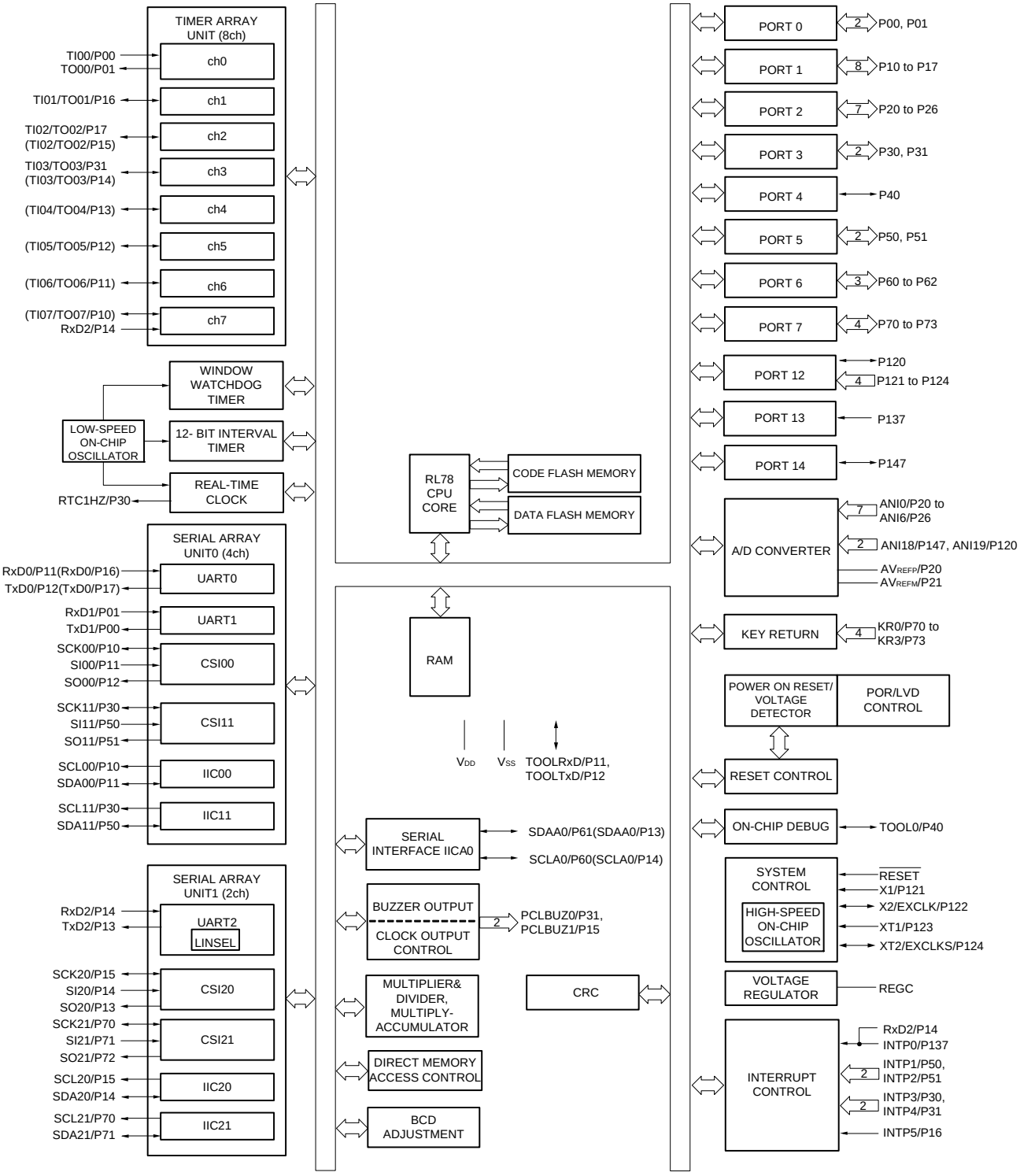

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.6 36-pin products



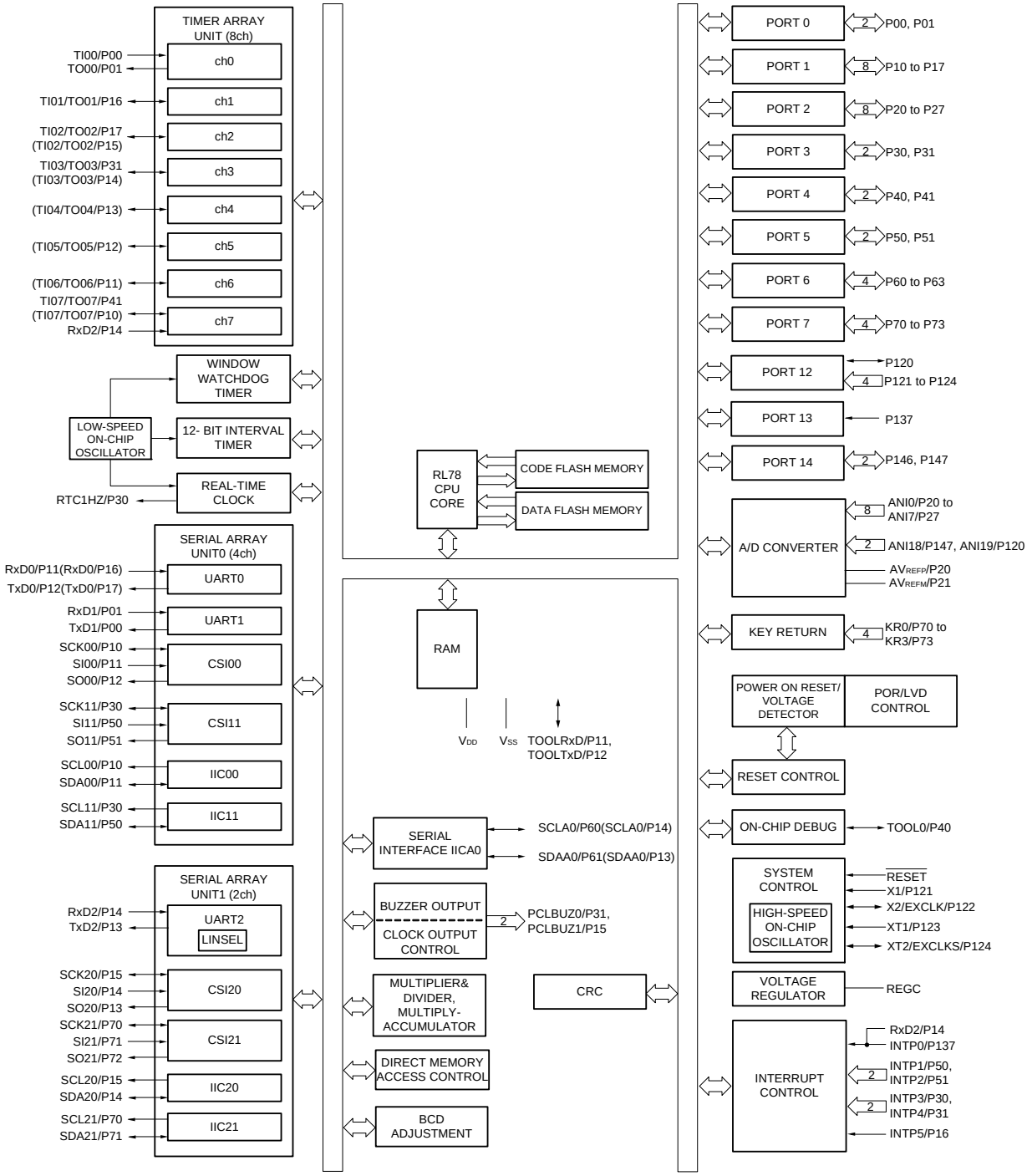

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.7 40-pin products



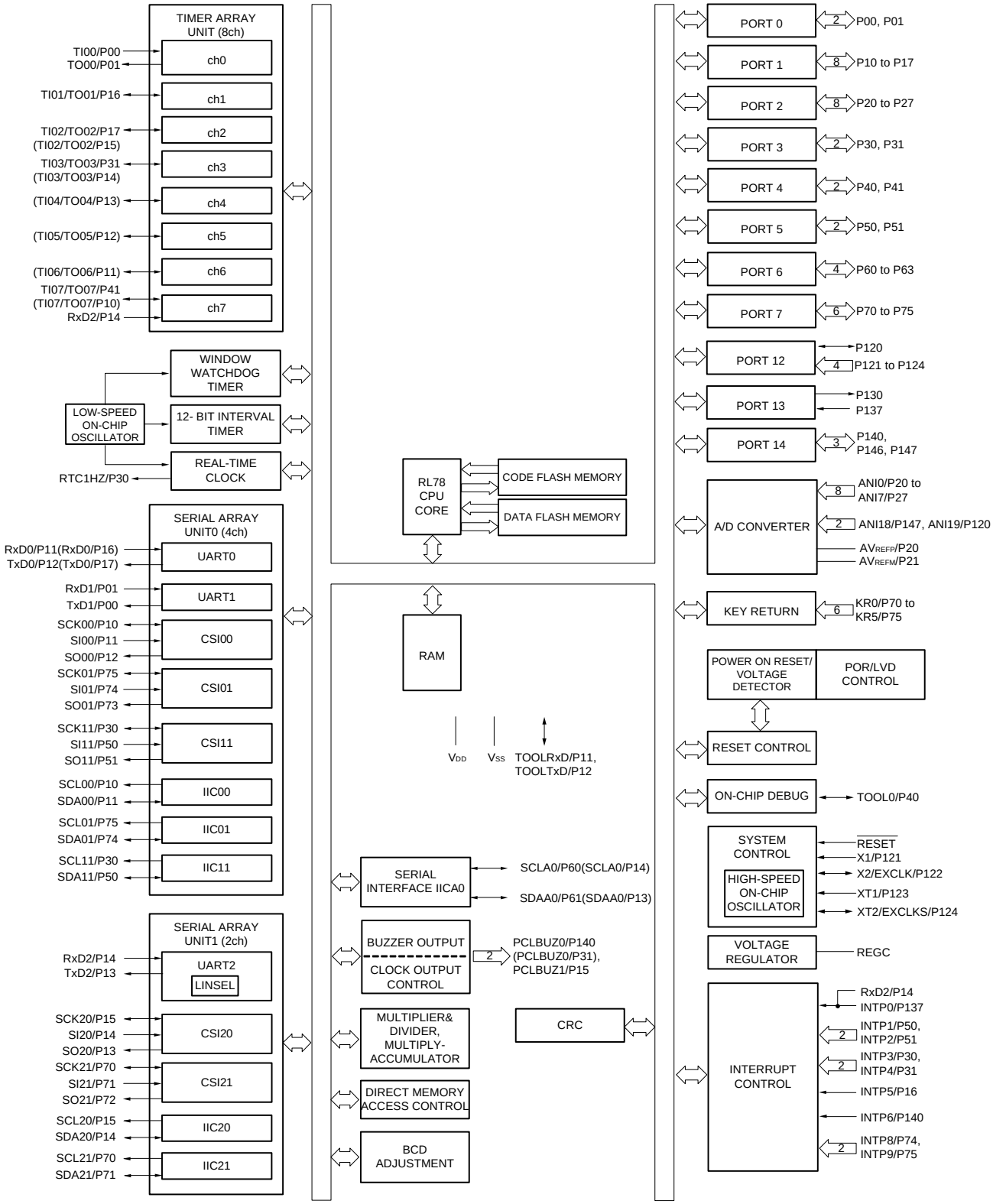

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.8 44-pin products



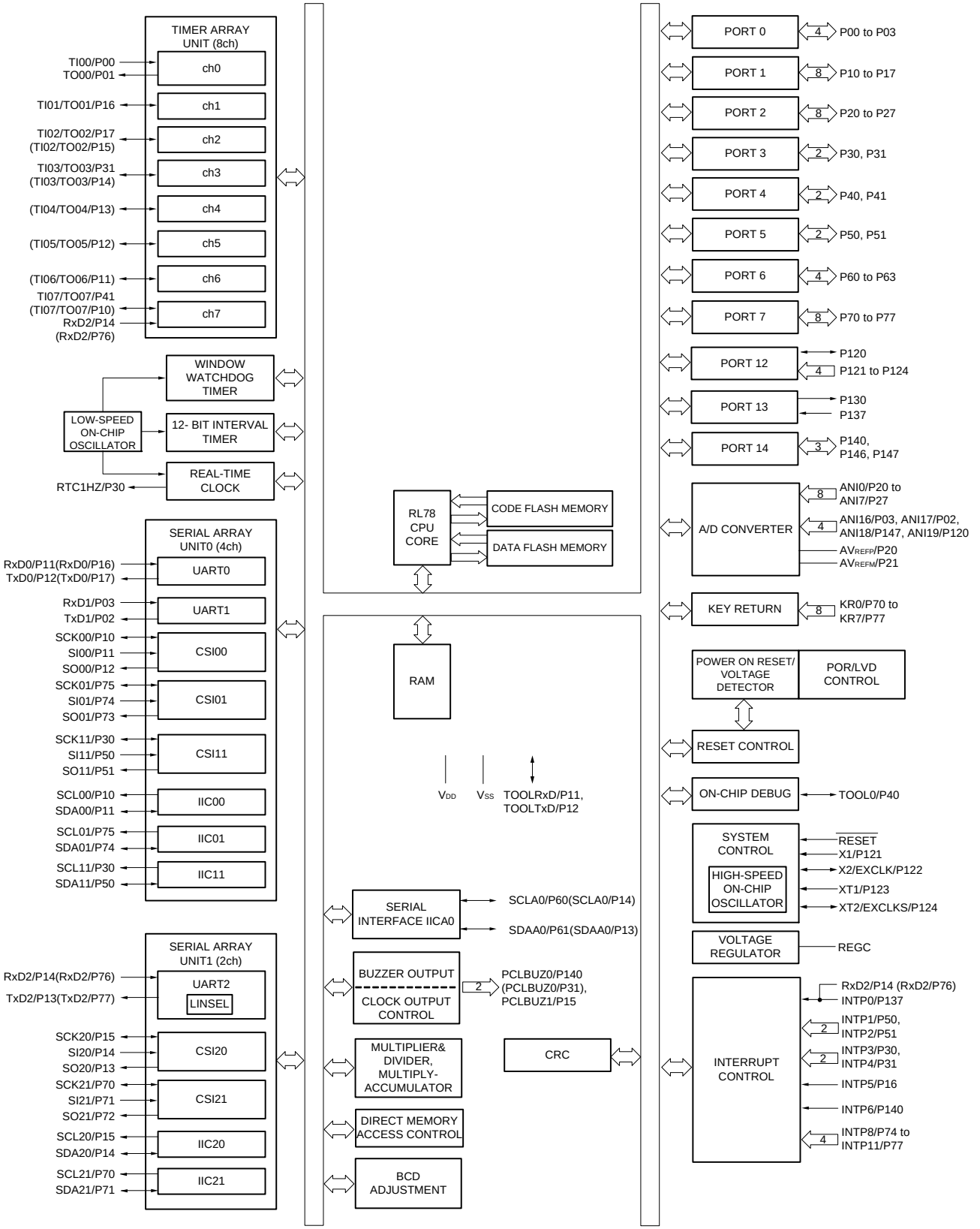

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.9 48-pin products



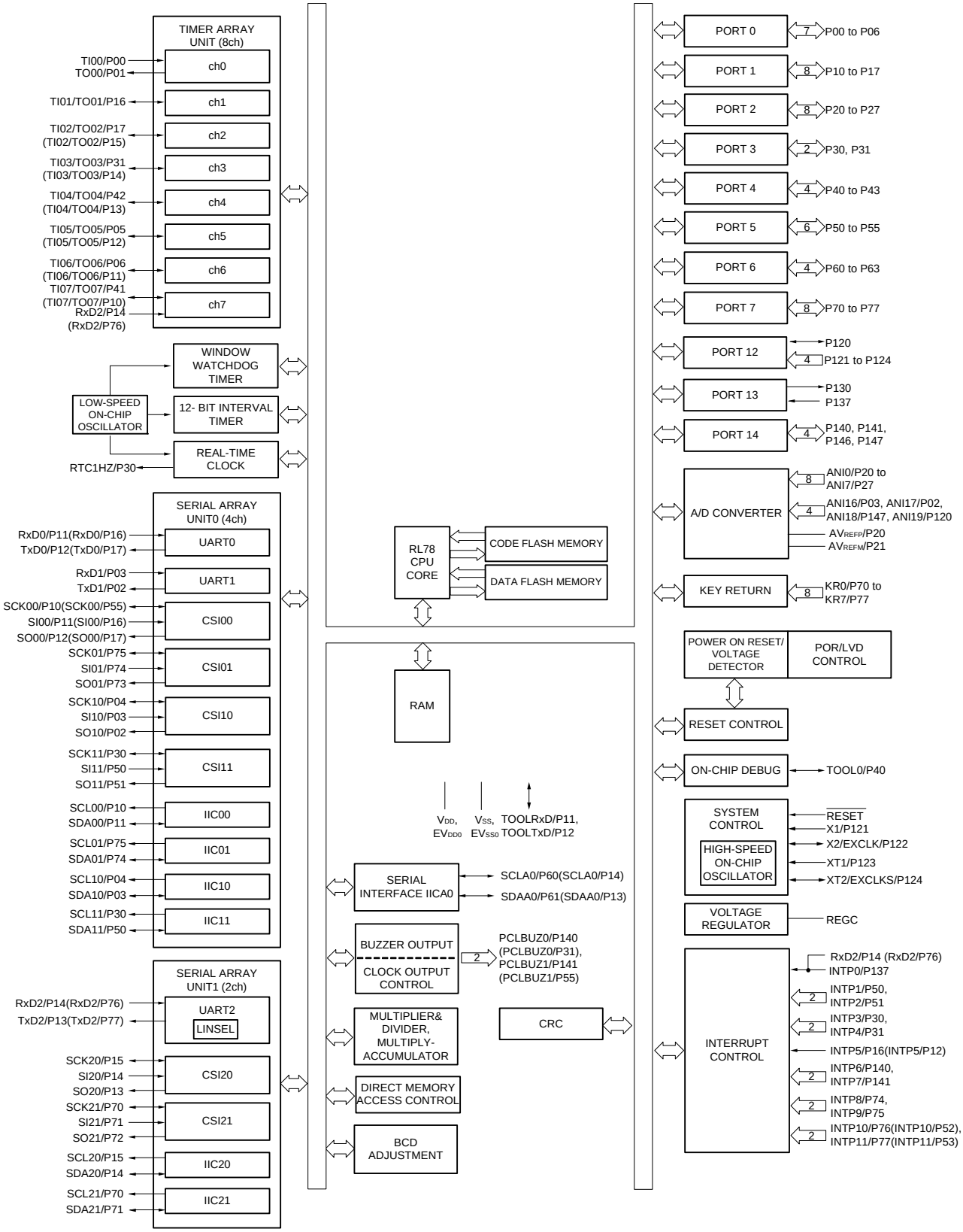

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.10 52-pin products



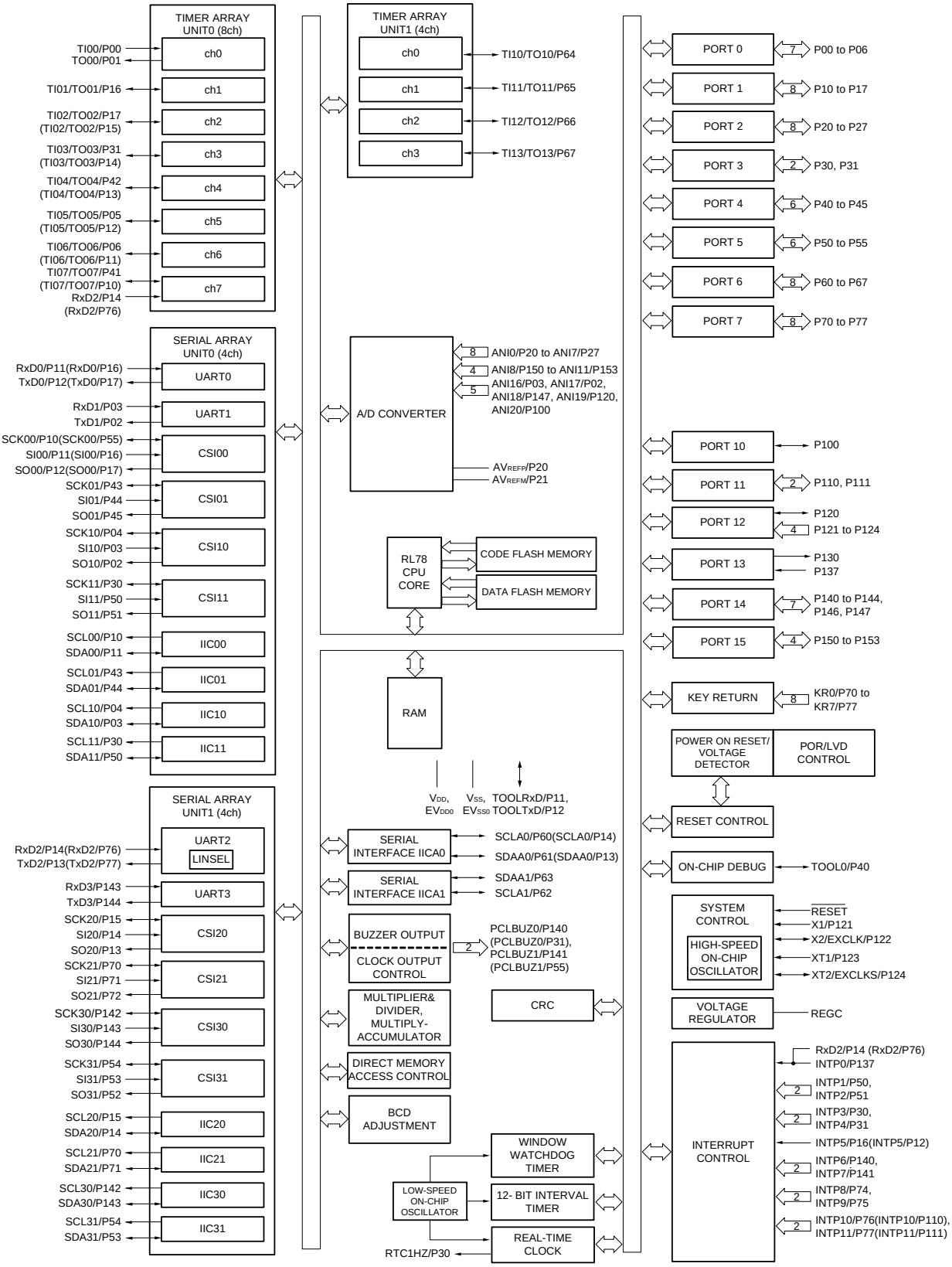

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.11 64-pin products



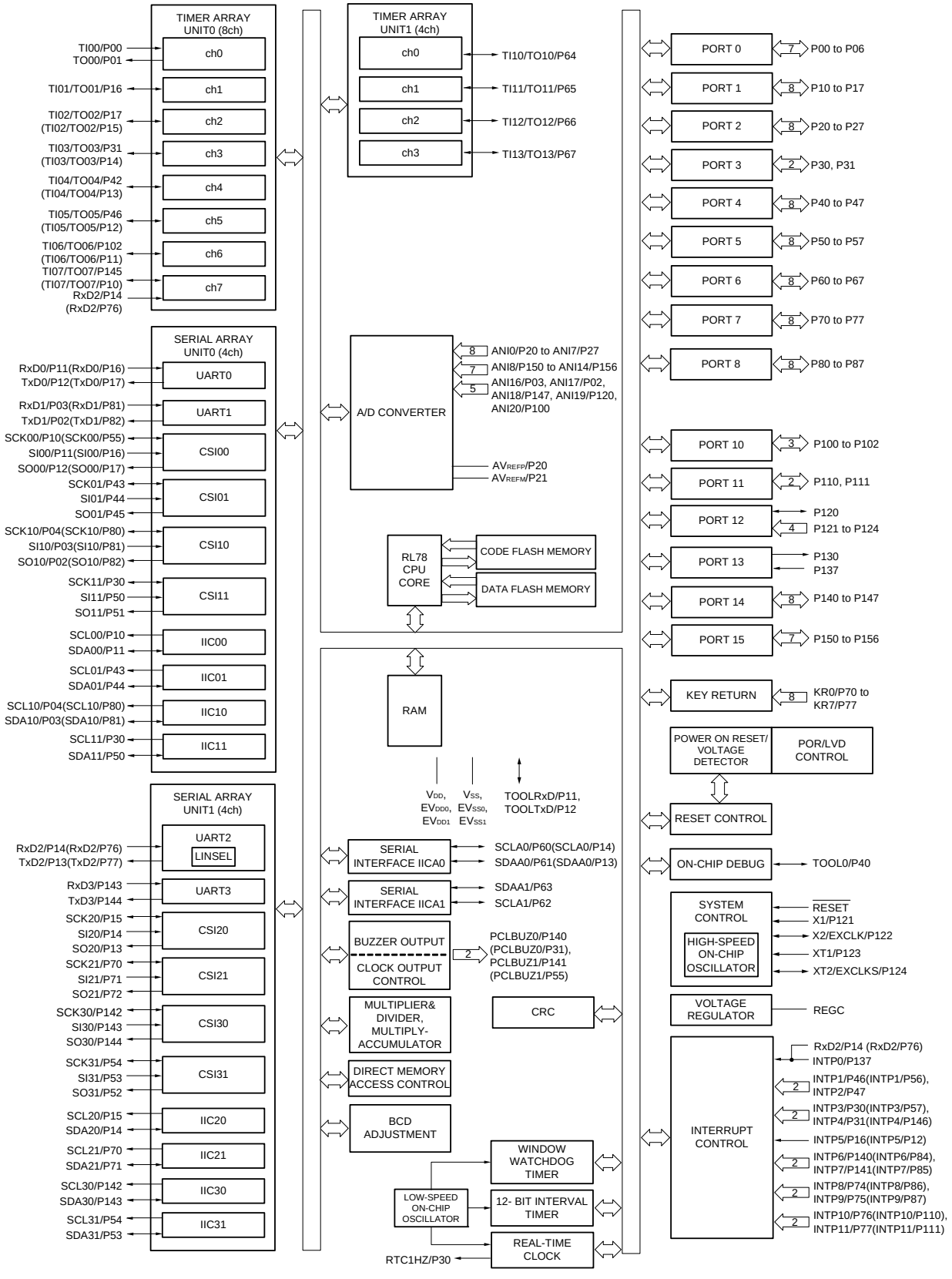

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.12 80-pin products



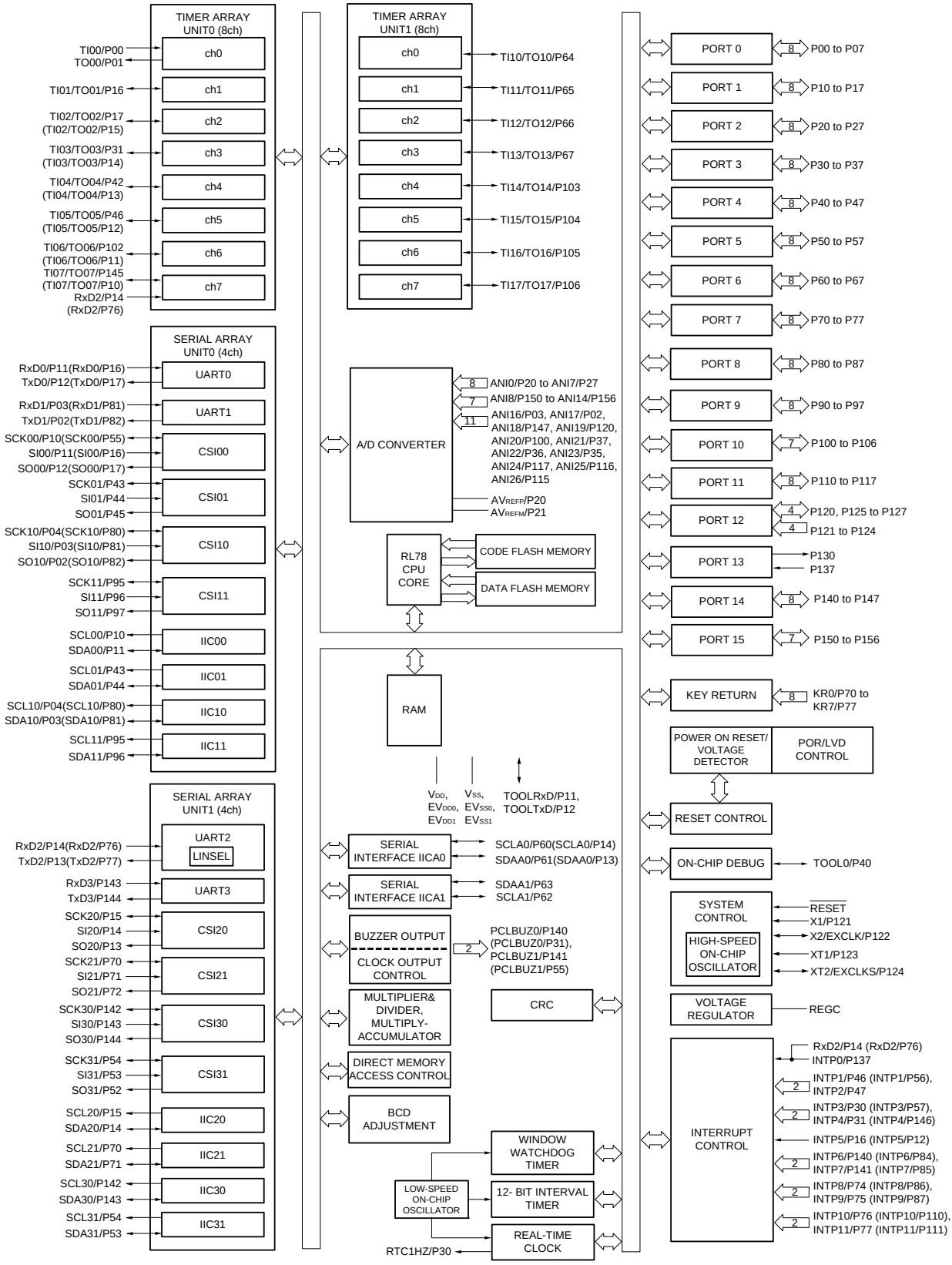

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.13 100-pin products




**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.14 128-pin products




**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.**

(1/2)

| Item | | 20-pin | | 24-pin | | 25-pin | | 30-pin | | 32-pin | | 36-pin | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F1006x | R5F1016x | R5F1007x | R5F1017x | R5F1008x | R5F1018x | R5F100Ax | R5F101Ax | R5F100Bx | R5F101Bx | R5F100Cx | R5F101Cx |
| Code flash memory (KB) | | 16 to 64 | | 16 to 64 | | 16 to 64 | | 16 to 128 | | 16 to 128 | | 16 to 128 | |
| Data flash memory (KB) | | 4 | – | 4 | – | 4 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – |
| RAM (KB) | | 2 to 4 Note1 | | 2 to 4 Note1 | | 2 to 4 Note1 | | 2 to 12 Note1 | | 2 to 12 Note1 | | 2 to 12 Note1 | |
| Address space | | 1 MB | | | | | | | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | | | |
| Subsystem clock | | – | | | | | | | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | | | | | | | |
| General-purpose registers | | (8-bit register × 8) × 4 banks | | | | | | | | | | | |
| Minimum instruction execution time | | 0.03125 µs (High-speed on-chip oscillator: $f_{IH}$ = 32 MHz operation) | | | | | | | | | | | |
| | | 0.05 µs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | | | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | | | | | | | |
| I/O port | Total | 16 | | 20 | | 21 | | 26 | | 28 | | 32 | |
| | CMOS I/O | 13<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 5) | | 15<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 6) | | 15<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 6) | | 21<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 9) | | 22<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 9) | | 26<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 10) | |
| | CMOS input | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | |
| | CMOS output | – | | – | | 1 | | – | | – | | – | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | – | | 2 | | 2 | | 2 | | 3 | | 3 | |
| Timer | 16-bit timer | 8 channels | | | | | | | | | | | |
| | Watchdog timer | 1 channel | | | | | | | | | | | |
| | Real-time clock (RTC) | 1 channel Note 2 | | | | | | | | | | | |
| | 12-bit interval timer (IT) | 1 channel | | | | | | | | | | | |
| | Timer output | 3 channels (PWM outputs: 2 Note 3) | | 4 channels (PWM outputs: 3 Note 3) | | | | 4 channels (PWM outputs: 3 Note 3),<br>8 channels (PWM outputs: 7 Note 3) Note 4 | | | | | |
| | RTC output | – | | | | | | | | | | | |

**Notes 1.** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = 6 to 8, A to C): Start address FF300H
R5F100xE, R5F101xE (x = 6 to 8, A to C): Start address FEF00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

**Notes 2.** Only the constant-period interrupt function when the low-speed on-chip oscillator clock ($f_{IL}$) is selected
**3.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
**4.** When setting to PIOR = 1

(2/2)

| Item | | 20-pin | | 24-pin | | 25-pin | | 30-pin | | 32-pin | | 36-pin | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F1006x | R5F1016x | R5F1007x | R5F1017x | R5F1008x | R5F1018x | R5F100Ax | R5F101Ax | R5F100Bx | R5F101Bx | R5F100Cx | R5F101Cx |
| Clock output/buzzer output | | – | | 1 | | 1 | | 2 | | 2 | | 2 | |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation) | | | | | | | | | | | |
| 8/10-bit resolution A/D converter | | 6 channels | | 6 channels | | 6 channels | | 8 channels | | 8 channels | | 8 channels | |
| Serial interface | | [20-pin, 24-pin, 25-pin products]<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>[30-pin, 32-pin products]<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART (UART supporting LIN-bus): 1 channel<br>[36-pin products]<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>• CSI: 2 channels/simplified $I^2C$: 2 channels/UART (UART supporting LIN-bus): 1 channel | | | | | | | | | | | |
| | $I^2C$ bus | – | | 1 channel | | 1 channel | | 1 channel | | 1 channel | | 1 channel | |
| Multiplier and divider/multiply-accumulator | | • 16 bits × 16 bits = 32 bits (Unsigned or signed)<br>• 32 bits ÷ 32 bits = 32 bits (Unsigned)<br>• 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | | | | | | | | | | |
| DMA controller | | 2 channels | | | | | | | | | | | |
| Vectored interrupt sources | Internal | 23 | | 24 | | 24 | | 27 | | 27 | | 27 | |
| | External | 3 | | 5 | | 5 | | 6 | | 6 | | 6 | |
| Key interrupt | | – | | | | | | | | | | | |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | | | | | | | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 V (TYP.)<br>• Power-down-reset: 1.50 V (TYP.) | | | | | | | | | | | |
| Voltage detector | | • Rising edge : 1.67 V to 4.06 V (14 stages)<br>• Falling edge : 1.63 V to 3.98 V (14 stages) | | | | | | | | | | | |
| On-chip debug function | | Provided | | | | | | | | | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | | | | | | | | | | | |
| Operating ambient temperature | | $T_A$ = 40 to +85°C (A: Consumer applications, D: Industrial applications )<br>$T_A$ = 40 to +105°C (G: Industrial applications) | | | | | | | | | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.**

(1/2)

| Item | | 40-pin | | 44-pin | | 48-pin | | 52-pin | | 64-pin | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F100Ex | R5F101Ex | R5F100Fx | R5F101Fx | R5F100Gx | R5F101Gx | R5F100Jx | R5F101Jx | R5F100Lx | R5F101Lx |
| Code flash memory (KB) | | 16 to 192 | | 16 to 512 | | 16 to 512 | | 32 to 512 | | 32 to 512 | |
| Data flash memory (KB) | | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – |
| RAM (KB) | | 2 to 16[Note1] | | 2 to 32[Note1] | | 2 to 32[Note1] | | 2 to 32[Note1] | | 2 to 32[Note1] | |
| Address space | | 1 MB | | | | | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)<br>32.768 kHz | | | | | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | | | | | |
| General-purpose registers | | (8-bit register × 8) × 4 banks | | | | | | | | | |
| Minimum instruction execution time | | 0.03125 µs (High-speed on-chip oscillator: $f_{IH}$ = 32 MHz operation) | | | | | | | | | |
| | | 0.05 µs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | | | | | |
| | | 30.5 µs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | | | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | | | | | |
| I/O port | Total | 36 | | 40 | | 44 | | 48 | | 58 | |
| | CMOS I/O | 28<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 10) | | 31<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 10) | | 34<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 11) | | 38<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 13) | | 48<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 15) | |
| | CMOS input | 5 | | 5 | | 5 | | 5 | | 5 | |
| | CMOS output | – | | – | | 1 | | 1 | | 1 | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | 3 | | 4 | | 4 | | 4 | | 4 | |
| Timer | 16-bit timer | 8 channels | | | | | | | | | |
| | Watchdog timer | 1 channel | | | | | | | | | |
| | Real-time clock (RTC) | 1 channel | | | | | | | | | |
| | 12-bit interval timer (IT) | 1 channel | | | | | | | | | |
| | Timer output | 4 channels (PWM outputs: 3 [Note 2]),<br>8 channels (PWM outputs: 7 [Note 2])[Note 3] | | 5 channels (PWM outputs: 4 [Note 2]),<br>8 channels (PWM outputs: 7 [Note 2]) [Note 3] | | | | | | 8 channels (PWM outputs: 7 [Note 2]) | |
| | RTC output | 1 channel<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | | | | | | | | |

**Notes 1.** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = E to G, J, L): Start address FF300H
R5F100xE, R5F101xE (x = E to G, J, L): Start address FEF00H
R5F100xJ, R5F101xJ (x = F, G, J, L): Start address FAF00H
R5F100xL, R5F101xL (x = F, G, J, L): Start address F7F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

**Notes 2.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
**3.** When setting to PIOR = 1

(2/2)

| Item | | 40-pin | | 44-pin | | 48-pin | | 52-pin | | 64-pin | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F100Ex | R5F101Ex | R5F100Fx | R5F101Fx | R5F100Gx | R5F101Gx | R5F100Jx | R5F101Jx | R5F100Lx | R5F101Lx |
| Clock output/buzzer output | | 2 | | 2 | | 2 | | 2 | | 2 | |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | | | | | | | |
| 8/10-bit resolution A/D converter | | 9 channels | | 10 channels | | 10 channels | | 12 channels | | 12 channels | |
| Serial interface | | [40-pin, 44-pin products]<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>• CSI: 2 channels/simplified $I^2C$: 2 channels/UART (UART supporting LIN-bus): 1 channel<br>[48-pin, 52-pin products]<br>• CSI: 2 channels/simplified $I^2C$: 2 channels/UART: 1 channel<br>• CSI: 1 channel/simplified $I^2C$: 1 channel/UART: 1 channel<br>• CSI: 2 channels/simplified $I^2C$: 2 channels/UART (UART supporting LIN-bus): 1 channel<br>[64-pin products]<br>• CSI: 2 channels/simplified $I^2C$: 2 channels/UART: 1 channel<br>• CSI: 2 channels/simplified $I^2C$: 2 channels/UART: 1 channel<br>• CSI: 2 channels/simplified $I^2C$: 2 channels/UART (UART supporting LIN-bus): 1 channel | | | | | | | | | |
| | $I^2C$ bus | 1 channel | | 1 channel | | 1 channel | | 1 channel | | 1 channel | |
| Multiplier and divider/multiply-accumulator | | • 16 bits × 16 bits = 32 bits (Unsigned or signed)<br>• 32 bits ÷ 32 bits = 32 bits (Unsigned)<br>• 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | | | | | | | | |
| DMA controller | | 2 channels | | | | | | | | | |
| Vectored interrupt sources | Internal | 27 | | 27 | | 27 | | 27 | | 27 | |
| | External | 7 | | 7 | | 10 | | 12 | | 13 | |
| Key interrupt | | 4 | | 4 | | 6 | | 8 | | 8 | |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | | | | | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 V (TYP.)<br>• Power-down-reset: 1.50 V (TYP.) | | | | | | | | | |
| Voltage detector | | • Rising edge : 1.67 V to 4.06 V (14 stages)<br>• Falling edge : 1.63 V to 3.98 V (14 stages) | | | | | | | | | |
| On-chip debug function | | Provided | | | | | | | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | | | | | | | | | |
| Operating ambient temperature | | $T_A$ = 40 to +85°C (A: Consumer applications, D: Industrial applications)<br>$T_A$ = 40 to +105°C (G: Industrial applications) | | | | | | | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin, 128-pin products]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.**

(1/2)

| Item | | 80-pin | | 100-pin | | 128-pin | |
|---|---|---|---|---|---|---|---|
| | | R5F100Mx | R5F101Mx | R5F100Px | R5F101Px | R5F100Sx | R5F101Sx |
| Code flash memory (KB) | | 96 to 512 | | 96 to 512 | | 192 to 512 | |
| Data flash memory (KB) | | 8 | – | 8 | – | 8 | – |
| RAM (KB) | | 8 to 32 Note 1 | | 8 to 32 Note 1 | | 16 to 32 Note 1 | |
| Address space | | 1 MB | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)<br>32.768 kHz | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | |
| General-purpose register | | (8-bit register × 8) × 4 banks | | | | | |
| Minimum instruction execution time | | 0.03125 µs (High-speed on-chip oscillator: $f_{IH}$ = 32 MHz operation) | | | | | |
| | | 0.05 µs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | |
| | | 30.5 µs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | |
| I/O port | Total | 74 | | 92 | | 120 | |
| | CMOS I/O | 64<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 21) | | 82<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 24) | | 110<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 25) | |
| | CMOS input | 5 | | 5 | | 5 | |
| | CMOS output | 1 | | 1 | | 1 | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | 4 | | 4 | | 4 | |
| Timer | 16-bit timer | 12 channels | | 12 channels | | 16 channels | |
| | Watchdog timer | 1 channel | | 1 channel | | 1 channel | |
| | Real-time clock (RTC) | 1 channel | | 1 channel | | 1 channel | |
| | 12-bit interval timer (IT) | 1 channel | | 1 channel | | 1 channel | |
| | Timer output | 12 channels<br>(PWM outputs: 10 Note 2) | | 12 channels<br>(PWM outputs: 10 Note 2) | | 16 channels<br>(PWM outputs: 14 Note 2) | |
| | RTC output | 1 channel<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | | | | |

**Notes 1.** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xJ, R5F101xJ (x = M, P): Start address FAF00H
R5F100xL, R5F101xL (x = M, P, S): Start address F7F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

**Notes 2.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

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| Item | | 80-pin | | 100-pin | | 128-pin | |
|---|---|---|---|---|---|---|---|
| | | R5F100Mx | R5F101Mx | R5F100Px | R5F101Px | R5F100Sx | R5F101Sx |
| Clock output/buzzer output | | 2 | | 2 | | 2 | |
| | | ● 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>● 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | | | |
| 8/10-bit resolution A/D converter | | 17 channels | | 20 channels | | 26 channels | |
| Serial interface | | [80-pin, 100-pin, 128-pin products]<br>● CSI: 2 channels/simplified $I^2C$: 2 channels/UART: 1 channel<br>● CSI: 2 channels/simplified $I^2C$: 2 channels/UART: 1 channel<br>● CSI: 2 channels/simplified $I^2C$: 2 channels/UART (UART supporting LIN-bus): 1 channel<br>● CSI: 2 channels/simplified $I^2C$: 2 channels/UART: 1 channel | | | | | |
| | $I^2C$ bus | 2 channels | | 2 channels | | 2 channels | |
| Multiplier and divider/multiply-accumulator | | ● 16 bits × 16 bits = 32 bits (Unsigned or signed)<br>● 32 bits ÷ 32 bits = 32 bits (Unsigned)<br>● 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | | | | |
| DMA controller | | 4 channels | | | | | |
| Vectored interrupt sources | Internal | 37 | | 37 | | 41 | |
| | External | 13 | | 13 | | 13 | |
| Key interrupt | | 8 | | 8 | | 8 | |
| Reset | | ● Reset by $\overline{\text{RESET}}$ pin<br>● Internal reset by watchdog timer<br>● Internal reset by power-on-reset<br>● Internal reset by voltage detector<br>● Internal reset by illegal instruction execution Note<br>● Internal reset by RAM parity error<br>● Internal reset by illegal-memory access | | | | | |
| Power-on-reset circuit | | ● Power-on-reset: 1.51 V (TYP.)<br>● Power-down-reset: 1.50 V (TYP.) | | | | | |
| Voltage detector | | ● Rising edge : 1.67 V to 4.06 V (14 stages)<br>● Falling edge : 1.63 V to 3.98 V (14 stages) | | | | | |
| On-chip debug function | | Provided | | | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | | | | | |
| Operating ambient temperature | | $T_A$ = 40 to +85°C (A: Consumer applications, D: Industrial applications )<br>$T_A$ = 40 to +105°C (G: Industrial applications) | | | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

# 2. ELECTRICAL SPECIFICATIONS ($T_A$ = –40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A$ = −40 to +85°C
R5F100xxAxx, R5F101xxAxx

D: Industrial applications $T_A$ = −40 to +85°C
R5F100xxDxx, R5F101xxDxx

G: Industrial applications when $T_A$ = −40 to +105°C products is used in the range of $T_A$ = −40 to +85°C
R5F100xxGxx

**Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. With products not provided with an $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ pin, replace $EV_{DD0}$ and $EV_{DD1}$ with $V_{DD}$, or replace $EV_{SS0}$ and $EV_{SS1}$ with $V_{SS}$.**

**3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product in the RL78/G13 User's Manual.**

## 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C) (1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | –0.5 to +6.5 | V |
| | $EV_{DD0}$, $EV_{DD1}$ | $EV_{DD0}$ = $EV_{DD1}$ | –0.5 to +6.5 | V |
| | $EV_{SS0}$, $EV_{SS1}$ | $EV_{SS0}$ = $EV_{SS1}$ | –0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | –0.3 to +2.8 and –0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | –0.3 to $EV_{DD0}$ +0.3 and –0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | –0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | –0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | –0.3 to $EV_{DD0}$ +0.3 and –0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{O2}$ | P20 to P27, P150 to P156 | –0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI26 | –0.3 to $EV_{DD0}$ +0.3 and –0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0 to ANI14 | –0.3 to $V_{DD}$ +0.3 and –0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |

**Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed $AV_{REF}$(+) + 0.3 V in case of A/D conversion target pin.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}$(+) : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | –40 | mA |
| | | Total of all pins –170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | –70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | –100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27, P150 to P156 | –0.5 | mA |
| | | Total of all pins | | –2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 40 | mA |
| | | Total of all pins 170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | –40 to +85 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 oscillator characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)Note | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | 1.0 | | 4.0 | MHz |
| XT1 clock oscillation frequency ($f_X$)Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G13 User's Manual.

### 2.2.2 On-chip oscillator characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | –20 to +85°C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | –1.0 | | +1.0 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | –5.0 | | +5.0 | % |
| | | –40 to –20°C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | –1.5 | | +1.5 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | –5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | –15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | –10.0 Note 2 | mA |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | –55.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | –10.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | –5.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | –2.5 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | –80.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | –19.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | –10.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | –5.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | –135.0 Note 4 | mA |
| | $I_{OH2}$ | Per pin for P20 to P27, P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | | –0.1 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | | –1.5 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $EV_{DD0}$, $EV_{DD1}$, $V_{DD}$ pins to an output pin.

**2.** However, do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx, R5F100xxGxx) is –100 mA.

**Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | | | | 20.0 Note 2 | mA |
| | | Per pin for P60 to P63 | | | | 15.0 Note 2 | mA |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 70.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 15.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 9.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 4.5 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 80.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 35.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 20.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 10.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 150.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27, P150 to P156 | | | | 0.4 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | | 5.0 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS0}$, $EV_{SS1}$ and $V_{SS}$ pin.

**2.** However, do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | 0.8$EV_{DD0}$ | | $EV_{DD0}$ | V |
| | $V_{IH2}$ | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 2.2 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 2.0 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 1.6 V ≤ $EV_{DD0}$ < 3.3 V | 1.5 | | $EV_{DD0}$ | V |
| | $V_{IH3}$ | P20 to P27, P150 to P156 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60 to P63 | | 0.7$EV_{DD0}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | 0 | | 0.2$EV_{DD0}$ | V |
| | $V_{IL2}$ | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 1.6 V ≤ $EV_{DD0}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P27, P150 to P156 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60 to P63 | | 0 | | 0.3$EV_{DD0}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is $EV_{DD0}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –10.0 mA | $EV_{DD0}$ – 1.5 | | | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $EV_{DD0}$ – 0.7 | | | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $EV_{DD0}$ – 0.6 | | | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $EV_{DD0}$ – 0.5 | | | V |
| | | | 1.6 V ≤ $EV_{DD0}$ < 5.5 V, $I_{OH1}$ = –1.0 mA | $EV_{DD0}$ – 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27, P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = –100 µA | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 20 mA | | | 1.3 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $EV_{DD0}$ < 5.5 V, $I_{OL1}$ = 0.3 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27, P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 µA | | | 0.4 | V |
| | $V_{OL3}$ | P60 to P63 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $EV_{DD0}$ < 5.5 V, $I_{OL3}$ = 1.0 mA | | | 0.4 | V |

**Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I$ = $EV_{DD0}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P27, P137, P150 to P156, $\overline{RESET}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I$ = $EV_{SS0}$ | | | | –1 | μA |
| | $I_{LIL2}$ | P20 to P27, P137, P150 to P156, $\overline{RESET}$ | $V_I$ = $V_{SS}$ | | | | –1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | –1 | μA |
| | | | | In resonator connection | | | –10 | μA |
| On-chip pll-up resistance | $R_U$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I$ = $EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 2.3.2 Supply current characteristics

#### (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 4.6 | 7.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.6 | 7.0 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.5 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.7 | 4.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.7 | 4.0 | mA |
| | | | LS (low-speed main) mode Note 5 | $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.2 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.2 | 1.8 | mA |
| | | | LV (low-voltage main) mode Note 5 | $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.2 | 1.7 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.2 | 1.7 | mA |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.0 | 4.6 | mA |
| | | | | | | Resonator connection | | 3.2 | 4.8 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.0 | 4.6 | mA |
| | | | | | | Resonator connection | | 3.2 | 4.8 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 1.9 | 2.7 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.7 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.9 | 2.7 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.7 | mA |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | mA |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = –40°C | Normal operation | Square wave input | | 4.1 | 4.9 | µA |
| | | | | | | Resonator connection | | 4.2 | 5.0 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.1 | 4.9 | µA |
| | | | | | | Resonator connection | | 4.2 | 5.0 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.2 | 5.5 | µA |
| | | | | | | Resonator connection | | 4.3 | 5.6 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.3 | 6.3 | µA |
| | | | | | | Resonator connection | | 4.4 | 6.4 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 4.6 | 7.7 | µA |
| | | | | | | Resonator connection | | 4.7 | 7.8 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.54 | 1.63 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.54 | 1.63 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.44 | 1.28 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 1.28 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.40 | 1.00 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.40 | 1.00 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 530 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 530 | µA |
| | | | LV (low-voltage main) mode Note 7 | $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 640 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 640 | µA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 330 | µA |
| | | | | | Resonator connection | | 145 | 380 | µA |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 95 | 330 | µA |
| | | | | | Resonator connection | | 145 | 380 | µA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = –40°C | Square wave input | | 0.25 | 0.57 | µA |
| | | | | | Resonator connection | | 0.44 | 0.76 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | µA |
| | | | | | Resonator connection | | 0.49 | 0.76 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.37 | 1.17 | µA |
| | | | | | Resonator connection | | 0.56 | 1.36 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.53 | 1.97 | µA |
| | | | | | Resonator connection | | 0.72 | 2.16 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 0.82 | 3.37 | µA |
| | | | | | Resonator connection | | 1.01 | 3.56 | µA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = –40°C | | | | 0.18 | 0.50 | µA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | µA |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | µA |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | µA |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | | 2.3 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | | 2.3 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | | 5.2 | 8.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | | 5.2 | 8.5 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | | 4.1 | 6.6 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | | 4.1 | 6.6 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | | 3.0 | 4.7 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | | 3.0 | 4.7 | mA |
| | | | LS (low-speed main) mode Note 5 | $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | | 1.3 | 2.1 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | | 1.3 | 2.1 | mA |
| | | | LV (low-voltage main) mode Note 5 | $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | | 1.3 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | | 1.3 | 1.8 | mA |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | | 3.4 | 5.5 | mA |
| | | | | | | Resonator connection | | | 3.6 | 5.7 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | | 3.4 | 5.5 | mA |
| | | | | | | Resonator connection | | | 3.6 | 5.7 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | | 2.1 | 3.2 | mA |
| | | | | | | Resonator connection | | | 2.1 | 3.2 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | | 2.1 | 3.2 | mA |
| | | | | | | Resonator connection | | | 2.1 | 3.2 | mA |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | | 1.2 | 2.0 | mA |
| | | | | | | Resonator connection | | | 1.2 | 2.0 | mA |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | | 1.2 | 2.0 | mA |
| | | | | | | Resonator connection | | | 1.2 | 2.0 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = –40°C | Normal operation | Square wave input | | | 4.8 | 5.9 | µA |
| | | | | | | Resonator connection | | | 4.9 | 6.0 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | | 4.9 | 5.9 | µA |
| | | | | | | Resonator connection | | | 5.0 | 6.0 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | | 5.0 | 7.6 | µA |
| | | | | | | Resonator connection | | | 5.1 | 7.7 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | | 5.2 | 9.3 | µA |
| | | | | | | Resonator connection | | | 5.3 | 9.4 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | | 5.7 | 13.3 | µA |
| | | | | | | Resonator connection | | | 5.8 | 13.4 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 1.86 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 1.86 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.50 | 1.45 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 1.45 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.44 | 1.11 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 1.11 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 290 | 620 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 290 | 620 | µA |
| | | | LV (low-voltage main) mode Note 7 | $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 440 | 680 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 440 | 680 | µA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 1.08 | mA |
| | | | | | Resonator connection | | 0.48 | 1.28 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 1.08 | mA |
| | | | | | Resonator connection | | 0.48 | 1.28 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 0.63 | mA |
| | | | | | Resonator connection | | 0.28 | 0.71 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 0.63 | mA |
| | | | | | Resonator connection | | 0.28 | 0.71 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 360 | µA |
| | | | | | Resonator connection | | 160 | 420 | µA |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 360 | µA |
| | | | | | Resonator connection | | 160 | 420 | µA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = –40°C | Square wave input | | 0.28 | 0.61 | µA |
| | | | | | Resonator connection | | 0.47 | 0.80 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.34 | 0.61 | µA |
| | | | | | Resonator connection | | 0.53 | 0.80 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.41 | 2.30 | µA |
| | | | | | Resonator connection | | 0.60 | 2.49 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.64 | 4.03 | µA |
| | | | | | Resonator connection | | 0.83 | 4.22 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 1.09 | 8.04 | µA |
| | | | | | Resonator connection | | 1.28 | 8.23 | µA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = –40°C | | | | 0.19 | 0.52 | µA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.52 | µA |
| | | | $T_A$ = +50°C | | | | 0.32 | 2.21 | µA |
| | | | $T_A$ = +70°C | | | | 0.55 | 3.94 | µA |
| | | | $T_A$ = +85°C | | | | 1.00 | 7.95 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 6.1 | 9.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 6.1 | 9.5 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 7.4 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 7.4 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.5 | 5.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.5 | 5.3 | mA |
| | | | LS (low-speed main) mode Note 5 | $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.5 | 2.3 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.5 | 2.3 | mA |
| | | | LV (low-voltage main) mode Note 5 | $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.5 | 2.0 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.5 | 2.0 | mA |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.9 | 6.1 | mA |
| | | | | | | Resonator connection | | 4.1 | 6.3 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.9 | 6.1 | mA |
| | | | | | | Resonator connection | | 4.1 | 6.3 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.5 | 3.7 | mA |
| | | | | | | Resonator connection | | 2.5 | 3.7 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.5 | 3.7 | mA |
| | | | | | | Resonator connection | | 2.5 | 3.7 | mA |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.4 | 2.2 | mA |
| | | | | | | Resonator connection | | 1.4 | 2.2 | mA |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.4 | 2.2 | mA |
| | | | | | | Resonator connection | | 1.4 | 2.2 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = –40°C | Normal operation | Square wave input | | 5.4 | 6.5 | µA |
| | | | | | | Resonator connection | | 5.5 | 6.6 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 5.5 | 6.5 | µA |
| | | | | | | Resonator connection | | 5.6 | 6.6 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.6 | 9.4 | µA |
| | | | | | | Resonator connection | | 5.7 | 9.5 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.9 | 12.0 | µA |
| | | | | | | Resonator connection | | 6.0 | 12.1 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.6 | 16.3 | µA |
| | | | | | | Resonator connection | | 6.7 | 16.4 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V @1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 1.89 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 1.89 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.50 | 1.48 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 1.48 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.44 | 1.12 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 1.12 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 290 | 620 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 290 | 620 | µA |
| | | | LV (low-voltage main) mode Note 7 | $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 460 | 700 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 460 | 700 | µA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 1.14 | mA |
| | | | | | Resonator connection | | 0.48 | 1.34 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 1.14 | mA |
| | | | | | Resonator connection | | 0.48 | 1.34 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 0.68 | mA |
| | | | | | Resonator connection | | 0.28 | 0.76 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 0.68 | mA |
| | | | | | Resonator connection | | 0.28 | 0.76 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 390 | µA |
| | | | | | Resonator connection | | 160 | 450 | µA |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 390 | µA |
| | | | | | Resonator connection | | 160 | 450 | µA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = –40°C | Square wave input | | 0.31 | 0.66 | µA |
| | | | | | Resonator connection | | 0.50 | 0.85 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.38 | 0.66 | µA |
| | | | | | Resonator connection | | 0.57 | 0.85 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.47 | 3.49 | µA |
| | | | | | Resonator connection | | 0.66 | 3.68 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.80 | 6.10 | µA |
| | | | | | Resonator connection | | 0.99 | 6.29 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 1.52 | 10.46 | µA |
| | | | | | Resonator connection | | 1.71 | 10.65 | µA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = –40°C | | | | 0.19 | 0.54 | µA |
| | | | $T_A$ = +25°C | | | | 0.26 | 0.54 | µA |
| | | | $T_A$ = +50°C | | | | 0.35 | 3.37 | µA |
| | | | $T_A$ = +70°C | | | | 0.68 | 5.98 | µA |
| | | | $T_A$ = +85°C | | | | 1.40 | 10.34 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V @1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (4) Peripheral Functions (Common to all products)

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | µA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | µA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | µA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | 0.22 | | µA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75.0 | | µA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | µA |
| LVD operating current | $I_{LVI}$ Notes 1, 7 | | | | 0.08 | | µA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.50 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 8 | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

**Notes 1.** Current flowing to $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Notes 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**8.** Current flowing only during data flash rewrite.

**9.** Current flowing only during self programming.

**10.** For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13 User's Manual**.**

**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 2.4 AC Characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | µs |
| | | | LV (low-voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | µs |
| | | Subsystem clock ($f_{SUB}$) operation | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | µs |
| | | In the self programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | µs |
| | | | LV (low-voltage main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | µs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 1.0 | | 4.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 60 | | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 120 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | µs |
| TI00 to TI07, TI10 to TI17 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$+10 | | | ns[Note] |
| TO00 to TO07, TO10 to TO17 output frequency | $f_{TO}$ | HS (high-speed main) mode | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LS (low-speed main) mode | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LV (low-voltage main) mode | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 2 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LS (low-speed main) mode | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LV (low-voltage main) mode | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | | µs |
| | | INTP1 to INTP11 | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR7 | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | | ns |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 1 | | | µs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | | 10 | | | µs |

(**Note** and **Remark** are listed on the next page.)

**Note** The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$

1.8 V ≤ $EV_{DD0}$ < 2.7 V : MIN. 125 ns

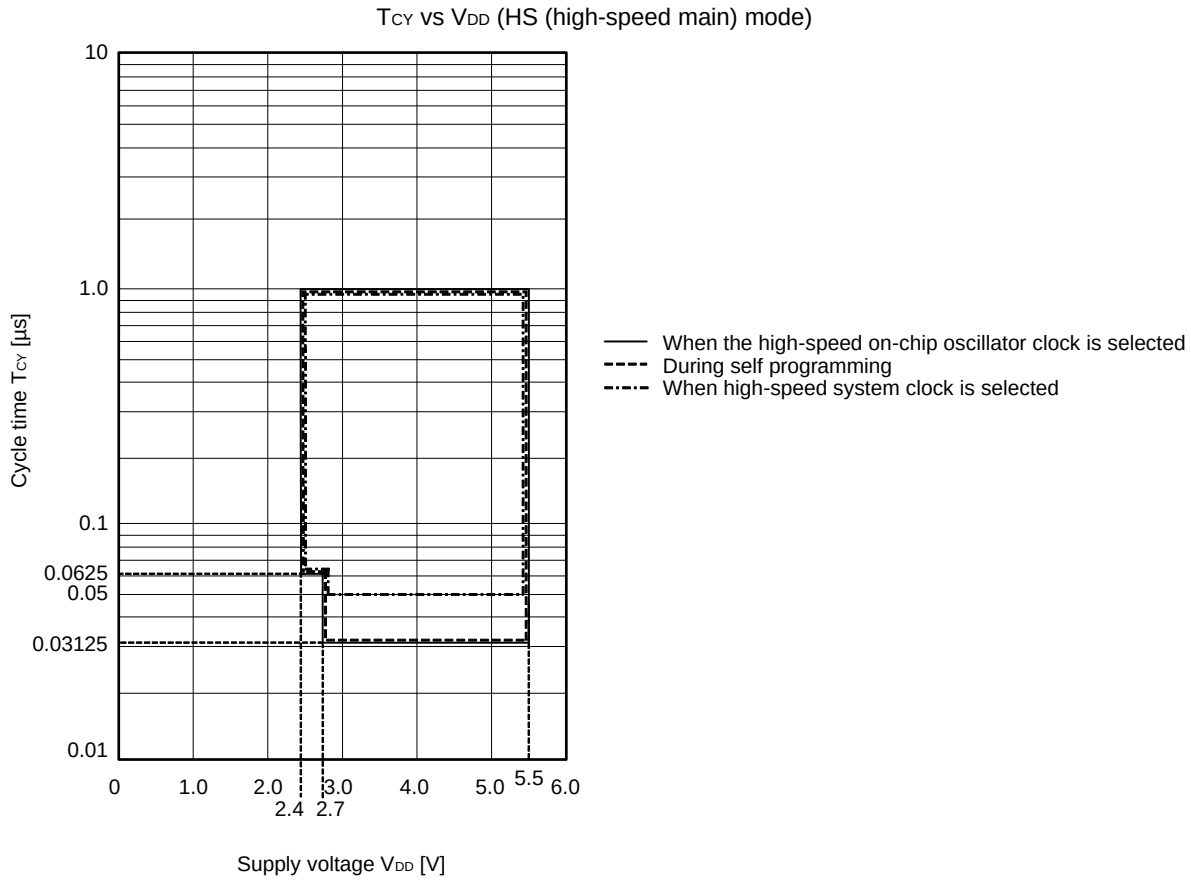
1.6 V ≤ $EV_{DD0}$ < 1.8 V : MIN. 250 ns

**Remark** $f_{MCK}$: Timer array unit operation clock frequency

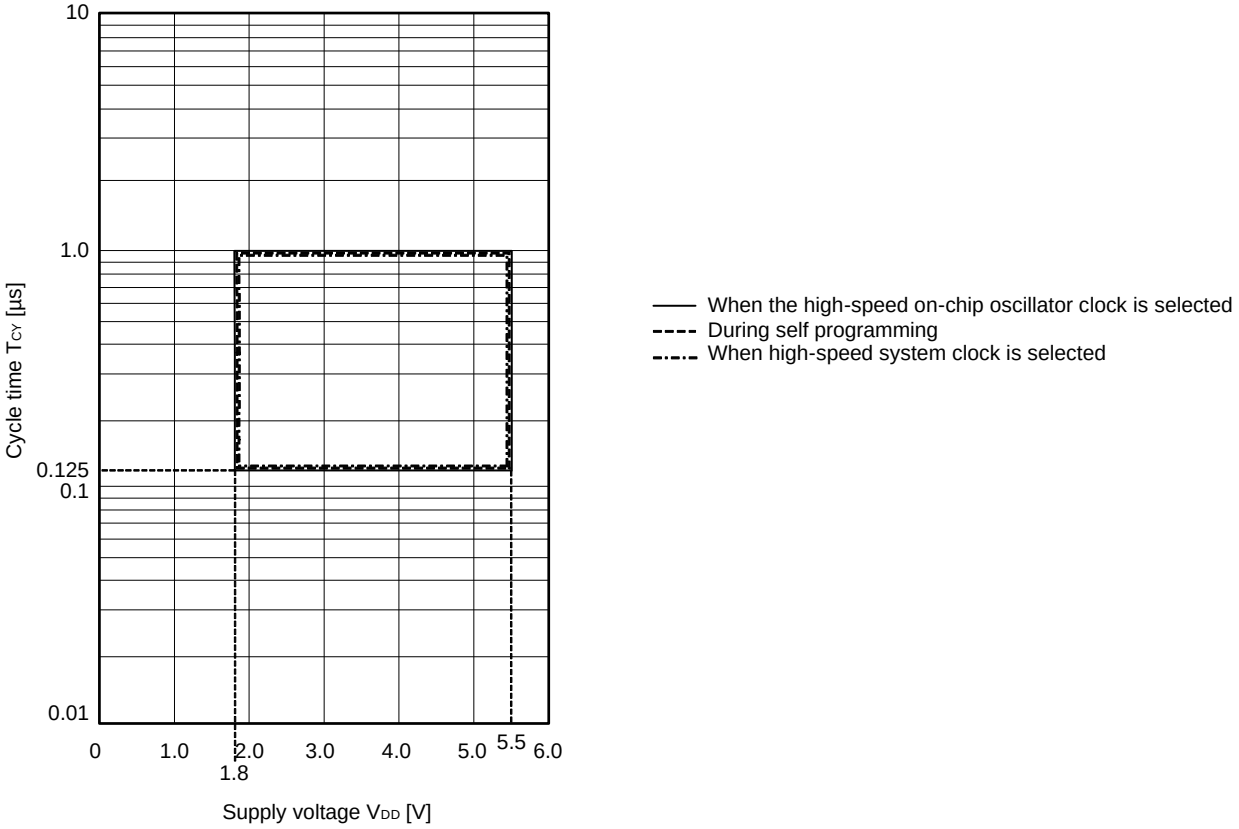
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

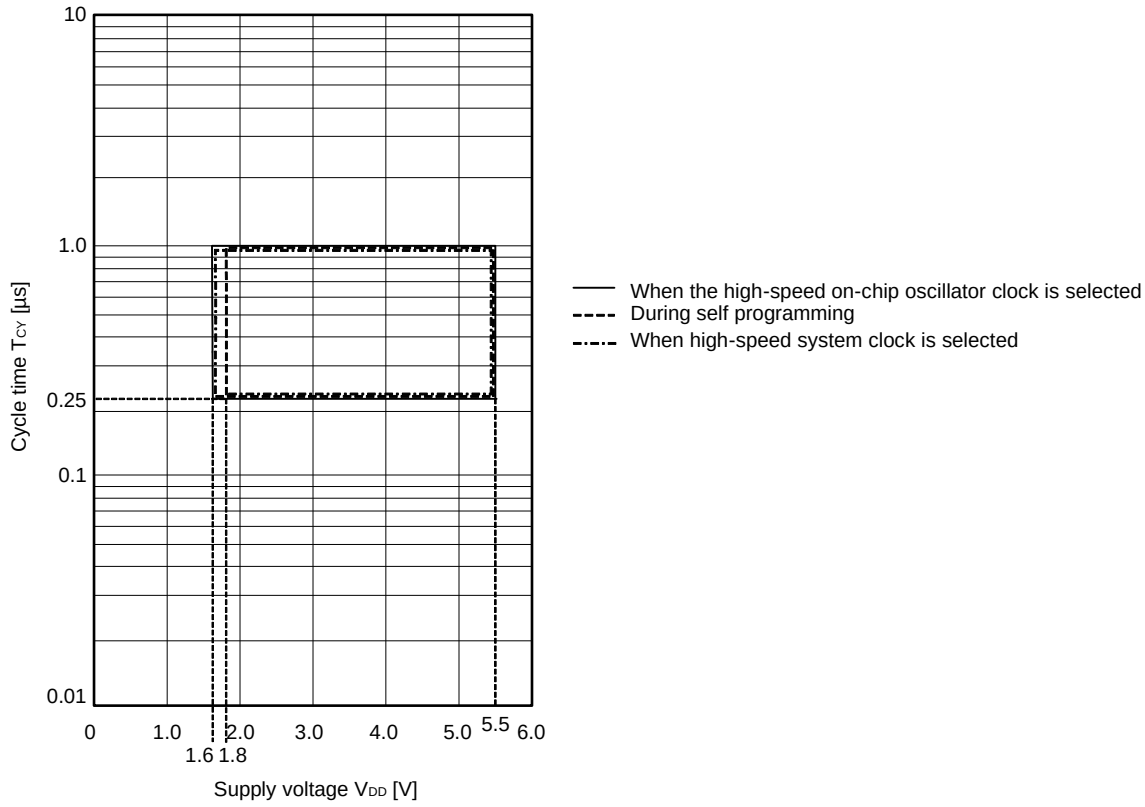
**Minimum Instruction Execution Time during Main System Clock Operation**



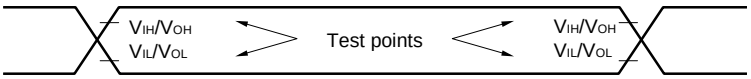
$T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)



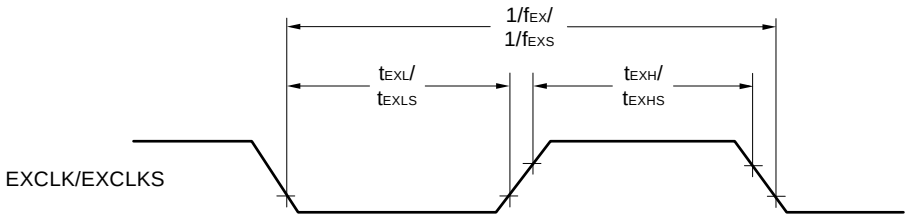

$T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)



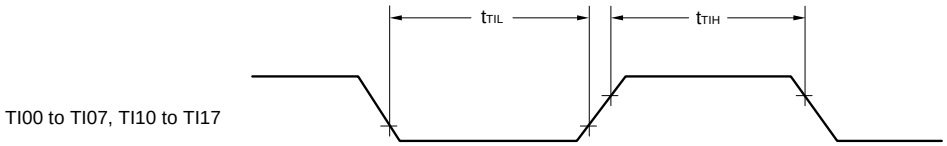
### AC Timing Test Points

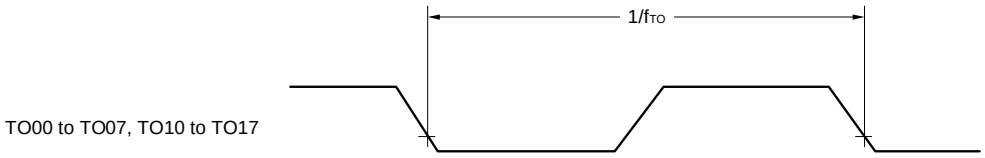



### External System Clock Timing

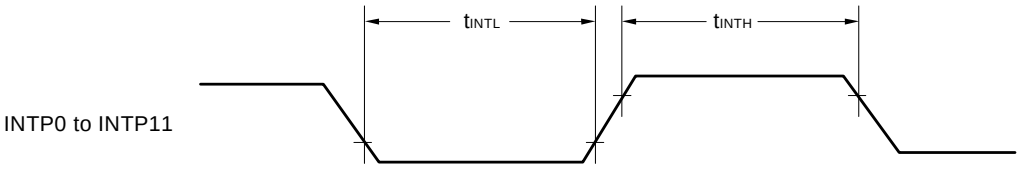



### TI/TO Timing

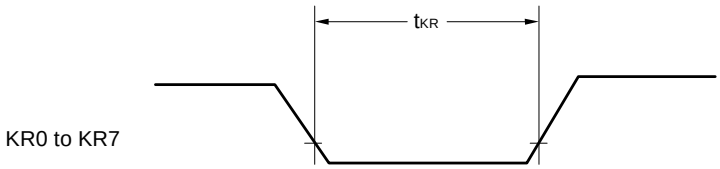


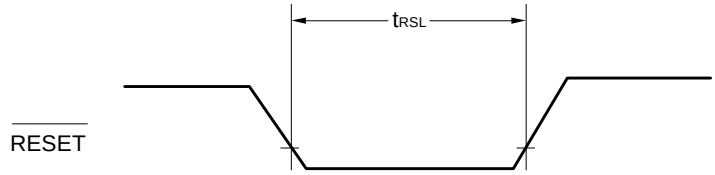

### Interrupt Request Input Timing




### Key Interrupt Input Timing

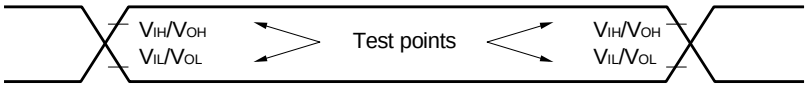



### $\overline{\text{RESET}}$ Input Timing



## 2.5 Peripheral Functions Characteristics

### AC Timing Test Points




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | – | | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | – | | | 1.3 | | 0.6 | Mbps |

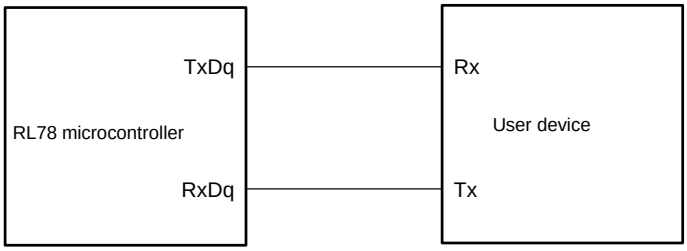
**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps
1.6 V ≤ $EV_{DD0}$ < 1.8 V : MAX. 0.6 Mbps

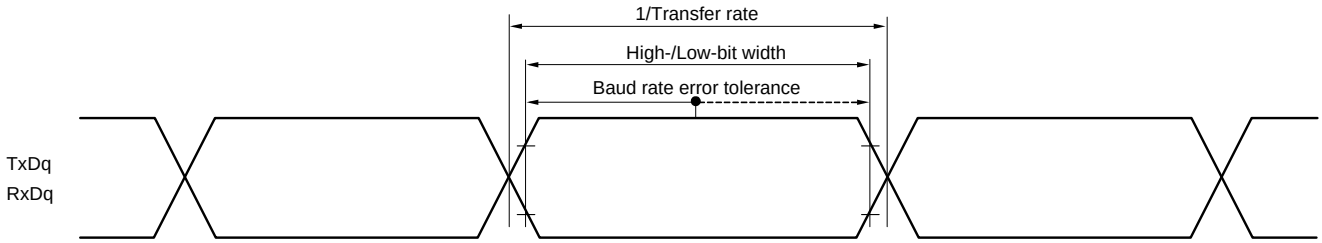
**3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 2/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 62.5 | | 250 | | 500 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 83.3 | | 250 | | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 7 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 10 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 23 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 20 pF Note 4 | | | 10 | | 10 | | 10 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** This value is valid only when CSI00’s peripheral I/O redirect function is not used.

**2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 125 | | 500 | | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 500 | | 1000 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | 500 | | 1000 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1000 | | 1000 | | 1000 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | – | | 1000 | | 1000 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 12 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 18 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 38 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 110 | | 110 | | 110 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 220 | | 220 | | 220 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 220 | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 19 | | 19 | | 19 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | 25 | | 25 | | 25 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | – | | 25 | | 25 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)**
**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | – | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | – | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 750 | | 6/$f_{MCK}$ and 750 | | 6/$f_{MCK}$ and 750 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 7 | | $t_{KCY2}$/2 – 7 | | $t_{KCY2}$/2 – 7 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 8 | | $t_{KCY2}$/2 – 8 | | $t_{KCY2}$/2 – 8 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 18 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 66 | | $t_{KCY2}$/2 – 66 | | $t_{KCY2}$/2 – 66 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | $t_{KCY2}$/2 – 66 | | $t_{KCY2}$/2 – 66 | | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+20 | | 1/$f_{MCK}$+30 | | 1/$f_{MCK}$+30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+30 | | 1/$f_{MCK}$+30 | | 1/$f_{MCK}$+30 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+40 | | 1/$f_{MCK}$+40 | | 1/$f_{MCK}$+40 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 1/$f_{MCK}$+40 | | 1/$f_{MCK}$+40 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+31 | | 1/$f_{MCK}$+31 | | 1/$f_{MCK}$+31 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+250 | | 1/$f_{MCK}$+250 | | 1/$f_{MCK}$+250 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 1/$f_{MCK}$+250 | | 1/$f_{MCK}$+250 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$+44 | | 2/$f_{MCK}$+110 | | 2/$f_{MCK}$+110 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$+75 | | 2/$f_{MCK}$+110 | | 2/$f_{MCK}$+110 | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$+110 | | 2/$f_{MCK}$+110 | | 2/$f_{MCK}$+110 | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$+220 | | 2/$f_{MCK}$+220 | | 2/$f_{MCK}$+220 | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 2/$f_{MCK}$+220 | | 2/$f_{MCK}$+220 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

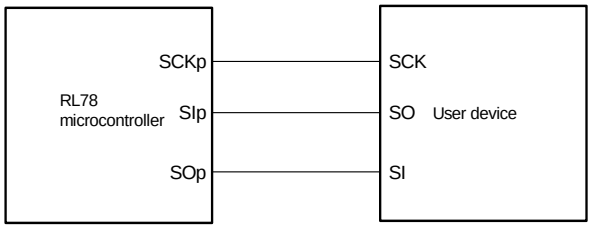
**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

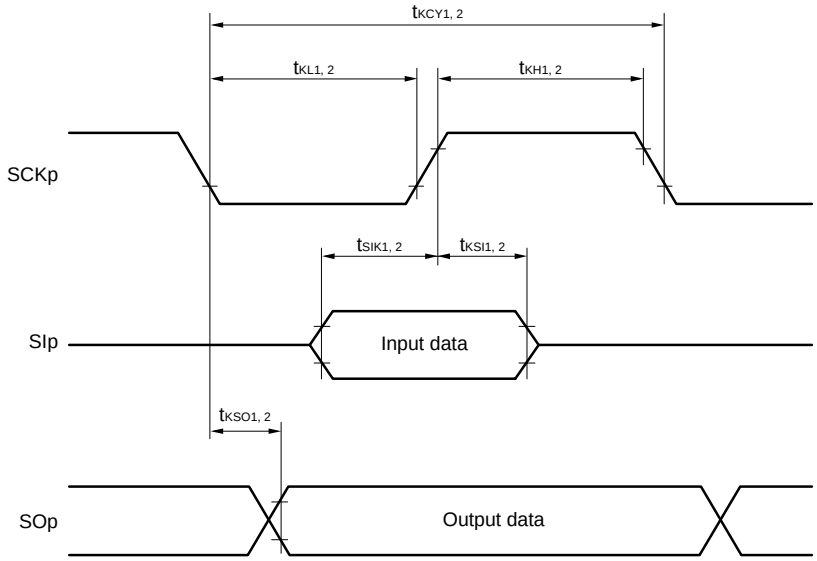
**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

**2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

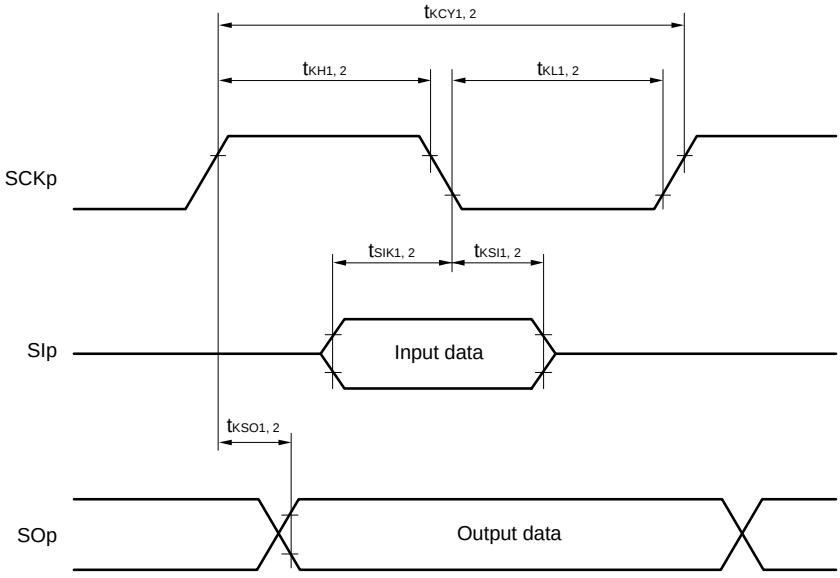
**CSI mode connection diagram (during communication at same potential)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

**2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**(5) During communication at same potential (simplified $I^2C$ mode) (1/2)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 400 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 250 Note 1 | | 250 Note 1 | | 250 Note 1 | kHz |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | – | | 250 Note 1 | | 250 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | – | | 1850 | | 1850 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | – | | 1850 | | 1850 | | ns |

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

**(5) During communication at same potential (simplified $I^2C$ mode) (2/2)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 85 Note2 | | $1/f_{MCK}$ + 145 Note2 | | $1/f_{MCK}$ + 145 Note2 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | $1/f_{MCK}$ + 145 Note2 | | $1/f_{MCK}$ + 145 Note2 | | $1/f_{MCK}$ + 145 Note2 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | $1/f_{MCK}$ + 230 Note2 | | $1/f_{MCK}$ + 230 Note2 | | $1/f_{MCK}$ + 230 Note2 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | $1/f_{MCK}$ + 290 Note2 | | $1/f_{MCK}$ + 290 Note2 | | $1/f_{MCK}$ + 290 Note2 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | – | | $1/f_{MCK}$ + 290 Note2 | | $1/f_{MCK}$ + 290 Note2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | – | | 0 | 405 | 0 | 405 | ns |

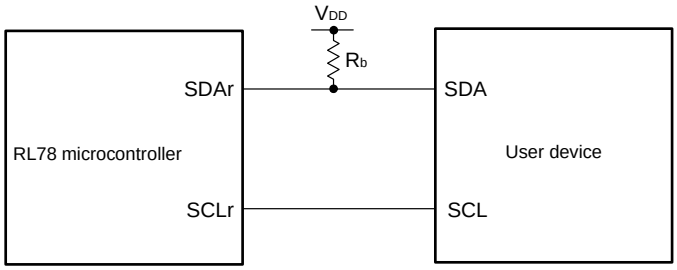
**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

**2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

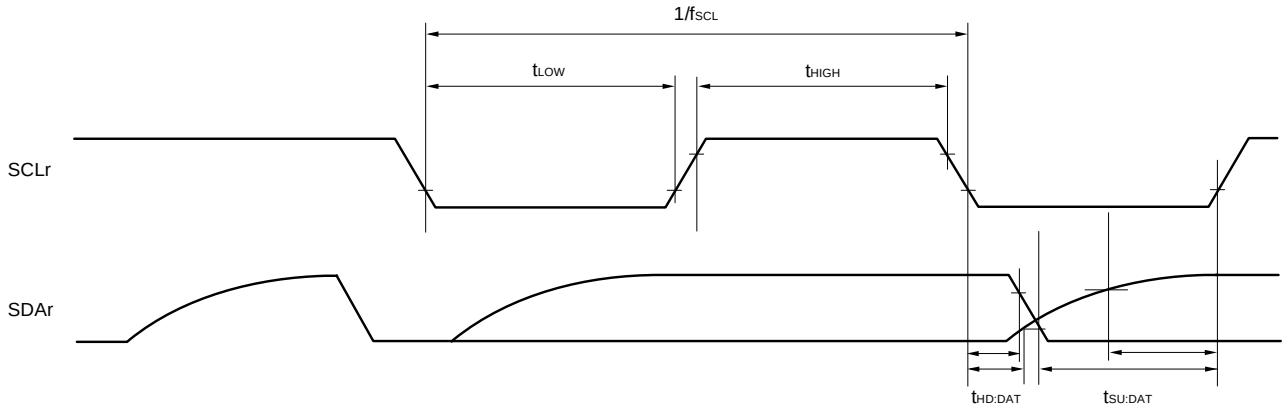
**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**Simplified I²C mode mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remarks 1.** $R_b$[Ω]:Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | Reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/6 Notes 1 to 3 | | $f_{MCK}$/6 Notes 1, 2 | | $f_{MCK}$/6 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**3.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps

**4.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | Transmission | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | **Note 1** | | **Note 1** | | **Note 1** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.8 Note 2 | | 2.8 Note 2 | | 2.8 Note 2 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | **Note 3** | | **Note 3** | | **Note 3** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 4 | | 1.2 Note 4 | | 1.2 Note 4 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | **Notes 5, 6** | | **Notes 5, 6** | | **Notes 5, 6** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 7 | | 0.43 Note 7 | | 0.43 Note 7 | Mbps |

**Notes 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**2.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**Notes 3.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**5.** Use it with $EV_{DD0} \geq V_b$.

**6.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

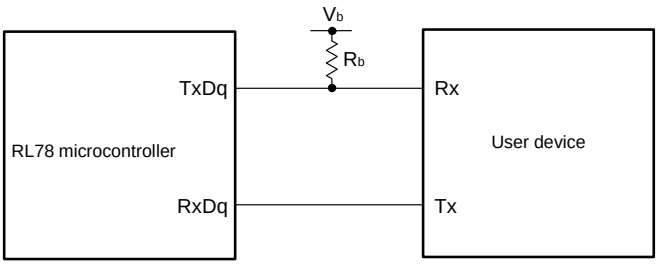
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

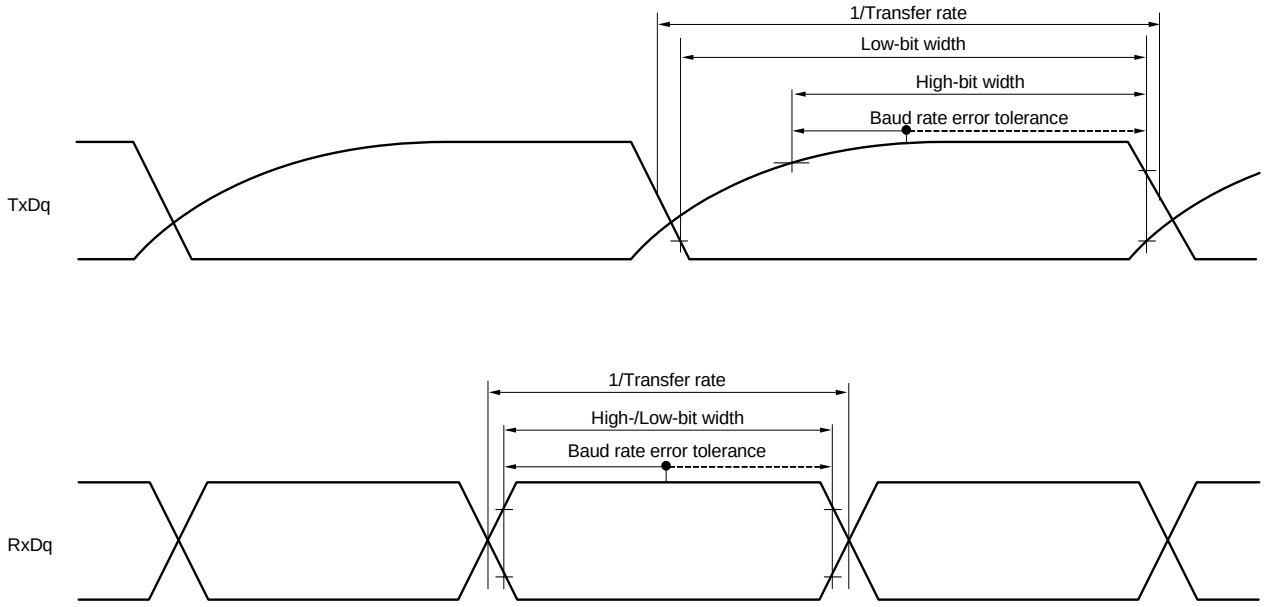
**7.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**



**UART mode bit width (during communication at different potential) (reference)**




**Remarks 1.** $R_b$[Ω]:Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 2/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | 1150 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 7 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 10 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | | 60 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | | 130 | ns |

(**Notes, Caution,** and **Remarks** are listed on the next page.)

**(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 23 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | 10 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $R_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**4.** This value is valid only when CSI00's peripheral I/O redirect function is not used.

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | 1150 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | 1150 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 75 | | $t_{KCY1}$/2 – 75 | | $t_{KCY1}$/2 – 75 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 170 | | $t_{KCY1}$/2 – 170 | | $t_{KCY1}$/2 – 170 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 – 458 | | $t_{KCY1}$/2 – 458 | | $t_{KCY1}$/2 – 458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 12 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 18 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |

**Note** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(Remarks** are listed two pages after the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 81 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | 479 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 100 | | 100 | | 100 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 195 | | 195 | | 195 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 483 | | 483 | | 483 | ns |

**Notes** **1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(Remarks** are listed on the page after the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

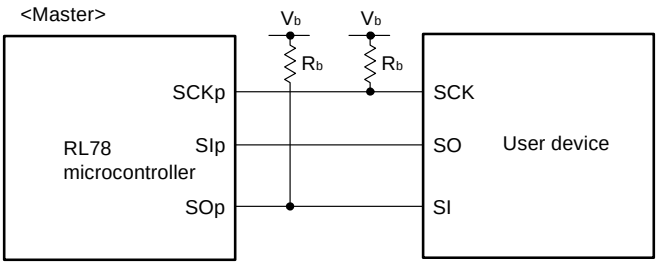
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 25 | | 25 | | 25 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | | 25 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | | 25 | ns |

**Notes** **1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
**2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**



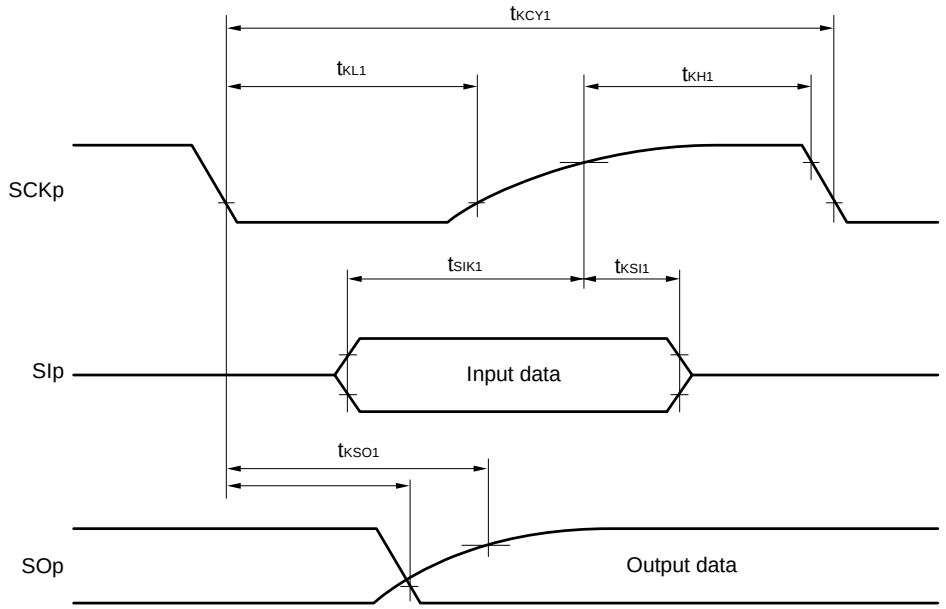

**Remarks 1.** $R_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number , n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

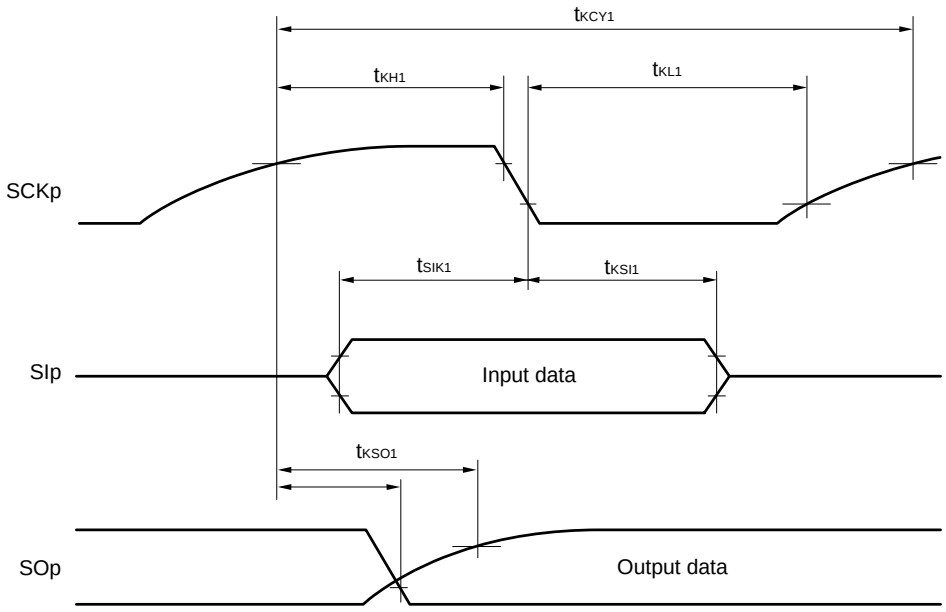
**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

**4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

**2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 14/ $f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/ $f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/ $f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/ $f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/ $f_{MCK}$ | | 10/ $f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 20/ $f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/ $f_{MCK}$ | | – | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/ $f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/ $f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/ $f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/ $f_{MCK}$ | | 10/ $f_{MCK}$ | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 24 MHz < $f_{MCK}$ | 48/ $f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/ $f_{MCK}$ | | – | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/ $f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/ $f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/ $f_{MCK}$ | | 16/ $f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/ $f_{MCK}$ | | 10/ $f_{MCK}$ | | 10/ $f_{MCK}$ | | ns |

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | $t_{KCY2}$/2 – 12 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

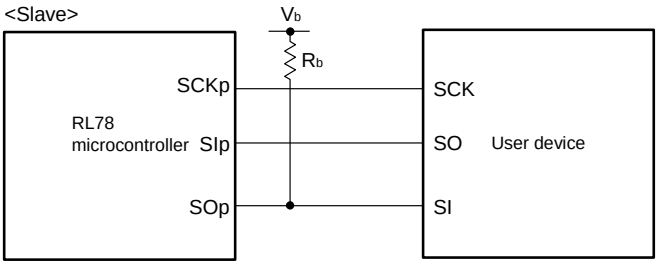
**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**



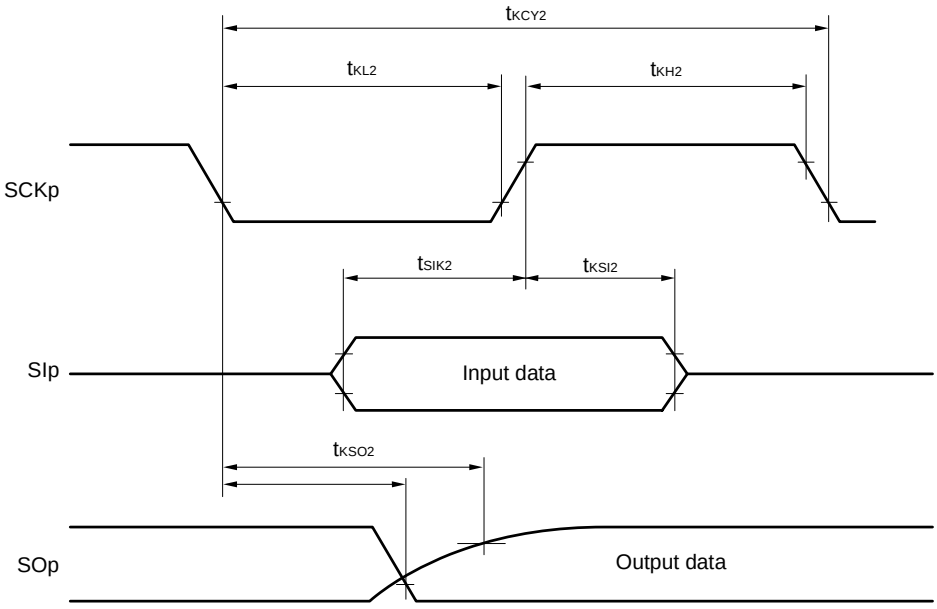

**Remarks 1.** $R_b$[Ω]:Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

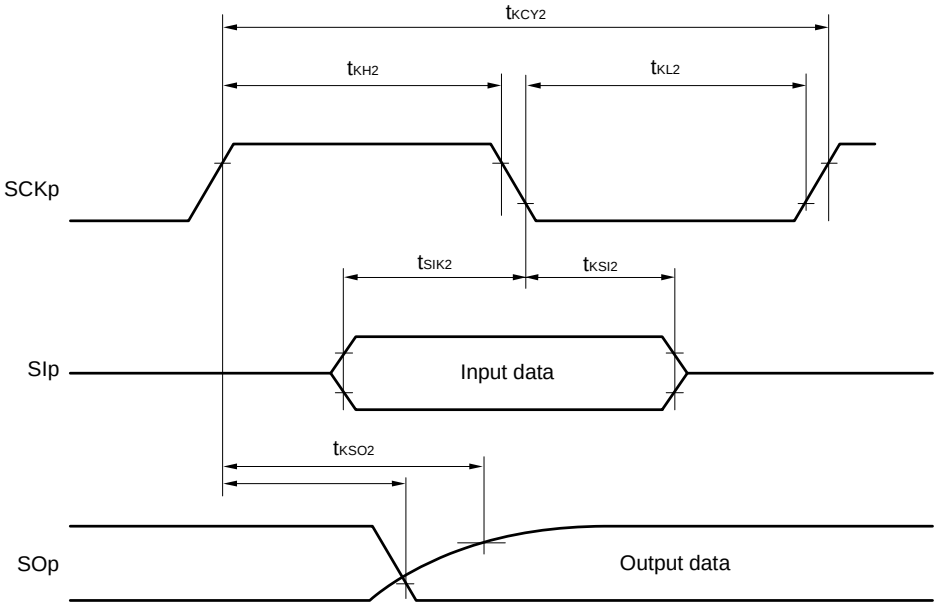
**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

**4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

**2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (1/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 ote 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 245 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | 610 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 675 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | 610 | | ns |

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (2/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 135 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 135 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | kHz |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | kHz |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

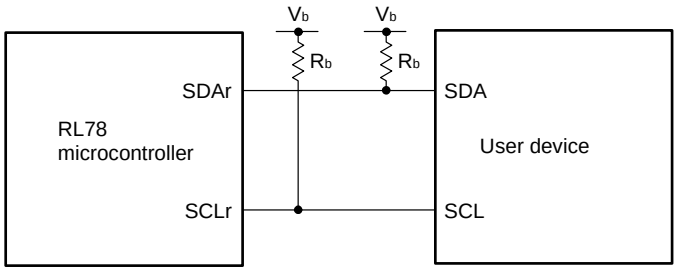
**2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**3.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

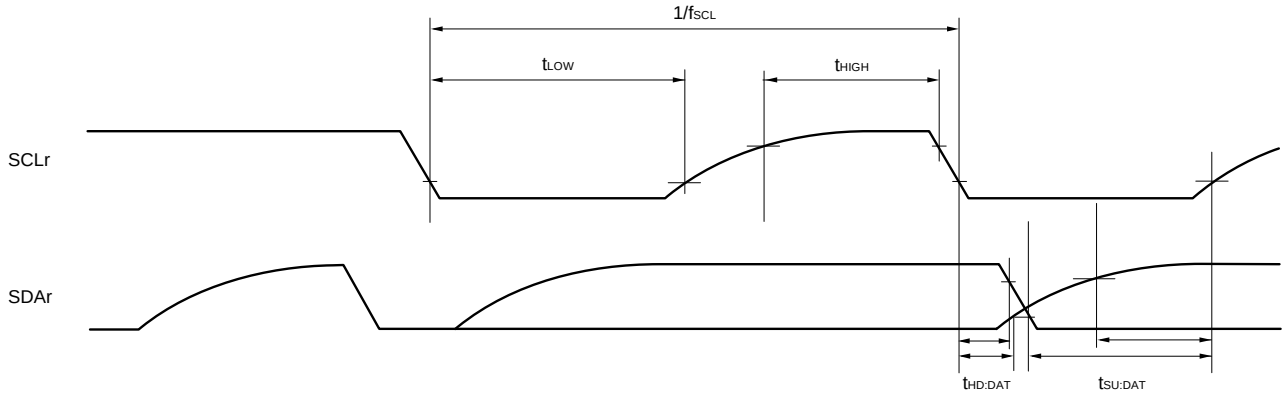
**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified $I^2C$ mode connection diagram (during communication at different potential)**




**Simplified $I^2C$ mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**2.** r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13)

### 2.5.2 Serial interface IICA

#### (1) $I^2C$ standard mode

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode: $f_{CLK}$ ≥ 1 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | – | | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 4.7 | | 4.7 | | µs |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 4.0 | | 4.0 | | µs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 4.7 | | 4.7 | | µs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 4.0 | | 4.0 | | µs |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 250 | | 250 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 0 | 3.45 | 0 | 3.45 | µs |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 4.0 | | 4.0 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | – | | 4.7 | | 4.7 | | µs |

(**Notes**, **Caution** and **Remark** are listed on the next page.)

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

### (2) $I^2C$ fast mode

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | µs |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

### (3) $I^2C$ fast mode plus

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode plus: $f_{CLK}$ ≥ 10 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 1000 | – | | – | | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | – | | – | | µs |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | – | | – | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.5 | | – | | – | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | – | | – | | µs |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 50 | | – | | – | | µs |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.45 | – | | – | | µs |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | – | | – | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.5 | | – | | – | | µs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

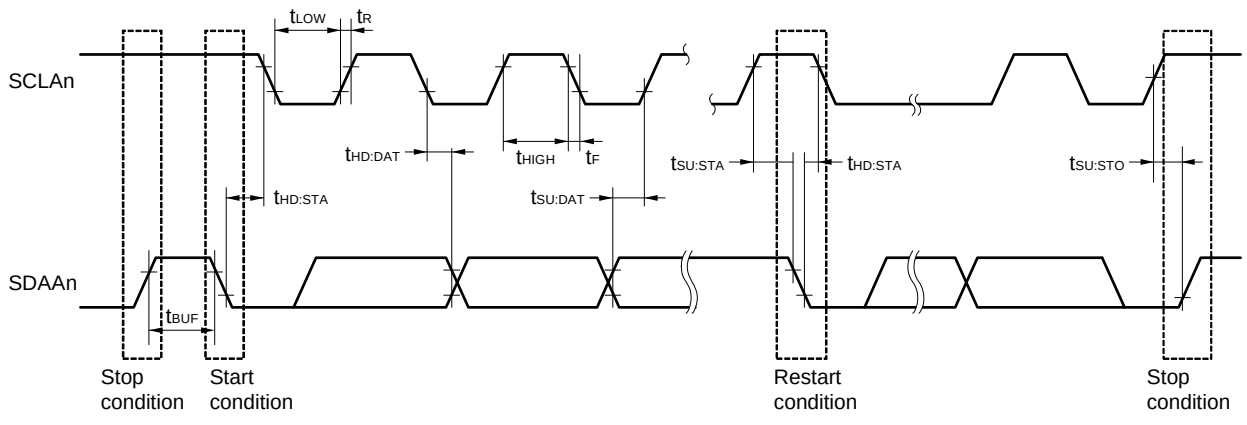
**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: $C_b$ = 120 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**




**Remark** n = 0, 1

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0 to ANI14 | Refer to **2.6.1 (1)**. | Refer to **2.6.1 (3)**. | Refer to **2.6.1 (4)**. |
| ANI16 to ANI26 | Refer to **2.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **2.6.1 (1)**. | | – |

**(1) When reference voltage (+)= $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2 to ANI14 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | µs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±0.50 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±0.50 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±5.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI14 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 5 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 5 | | | V |

(**Notes** are listed on the next page.)

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** Values when the conversion time is set to 57 µs (min.) and 95 µs (max.).

**5.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | 1.2 | ±8.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution Target ANI pin : ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±6.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI26 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**5.** When the conversion time is set to 57 µs (min.) and 95 µs (max.).

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | 1.2 | ±10.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | µs |
| Conversion time | $t_{CONV}$ | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±6.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI14 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI26 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | V |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 4 | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When the conversion time is set to 57 µs (min.) and 95 µs (max.).

**4.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26**

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (–) = $AV_{REFM}$ = 0 V Note 4, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ Note 3 | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

### 2.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode)**

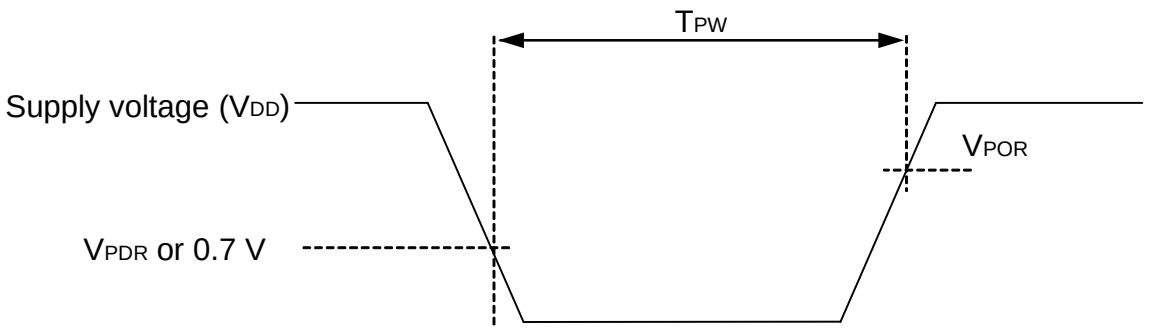
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.6.3 POR circuit characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | The power supply voltage is rising. | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | The power supply voltage is falling. | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width[Note] | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



### 2.6.4 LVD circuit characteristics

#### LVD Detection Voltage of Reset Mode and Interrupt Mode

**($T_A$ = –40 to +85°C, $V_{PDR} \le V_{DD} \le 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVD0}$ | The power supply voltage is rising. | 3.98 | 4.06 | 4.14 | V |
| | | | The power supply voltage is falling. | 3.90 | 3.98 | 4.06 | V |
| | | $V_{LVD1}$ | The power supply voltage is rising. | 3.68 | 3.75 | 3.82 | V |
| | | | The power supply voltage is falling. | 3.60 | 3.67 | 3.74 | V |
| | | $V_{LVD2}$ | The power supply voltage is rising. | 3.07 | 3.13 | 3.19 | V |
| | | | The power supply voltage is falling. | 3.00 | 3.06 | 3.12 | V |
| | | $V_{LVD3}$ | The power supply voltage is rising. | 2.96 | 3.02 | 3.08 | V |
| | | | The power supply voltage is falling. | 2.90 | 2.96 | 3.02 | V |
| | | $V_{LVD4}$ | The power supply voltage is rising. | 2.86 | 2.92 | 2.97 | V |
| | | | The power supply voltage is falling. | 2.80 | 2.86 | 2.91 | V |
| | | $V_{LVD5}$ | The power supply voltage is rising. | 2.76 | 2.81 | 2.87 | V |
| | | | The power supply voltage is falling. | 2.70 | 2.75 | 2.81 | V |
| | | $V_{LVD6}$ | The power supply voltage is rising. | 2.66 | 2.71 | 2.76 | V |
| | | | The power supply voltage is falling. | 2.60 | 2.65 | 2.70 | V |
| | | $V_{LVD7}$ | The power supply voltage is rising. | 2.56 | 2.61 | 2.66 | V |
| | | | The power supply voltage is falling. | 2.50 | 2.55 | 2.60 | V |
| | | $V_{LVD8}$ | The power supply voltage is rising. | 2.45 | 2.50 | 2.55 | V |
| | | | The power supply voltage is falling. | 2.40 | 2.45 | 2.50 | V |
| | | $V_{LVD9}$ | The power supply voltage is rising. | 2.05 | 2.09 | 2.13 | V |
| | | | The power supply voltage is falling. | 2.00 | 2.04 | 2.08 | V |
| | | $V_{LVD10}$ | The power supply voltage is rising. | 1.94 | 1.98 | 2.02 | V |
| | | | The power supply voltage is falling. | 1.90 | 1.94 | 1.98 | V |
| | | $V_{LVD11}$ | The power supply voltage is rising. | 1.84 | 1.88 | 1.91 | V |
| | | | The power supply voltage is falling. | 1.80 | 1.84 | 1.87 | V |
| | | $V_{LVD12}$ | The power supply voltage is rising. | 1.74 | 1.77 | 1.81 | V |
| | | | The power supply voltage is falling. | 1.70 | 1.73 | 1.77 | V |
| | | $V_{LVD13}$ | The power supply voltage is rising. | 1.64 | 1.67 | 1.70 | V |
| | | | The power supply voltage is falling. | 1.60 | 1.63 | 1.66 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | | 300 | µs |

### LVD Detection Voltage of Interrupt & Reset Mode

**($T_A$ = –40 to +85°C, $V_{PDR} \le V_{DD} \le 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDA0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 0, falling reset voltage | | | 1.60 | 1.63 | 1.66 | V |
| | $V_{LVDA1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | $V_{LVDA2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDA3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDB0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 1, falling reset voltage | | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 0, falling reset voltage | | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDC3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V |
| | | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V |
| | | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

### 2.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

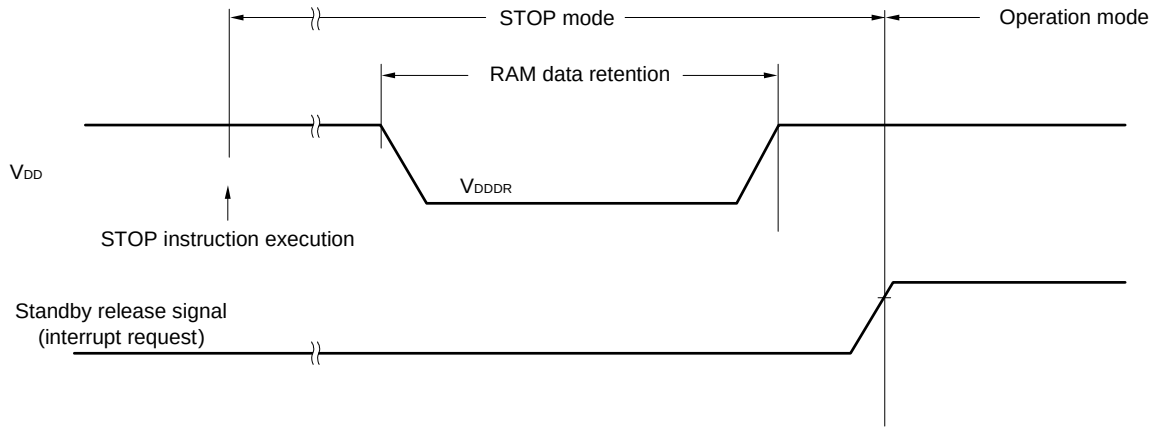
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**

## 2.7 RAM Data Retention Characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46[Note] | | 5.5 | V |

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.




## 2.8 Flash Memory Programming Characteristics

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years $T_A$ = 85°C | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 years $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

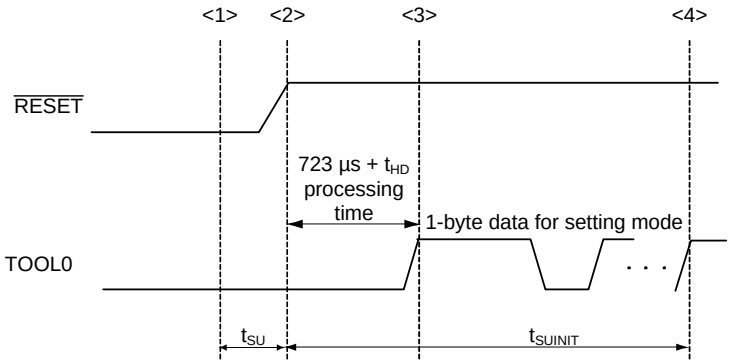
**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 2.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | POR and LVD reset must be released before the external reset is released. | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | $t_{SU}$ | POR and LVD reset must be released before the external reset is released. | 10 | | | µs |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must be released before the external reset is released. | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

$t_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

# 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = –40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A$ = –40 to +105°C
R5F100xxGxx

**Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. With products not provided with an $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ pin, replace $EV_{DD0}$ and $EV_{DD1}$ with $V_{DD}$, or replace $EV_{SS0}$ and $EV_{SS1}$ with $V_{SS}$.**

**3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product in the RL78/G13 User's Manual.**

**4. Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

**Remark** When RL78/G13 is used in the range of $T_A$ = –40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS ($T_A$ = –40 to +85°C)**.

There are following differences between the products "G: Industrial applications ($T_A$ = –40 to +105°C)" and the products "A: Consumer applications, and D: Industrial applications".

| Parameter | Application | |
|---|---|---|
| | A: Consumer applications,<br>D: Industrial applications | G: Industrial applications |
| Operating ambient temperature | $T_A$ = -40 to +85°C | $T_A$ = -40 to +105°C |
| Operating mode<br>Operating voltage range | HS (high-speed main) mode:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz<br>LS (low-speed main) mode:<br>1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz<br>LV (low-voltage main) mode:<br>1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz | HS (high-speed main) mode only:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| High-speed on-chip oscillator clock accuracy | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V<br>±1.0%@ $T_A$ = -20 to +85°C<br>±1.5%@ $T_A$ = -40 to -20°C<br>1.6 V ≤ $V_{DD}$ < 1.8 V<br>±5.0%@ $T_A$ = -20 to +85°C<br>±5.5%@ $T_A$ = -40 to -20°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V<br>±2.0%@ $T_A$ = +85 to +105°C<br>±1.0%@ $T_A$ = -20 to +85°C<br>±1.5%@ $T_A$ = -40 to -20°C |
| Serial array unit | UART<br>CSI: $f_{CLK}$/2 (supporting 16 Mbps), $f_{CLK}$/4<br>Simplified $I^2C$ communication | UART<br>CSI: $f_{CLK}$/4<br>Simplified $I^2C$ communication |
| IICA | Normal mode<br>Fast mode<br>Fast mode plus | Normal mode<br>Fast mode |
| Voltage detector | Rise detection voltage: 1.67 V to 4.06 V (14 levels)<br>Fall detection voltage: 1.63 V to 3.98 V (14 levels) | Rise detection voltage: 2.61 V to 4.06 V (8 levels)<br>Fall detection voltage: 2.55 V to 3.98 V (8 levels) |

(**Remark** is listed on the next page.)

**Remark** The electrical characteristics of the products G: Industrial applications ($T_A$ = -40 to +105°C) are different from those of the products "A: Consumer applications, and D: Industrial applications". For details, refer to **3.1** to **3.10**.

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C) (1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | –0.5 to +6.5 | V |
| | $EV_{DD0}$, $EV_{DD1}$ | $EV_{DD0}$ = $EV_{DD1}$ | –0.5 to +6.5 | V |
| | $EV_{SS0}$, $EV_{SS1}$ | $EV_{SS0}$ = $EV_{SS1}$ | –0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | –0.3 to +2.8<br>and –0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | –0.3 to $EV_{DD0}$ +0.3<br>and –0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | –0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | –0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | –0.3 to $EV_{DD0}$ +0.3<br>and –0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{O2}$ | P20 to P27, P150 to P156 | –0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI26 | –0.3 to $EV_{DD0}$ +0.3<br>and –0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0 to ANI14 | –0.3 to $V_{DD}$ +0.3<br>and –0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |

**Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed $AV_{REF}$(+) + 0.3 V in case of A/D conversion target pin**.**

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}$(+) : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | –40 | mA |
| | | Total of all pins –170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | –70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | –100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27, P150 to P156 | –0.5 | mA |
| | | Total of all pins | | –2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 40 | mA |
| | | Total of all pins 170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | –40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.2 Oscillator Characteristics

### 3.2.1 X1, XT1 oscillator characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)Note | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | MHz |
| XT1 clock oscillation frequency ($f_X$)Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G13 User's Manual.

### 3.2.2 On-chip oscillator characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | –20 to +85°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | –1.0 | | +1.0 | % |
| | | –40 to –20°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | –1.5 | | +1.5 | % |
| | | +85 to +105°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | –2.0 | | +2.0 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | –15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

## 3.3 DC Characteristics

### 3.3.1 Pin characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | –3.0 [Note 2] | mA |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% [Note 3]) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | –30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | –10.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | –5.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% [Note 3]) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | –30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | –19.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | –10.0 | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | –60.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P27, P150 to P156 | 2,4 V ≤ $V_{DD}$ ≤ 5.5 V | | | –0.1 [Note 2] | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | –1.5 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $EV_{DD0}$, $EV_{DD1}$, $V_{DD}$ pins to an output pin.

**2.** Do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | | | | 8.5 Note 2 | mA |
| | | Per pin for P60 to P63 | | | | 15.0 Note 2 | mA |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 15.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 9.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 35.0 | mA |
| | | | 2,4 V ≤ $EV_{DD0}$ < 2.7 V | | | 20.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 80.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27, P150 to P156 | | | | 0.4 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 2,4 V ≤ $V_{DD}$ ≤ 5.5 V | | | 5.0 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS0}$, $EV_{SS1}$ and $V_{SS}$ pin.

**2.** Do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | 0.8$EV_{DD0}$ | | $EV_{DD0}$ | V |
| | $V_{IH2}$ | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 2.2 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 2.0 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD0}$ < 3.3 V | 1.5 | | $EV_{DD0}$ | V |
| | $V_{IH3}$ | P20 to P27, P150 to P156 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60 to P63 | | 0.7$EV_{DD0}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | 0 | | 0.2$EV_{DD0}$ | V |
| | $V_{IL2}$ | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD0}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P27, P150 to P156 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60 to P63 | | 0 | | 0.3$EV_{DD0}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is $EV_{DD0}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $EV_{DD0}$ – 0.7 | | | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $EV_{DD0}$ – 0.6 | | | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $EV_{DD0}$ – 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27, P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = –100 µA | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27, P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 µA | | | 0.4 | V |
| | $V_{OL3}$ | P60 to P63 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |

**Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I$ = $EV_{DD0}$ | | | | 1 | µA |
| | $I_{LIH2}$ | P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$ | $V_I$ = $V_{DD}$ | | | | 1 | µA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | µA |
| | | | | In resonator connection | | | 10 | µA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I$ = $EV_{SS0}$ | | | | –1 | µA |
| | $I_{LIL2}$ | P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$ | $V_I$ = $V_{SS}$ | | | | –1 | µA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | –1 | µA |
| | | | | In resonator connection | | | –10 | µA |
| On-chip pll-up resistance | $R_U$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I$ = $EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 3.3.2 Supply current characteristics

**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 4.6 | 7.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.6 | 7.5 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.8 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.8 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.7 | 4.2 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.7 | 4.2 | mA |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 1.9 | 2.9 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.9 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.9 | 2.9 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.9 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = –40°C | Normal operation | Square wave input | | 4.1 | 4.9 | µA |
| | | | | | | Resonator connection | | 4.2 | 5.0 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.1 | 4.9 | µA |
| | | | | | | Resonator connection | | 4.2 | 5.0 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.2 | 5.5 | µA |
| | | | | | | Resonator connection | | 4.3 | 5.6 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.3 | 6.3 | µA |
| | | | | | | Resonator connection | | 4.4 | 6.4 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 4.6 | 7.7 | µA |
| | | | | | | Resonator connection | | 4.7 | 7.8 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 6.9 | 19.7 | µA |
| | | | | | | Resonator connection | | 7.0 | 19.8 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.54 | 2.90 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.54 | 2.90 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.44 | 2.30 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 2.30 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.40 | 1.70 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.40 | 1.70 | mA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = –40°C | Square wave input | | 0.25 | 0.57 | µA |
| | | | | | Resonator connection | | 0.44 | 0.76 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | µA |
| | | | | | Resonator connection | | 0.49 | 0.76 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.37 | 1.17 | µA |
| | | | | | Resonator connection | | 0.56 | 1.36 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.53 | 1.97 | µA |
| | | | | | Resonator connection | | 0.72 | 2.16 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 0.82 | 3.37 | µA |
| | | | | | Resonator connection | | 1.01 | 3.56 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +105°C | Square wave input | | 3.01 | 15.37 | µA |
| | | | | | Resonator connection | | 3.20 | 15.56 | µA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = –40°C | | | | 0.18 | 0.50 | µA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | µA |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | µA |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | µA |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | µA |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.30 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.3 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 5.2 | 9.2 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.2 | 9.2 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.1 | 7.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.1 | 7.0 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.0 | 5.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.0 | 5.0 | mA |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.4 | 5.9 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.0 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.4 | 5.9 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.0 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.1 | 3.5 | mA |
| | | | | | | Resonator connection | | 2.1 | 3.5 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.1 | 3.5 | mA |
| | | | | | | Resonator connection | | 2.1 | 3.5 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = –40°C | Normal operation | Square wave input | | 4.8 | 5.9 | µA |
| | | | | | | Resonator connection | | 4.9 | 6.0 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.9 | 5.9 | µA |
| | | | | | | Resonator connection | | 5.0 | 6.0 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.0 | 7.6 | µA |
| | | | | | | Resonator connection | | 5.1 | 7.7 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.2 | 9.3 | µA |
| | | | | | | Resonator connection | | 5.3 | 9.4 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.7 | 13.3 | µA |
| | | | | | | Resonator connection | | 5.8 | 13.4 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 10.0 | 46.0 | µA |
| | | | | | | Resonator connection | | 10.0 | 46.0 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.40 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.40 | mA |
| | | | | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.50 | 2.70 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 2.70 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.44 | 1.90 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 1.90 | mA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 2.10 | mA |
| | | | | | Resonator connection | | 0.48 | 2.20 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 2.10 | mA |
| | | | | | Resonator connection | | 0.48 | 2.20 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 1.10 | mA |
| | | | | | Resonator connection | | 0.28 | 1.20 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 1.10 | mA |
| | | | | | Resonator connection | | 0.28 | 1.20 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = –40°C | Square wave input | | 0.28 | 0.61 | µA |
| | | | | | Resonator connection | | 0.47 | 0.80 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.34 | 0.61 | µA |
| | | | | | Resonator connection | | 0.53 | 0.80 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.41 | 2.30 | µA |
| | | | | | Resonator connection | | 0.60 | 2.49 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.64 | 4.03 | µA |
| | | | | | Resonator connection | | 0.83 | 4.22 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 1.09 | 8.04 | µA |
| | | | | | Resonator connection | | 1.28 | 8.23 | µA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +105°C | Square wave input | | 5.50 | 41.00 | µA |
| | | | | | Resonator connection | | 5.50 | 41.00 | µA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = –40°C | | | | 0.19 | 0.52 | µA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.52 | µA |
| | | | $T_A$ = +50°C | | | | 0.32 | 2.21 | µA |
| | | | $T_A$ = +70°C | | | | 0.55 | 3.94 | µA |
| | | | $T_A$ = +85°C | | | | 1.00 | 7.95 | µA |
| | | | $T_A$ = +105°C | | | | 5.00 | 40.00 | µA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) Peripheral Functions (Common to all products)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | µA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | µA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | µA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | 0.22 | | µA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75.0 | | µA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | µA |
| LVD operating current | $I_{LVD}$ Notes 1, 7 | | | | 0.08 | | µA |
| Self programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.50 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 8 | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.50 | 1.10 | mA |
| | | | The A/D conversion operations are performed, low-voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 2.04 | mA |
| | | CSI/UART operation | | | 0.70 | 1.54 | mA |

**Notes 1.** Current flowing to the $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates.

**6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter is in operation.

**Notes 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**8.** Current flowing only during data flash rewrite.

**9.** Current flowing only during self programming.

**10.** For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13 User's Manual.

**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 3.4 AC Characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

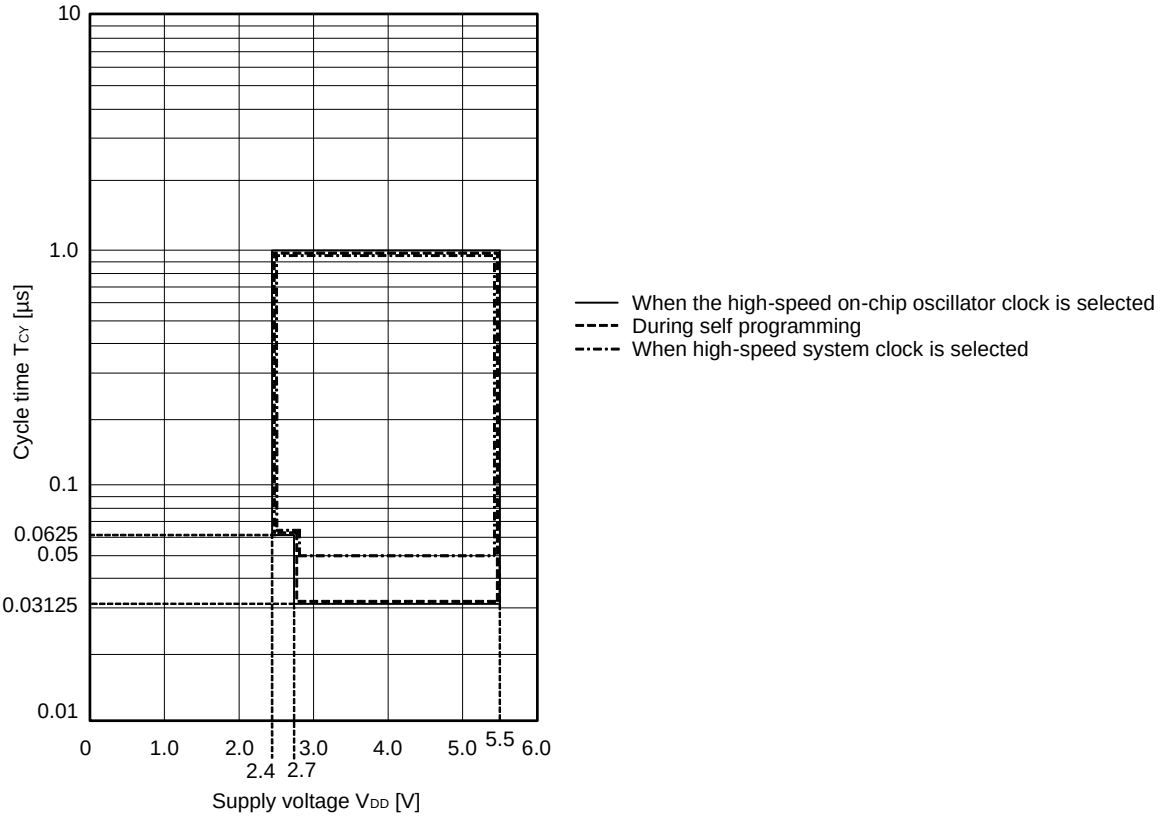
| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | Subsystem clock ($f_{SUB}$) operation | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | µs |
| | | In the self programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | µs |
| TI00 to TI07, TI10 to TI17 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$+10 | | | ns[Note] |
| TO00 to TO07, TO10 to TO17 output frequency | $f_{TO}$ | HS (high-speed main) mode | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | | µs |
| | | INTP1 to INTP11 | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR7 | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | | 10 | | | µs |

**Note** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$
2.4V ≤ $EV_{DD0}$ < 2.7 V : MIN. 125 ns

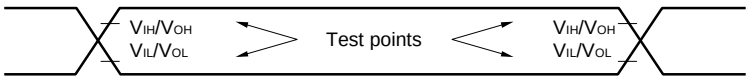
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).
m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

**Minimum Instruction Execution Time during Main System Clock Operation**

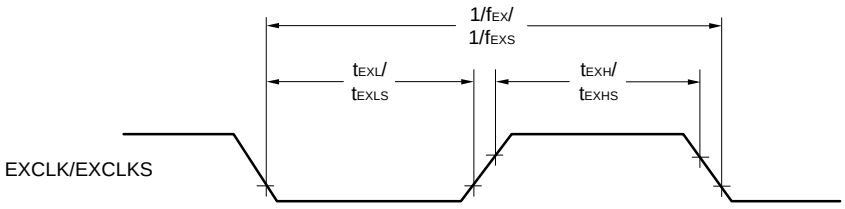
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



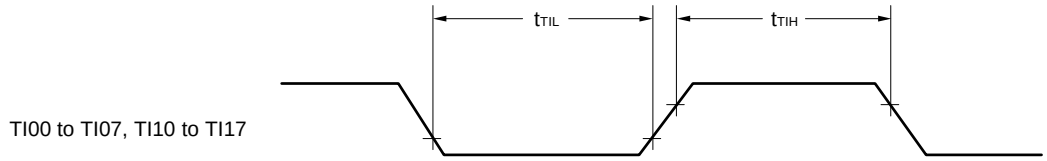

**AC Timing Test Points**

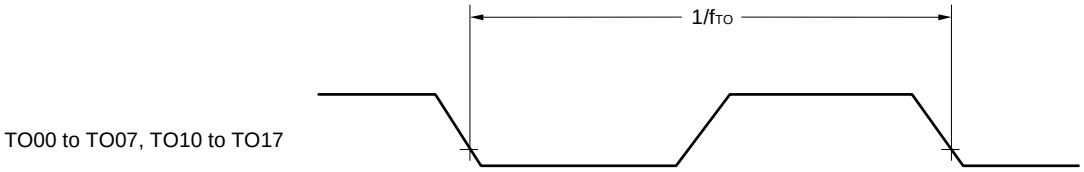



**External System Clock Timing**

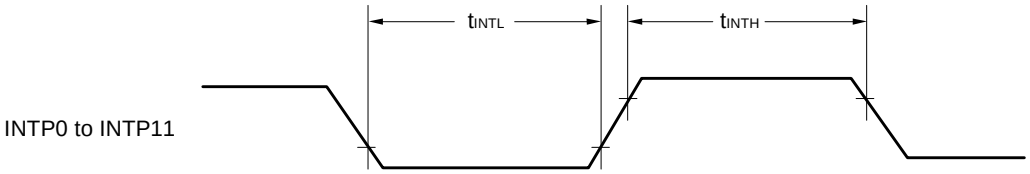


**TI/TO Timing**

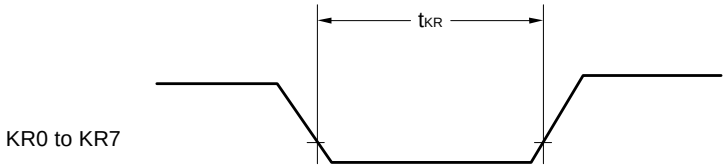


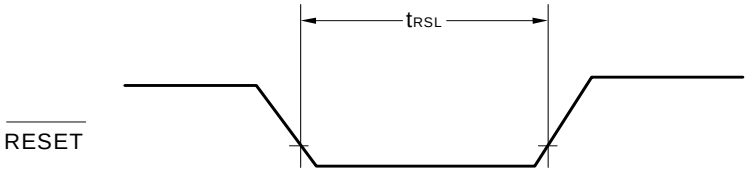

**Interrupt Request Input Timing**




**Key Interrupt Input Timing**

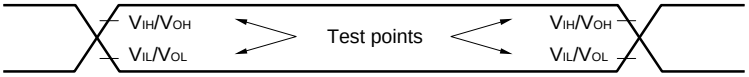



**$\overline{\text{RESET}}$ Input Timing**



## 3.5 Peripheral Functions Characteristics

**AC Timing Test Points**




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

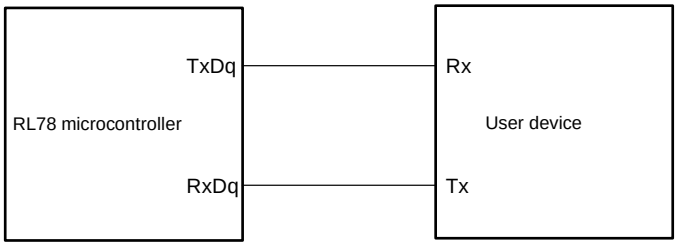
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate Note 1 | | | | $f_{MCK}$/12 Note 2 | bps |
| | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | 2.6 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

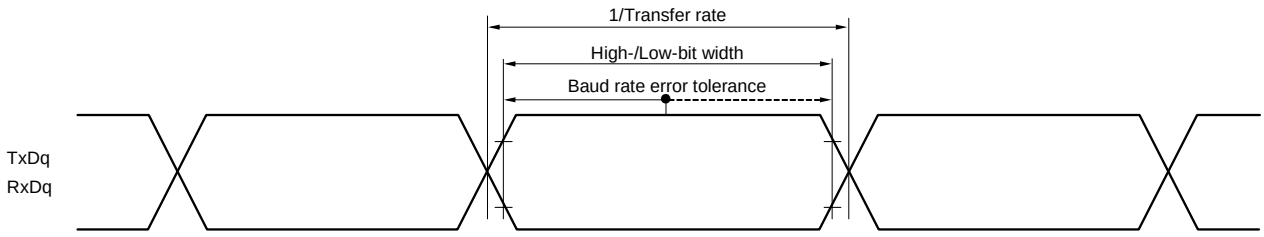
**2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 1.3 Mbps

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 76 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 113 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | | | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 30 pF Note 4 | | | 50 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 16/$f_{MCK}$ | | ns |
| | | | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 14 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 16 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 36 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+60 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+62 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$+66 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$+113 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

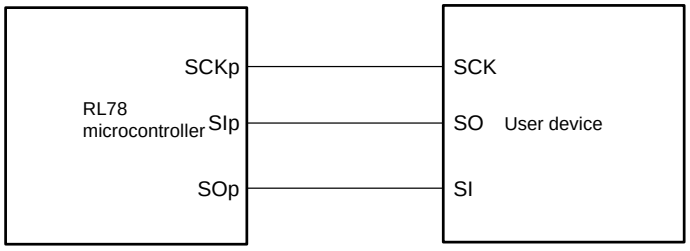
**5.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

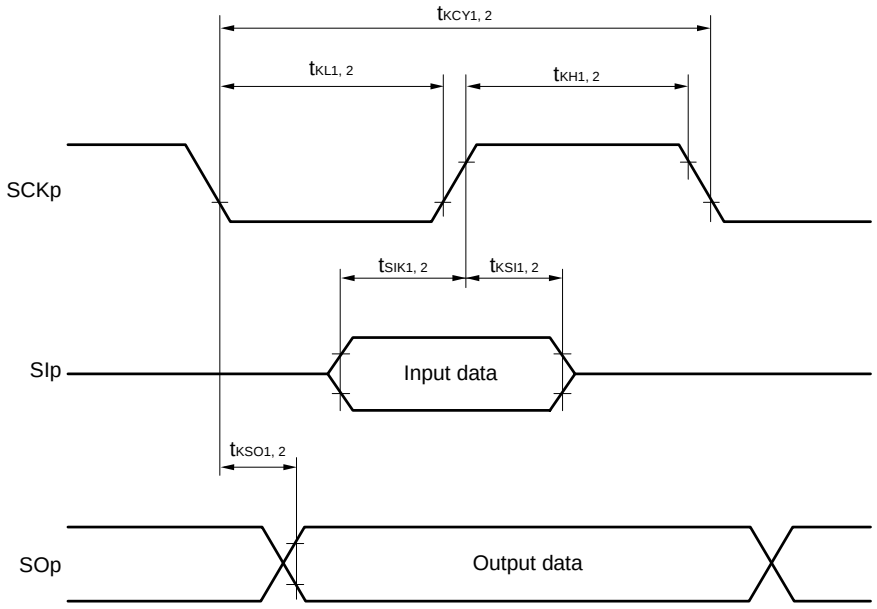
**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

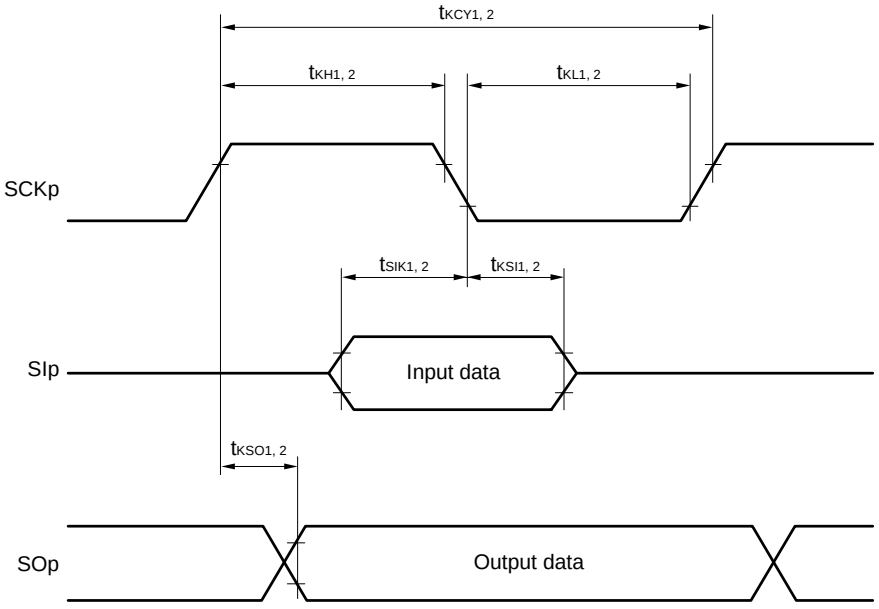
**CSI mode connection diagram (during communication at same potential)**



**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

**2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

### (4) During communication at same potential (simplified $I^2C$ mode)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 220 Note2 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

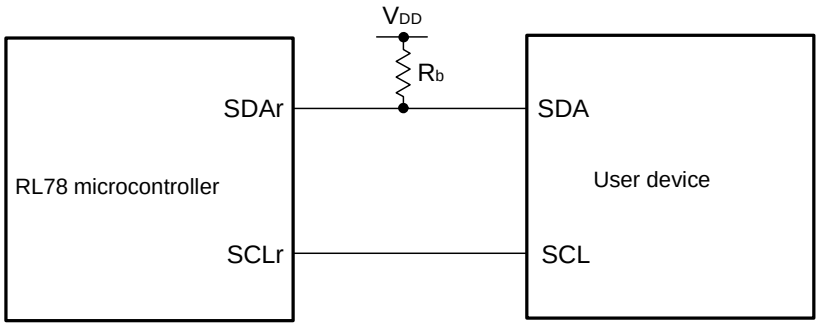
**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

**2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

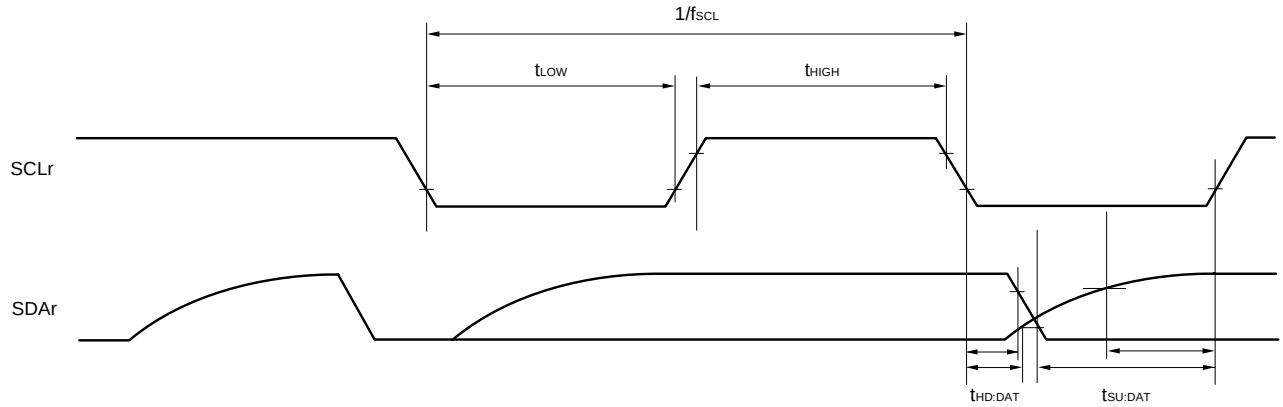
**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**Simplified I²C mode mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remarks 1.** $R_b$[Ω]:Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

**(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | |
| Transfer rate | | Reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | $f_{MCK}$/12 Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | 2.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | $f_{MCK}$/12 Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | 2.6 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | $f_{MCK}$/12 Notes 1,2 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | 2.6 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 1.3 Mbps

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | |
| Transfer rate | | Transmission | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | **Note 1** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.6 Note 2 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | **Note 3** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 4 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | **Note 5** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 6 | Mbps |

**Notes 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**2.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**3.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.4 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**Notes 5.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

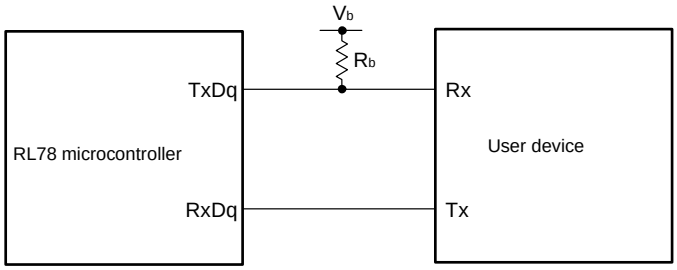
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

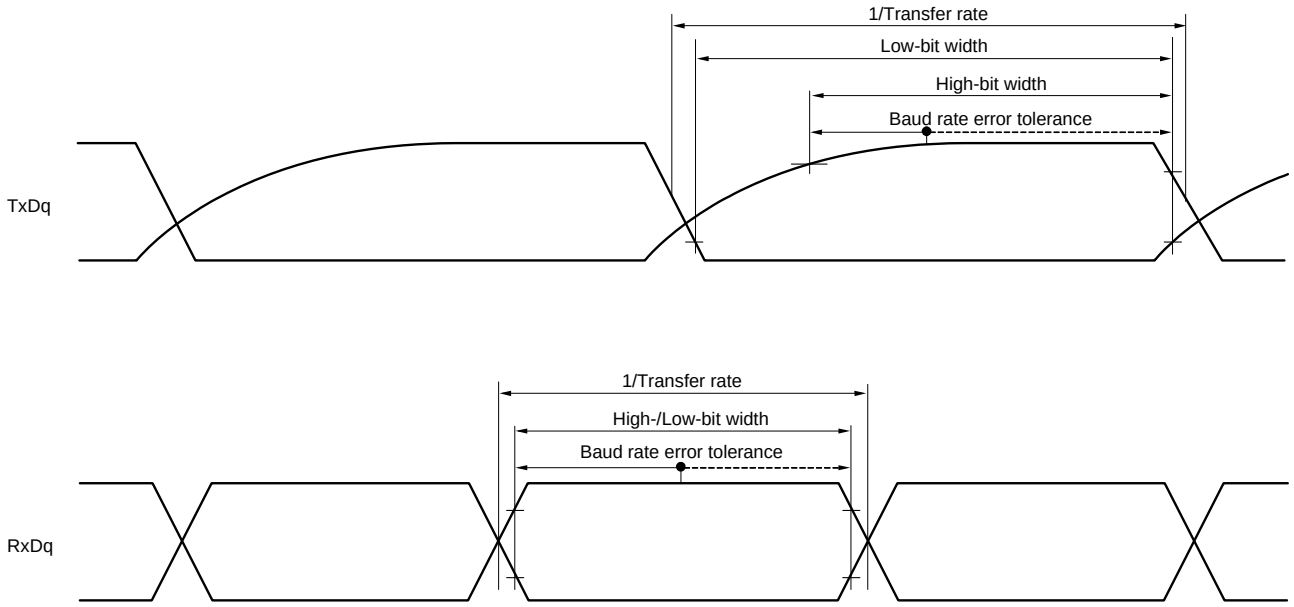
**6.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**



**UART mode bit width (during communication at different potential) (reference)**




**Remarks 1.** $R_b$[Ω]:Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 150 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 340 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 – 916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 – 100 | | ns |

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |

**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

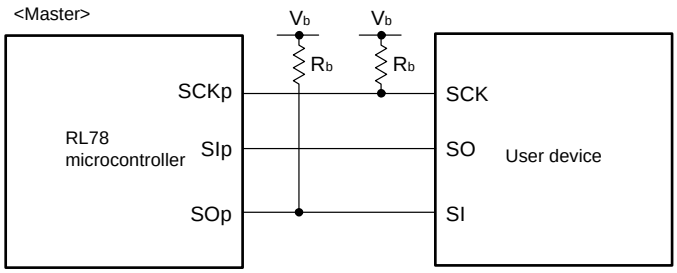
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 88 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 50 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 50 | ns |

**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**



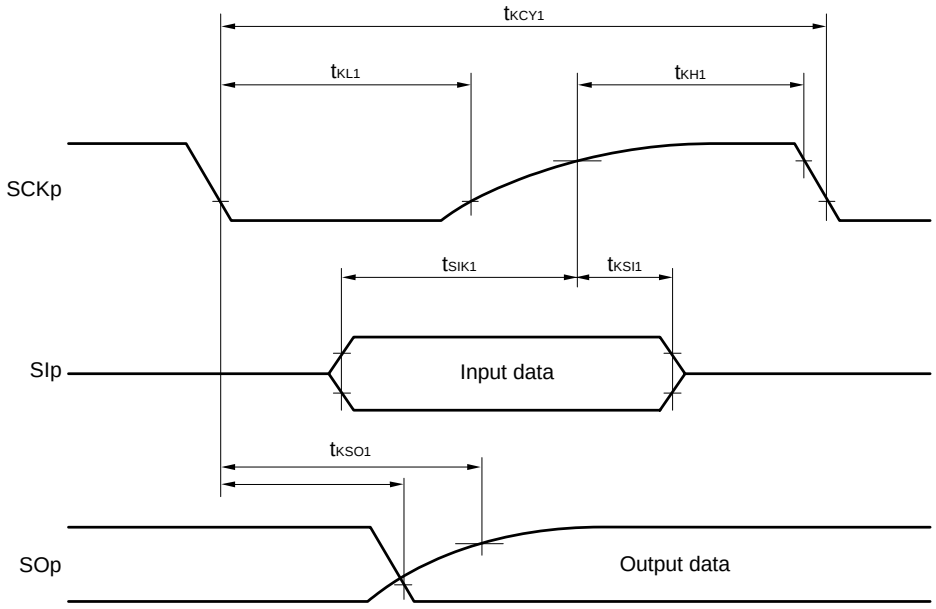

**Remarks 1.** $R_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number , n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

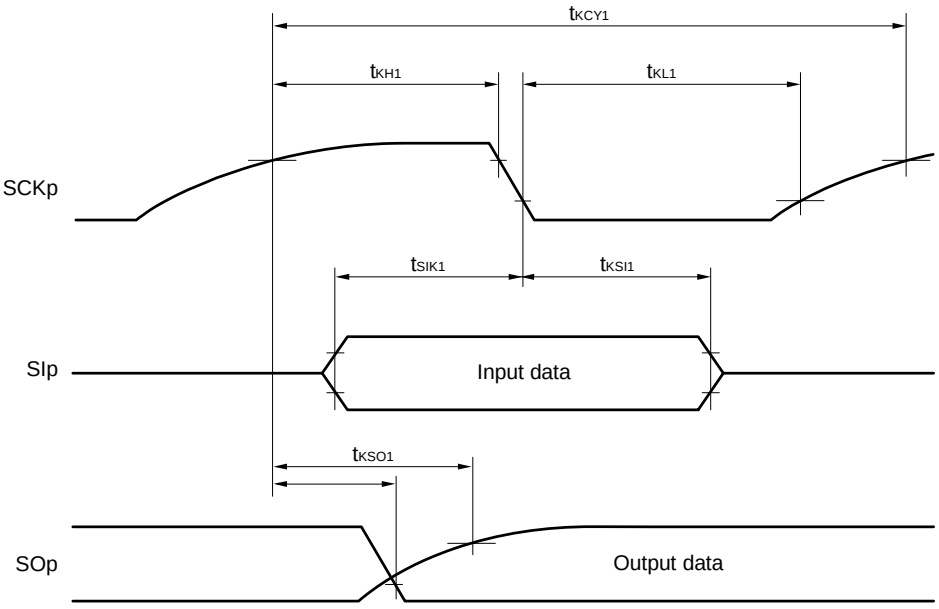
**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

**4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

**2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 28/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 40/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 24 MHz < $f_{MCK}$ | 96/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note2 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

**Notes 1.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

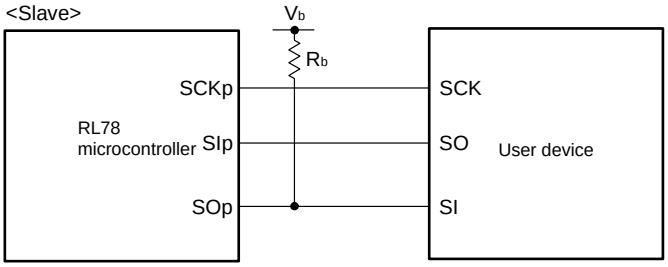
**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**CSI mode connection diagram (during communication at different potential)**



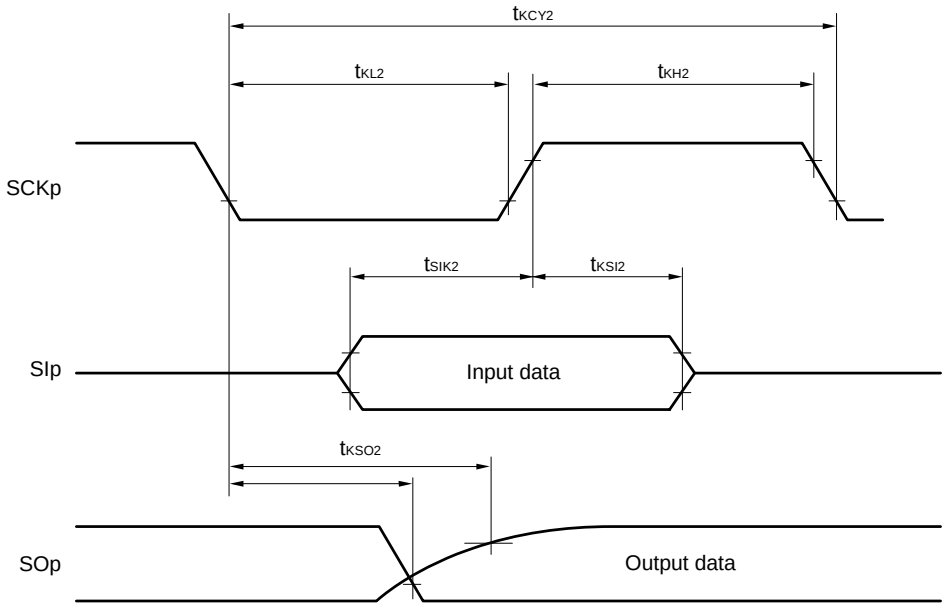

**Remarks 1.** $R_b$[Ω]:Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

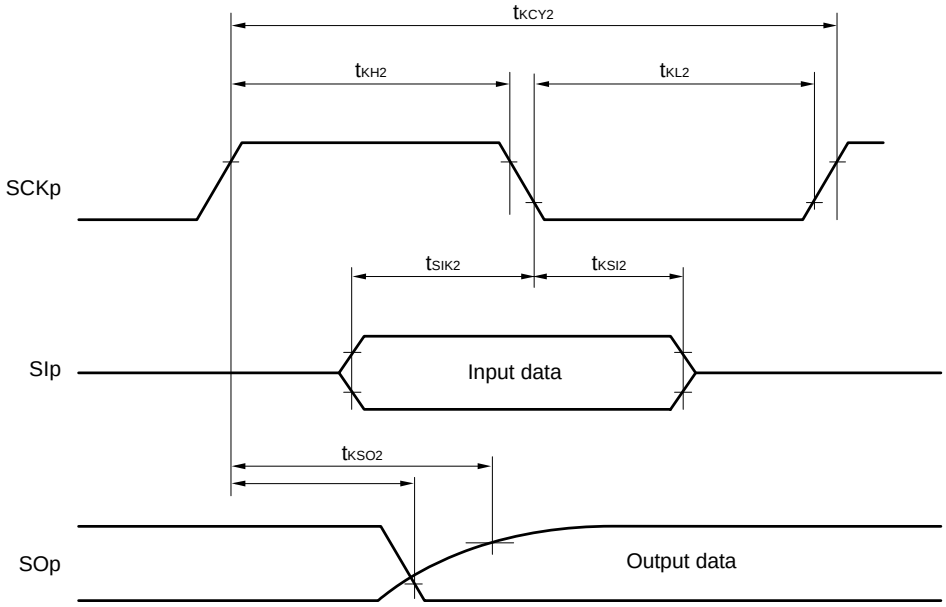
**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

**4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

**2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (1/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 100 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 100 Note 1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 4600 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 4600 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 4650 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 620 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 500 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 2700 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 2400 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1830 | | ns |

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (2/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 340 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 340 Note 2 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | $1/f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | $1/f_{MCK}$ + 570 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 1420 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 1215 | ns |

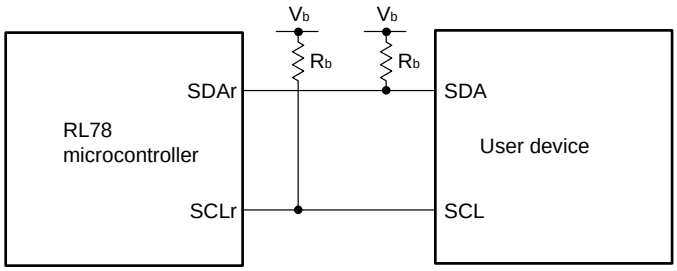
**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

**2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

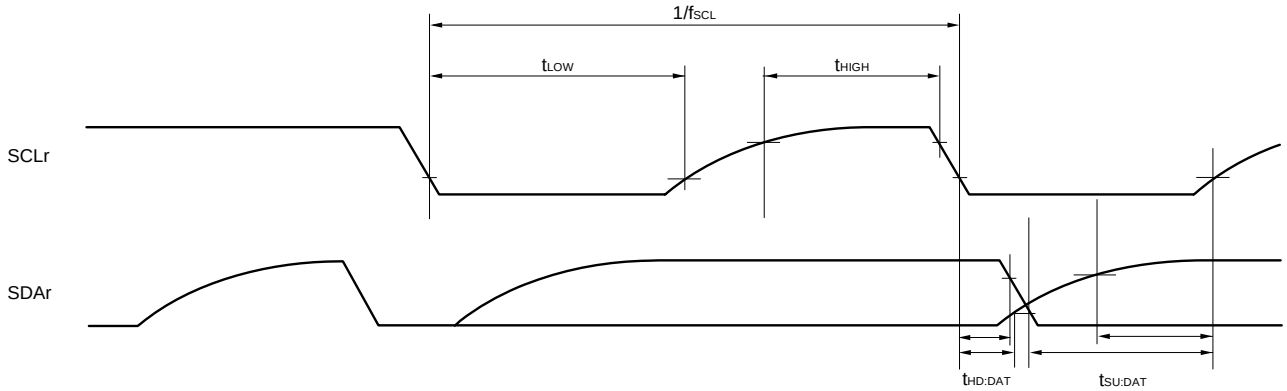
**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $R_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**2.** r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13)

### 3.5.2 Serial interface IICA

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | – | – | 0 | 400 | kHz |
| | | Standard mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | – | – | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 4.7 | | 0.6 | | µs |
| Hold time[Note 1] | $t_{HD:STA}$ | | 4.0 | | 0.6 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | 4.7 | | 1.3 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | 4.0 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | 0 | 3.45 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU:STO}$ | | 4.0 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | µs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

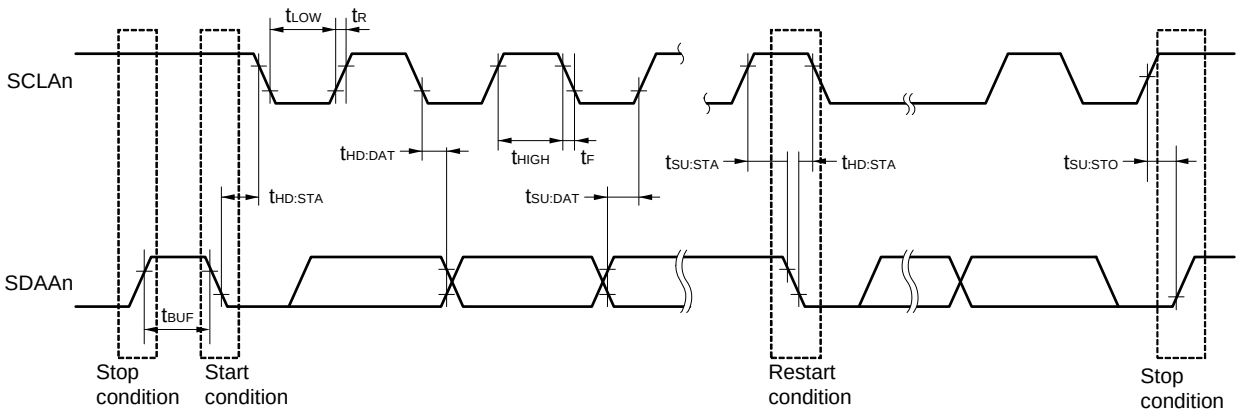
**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ
Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**




**Remark n = 0, 1**

## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0 to ANI14 | Refer to **3.6.1 (1)**. | Refer to **3.6.1 (3)**. | Refer to **3.6.1 (4)**. |
| ANI16 to ANI26 | Refer to **3.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **3.6.1 (1)**. | | – |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2 to ANI14 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| Full-scale error[Notes 1, 2] | $E_{FS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| Integral linearity error [Note 1] | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Differential linearity error [Note 1] | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI14 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage output<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ [Note 4] | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ [Note 4] | | | V |

(**Notes** are listed on the next page.)

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin : ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI26 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI14, ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI14 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI26 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage output (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 3 | | | V |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 3 | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (–) = $AV_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ Note 3 | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

### 3.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode)**

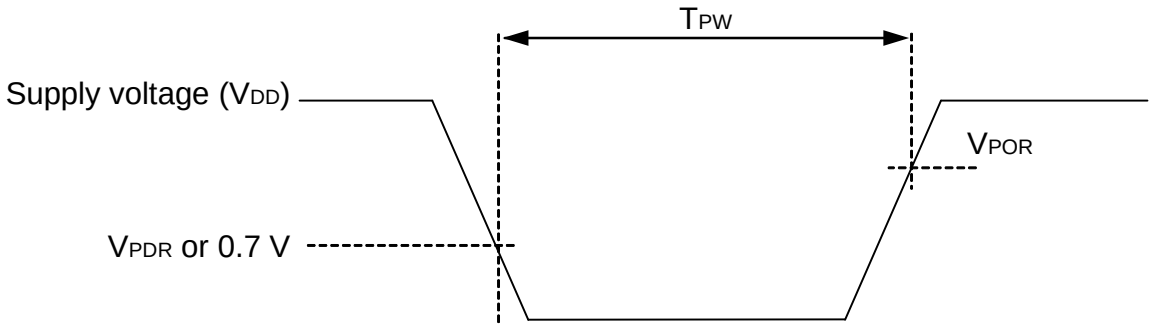
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 3.6.3 POR circuit characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | The power supply voltage is rising. | 1.45 | 1.51 | 1.57 | V |
| | $V_{PDR}$ | The power supply voltage is falling. | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width Note | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



### 3.6.4 LVD circuit characteristics

#### LVD Detection Voltage of Reset Mode and Interrupt Mode

**($T_A$ = –40 to +105°C, $V_{PDR} \le V_{DD} \le 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVD0}$ | The power supply voltage is rising. | 3.90 | 4.06 | 4.22 | V |
| | | | The power supply voltage is falling. | 3.83 | 3.98 | 4.13 | V |
| | | $V_{LVD1}$ | The power supply voltage is rising. | 3.60 | 3.75 | 3.90 | V |
| | | | The power supply voltage is falling. | 3.53 | 3.67 | 3.81 | V |
| | | $V_{LVD2}$ | The power supply voltage is rising. | 3.01 | 3.13 | 3.25 | V |
| | | | The power supply voltage is falling. | 2.94 | 3.06 | 3.18 | V |
| | | $V_{LVD3}$ | The power supply voltage is rising. | 2.90 | 3.02 | 3.14 | V |
| | | | The power supply voltage is falling. | 2.85 | 2.96 | 3.07 | V |
| | | $V_{LVD4}$ | The power supply voltage is rising. | 2.81 | 2.92 | 3.03 | V |
| | | | The power supply voltage is falling. | 2.75 | 2.86 | 2.97 | V |
| | | $V_{LVD5}$ | The power supply voltage is rising. | 2.70 | 2.81 | 2.92 | V |
| | | | The power supply voltage is falling. | 2.64 | 2.75 | 2.86 | V |
| | | $V_{LVD6}$ | The power supply voltage is rising. | 2.61 | 2.71 | 2.81 | V |
| | | | The power supply voltage is falling. | 2.55 | 2.65 | 2.75 | V |
| | | $V_{LVD7}$ | The power supply voltage is rising. | 2.51 | 2.61 | 2.71 | V |
| | | | The power supply voltage is falling. | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | | 300 | µs |

#### LVD Detection Voltage of Interrupt & Reset Mode

**($T_A$ = –40 to +105°C, $V_{PDR} \le V_{DD} \le 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.90 | 4.06 | 4.22 | V |
| | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

### 3.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

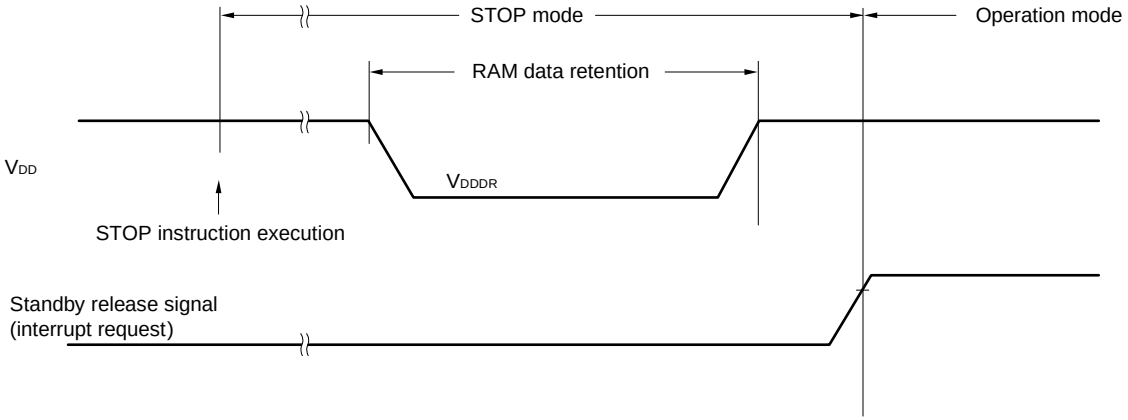
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

## 3.7 RAM Data Retention Characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.44 Note | | 5.5 | V |

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.




## 3.8 Flash Memory Programming Characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years $T_A$ = 85°C Note 4 | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 years $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C Note 4 | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C Note 4 | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library.

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

**4.** This temperature is the average value at which data are retained.

## 3.9 Dedicated Flash Memory Programmer Communication (UART)

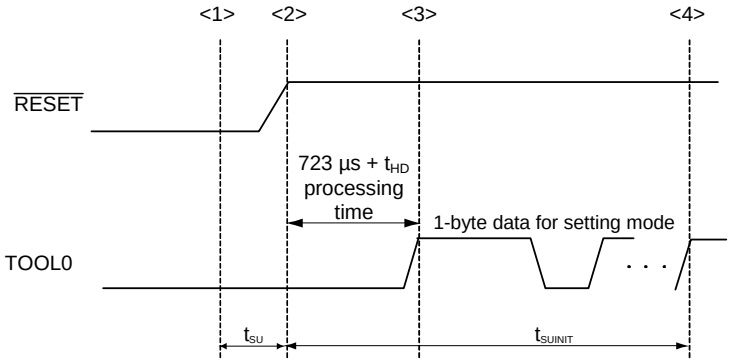
**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 3.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | POR and LVD reset must be released before the external reset is released. | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | $t_{SU}$ | POR and LVD reset must be released before the external reset is released. | 10 | | | µs |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must be released before the external reset is released. | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

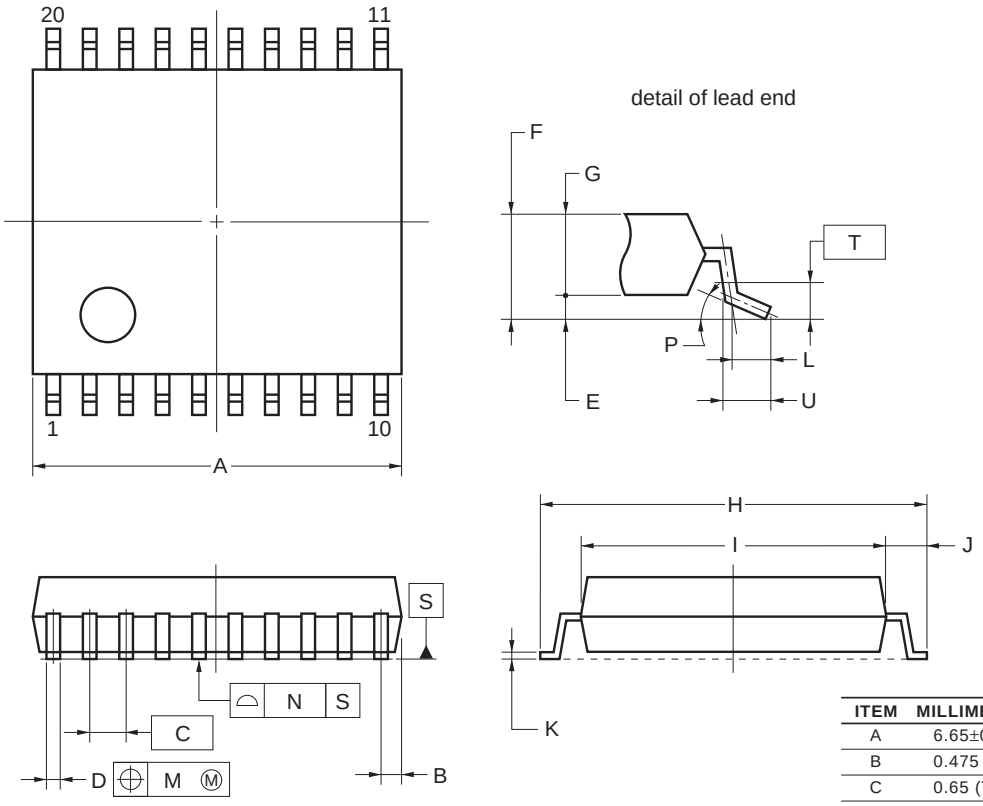
$t_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

$t_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

# 4. PACKAGE DRAWINGS

## 4.1 20-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP20-0300-0.65 | PLSP0020JC-A | S20MC-65-5A4-3 | 0.12 |




**NOTE**
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 6.65±0.15 |
| B | 0.475 MAX. |
| C | 0.65 (T.P.) |
| D | $0.24^{+0.08}_{-0.07}$ |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| T | 0.25 |
| U | 0.6±0.15 |

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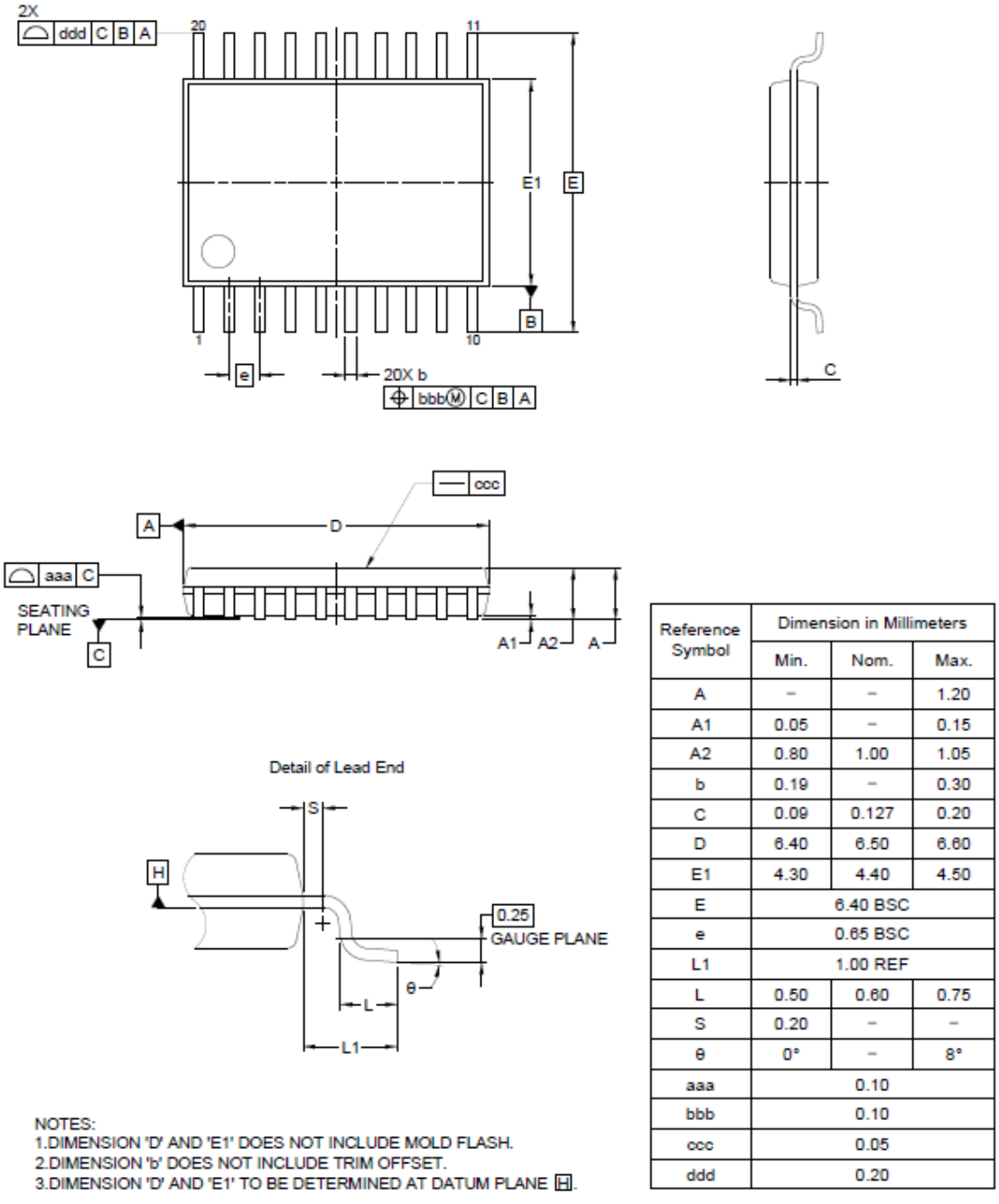
<R>

| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-TSSOP20-4.40x6.50-0.65 | PTSP0020JI-A | 0.08 |

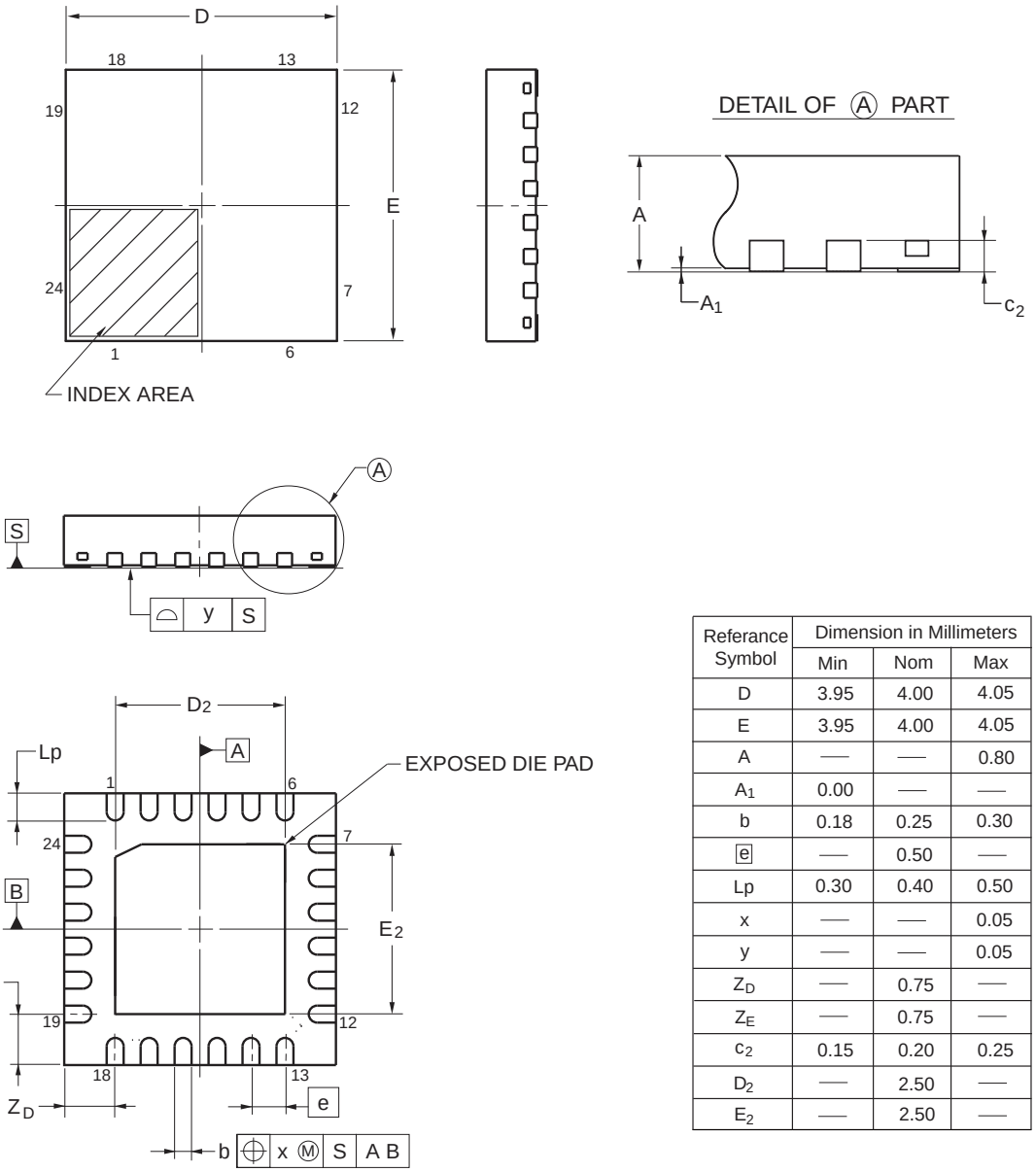



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | – | – | 1.20 |
| A1 | 0.05 | – | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | – | 0.30 |
| C | 0.09 | 0.127 | 0.20 |
| D | 6.40 | 6.50 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.40 BSC | | |
| e | 0.65 BSC | | |
| L1 | 1.00 REF | | |
| L | 0.50 | 0.60 | 0.75 |
| S | 0.20 | – | – |
| θ | 0° | – | 8° |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.05 | | |
| ddd | 0.20 | | |

NOTES:
1.DIMENSION "D" AND "E1" DOES NOT INCLUDE MOLD FLASH.
2.DIMENSION "b" DOES NOT INCLUDE TRIM OFFSET.
3.DIMENSION "D" AND "E1" TO BE DETERMINED AT DATUM PLANE H.

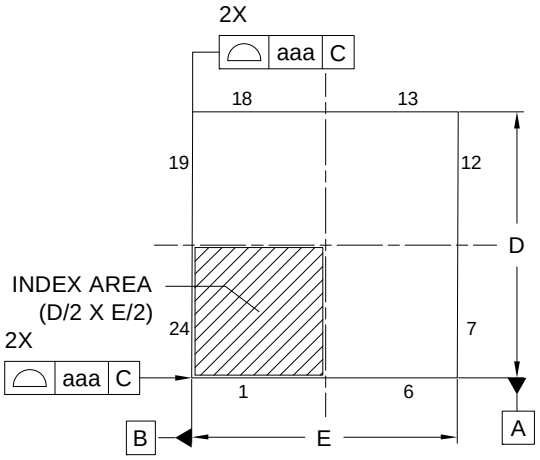
## 4.2 24-pin Package

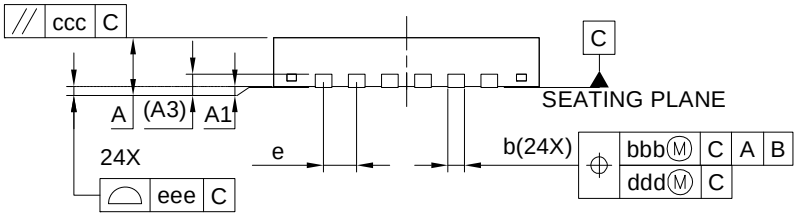
| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN24-4x4-0.50 | PWQN0024KE-A | P24K8-50-CAB-3 | 0.04 |

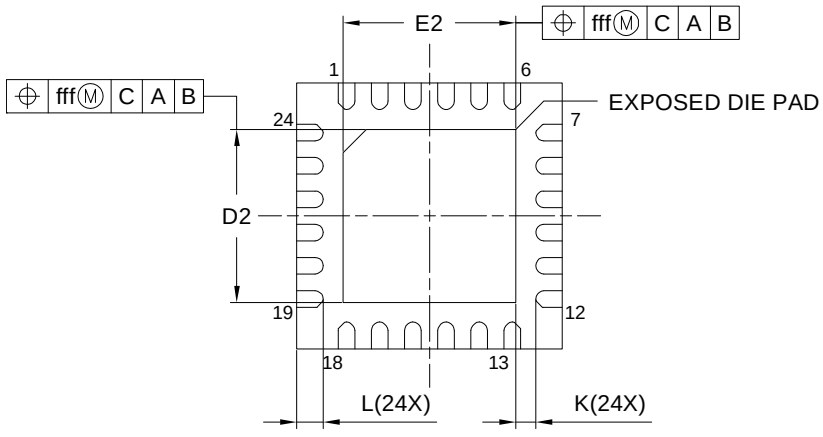



| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 3.95 | 4.00 | 4.05 |
| E | 3.95 | 4.00 | 4.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 2.50 | — |
| $E_2$ | — | 2.50 | — |

| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN024-4x4-0.50 | PWQN0024KF-A | 0.04 |



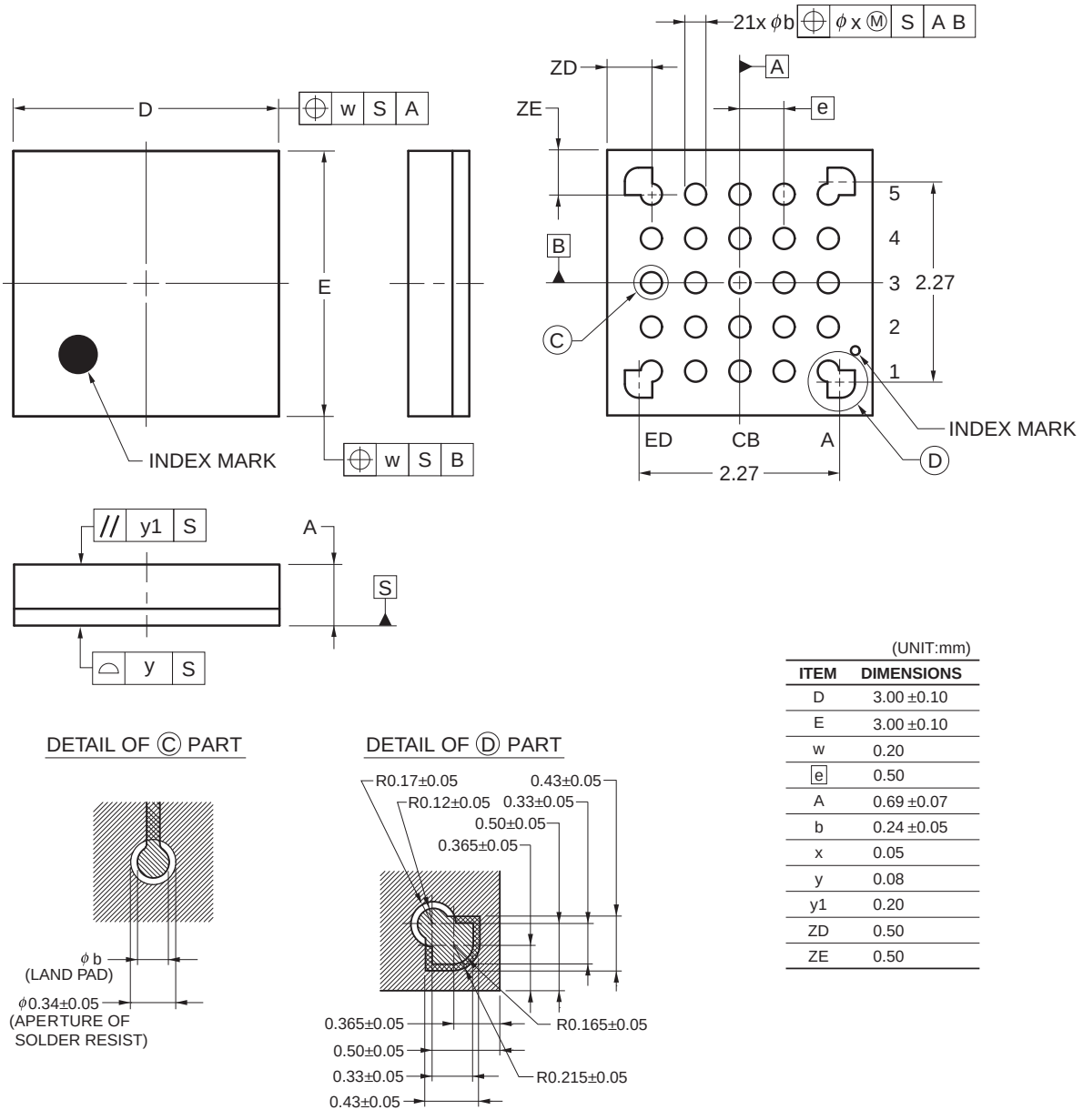




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 REF. | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 4.00 BSC | |
| E | | 4.00 BSC | |
| e | | 0.50 BSC | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| D2 | 2.55 | 2.60 | 2.65 |
| E2 | 2.55 | 2.60 | 2.65 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

### 4.3 25-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-WFLGA25-3x3-0.50 | PWLG0025KA-A | P25FC-50-2N2-2 | 0.01 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 3.00 ±0.10 |
| E | 3.00 ±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69 ±0.07 |
| b | 0.24 ±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.50 |
| ZE | 0.50 |

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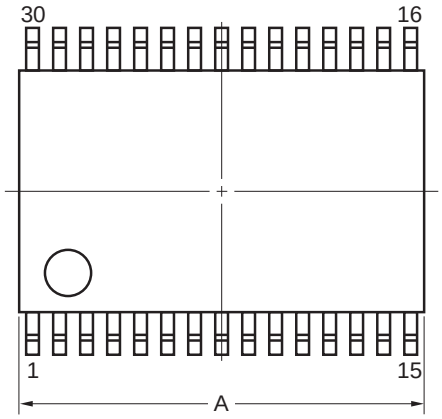
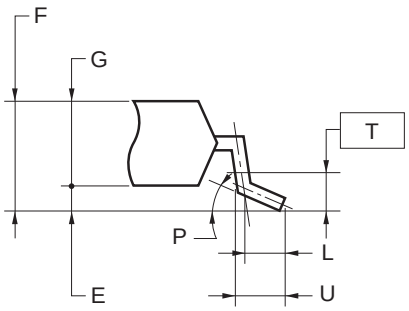
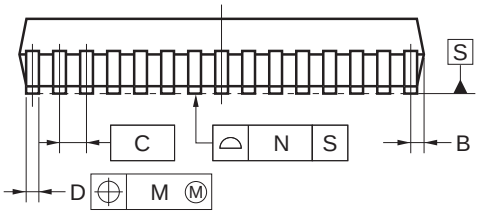
## 4.4 30-pin Package

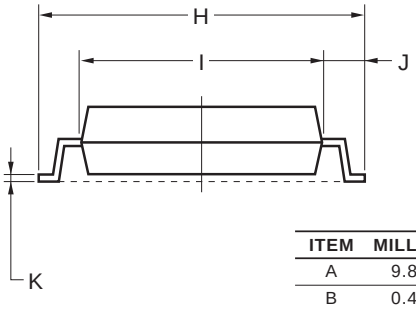
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |




detail of lead end




**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | $0.24^{+0.08}_{-0.07}$ |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| T | 0.25 |
| U | 0.6±0.15 |

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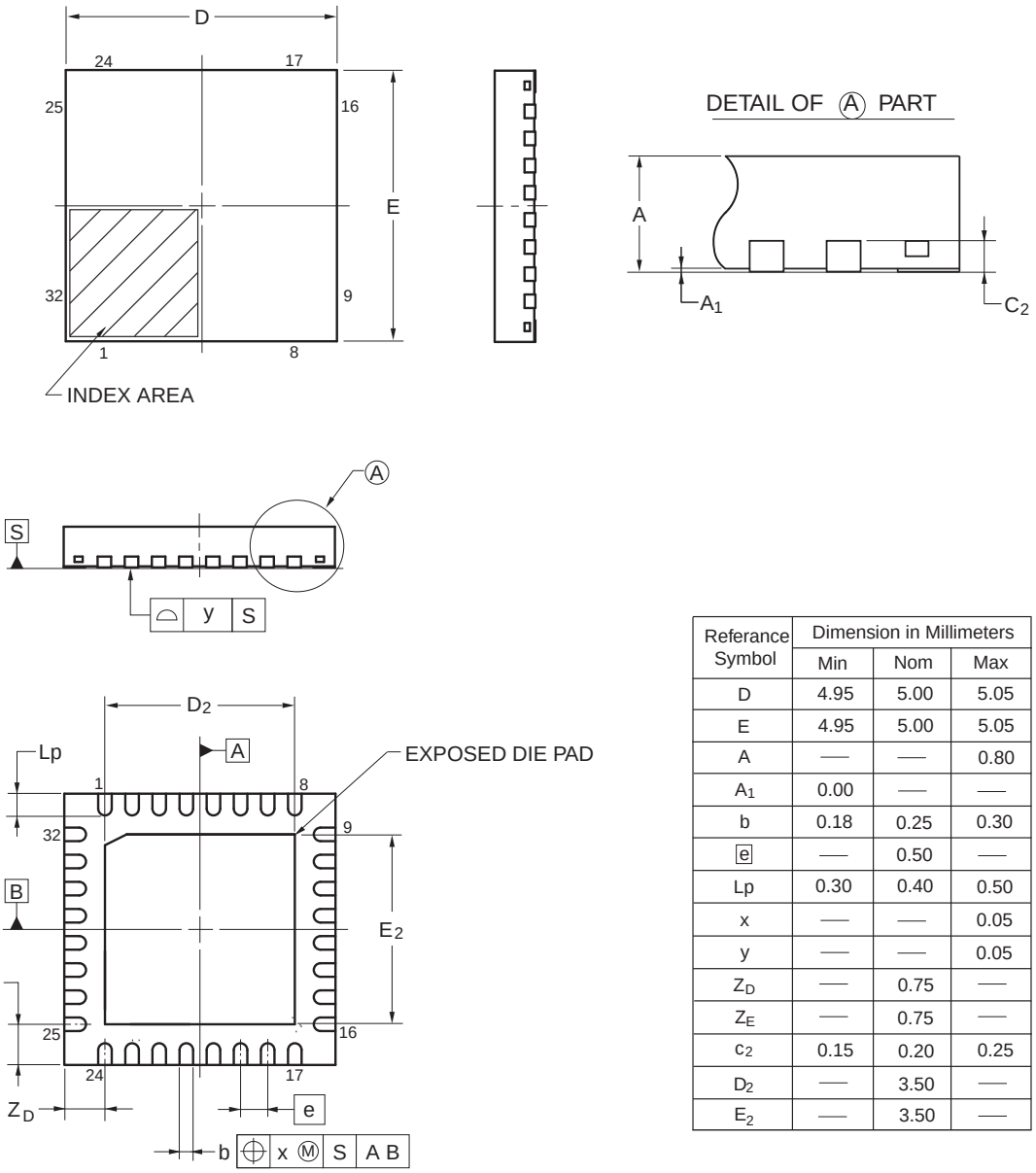
## 4.5 32-pin Package

| JEITA Package code | RENESAS code | Previous code | MASS (TYP.)[g] |
|---|---|---|---|
| P-HWQFN32-5x5-0.50 | PWQN0032KB-A | P32K8-50-3B4-5 | 0.06 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 4.95 | 5.00 | 5.05 |
| E | 4.95 | 5.00 | 5.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 3.50 | — |
| $E_2$ | — | 3.50 | — |

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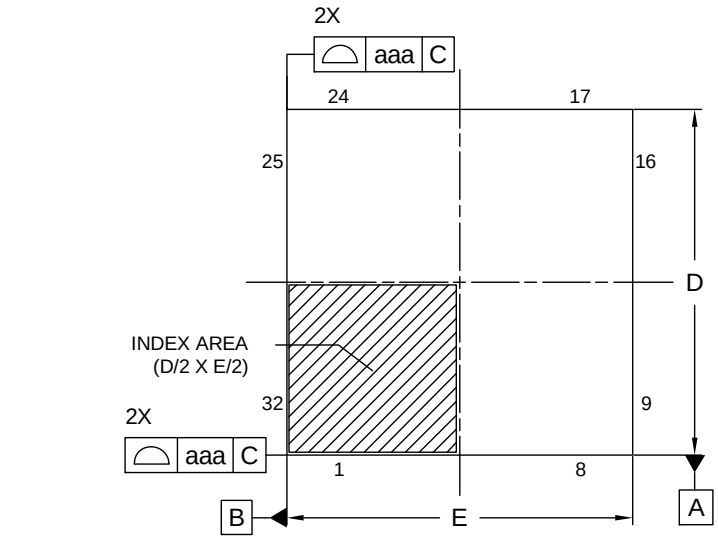
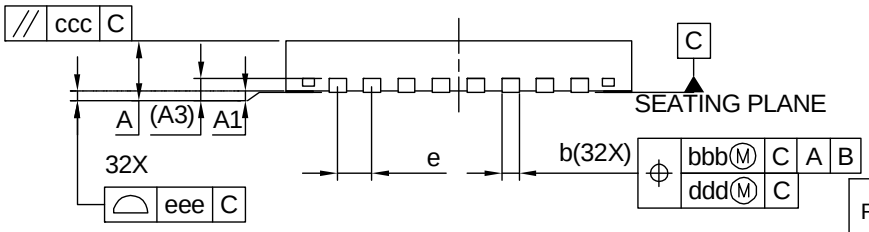
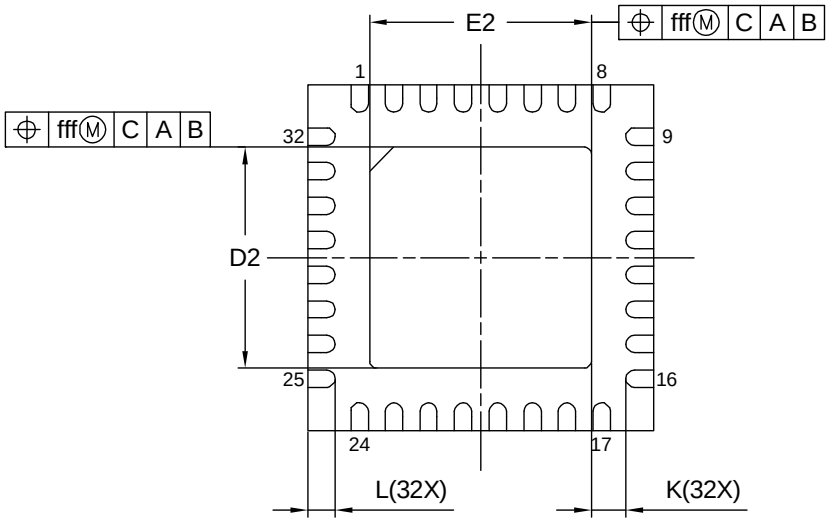
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN032-5x5-0.50 | PWQN0032KE-A | 0.06 |



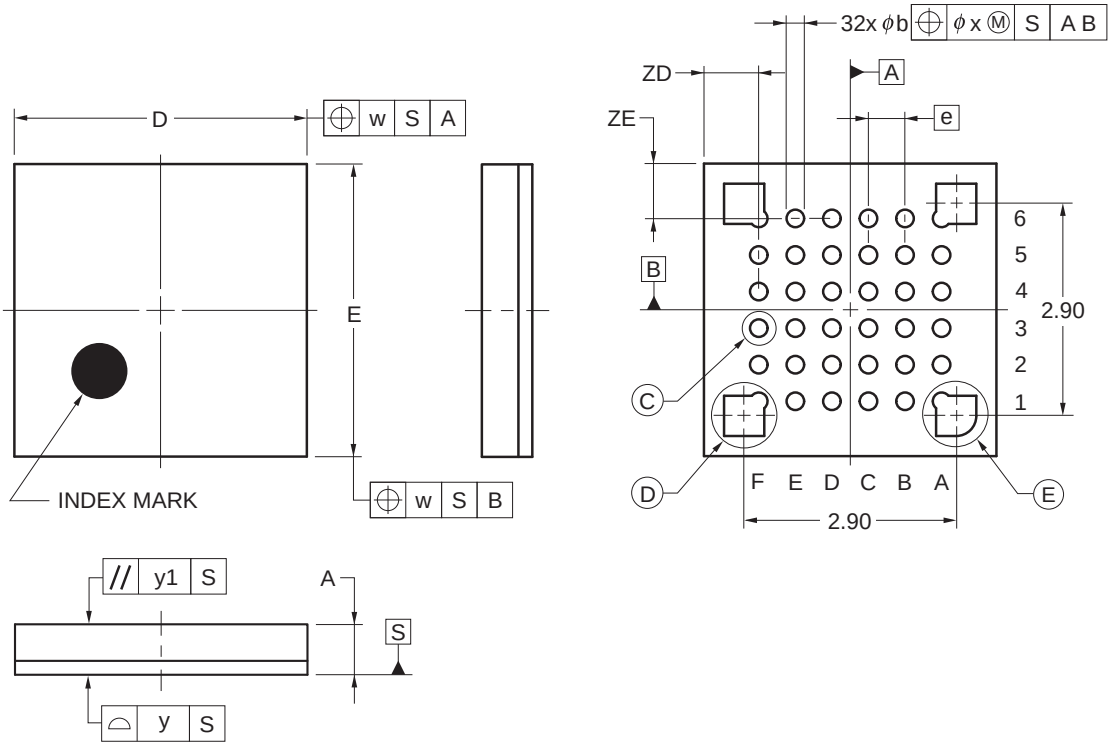



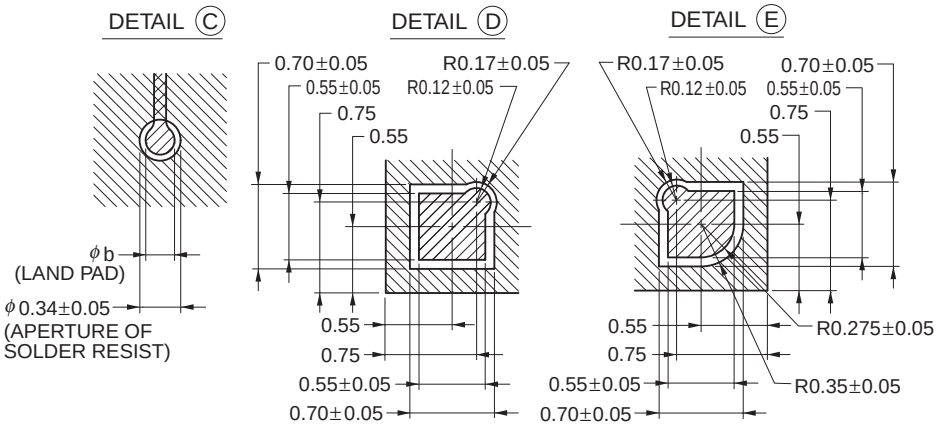




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | 0.02 | 0.05 |
| $A_3$ | | 0.203 REF. | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 5.00 BSC | |
| E | | 5.00 BSC | |
| e | | 0.50 BSC | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| $D_2$ | 3.15 | 3.20 | 3.25 |
| $E_2$ | 3.15 | 3.20 | 3.25 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

## 4.6 36-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-WFLGA36-4x4-0.50 | PWLG0036KA-A | P36FC-50-AA4-2 | 0.023 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 4.00±0.10 |
| E | 4.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

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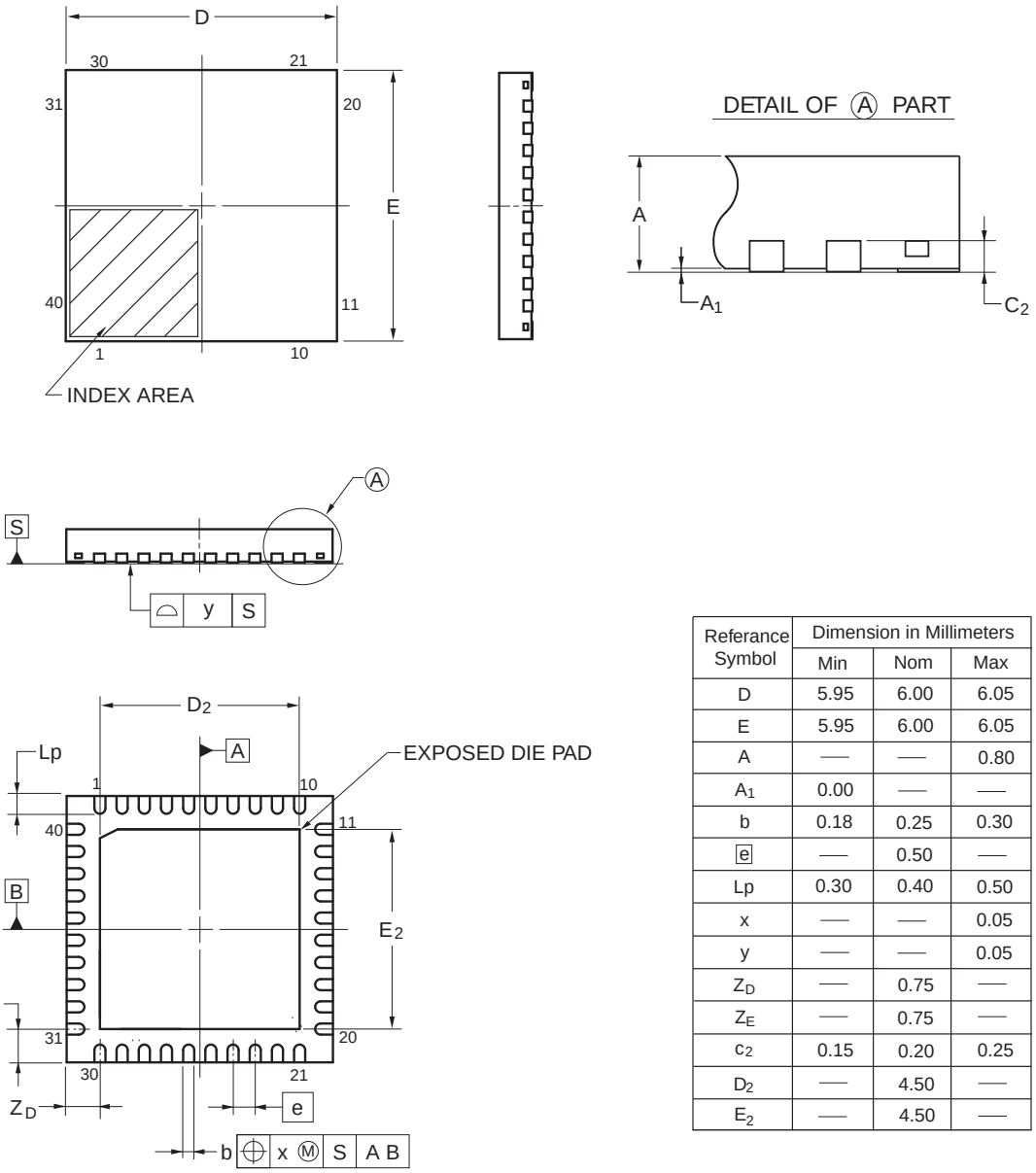
## 4.7 40-pin Package

| JEITA Package code | RENESAS code | Previous code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN40-6x6-0.50 | PWQN0040KC-A | P40K8-50-4B4-5 | 0.09 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 5.95 | 6.00 | 6.05 |
| E | 5.95 | 6.00 | 6.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 4.50 | — |
| $E_2$ | — | 4.50 | — |

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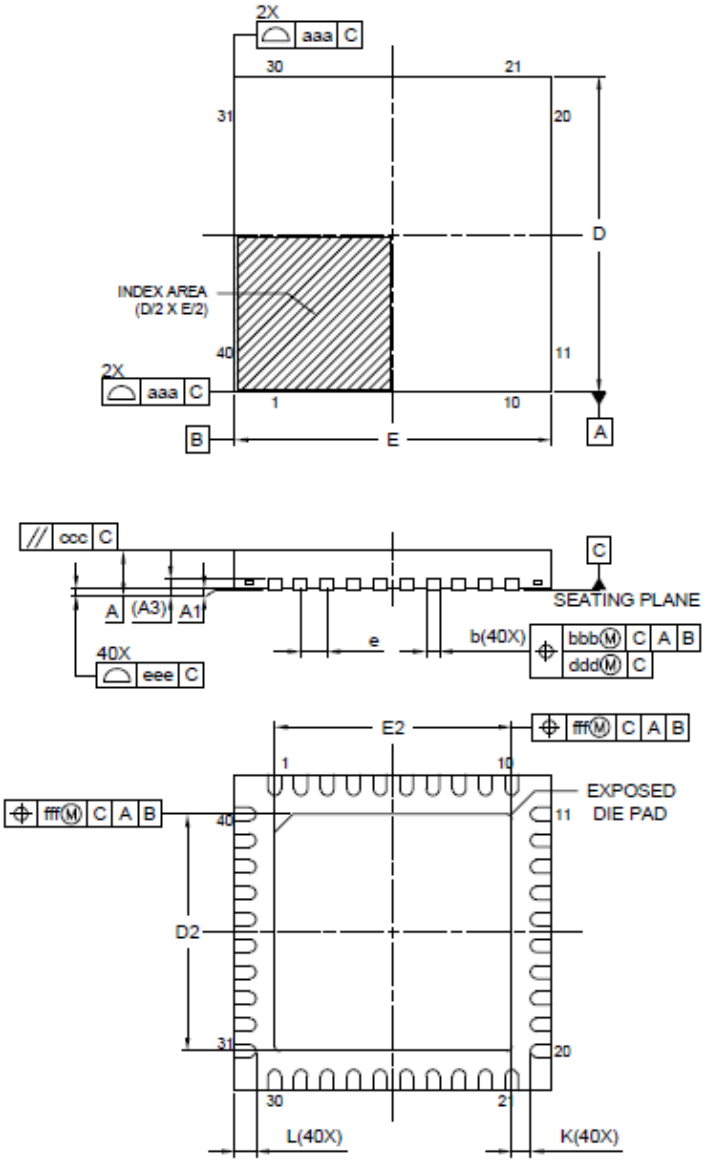
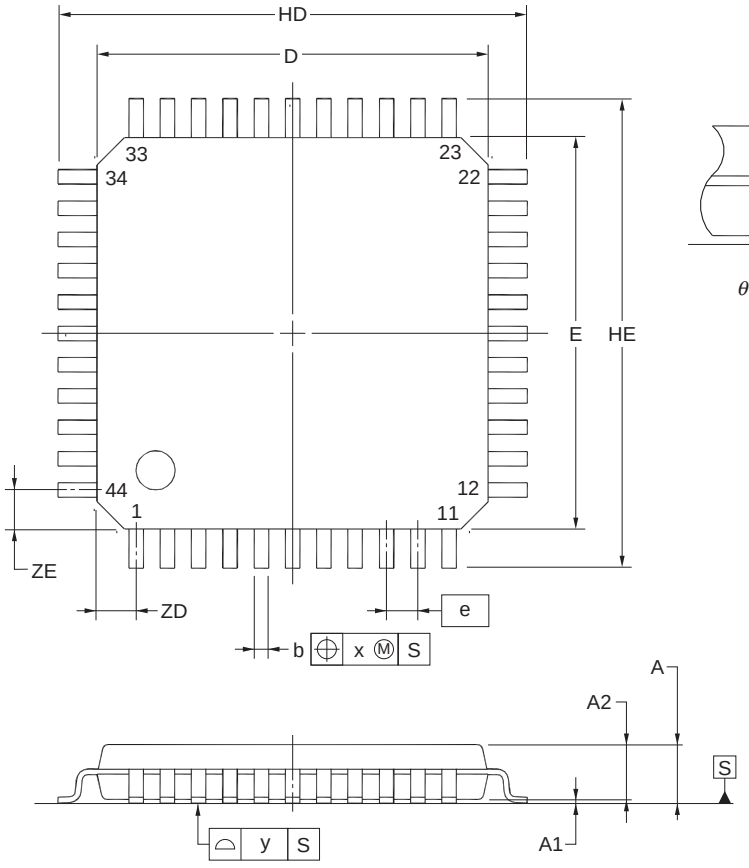
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN040-6x6-0.50 | PWQN0040KD-A | 0.08 |

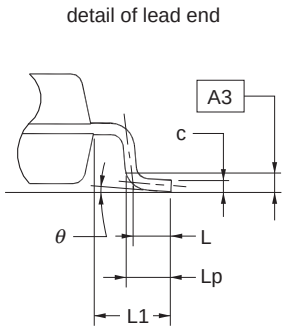



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | 0.02 | 0.05 |
| $A_3$ | | 0.203 REF. | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 6.00 BSC | |
| E | | 6.00 BSC | |
| e | | 0.50 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| $D_2$ | 4.45 | 4.50 | 4.55 |
| $E_2$ | 4.45 | 4.50 | 4.55 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

## 4.8 44-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.20 |
| E | 10.00±0.20 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.37^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |
| ZD | 1.00 |
| ZE | 1.00 |

**NOTE**
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

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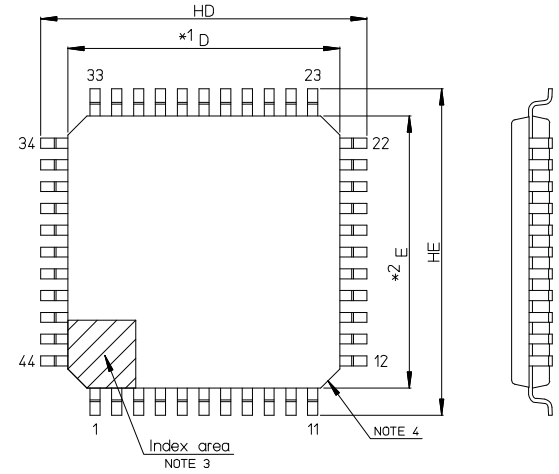
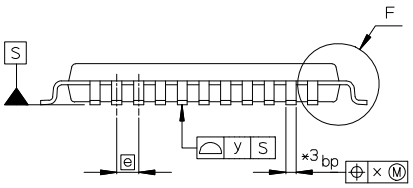
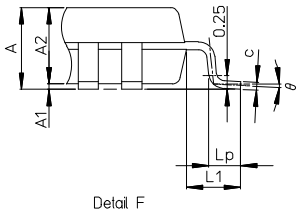
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP44-10x10-0.80 | PLQP0044GC-D | —— | 0.36g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

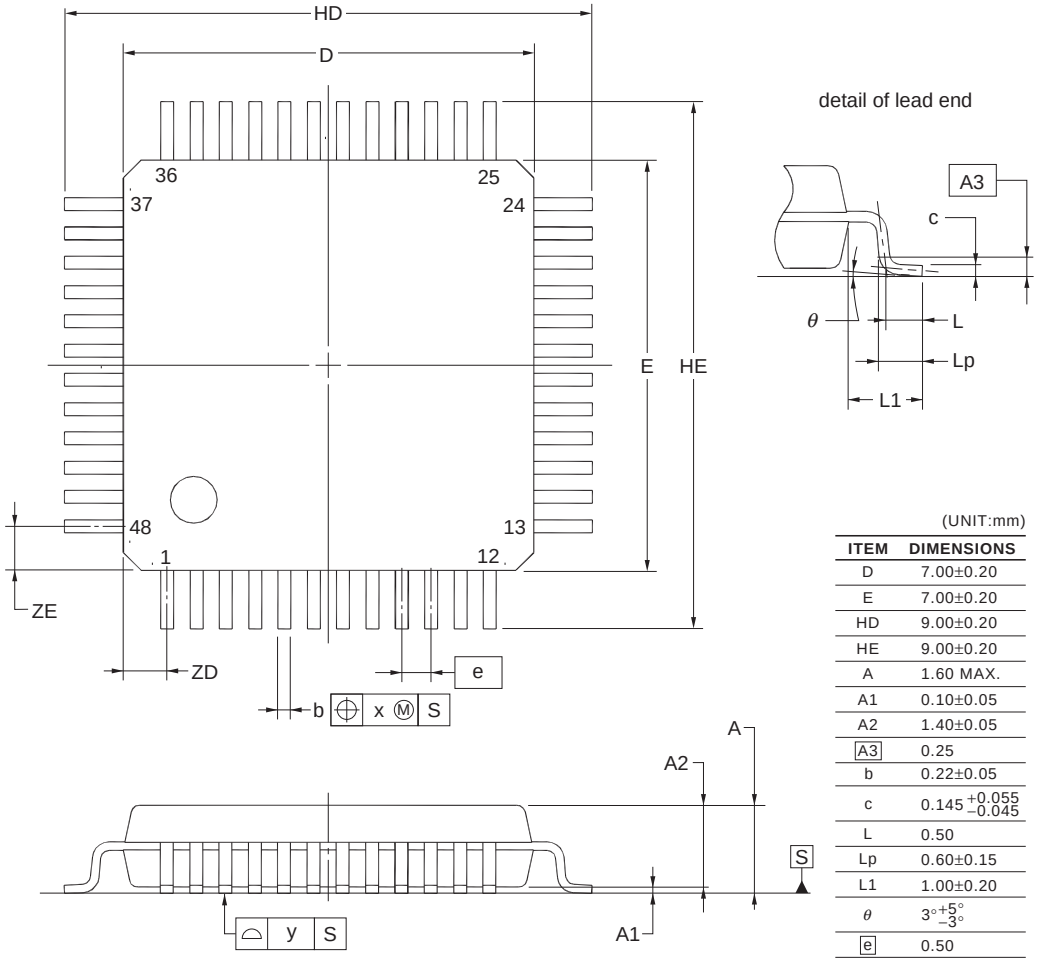



Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.8 | 10.0 | 10.2 |
| E | 9.8 | 10.0 | 10.2 |
| A2 | —— | 1.4 | —— |
| HD | 11.8 | 12.0 | 12.2 |
| HE | 11.8 | 12.0 | 12.2 |
| A | —— | —— | 1.6 |
| A1 | 0.05 | —— | 0.15 |
| bp | 0.22 | 0.37 | 0.45 |
| c | 0.09 | —— | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | —— | 0.80 | —— |
| x | —— | —— | 0.20 |
| y | —— | —— | 0.10 |
| Lp | 0.45 | 0.6 | 0.75 |
| L1 | —— | 1.0 | —— |

## 4.9 48-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KF-A | P48GA-50-8EU-1 | 0.16 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.20 |
| E | 7.00±0.20 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 0.75 |
| ZE | 0.75 |

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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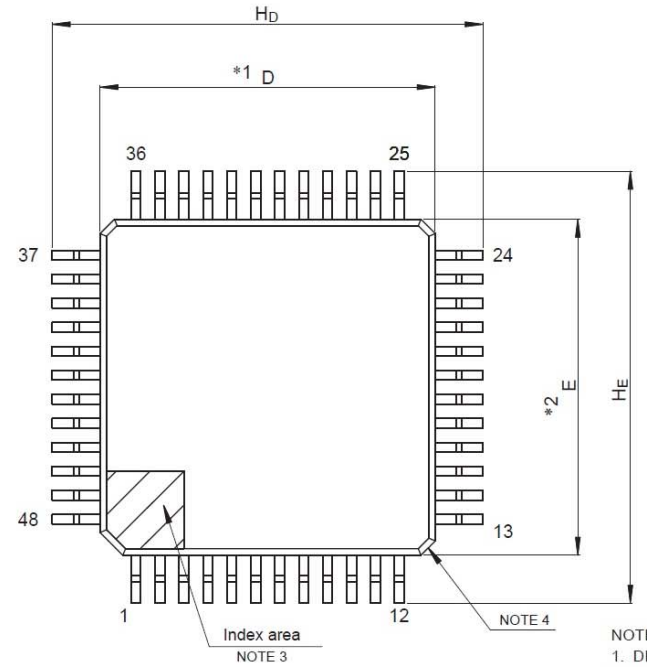
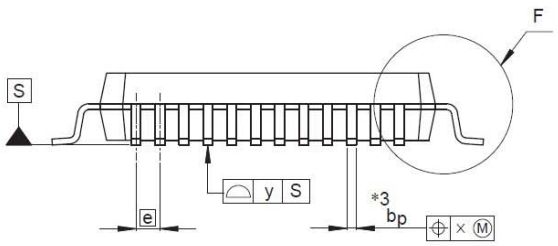
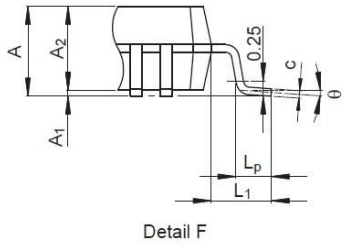
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KB-B | — | 0.2 |

Unit: mm




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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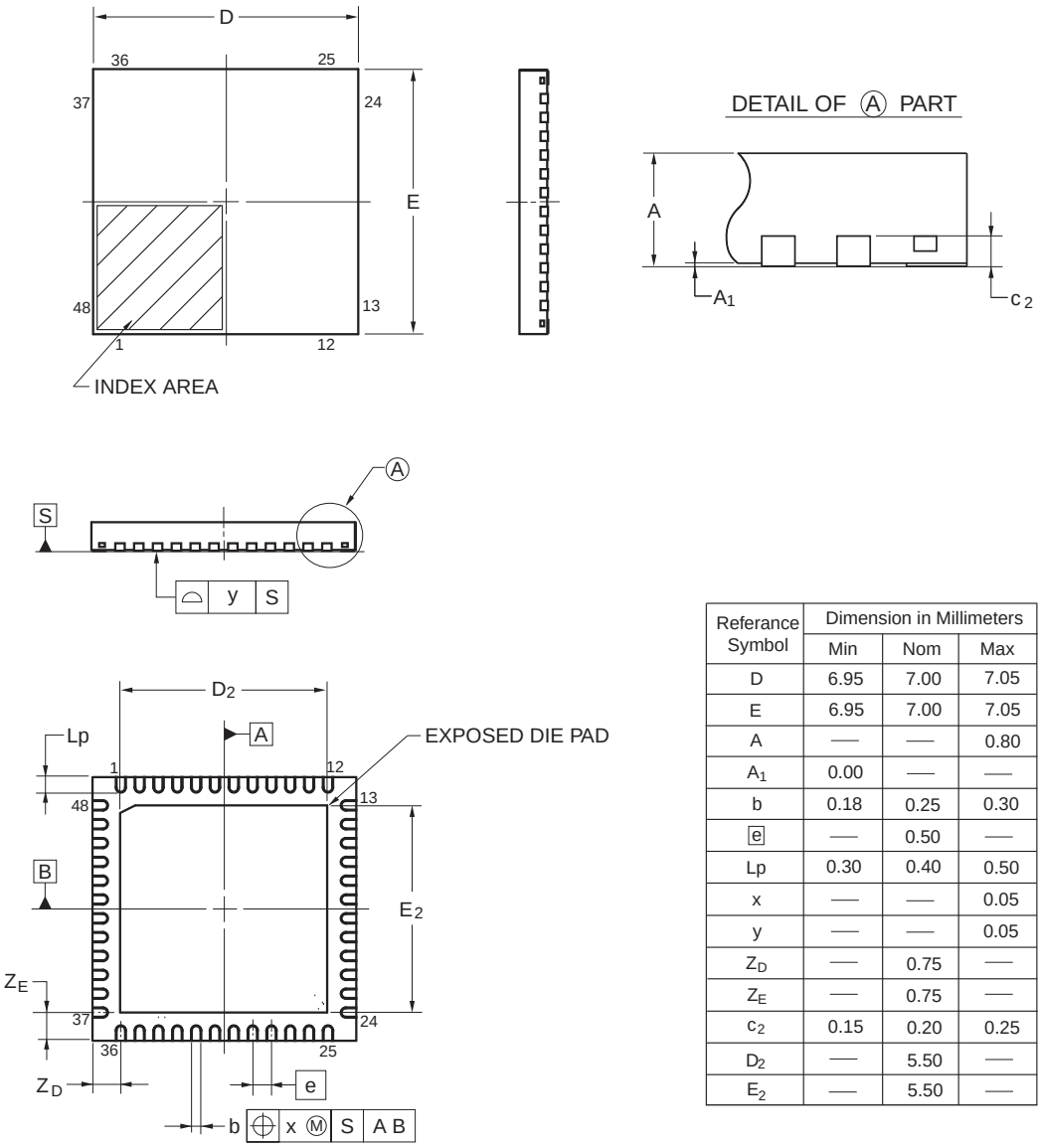
| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-6 | 0.13 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.95 | 7.00 | 7.05 |
| E | 6.95 | 7.00 | 7.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 5.50 | — |
| $E_2$ | — | 5.50 | — |

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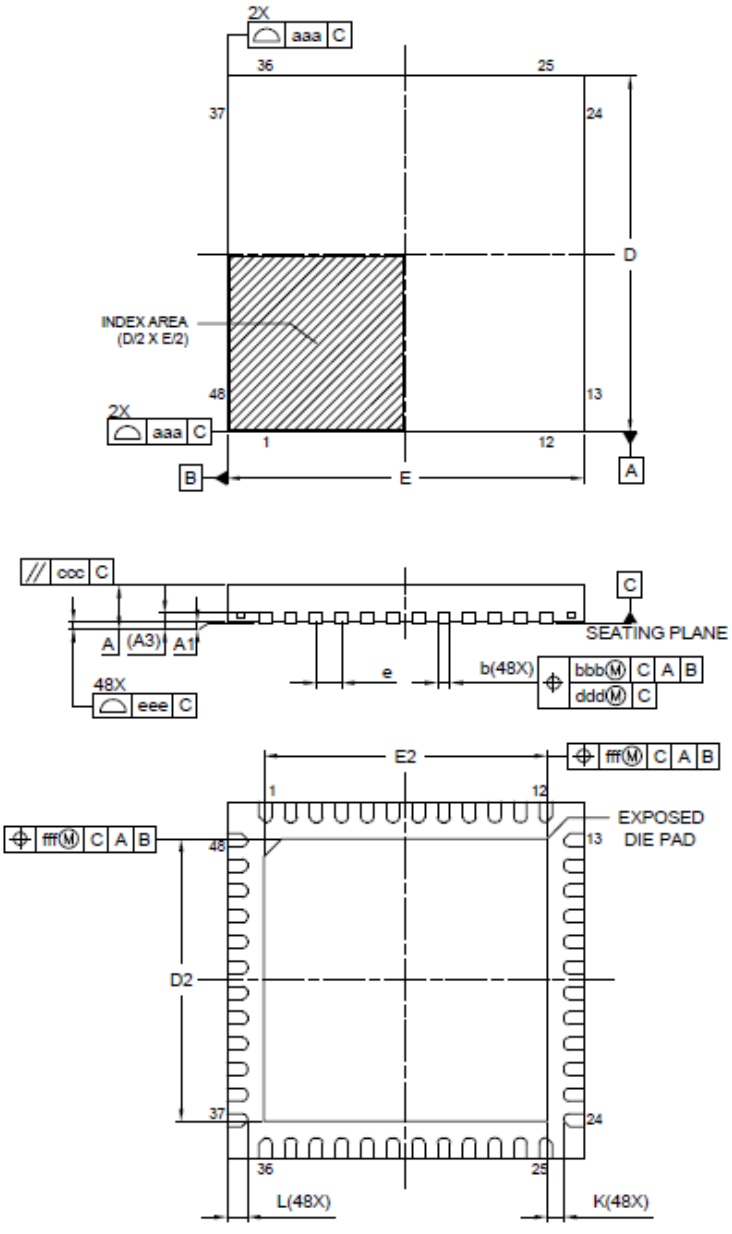
<R>

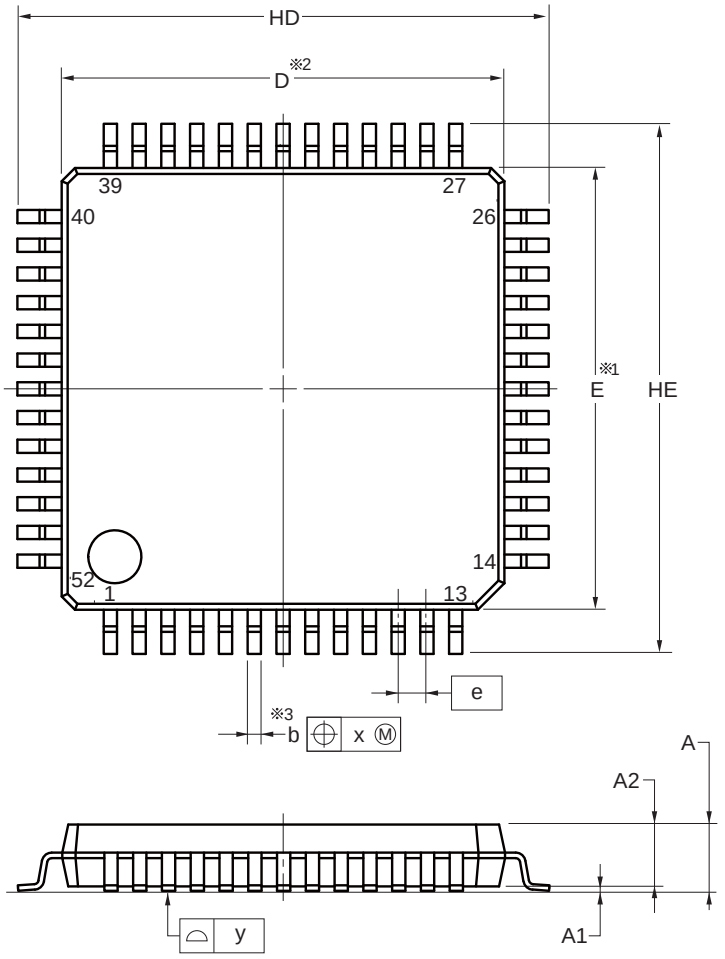
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN048-7x7-0.50 | PWQN0048KE-A | 0.13 |

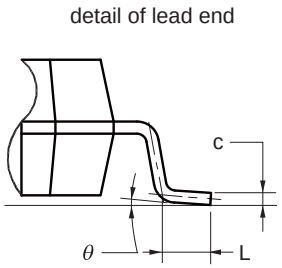



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | 0.02 | 0.05 |
| $A_3$ | | 0.203 REF. | |
| b | 0.20 | 0.25 | 0.30 |
| D | | 7.00 BSC | |
| E | | 7.00 BSC | |
| e | | 0.50 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| $D_2$ | 5.50 | 5.55 | 5.60 |
| $E_2$ | 5.50 | 5.55 | 5.60 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

### 4.10 52-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP52-10x10-0.65 | PLQP0052JA-A | P52GB-65-GBS-1 | 0.3 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.10 |
| E | 10.00±0.10 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40 |
| b | 0.32±0.05 |
| c | 0.145±0.055 |
| L | 0.50±0.15 |
| θ | 0° to 8° |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

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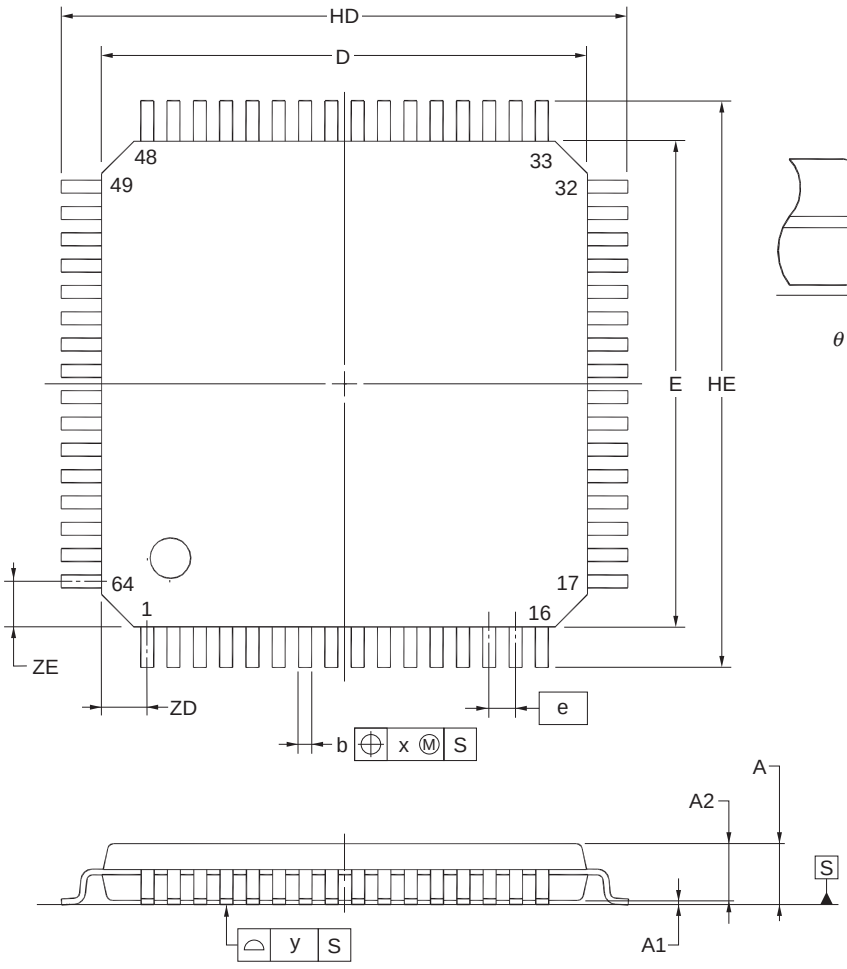
## 4.11 64-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP64-12x12-0.65 | PLQP0064JA-A | P64GK-65-UET-2 | 0.51 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 12.00±0.20 |
| E | 12.00±0.20 |
| HD | 14.00±0.20 |
| HE | 14.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.32^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |
| ZD | 1.125 |
| ZE | 1.125 |

**NOTE**
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

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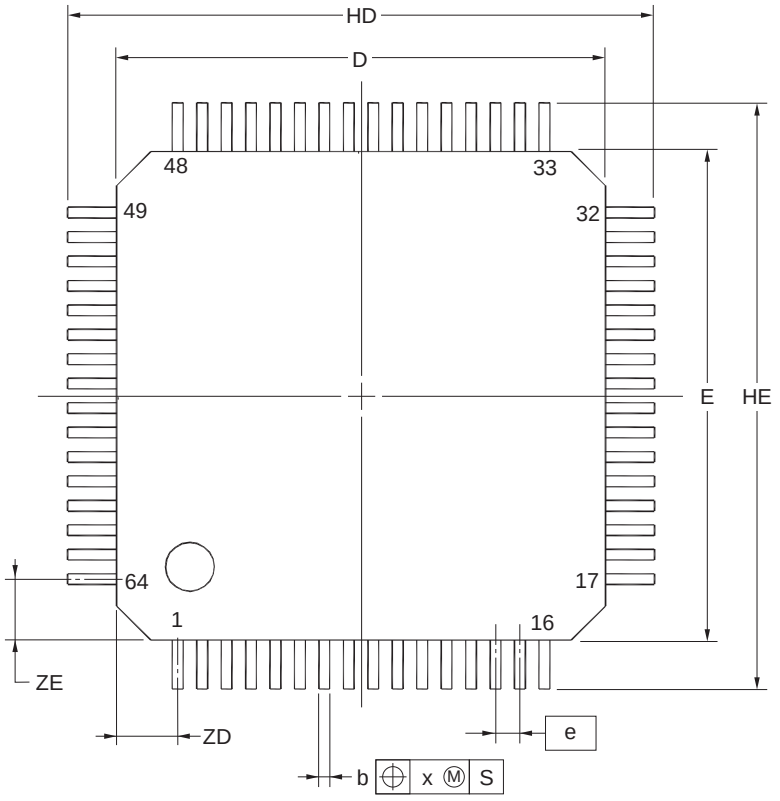
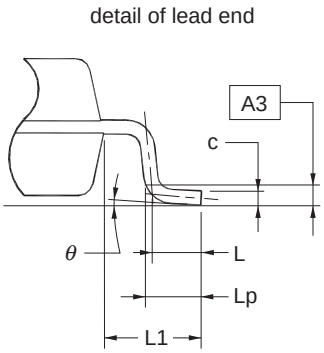
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KF-A | P64GB-50-UEU-2 | 0.35 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.20 |
| E | 10.00±0.20 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.25 |
| ZE | 1.25 |

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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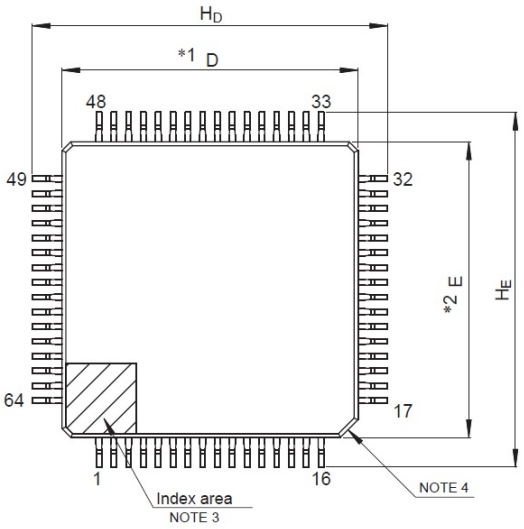
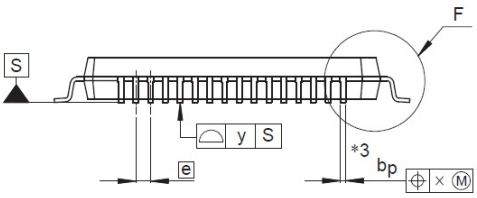
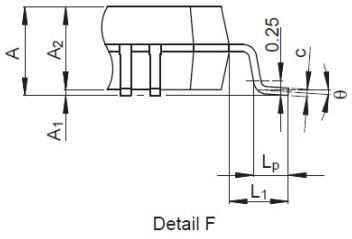
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | — | 0.3 |

Unit: mm






Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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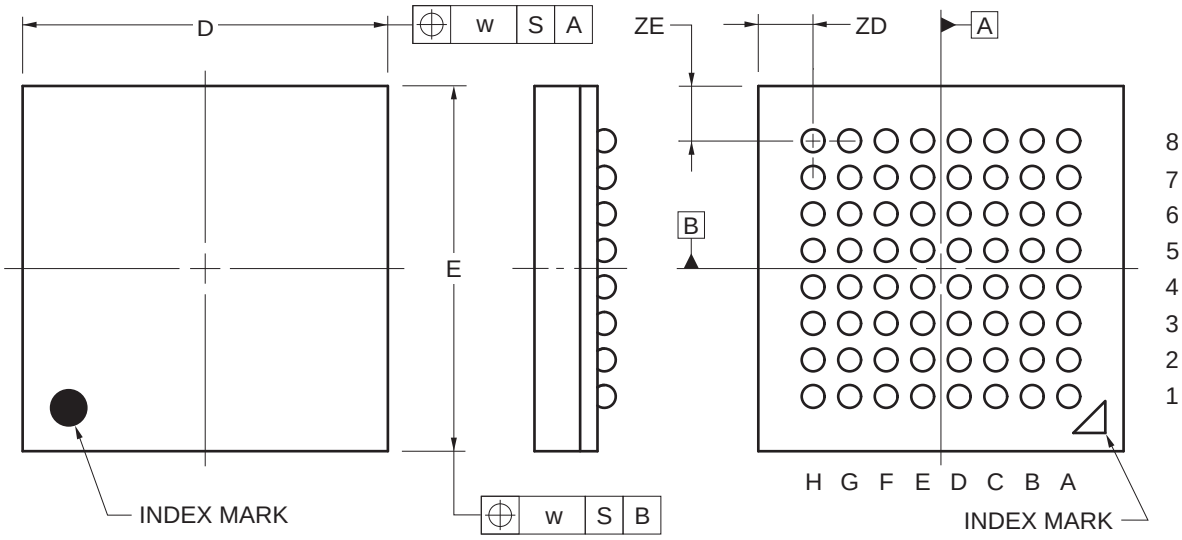
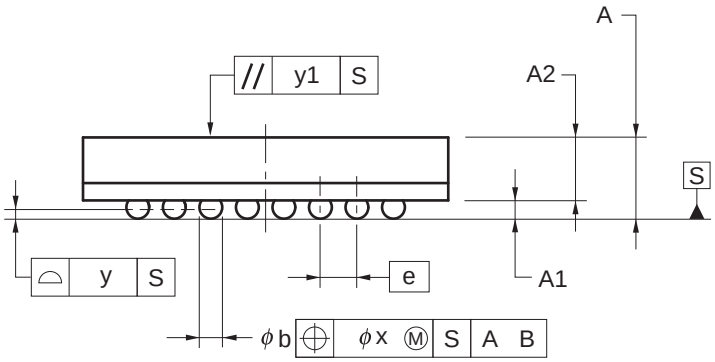
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-VFBGA64-4x4-0.40 | PVBG0064LA-A | P64F1-40-AA2-2 | 0.03 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 4.00±0.10 |
| E | 4.00±0.10 |
| w | 0.15 |
| A | 0.89±0.10 |
| A1 | 0.20±0.05 |
| A2 | 0.69 |
| e | 0.40 |
| b | 0.25±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.60 |
| ZE | 0.60 |

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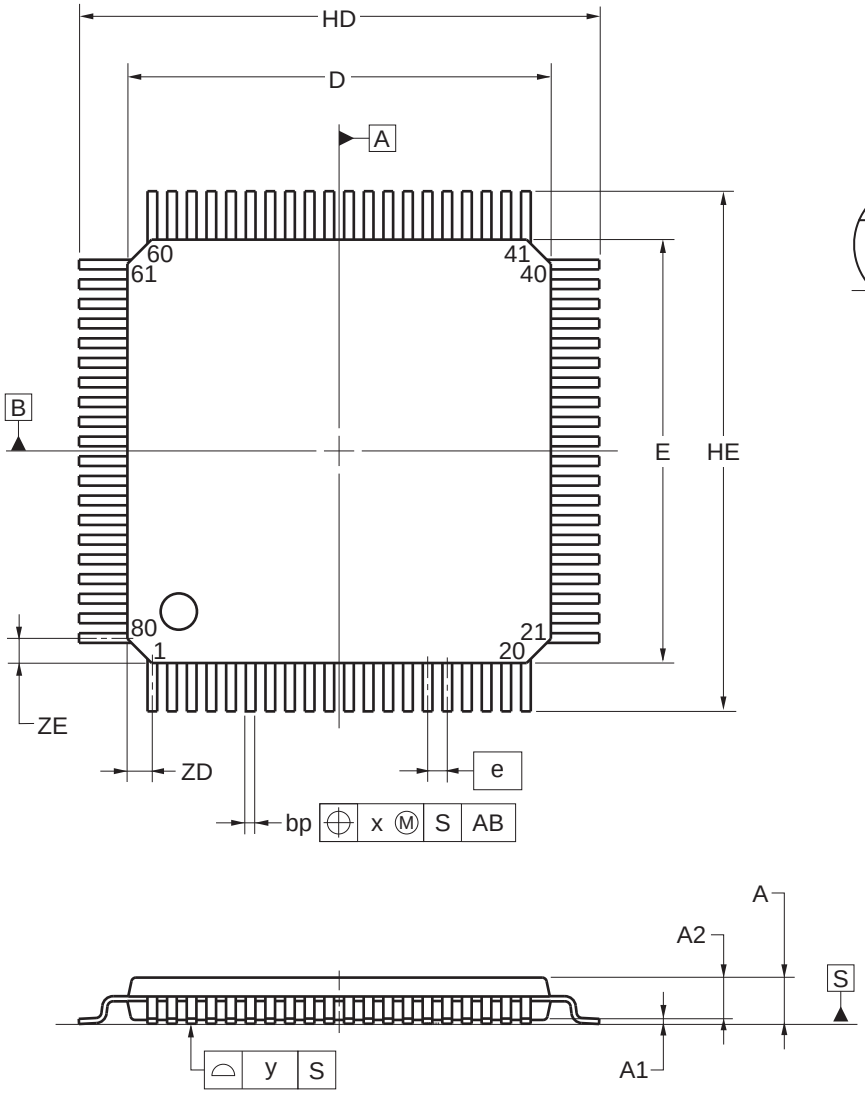
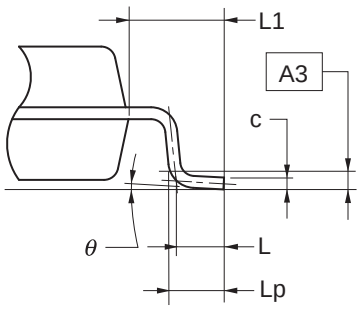
### 4.12 80-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP80-14x14-0.65 | PLQP0080JB-E | P80GC-65-UBT-2 | 0.69 |




detail of lead end




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.80 | 14.00 | 14.20 |
| E | 13.80 | 14.00 | 14.20 |
| HD | 17.00 | 17.20 | 17.40 |
| HE | 17.00 | 17.20 | 17.40 |
| A | — | — | 1.70 |
| A1 | 0.05 | 0.125 | 0.20 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | — | 0.25 | — |
| bp | 0.26 | 0.32 | 0.38 |
| c | 0.10 | 0.145 | 0.20 |
| L | — | 0.80 | — |
| Lp | 0.736 | 0.886 | 1.036 |
| L1 | 1.40 | 1.60 | 1.80 |
| θ | 0° | 3° | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| ZD | — | 0.825 | — |
| ZE | — | 0.825 | — |

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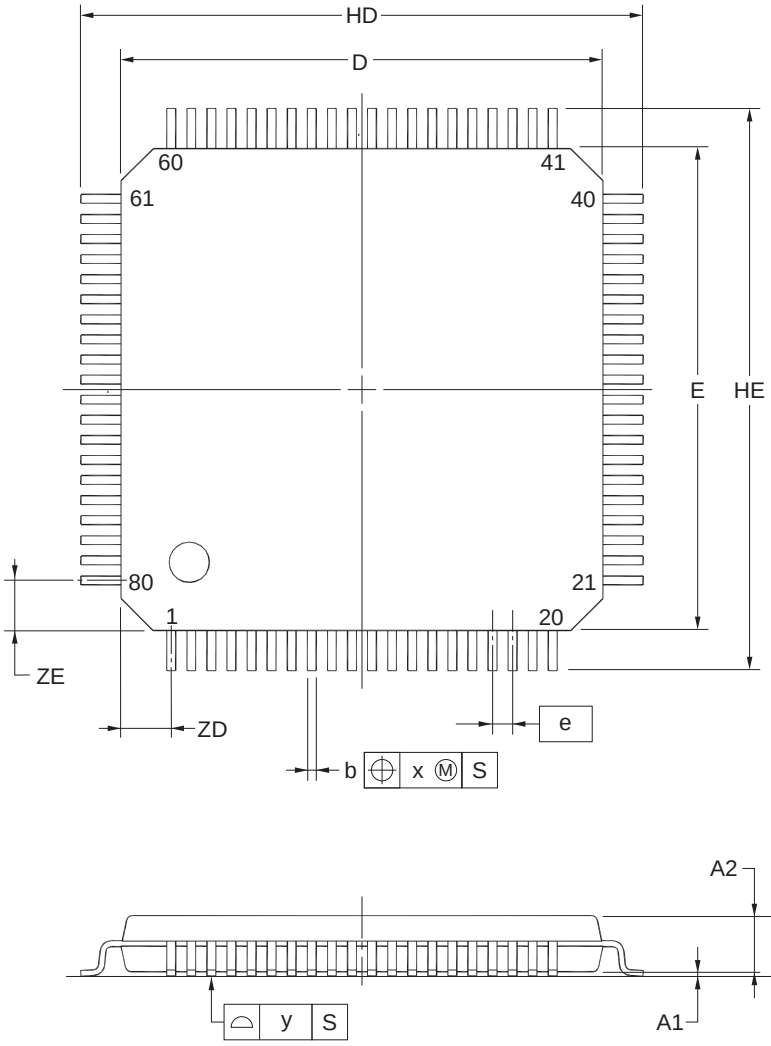
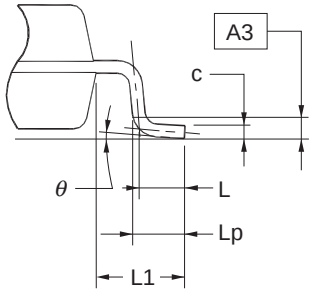
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP80-12x12-0.50 | PLQP0080KE-A | P80GK-50-8EU-2 | 0.53 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 12.00±0.20 |
| E | 12.00±0.20 |
| HD | 14.00±0.20 |
| HE | 14.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.25 |
| ZE | 1.25 |

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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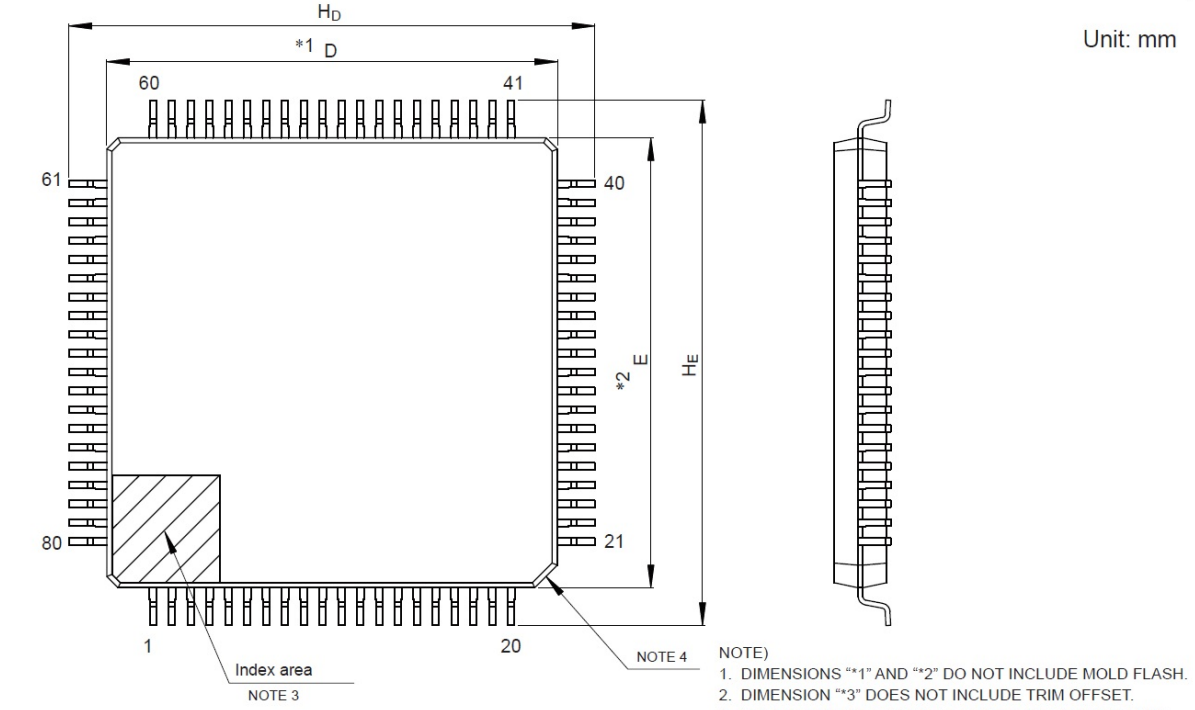
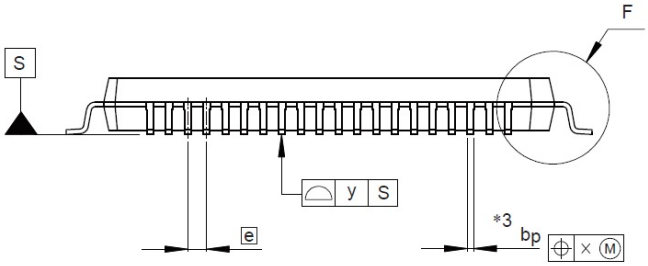
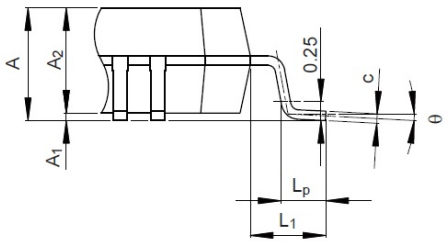
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP80-12x12-0.50 | PLQP0080KB-B | — | 0.5 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.




Detail F

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 11.9 | 12.0 | 12.1 |
| E | 11.9 | 12.0 | 12.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 13.8 | 14.0 | 14.2 |
| $H_E$ | 13.8 | 14.0 | 14.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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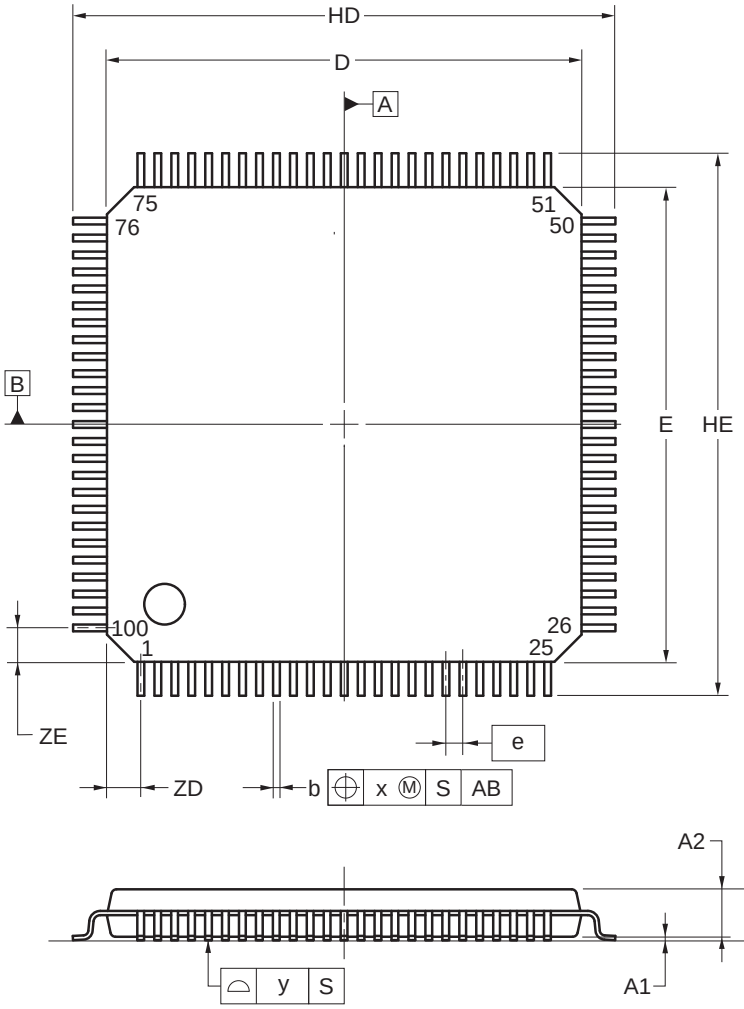
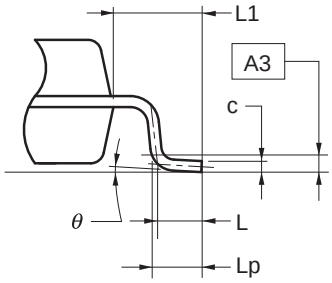
### 4.13 100-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KE-A | P100GC-50-GBR-1 | 0.69 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 14.00±0.20 |
| E | 14.00±0.20 |
| HD | 16.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.00 |
| ZE | 1.00 |

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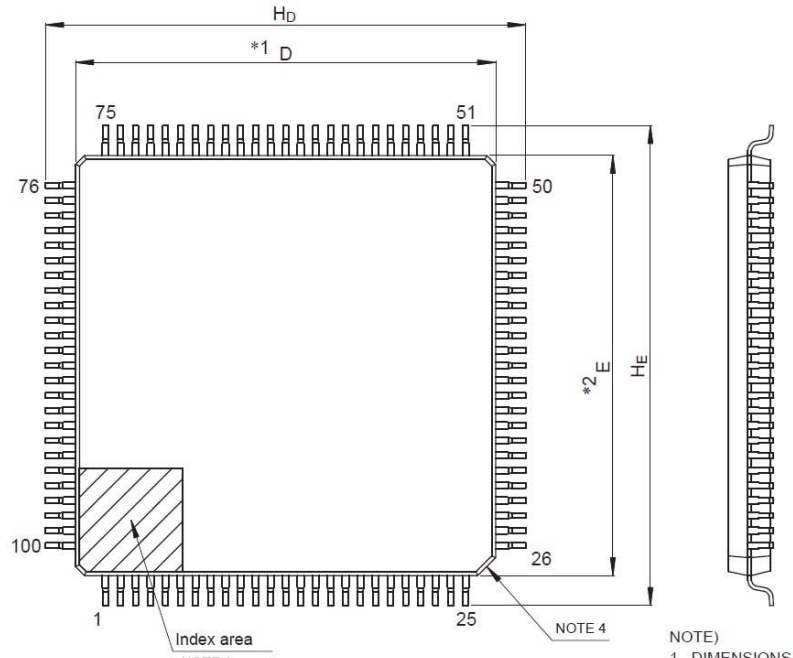
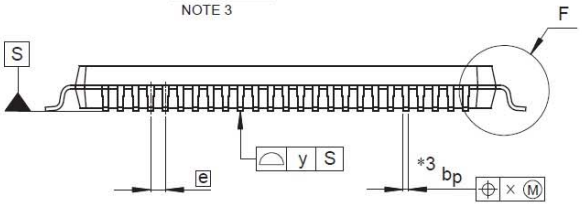
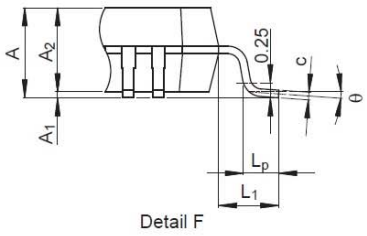
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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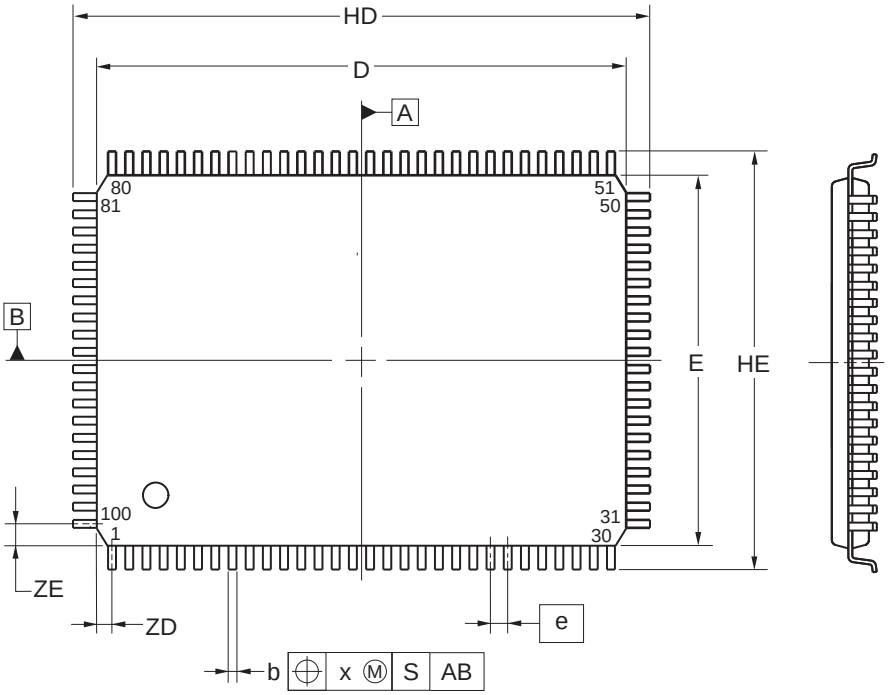
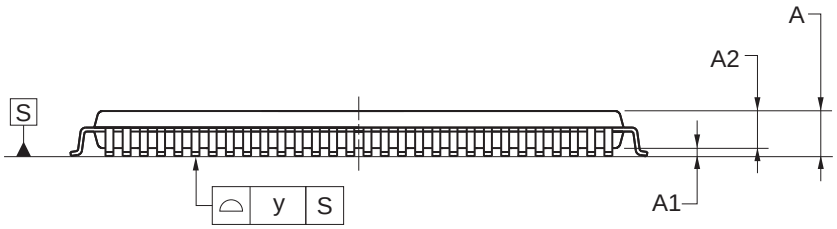
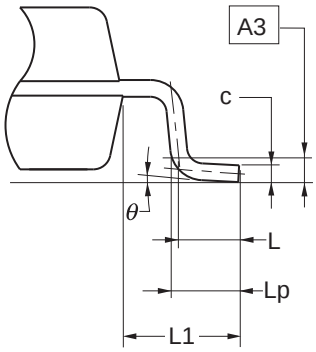
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP100-14x20-0.65 | PLQP0100JC-A | P100GF-65-GBN-1 | 0.92 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 20.00±0.20 |
| E | 14.00±0.20 |
| HD | 22.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.32^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |
| ZD | 0.575 |
| ZE | 0.825 |

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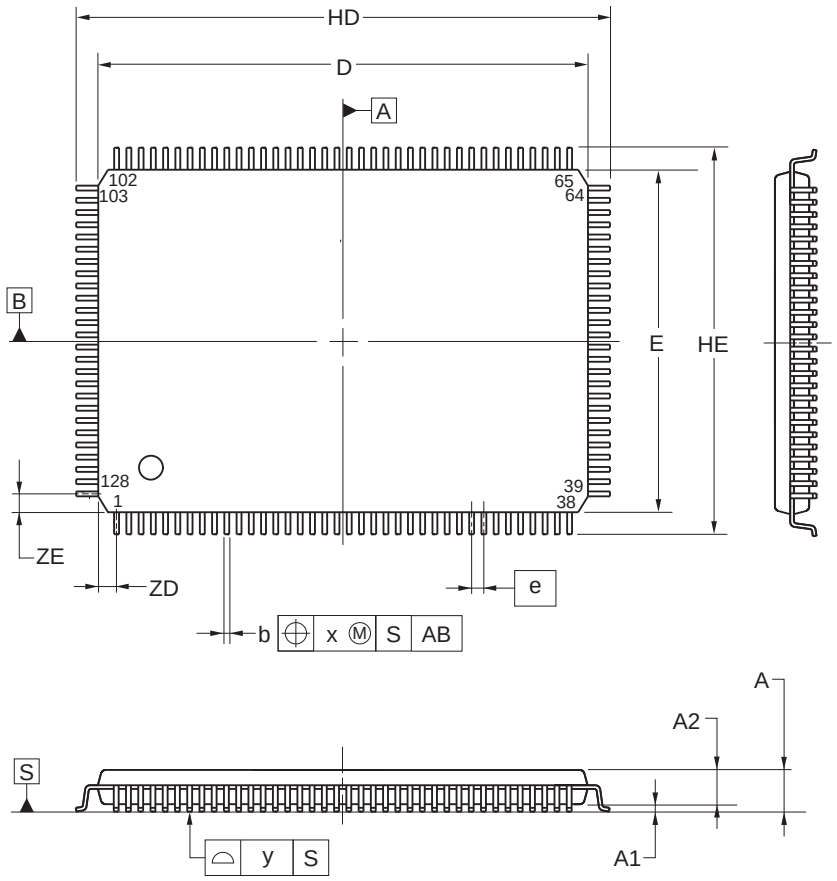
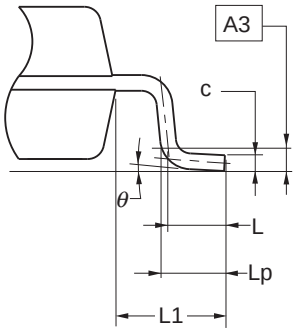
### 4.14 128-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP128-14x20-0.50 | PLQP0128KD-A | P128GF-50-GBP-1 | 0.92 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 20.00±0.20 |
| E | 14.00±0.20 |
| HD | 22.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 0.75 |
| ZE | 0.75 |

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| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Feb 29, 2012 | - | First Edition issued |
| 2.00 | Oct 12, 2012 | 7 | Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected. |
| | | 25 | 1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected. |
| | | 40, 42, 44 | 1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected. |
| | | 41, 43, 45 | 1.6 Outline of Functions: Lists of Descriptions changed. |
| | | 59, 63, 67 | Descriptions of Note 8 in a table corrected. |
| | | 68 | (4) Common to RL78/G13 all products: Descriptions of Notes corrected. |
| | | 69 | 2.4 AC Characteristics: Symbol of external system clock frequency corrected. |
| | | 96 to 98 | 2.6.1 A/D converter characteristics: Notes of overall error corrected. |
| | | 100 | 2.6.2 Temperature sensor characteristics: Parameter name corrected. |
| | | 104 | 2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected. |
| | | 116 | 3.10 52-pin products: Package drawings of 52-pin products corrected. |
| | | 120 | 3.12 80-pin products: Package drawings of 80-pin products corrected. |
| 3.00 | Aug 02, 2013 | 1 | Modification of 1.1 Features |
| | | 3 | Modification of 1.2 List of Part Numbers |
| | | 4 to 15 | Modification of Table 1-1. List of Ordering Part Numbers, note, and caution |
| | | 16 to 32 | Modification of package type in 1.3.1 to 1.3.14 |
| | | 33 | Modification of description in 1.4 Pin Identification |
| | | 48, 50, 52 | Modification of caution, table, and note in 1.6 Outline of Functions |
| | | 55 | Modification of description in table of Absolute Maximum Ratings ($T_A$ = 25°C) |
| | | 57 | Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics |
| | | 57 | Modification of table in 2.2.2 On-chip oscillator characteristics |
| | | 58 | Modification of note 3 of table (1/5) in 2.3.1 Pin characteristics |
| | | 59 | Modification of note 3 of table (2/5) in 2.3.1 Pin characteristics |
| | | 63 | Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 64 | Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 65 | Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 66 | Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 68 | Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products |
| | | 70 | Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products |
| | | 72 | Modification of notes 1 and 4 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products |
| | | 74 | Modification of notes 1, 5, and 6 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products |
| | | 75 | Modification of (4) Peripheral Functions (Common to all products) |
| | | 77 | Modification of table in 2.4 AC Characteristics |
| | | 78, 79 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 80 | Modification of figures of AC Timing Test Points and External System Clock Timing |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 3.00 | Aug 02, 2013 | 81 | Modification of figure of AC Timing Test Points |
| | | 81 | Modification of description and note 3 in (1) During communication at same potential (UART mode) |
| | | 83 | Modification of description in (2) During communication at same potential (CSI mode) |
| | | 84 | Modification of description in (3) During communication at same potential (CSI mode) |
| | | 85 | Modification of description in (4) During communication at same potential (CSI mode) (1/2) |
| | | 86 | Modification of description in (4) During communication at same potential (CSI mode) (2/2) |
| | | 88 | Modification of table in (5) During communication at same potential (simplified $I^2C$ mode) (1/2) |
| | | 89 | Modification of table and caution in (5) During communication at same potential (simplified $I^2C$ mode) (2/2) |
| | | 91 | Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2) |
| | | 92, 93 | Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) |
| | | 94 | Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) |
| | | 95 | Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2) |
| | | 96 | Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2) |
| | | 97 | Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3) |
| | | 98 | Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3) |
| | | 99 | Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) |
| | | 100 | Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) |
| | | 102 | Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2) |
| | | 103 | Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2) |
| | | 106 | Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (1/2) |
| | | 107 | Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (2/2) |
| | | 109 | Addition of (1) $I^2C$ standard mode |
| | | 111 | Addition of (2) $I^2C$ fast mode |
| | | 112 | Addition of (3) $I^2C$ fast mode plus |
| | | 112 | Modification of IICA serial transfer timing |
| | | 113 | Addition of table in 2.6.1 A/D converter characteristics |
| | | 113 | Modification of description in 2.6.1 (1) |
| | | 114 | Modification of notes 3 to 5 in 2.6.1 (1) |
| | | 115 | Modification of description and notes 2, 4, and 5 in 2.6.1 (2) |
| | | 116 | Modification of description and notes 3 and 4 in 2.6.1 (3) |
| | | 117 | Modification of description and notes 3 and 4 in 2.6.1 (4) |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 3.00 | Aug 02, 2013 | 118 | Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics |
| | | 118 | Modification of table and note in 2.6.3 POR circuit characteristics |
| | | 119 | Modification of table in 2.6.4 LVD circuit characteristics |
| | | 120 | Modification of table of LVD Detection Voltage of Interrupt & Reset Mode |
| | | 120 | Renamed to 2.6.5 Power supply voltage rising slope characteristics |
| | | 122 | Modification of table, figure, and remark in 2.10 Timing Specs for Switching Flash Memory Programming Modes |
| | | 123 | Modification of caution 1 and description |
| | | 124 | Modification of table and remark 3 in Absolute Maximum Ratings ($T_A$ = 25°C) |
| | | 126 | Modification of table, note, caution, and remark in 3.2.1 X1, XT1 oscillator characteristics |
| | | 126 | Modification of table in 3.2.2 On-chip oscillator characteristics |
| | | 127 | Modification of note 3 in 3.3.1 Pin characteristics (1/5) |
| | | 128 | Modification of note 3 in 3.3.1 Pin characteristics (2/5) |
| | | 133 | Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (1/2) |
| | | 135 | Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (2/2) |
| | | 137 | Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (1/2) |
| | | 139 | Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (2/2) |
| | | 140 | Modification of (3) Peripheral Functions (Common to all products) |
| | | 142 | Modification of table in 3.4 AC Characteristics |
| | | 143 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 143 | Modification of figure of AC Timing Test Points |
| | | 143 | Modification of figure of External System Clock Timing |
| | | 145 | Modification of figure of AC Timing Test Points |
| | | 145 | Modification of description, note 1, and caution in (1) During communication at same potential (UART mode) |
| | | 146 | Modification of description in (2) During communication at same potential (CSI mode) |
| | | 147 | Modification of description in (3) During communication at same potential (CSI mode) |
| | | 149 | Modification of table, note 1, and caution in (4) During communication at same potential (simplified $I^2C$ mode) |
| | | 151 | Modification of table, note 1, and caution in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2) |
| | | 152 to 154 | Modification of table, notes 2 to 6, caution, and remarks 1 to 4 in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) |
| | | 155 | Modification of table in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3) |
| | | 156 | Modification of table and caution in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3) |
| | | 157, 158 | Modification of table, caution, and remarks 3 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) |
| | | 160, 161 | Modification of table and caution in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) |

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| 3.00 | Aug 02, 2013 | 163 | Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (1/2) |
| | | 164, 165 | Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (2/2) |
| | | 166 | Modification of table in 3.5.2 Serial interface IICA |
| | | 166 | Modification of IICA serial transfer timing |
| | | 167 | Addition of table in 3.6.1 A/D converter characteristics |
| | | 167, 168 | Modification of table and notes 3 and 4 in 3.6.1 (1) |
| | | 169 | Modification of description in 3.6.1 (2) |
| | | 170 | Modification of description and note 3 in 3.6.1 (3) |
| | | 171 | Modification of description and notes 3 and 4 in 3.6.1 (4) |
| | | 172 | Modification of table and note in 3.6.3 POR circuit characteristics |
| | | 173 | Modification of table of LVD Detection Voltage of Interrupt & Reset Mode |
| | | 173 | Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics |
| | | 174 | Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART) |
| | | 175 | Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes |
| 3.10 | Nov 15, 2013 | 123 | Caution 4 added. |
| | | 125 | Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted. |
| 3.30 | Mar 31, 2016 | 18 | Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products |
| | | 49 | Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products] |
| | | 51 | Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products] |
| | | 53 | Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products] |
| | | 110 to 112, 167 | $\overline{ACK}$ corrected to ACK |
| 3.40 | May 31, 2018 | 172 | Addition of note in 3.6.3 POR circuit characteristics |
| 3.41 | Jan 31, 2020 | 3 | Addition of packaging specifications in Figure 1-1 Part Number, Memory Size, and Package of RL78/G13 |
| | | 4 to 28 | Addition of ordering part numbers and RENESAS codes in Table 1-1 List of Ordering Part Numbers |
| | | 189, 190, 192 to 194, 196 to 198, 200, 202 to 205, 207 to 209, 211, 213, 214 | Modification of the titles of the subchapters and deletion of product names in Chapter 4 |
| | | 191 | Addition of figure in 4.2 24-pin Package |
| | | 195 | Addition of figure in 4.3 32-pin Package |
| | | 199 | Addition of figure in 4.8 44-pin Package |

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| 3.41 | Jan 31, 2020 | 201 | Addition of figure in 4.9 48-pin Package |
| | | 206 | Addition of figure in 4.11 64-pin Package |
| | | 210 | Addition of figure in 4.12 80-pin Package |
| | | 212 | Addition of figure in 4.13 100-pin Package |
| 3.50 | Jun 30, 2020 | 1 | Modification of description in 1.1 Features |
| | | 3 | Modification of Figure 1-1 Part Number, Memory Size, and Package of RL78/G13 |
| | | 4 to 11 | Modification of Table 1-1 List of Ordering Part Numbers |
| | | 12 | Addition of packaging specifications in 1.3.1 20-pin products |
| | | 173 | Addition of package drawing in 4.1 20-pin Package |
| | | 182 | Addition of package drawing in 4.7 40-pin Package |
| | | 188 | Addition of package drawing in 4.9 48-pin Package |

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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